



**THE DATASHEET OF
A3906SESTR-T**

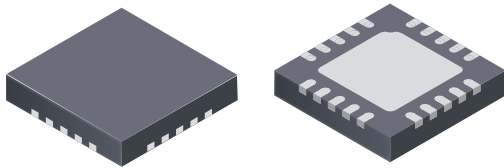


Low Voltage Stepper and Single/Dual DC Motor Driver

FEATURES AND BENEFITS

- 2.5 to 9 V operation
- Internal PWM current limit control
- Synchronous rectification for reduced power dissipation
- Peak current output flag
- Undervoltage lockout
- Low $R_{DS(on)}$ outputs
- Small package
- Brake mode for DC motors
- Sleep function
- Crossover-current protection
- Thermal shutdown

PACKAGE: 20-contact QFN (suffix ES)



Not to scale

DESCRIPTION

Designed for pulse-width modulated (PWM) control of low voltage stepper motors, and single and dual DC motors, the A3906 is capable of output currents up to 1 A per channel and operating voltages from 2.5 to 9 V.

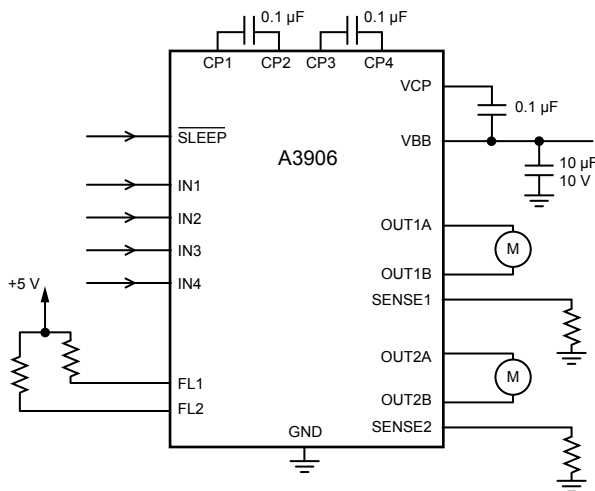
The A3906 has an internal fixed off-time PWM timer that sets a peak current based on the selection of a current sense resistor. An overcurrent output flag is provided that notifies the user when the current in the motor winding reaches the peak current determined by the sense resistor. The fault output does not affect driver operation.

The A3906 is provided in a 20-contact, 4 mm × 4 mm, 0.75 mm nominal overall height QFN, with exposed pad for enhanced thermal dissipation. It is lead (Pb) free, with 100% matte tin leadframe plating.

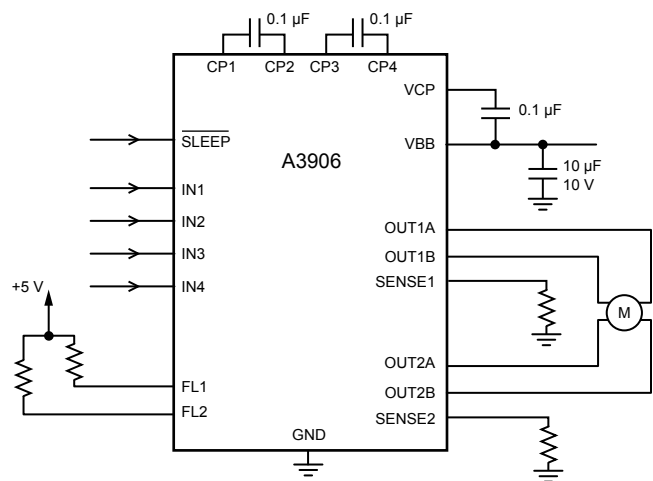
Applications include the following:

- Digital still cameras (DSC)
- Cell phone cameras
- USB-powered devices
- Battery-powered devices

Typical Applications



Dual DC motor application



Stepper motor application

SELECTION GUIDE

| Part Number | Packing | Package |
|--------------|----------------------------|-------------------------------------|
| A3906SESTR-T | 1500 pieces per 7-in. reel | 20-pin QFN with exposed thermal pad |

ABSOLUTE MAXIMUM RATINGS

| Characteristic | Symbol | Notes | Rating | Units | |
|--|----------------|--|----------------|-------|---|
| Load Supply Voltage | V_{BB} | | 9.6 | V | |
| Logic Input Voltage Range | V_{IN} | | -0.3 to 7 | V | |
| Sense Voltage | V_{SENSEX} | Continuous | 0.5 | V | |
| | | Pulsed, $t_w < 1 \mu s$ | 1 | V | |
| Output Current | I_{OUT} | May be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C. | Continuous | 1 | A |
| | | | Peak, DC < 30% | 1.5 | A |
| Output Current in Paralleled Operation | $I_{OUT(par)}$ | | Continuous | 2 | A |
| | | | Peak, DC < 30% | 2.5 | A |
| Operating Temperature Range | T_A | Range S | -20 to 85 | °C | |
| Junction Temperature | $T_{J(max)}$ | | 150 | °C | |
| Storage Temperature Range | T_{stg} | | -40 to 150 | °C | |

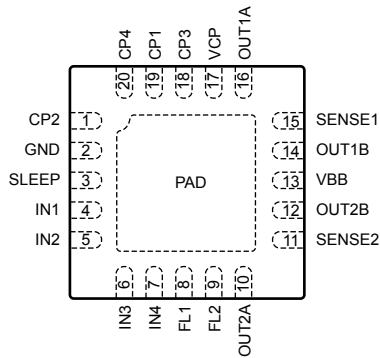
THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

| Characteristic | Symbol | Test Conditions* | Value | Units |
|----------------------------|-----------------|-------------------------------------|-------|-------|
| Package Thermal Resistance | $R_{\theta JA}$ | 4-layer PCB based on JEDEC standard | 37 | °C/W |

*Additional thermal information available on the Allegro website.

PINOUT DIAGRAM AND TERMINAL LIST

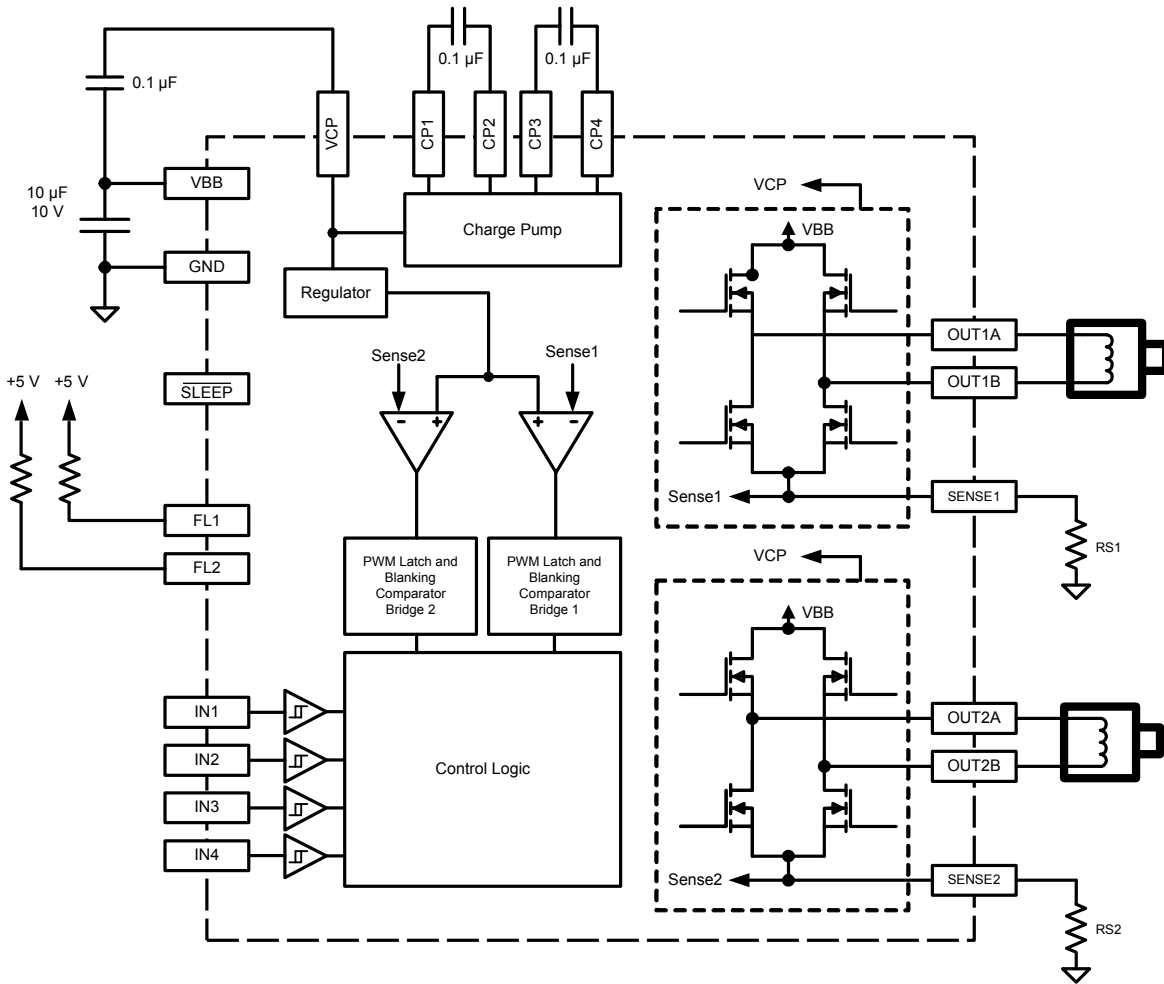
PINOUT DIAGRAM



TERMINAL LIST TABLE

| Number | Name | Function |
|--------|--------|--|
| 1 | CP2 | Charge pump capacitor terminal 2 |
| 2 | GND | Ground |
| 3 | SLEEP | Sleep logic input, active low |
| 4 | IN1 | Control input |
| 5 | IN2 | Control input |
| 6 | IN3 | Control input |
| 7 | IN4 | Control input |
| 8 | FL1 | Current limit flag, bridge 1 |
| 9 | FL2 | Current limit flag bridge 2 |
| 10 | OUT2A | DMOS full-bridge 2, output A |
| 11 | SENSE2 | Current sense resistor terminal, bridge 2 |
| 12 | OUT2B | DMOS full-bridge 2, output B |
| 13 | VBB | Supply Voltage |
| 14 | OUT1B | DMOS full-bridge 1, output B |
| 15 | SENSE1 | Current sense resistor terminal, bridge 1 |
| 16 | OUT1A | DMOS full-bridge 1, output A |
| 17 | VCP | Reservoir capacitor terminal |
| 18 | CP3 | Charge pump capacitor terminal 3 |
| 19 | CP1 | Charge pump capacitor terminal 1 |
| 20 | CP4 | Charge pump capacitor terminal 4 |
| - | PAD | Exposed pad for enhanced thermal performance |

FUNCTIONAL BLOCK DIAGRAM

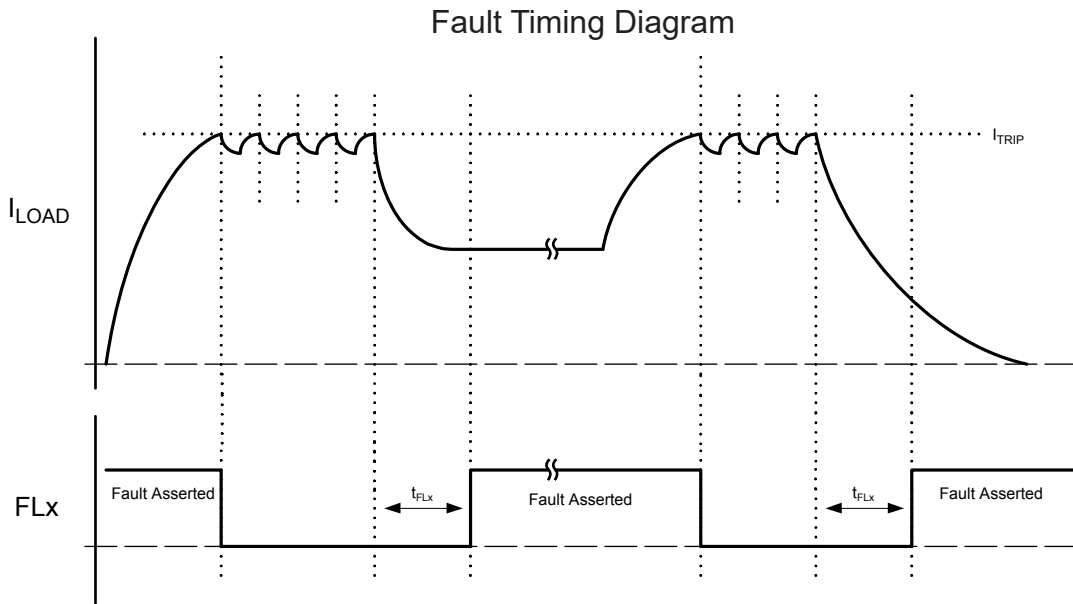


ELECTRICAL CHARACTERISTICS [1][2]: Valid at $T_A = 25^\circ\text{C}$ and $V_{BB} = 2.5$ to 9 V, unless otherwise noted

| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Units |
|-------------------------------------|----------------|---|------|-------|------|------------------|
| Operating Voltage Range | V_{BB} | | 2.5 | – | 9 | V |
| VBB Supply Current | I_{BB} | $I_{OUT} = 0$ mA, PWM = 50 kHz, Duty Cycle = 50% | – | 5 | – | mA |
| | | $I_{OUT} = 0$ mA, outputs disabled, $V_{BB} = 9.6$ V | – | 3 | – | mA |
| | | Sleep mode, $V_{IN} < 0.4$ V | – | 150 | 500 | nA |
| Output Resistance | $R_{DS(on)}$ | Source driver, $I_{OUT} = 400$ mA, $V_{BB} = 3$ V, $T_J = 25^\circ\text{C}$ | – | 0.52 | 0.60 | Ω |
| | | Source driver, $I_{OUT} = 400$ mA, $V_{BB} = 3$ V, $T_J = 85^\circ\text{C}$ | – | 0.78 | – | Ω |
| | | Sink driver, $I_{OUT} = 400$ mA, $V_{BB} = 3$ V, $T_J = 25^\circ\text{C}$ | – | 0.62 | 0.74 | Ω |
| | | Sink driver, $I_{OUT} = 400$ mA, $V_{BB} = 3$ V, $T_J = 85^\circ\text{C}$ | – | 0.93 | – | Ω |
| Current Trip Sense Voltage | V_{SENSE} | FLx falling edge | 160 | 200 | 240 | mV |
| Clamp Diode Voltage | V_f | $I = 400$ mA | – | – | 1 | V |
| Output Leakage Current | I_{DSS} | Outputs, $V_{OUT} = 9$ V | –20 | – | 20 | μA |
| CONTROL LOGIC | | | | | | |
| Logic Input Voltage | $V_{IN(1)}$ | | 2.0 | – | 5.5 | V |
| | $V_{IN(0)}$ | | – | – | 0.8 | V |
| Logic Input Current | $I_{IN(1)}$ | $V_{IN} = 5.5$ V | – | <100 | 500 | nA |
| | $I_{IN(0)}$ | $V_{IN} = 0.8$ V | – | <–100 | –500 | nA |
| Input Hysteresis | V_{INHys} | | – | 150 | – | mV |
| $\overline{\text{SLEEP}}$ Input | $V_{SLEEP(0)}$ | | – | – | 0.4 | V |
| | $V_{SLEEP(1)}$ | | 2 | – | – | V |
| Fault Output | V_{FLx} | Flag asserted, $I_{FLx} = 1$ mA | – | – | 200 | mV |
| Fault Output Leakage Current | I_{FLx} | $V_{FLx} = 5$ V | – | – | 1 | μA |
| Fault Output Timer | t_{FLx} | Reset of PWM latch | – | 300 | – | μs |
| Blank Time | t_{BLANK} | | 2.1 | 3 | 3.9 | μs |
| Fixed Off-Time | t_{OFF} | | – | 30 | – | μs |
| Propagation Delay Time | $t_{pd(on)}$ | Input high to source on, input low to source off | 100 | 235 | 350 | ns |
| | $t_{pd(off)}$ | Input low to sink off, input high to sink on | 50 | 100 | 200 | ns |
| PROTECTION CIRCUITRY | | | | | | |
| Crossover Delay | t_{COD} | | 200 | 425 | 650 | ns |
| VBB Undervoltage Lockout Threshold | V_{BBUVLO} | V_{BB} rising | 2.2 | 2.31 | 2.45 | V |
| VBB Undervoltage Lockout Hysteresis | $V_{BBUVHYS}$ | | 200 | 300 | 400 | mV |
| Thermal Shutdown Temperature | T_{JTSD} | | – | 165 | – | $^\circ\text{C}$ |
| Thermal Shutdown Hysteresis | $T_{JTSDHYS}$ | | – | 15 | – | $^\circ\text{C}$ |

[1] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.

[2] Specifications over the operating temperature range are assured by design and characterization.



NOTE: Timer resets after each reset of the PWM latch.

Control Logic

DC Motor Operation

| IN1 | IN2 | IN3 | IN4 | OUT1A | OUT1B | OUT2A | OUT2B | Function |
|-----|-----|-----|-----|-------|-------|-------|-------|----------|
| 0 | 0 | 0 | 0 | Off | Off | Off | Off | Disabled |
| 1 | 0 | 1 | 0 | High | Low | High | Low | Forward |
| 0 | 1 | 0 | 1 | Low | High | Low | High | Reverse |
| 1 | 1 | 1 | 1 | Low | Low | Low | Low | Brake |

Stepper Motor Operation

| IN1 | IN2 | IN3 | IN4 | OUT1A | OUT1B | OUT2A | OUT2B | Function | |
|-----|-----|-----|-----|-------|-------|-------|-------|-------------|----------|
| 0 | 0 | 0 | 0 | Off | Off | Off | Off | Disabled | Disabled |
| 1 | 0 | 1 | 0 | High | Low | High | Low | Full Step 1 | ½ Step 1 |
| 0 | 0 | 1 | 0 | Off | Off | High | Low | – | ½ Step 2 |
| 0 | 1 | 1 | 0 | Low | High | High | Low | Full Step 2 | ½ Step 3 |
| 0 | 1 | 0 | 0 | Low | High | Off | Off | – | ½ Step 4 |
| 0 | 1 | 0 | 1 | Low | High | Low | High | Full Step 3 | ½ Step 5 |
| 0 | 0 | 0 | 1 | Off | Off | Low | High | – | ½ Step 6 |
| 1 | 0 | 0 | 1 | High | Low | Low | High | Full Step 4 | ½ Step 7 |
| 1 | 0 | 0 | 0 | High | Low | Off | Off | – | ½ Step 8 |

FUNCTIONAL DESCRIPTION

Device Operation. The A3906 is a dual full-bridge low voltage motor driver capable of operating one stepper motor, two DC motors, or one high current DC motor. MOSFET output stages substantially reduce the voltage drop and the power dissipation of the outputs of the A3906, compared to typical drivers with bipolar transistors.

Output current can be regulated by pulse width modulating (PWM) the inputs. In addition, supporting external PWM of the driver, the A3906 limits the peak current by internally PWMing the source driver when the current in the winding exceeds the peak current, which is determined by a sense resistor. A fault output notifies the user that peak current was reached. If internal current limiting is not needed, the sense pin should be shorted to ground.

Internal circuit protection includes thermal shutdown with hysteresis, undervoltage lockout, internal clamp diodes, and crossover current protection.

The A3906 is designed for portable applications, providing a power-off low current sleep mode and an operating voltage of 2.5 to 9 V.

External PWM. Output current regulation can be achieved by pulse width modulating the inputs. Slow decay mode is selected by holding one input high while PWMing the other input. Holding one input low and PWMing the other input results in fast decay. Refer to the Applications Information section for further information.

Blanking. This function blanks the output of the current sense comparator when the outputs are switched. The comparator output is blanked to prevent false overcurrent detections due to reverse recovery currents of the clamp diodes or to switching transients related to the capacitance of the load. The blank time, t_{BLANK} , is approximately 3 μs .

Sleep Mode. An active-low control input used to minimize power consumption when the A3906 is not in use. This disables much of the internal circuitry including the output drivers, internal regulator, and charge pump. A logic high allows normal operation. When coming out of sleep mode, wait 1.5 ms before issuing a command, to allow the internal regulator and charge pump to stabilize.

Enable. When all logic inputs are pulled to logic low, the outputs of the bridges are disabled. The charge pump and internal circuitry continue to run when the outputs are disabled.

Charge Pump. (CP1, CP2, CP3, and CP4) When supply voltages are lower than 3.5 V, the two-stage charge pump triples the input voltage to a maximum of 7 V above the supply. The charge pump is used to create a supply voltage greater than V_{BB} , to drive the source-side DMOS gates. For pumping purposes, a 0.1 μF ceramic capacitor should be connected between CP1 and CP2, and between CP3 and CP4. A 0.1 μF ceramic capacitor is required between VCP and VBB, to act as a reservoir to operate the high-side DMOS devices.

Thermal Shutdown. The A3906 will disable the outputs if the junction temperature reaches 165°C. When the junction temperature drops 15°C, the outputs will be enabled.

Brake Mode. When driving DC motors, the A3906 goes into brake mode (turns on both sink drivers) when both of its inputs are high (IN1 and IN2, or IN3 and IN4). There is no protection during braking, so care must be taken to ensure that the peak current during braking does not exceed the absolute maximum current.

Internal PWM Current Control. Each full-bridge is controlled by a fixed off-time PWM current control circuit that limits the load current to a desired value, I_{TRIP} . Initially, a diagonal pair of source and sink DMOS outputs are enabled and current flows through the motor winding and the current sense resistor, R_{Sx} . When the voltage across R_{Sx} equals the internal reference voltage, the current sense comparator resets the PWM latch, which turns off the source driver.

The maximum value of current limiting, $I_{\text{TRIP}(\text{max})}$, is set by the selection of the sense resistor, R_{Sx} , and is approximated by a transconductance function:

$$I_{\text{TRIP}(\text{max})} = 0.2 / R_{\text{S}} .$$

It is critical to ensure the maximum rating on SENSEx pins (0.5 V) is not exceeded.

Synchronous Rectification. When a PWM off-cycle is triggered by an internal fixed off-time cycle, load current recirculates in slow decay SR mode. During slow decay, current recirculates through the sink-side FET and the sink-side body diode. The SR feature enables the sink-side FET, effectively shorting out the body diode. The sink driver is not enabled until the source driver is turned off and the crossover delay has expired. This feature helps lower the voltage drop during current recirculation, lowering power dissipation in the bridge.

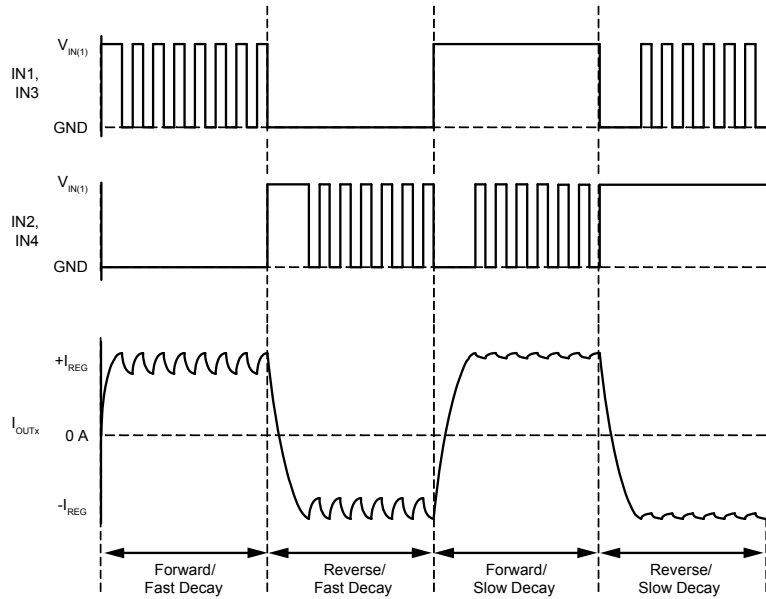
Overcurrent Output Flag. When the peak current (set by the external resistor) is reached, the fault pin, FLx, is pulled low. When a reset of the PWM latch occurs, the fault timer begins. At each PWM latch reset, the timer is reset to zero. After approximately 300 μ s, if no peak current event was triggered, the timer expires and the fault is released. This ensures that during PWM current limiting, the fault pin remains in a fault state.

APPLICATIONS INFORMATION

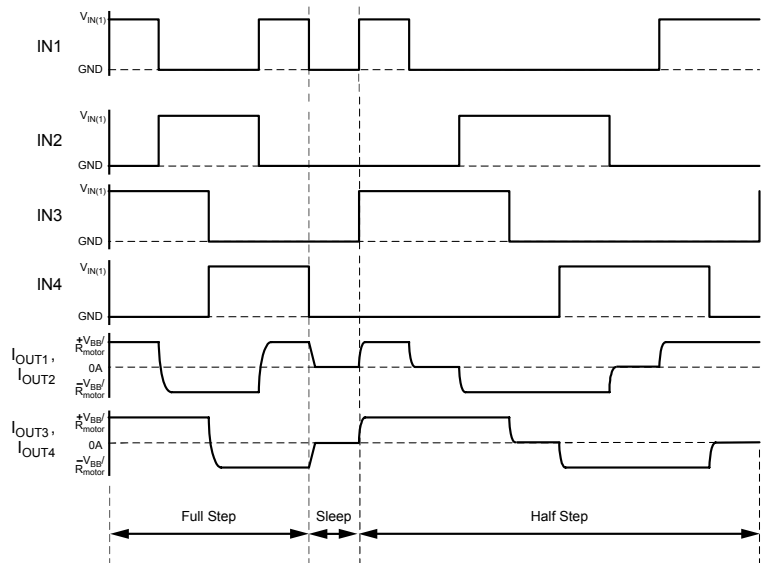
External PWM. If external PWM is used, the internal current control can either be disabled by shorting the SENSEx pin to ground, or it can be used to limit the peak current to a value under the stall current to prevent motor heating. External PWM IN1 control is shown in the upper figure.

Stepper Motor Control. The A3906 also can be used to control a bipolar stepper motor. The control logic for stepper motor control is shown in the lower figure. The driver is capable of operating in full- and half-step modes.

PWM current control in fast and slow decay modes



Stepper motor control in full- and half-step modes



Parallel Operation. The A3906 can be paralleled for applications that require higher output currents. In paralleled mode the driver can source 2 A continuous. The A3906 has two completely independent bridges with separate overcurrent latches. This allows the device to supply two separate loads, and as a result, when paralleled it is imperative that the internal current control is disabled by shorting the sense pins to ground.

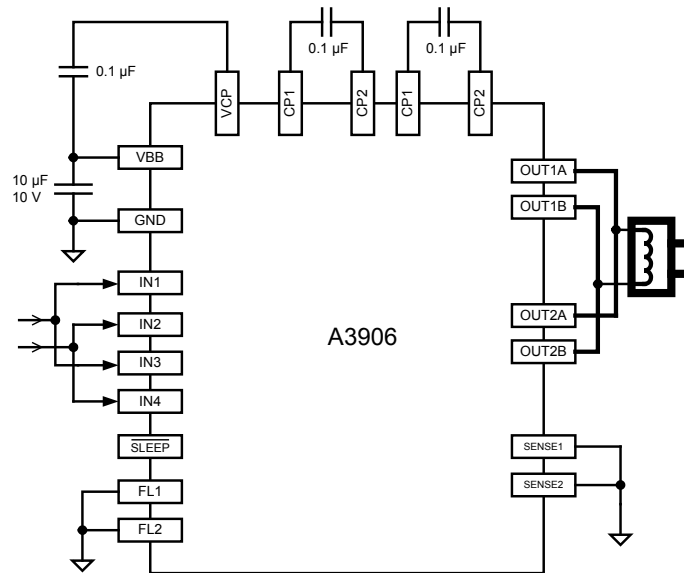
Because the overcurrent trip threshold is internally fixed at 0.2 V, the trace resistance must be kept small so the internal current latch is not triggered prematurely. With acceptable margin, the voltage drop across the trace resistance should be under 0.1 V. At a peak current of 2.5 A, the trace resistance should be kept below 40 mΩ to prevent false tripping of the overcurrent latch.

Each bridge has some variation in propagation delay. During this time it is possible that one bridge will have to support the full

load current for a very short period of time. Propagation delays are characterized and guard banded to protect the driver from damage during these events.

Layout. The printed circuit board should use a heavy ground-plane. For optimum electrical and thermal performance, the A3906 must be soldered directly onto the board. On the underside of the A3906 package is an exposed pad, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to an exposed surface on the PCB. Thermal vias are used to transfer heat to other layers of the PCB.

Grounding. In order to minimize the effects of ground bounce and offset issues, it is important to have a low impedance single-point ground, known as a *star ground*, located very close to the device. By making the connection between the exposed thermal pad and the ground plane directly under the A3906, that area



DC Motor Operation (Parallel Bridge)

| IN1/IN3 | IN2/IN4 | OUT1A/2A | OUT1B/2B | Function |
|---------|---------|----------|----------|----------|
| 0 | 0 | OFF | OFF | Disabled |
| 1 | 0 | H | L | FOR |
| 0 | 1 | L | H | REV |
| 1 | 1 | L | L | BRAKE |

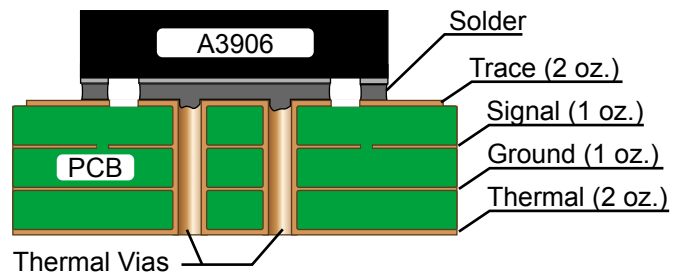
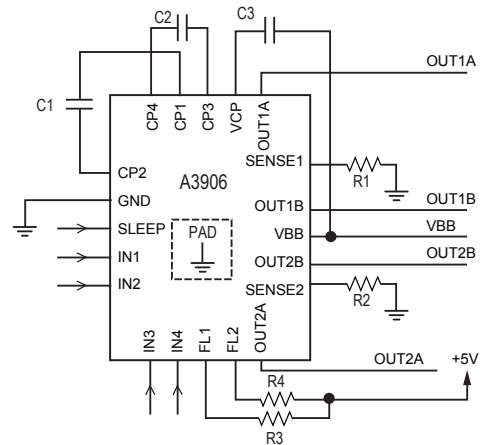
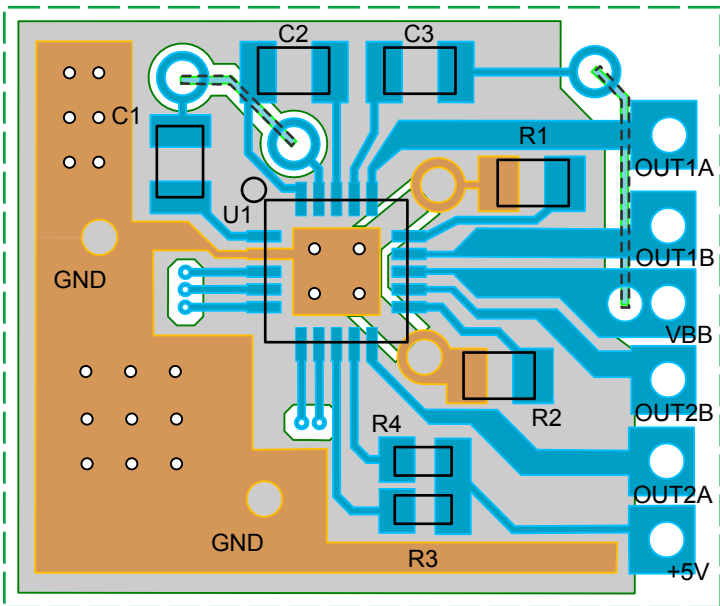
becomes an ideal location for a star ground point. A low impedance ground will prevent ground bounce during high current operation and ensure that the supply voltage remains stable at the input terminal. The recommended PCB layout shown in the diagram below, illustrates how to create a star ground under the device, to serve both as low impedance ground point and thermal path.

The two input capacitors should be placed in parallel, and as close to the device supply pins as possible. The ceramic capacitor should be closer to the pins than the bulk capacitor. This is necessary because the ceramic capacitor will be responsible for delivering the high frequency current components.

Sense Pins. The sense resistors, RS_x , should have a very low impedance path to ground, because they must carry a large current while supporting very accurate voltage measurements by the current sense comparators. Long ground traces will cause additional voltage drops, adversely affecting the ability of the comparators to accurately measure the current in the windings. As shown in the layout below, the SENSE x pins have very short traces to the RS_x resistors and very thick, low impedance traces directly to the star ground underneath the device. If possible, there should be no other components on the sense circuits.

Note: When selecting a value for the sense resistors, be sure not to exceed the maximum voltage on the SENSE x pins of ± 500 mV.

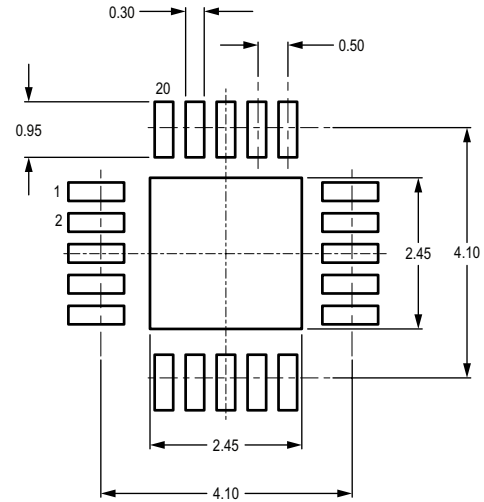
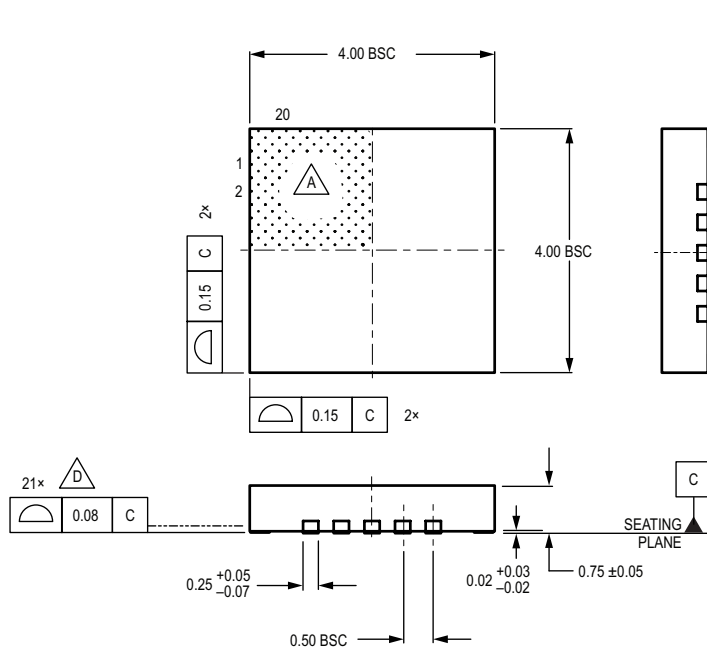
PCB Layout



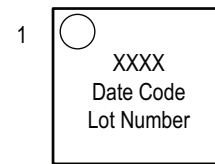
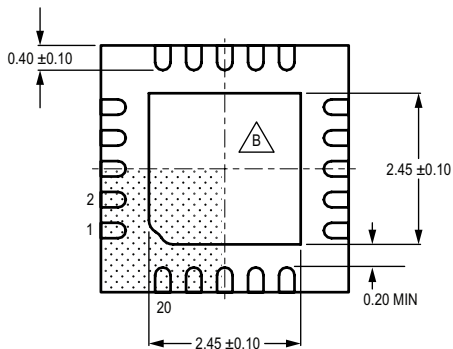
ES PACKAGE, 20-CONTACT QFN WITH EXPOSED THERMAL PAD

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000222 Rev. 4 or JEDEC MO-220WGGD)
 Dimensions in millimeters – NOT TO SCALE
 Exact case and lead configuration at supplier discretion within limits shown



C PCB Layout Reference View



E Standard Branding Reference View

Lines 1, 2, 3 = 6 characters

Line 1: Part Number
 Line 2: 4 digit Date Code
 Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Pin 1 Dot top left
 Center align

- A** Terminal #1 mark area
- B** Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)
- C** Reference land pattern layout (reference IPC7351 QFN50P400X400X80-21BM); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)
- D** Coplanarity includes exposed thermal pad and terminals
- E** Branding scale and appearance at supplier discretion.

Revision History

| Number | Date | Description |
|--------|----------------|---|
| 5 | April 4, 2019 | Minor editorial updates |
| 6 | March 25, 2022 | Updated package drawing (page 12) and minor editorial updates |

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