



**THE DATASHEET OF
A1280A-PQ160I**



ACT 2 Family FPGAs

Features

- Up to 8,000 Gate Array Gates (20,000 PLD equivalent gates)
- Replaces up to 200 TTL Packages
- Replaces up to eighty 20-Pin PAL[®] Packages
- Design Library with over 500 Macro Functions
- Single-Module Sequence Functions
- Wide-Input Combinatorial Functions
- Up to 1,232 Programmable Logic Modules
- Up to 998 Flip-Flops
- Datapath Performance at 105 MHz
- 16-Bit Accumulator Performance to 39 MHz
- Two In-Circuit Diagnostic Probe Pins Support Speed Analysis to 50 MHz
- Two High-Speed, Low-Skew Clock Networks
- I/O Drive to 10 mA
- Nonvolatile, User Programmable
- Logic Fully Tested Prior to Shipment
- 1.0 micron CMOS Technology

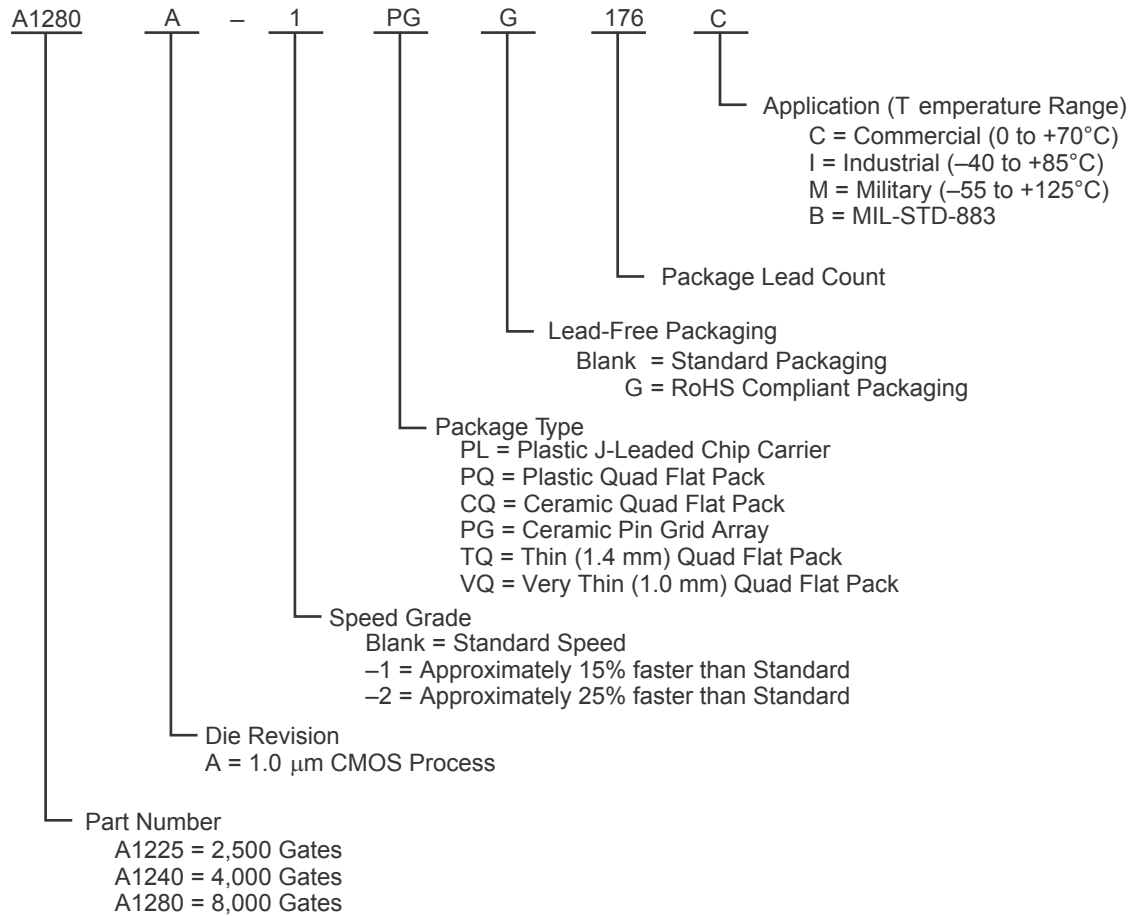
Table 1 • ACT 2 Product Family Profile

| Device | A1225A | A1240A | A1280A |
|--------------------------------|---------|---------|---------|
| Capacity | | | |
| Gate Array Equivalent Gates | 2,500 | 4,000 | 8,000 |
| PLD Equivalent Gates | 6,250 | 10,000 | 20,000 |
| TTL Equivalent Package | 63 | 100 | 200 |
| 20-Pin PAL Equivalent Packages | 25 | 40 | 80 |
| Logic Modules | | | |
| S-Module | 231 | 348 | 624 |
| C-Module | 220 | 336 | 608 |
| Flip-Flops (maximum) | 382 | 568 | 998 |
| Routing Resources | | | |
| Horizontal Tracks/Channel | 36 | 36 | 36 |
| Vertical Tracks/Channel | 15 | 15 | 15 |
| PLICE Antifuse Elements | 250,000 | 400,000 | 750,000 |
| User I/Os (maximum) | 83 | 104 | 140 |
| Performance¹ | | | |
| 16-Bit Prescaled Counters | 105 MHz | 100 MHz | 85 MHz |
| 16-Bit Loadable Counters | 70 MHz | 69 MHz | 67 MHz |
| 16-Bit Accumulators | 39 MHz | 38 MHz | 36 MHz |
| Packages² | | | |
| CPGA | PG100 | PG132 | PG176 |
| PLCC | PL84 | PL84 | PL84 |
| PQFP | PQ100 | PQ144 | PQ160 |
| VQFP | VQ100 | – | – |
| TQFP | – | TQ176 | TQ176 |
| CQFP | – | – | CQ172 |

Notes:

1. Performance is based on –2 speed devices at commercial worst-case operating conditions using PREP Benchmarks, Suite #1, Version 1.2, dated 3-28-93. Any analysis is not endorsed by PREP.
2. See the "Product Plan" on page III for package availability.

Ordering Information



Product Plan

| Device/Package | Speed Grade ¹ | | | Application ¹ | | | |
|---|--------------------------|----|----|--------------------------|---|---|---|
| | Std. | -1 | -2 | C | I | M | B |
| A1225A Device | | | | | | | |
| 84-Pin Plastic Leaded Chip Carrier (PL) | ✓ | ✓ | ✓ | ✓ | ✓ | - | - |
| 100-Pin Plastic Quad Flatpack (PQ) | ✓ | ✓ | ✓ | ✓ | ✓ | - | - |
| 100-Pin Very Thin Quad Flatpack (VQ) | ✓ | ✓ | ✓ | ✓ | - | - | - |
| 100-Pin Ceramic Pin Grid Array (PG) | ✓ | ✓ | ✓ | ✓ | - | - | - |
| A1240A Device | | | | | | | |
| 84-Pin Plastic Leaded Chip Carrier (PL) | ✓ | ✓ | ✓ | ✓ | ✓ | - | - |
| 132-Pin Ceramic Pin Grid Array (PG) | ✓ | ✓ | ✓ | ✓ | - | ✓ | ✓ |
| 144-Pin Plastic Quad Flat Pack (PQ) | ✓ | ✓ | ✓ | ✓ | ✓ | - | - |
| 176-Pin Thin (1.4 mm) Quad Flat Pack (TQ) | ✓ | ✓ | ✓ | ✓ | - | - | - |
| A1280A Device | | | | | | | |
| 160-Pin Plastic Quad Flatpack (PQ) | ✓ | ✓ | ✓ | ✓ | ✓ | - | - |
| 172-Pin Ceramic Quad Flatpack (CQ) | ✓ | ✓ | ✓ | ✓ | - | ✓ | ✓ |
| 176-Pin Ceramic Pin Grid Array (PG) | ✓ | ✓ | ✓ | ✓ | - | ✓ | ✓ |
| 176-Pin Thin (1.4 mm) Quad Flat Pack (TQ) | ✓ | ✓ | ✓ | ✓ | - | - | - |

Notes:

1. Applications:
 C = Commercial
 I = Industrial
 M = Military
 B = MIL-STD-883

- Availability:
 ✓ = Available
 P = Planned
 - = Not planned

- Speed Grade:
 -1 = Approx. 15% faster than Std.
 -2 = Approx. 25% faster than Std.

2. Contact your Microsemi SoC Products Group sales representative for product availability.

Device Resources

| Device Series | Logic Modules | Gates | User I/Os | | | | | | | | | |
|---------------|---------------|-------|-----------|-------|-------|-------|-------|-------|------|-------|-------|-------|
| | | | PG176 | PG132 | PG100 | PQ160 | PQ144 | PQ100 | PL84 | CQ172 | TQ176 | VQ100 |
| A1225A | 451 | 2,500 | - | - | 83 | - | - | 83 | 72 | - | - | 83 |
| A1240A | 684 | 4,000 | - | 104 | - | - | 104 | - | 72 | - | 104 | - |
| A1280A | 1,232 | 8,000 | 140 | - | - | 125 | - | - | 72 | 140 | 140 | - |

Contact your local Microsemi SoC Products Group representative for device availability:

<http://www.microsemi.com/soc/contact/default.aspx>.

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1 – ACT 2 Family Overview

General Description

The ACT 2 family represents Actel's second generation of field programmable gate arrays (FPGAs). The ACT 2 family presents a two-module architecture, consisting of C-modules and S-modules. These modules are optimized for both combinatorial and sequential designs. Based on Actel's patented channeled array architecture, the ACT 2 family provides significant enhancements to gate density and performance while maintaining downward compatibility with the ACT 1 design environment and upward compatibility with the ACT 3 design environment. The devices are implemented in silicon gate, 1.0- μm , two-level metal CMOS, and employ Actel's PLICE® antifuse technology. This revolutionary architecture offers gate array design flexibility, high performance, and fast time-to-production with user programming. The ACT 2 family is supported by the Designer and Designer Advantage Systems, which offers automatic pin assignment, validation of electrical and design rules, automatic placement and routing, timing analysis, user programming, and diagnostic probe capabilities. The systems are supported on the following platforms: 386/486™ PC, Sun™, and HP™ workstations. The systems provide CAE interfaces to the following design environments: Cadence, Viewlogic®, Mentor Graphics®, and OrCAD™.

2 – Detailed Specifications

Operating Conditions

Table 2-1 • Absolute Maximum Ratings¹

| Symbol | Parameter | Limits | Units |
|------------------|--------------------------------------|-------------------|-------|
| VCC | DC supply voltage | –0.5 to +7.0 | V |
| VI | Input voltage | –0.5 to VCC + 0.5 | V |
| VO | Output voltage | –0.5 to VCC + 0.5 | V |
| IIO | I/O source sink current ² | ±20 | mA |
| T _{STG} | Storage temperature | –65 to +150 | °C |

Notes:

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the recommended operating conditions.
2. Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than VCC + 0.5 V for less than GND –0.5 V, the internal protection diodes will be forward biased and can draw excessive current.

Table 2-2 • Recommended Operating Conditions

| Parameter | Commercial | Industrial | Military | Units |
|------------------------|------------|------------|-------------|-------|
| Temperature range* | 0 to +70 | –40 to +85 | –55 to +125 | °C |
| Power supply tolerance | ±5 | ±10 | ±10 | %VCC |

Note: *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.

Table 2-3 • Electrical Specifications

| Symbol | Parameter | Commercial | | Industrial | | Military | | Units |
|--|--|------------|-----------|------------|-----------|----------|-----------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| VOH ¹ | (IOH = -10 mA) ² | 2.4 | - | - | - | - | - | V |
| | (IOH = -6 mA) | 3.84 | - | - | - | - | - | V |
| | (IOH = -4 mA) | - | - | 3.7 | - | 3.7 | - | V |
| VOL ¹ | (IOL = 10 mA) ² | - | 0.5 | - | - | - | - | V |
| | (IOL = 6 mA) | - | 0.33 | - | 0.40 | - | 0.40 | V |
| VIL | | -0.3 | 0.8 | -0.3 | 0.8 | -0.3 | 0.8 | V |
| VIH | | 2.0 | VCC + 0.3 | 2.0 | VCC + 0.3 | 2.0 | VCC + 0.3 | V |
| Input Transition Time t _R , t _F ² | | - | 500 | - | 500 | - | 500 | ns |
| C _{IO} I/O capacitance ^{2,3} | | - | 10 | - | 10 | - | 10 | pF |
| Standby Current, ICC ⁴ (typical = 1 mA) | | - | 2 | - | 10 | - | 20 | mA |
| Leakage Current ⁵ | | -10 | +10 | -10 | +10 | -10 | +10 | μA |
| ICC(D) | Dynamic VCC supply current. See the Power Dissipation section. | | | | | | | |

Notes:

1. Only one output tested at a time. VCC = minimum.
2. Not tested, for information only.
3. Includes worst-case PG176 package capacitance. VOUT = 0 V, f = 1 MHz
4. All outputs unloaded. All inputs = VCC or GND, typical ICC = 1 mA. ICC limit includes IPP and ISV during normal operations.
5. VOUT, VIN = VCC or GND.

Package Thermal Characteristics

The device junction to case thermal characteristic is θ_{jc} , and the junction to ambient air characteristic is θ_{ja} . The thermal characteristics for θ_{ja} are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a PQ160 package at commercial temperature and still air is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja} \text{ °C/W}} = \frac{150\text{°C} - 70\text{°C}}{33\text{°C/W}} = 2.4 \text{ W}$$

EQ 1

Table 2-4 • Package Thermal Characteristics

| Package Type* | Pin Count | θ_{jc} | θ_{ja} Still Air | θ_{ja} 300 ft./min. | Units |
|------------------------------------|-----------|---------------|----------------------------|-------------------------------|-------|
| Ceramic Pin Grid Array | 100 | 5 | 35 | 17 | °C/W |
| | 132 | 5 | 30 | 15 | °C/W |
| | 176 | 8 | 23 | 12 | °C/W |
| Ceramic Quad Flatpack | 172 | 8 | 25 | 15 | °C/W |
| Plastic Quad Flatpack ¹ | 100 | 13 | 48 | 40 | °C/W |
| | 144 | 15 | 40 | 32 | °C/W |
| | 160 | 15 | 38 | 30 | °C/W |
| Plastic Leaded Chip Carrier | 84 | 12 | 37 | 28 | °C/W |
| Very Thin Quad Flatpack | 100 | 12 | 43 | 35 | °C/W |
| Thin Quad Flatpack | 176 | 15 | 32 | 25 | °C/W |

Notes: (Maximum Power in Still Air)

1. Maximum power dissipation values for PQFP packages are 1.9 W (PQ100), 2.3 W (PQ144), and 2.4 W (PQ160).
2. Maximum power dissipation for PLCC packages is 2.7 W.
3. Maximum power dissipation for VQFP packages is 2.3 W.
4. Maximum power dissipation for TQFP packages is 3.1 W.

Power Dissipation

$$P = [\text{ICC standby} + \text{ICC active}] * V_{CC} + \text{IOL} * \text{VOL} * N + \text{IOH} * (V_{CC} - \text{VOH}) * M$$

EQ 2

where:

ICC standby is the current flowing when no inputs or outputs are changing

ICC active is the current flowing due to CMOS switching.

IOL and IOH are TTL sink/source currents.

VOL and VOH are TTL level output voltages.

N is the number of outputs driving TTL loads to VOL.

M is the number of outputs driving TTL loads to VOH.

An accurate determination of N and M is problematical because their values depend on the family type, design details, and on the system I/O. The power can be divided into two components: static and active.

Static Power Component

Microsemi FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated in [Table 2-5](#) for commercial, worst case conditions.

Table 2-5 • Standby Power Calculation

| ICC | VCC | Power |
|------|--------|---------|
| 2 mA | 5.25 V | 10.5 mW |

The static power dissipated by TTL loads depends on the number of outputs driving high or low and the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33 V will generate 42 mW with all outputs driving low, and 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs.

An additional component of the active power dissipation is the totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by [EQ 3](#).

$$\text{Power } (\mu\text{W}) = C_{\text{EQ}} * V_{\text{CC}}^2 * F$$

EQ 3

Where:

C_{EQ} is the equivalent capacitance expressed in pF.

VCC is the power supply in volts.

F is the switching frequency in MHz.

Equivalent capacitance is calculated by measuring ICC active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown in [Table 2-6](#).

Table 2-6 • CEQ Values for Microsemi FPGAs

| Item | CEQ Value |
|---|-----------|
| Modules (C_{EQM}) | 5.8 |
| Input Buffers (C_{EQI}) | 12.9 |
| Output Buffers (C_{EQO}) | 23.8 |
| Routed Array Clock Buffer Loads (C_{EQCR}) | 3.9 |

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. EQ 4 shows a piece-wise linear summation over all components.

$$\begin{aligned} \text{Power} = & VCC^2 * [(m * C_{EQM} * f_m)_{\text{modules}} + (n * C_{EQI} * f_n)_{\text{inputs}} \\ & + (p * (C_{EQO} + C_L) * f_p)_{\text{outputs}} \\ & + 0.5 * (q1 * C_{EQCR} * f_{q1})_{\text{routed_Clk1}} + (r1 * f_{q1})_{\text{routed_Clk1}} \\ & + 0.5 * (q2 * C_{EQCR} * f_{q2})_{\text{routed_Clk2}} + (r2 * f_{q2})_{\text{routed_Clk2}} \end{aligned}$$

EQ 4

Where:

- m = Number of logic modules switching at f_m
- n = Number of input buffers switching at f_n
- p = Number of output buffers switching at f_p
- q1 = Number of clock loads on the first routed array clock
- q2 = Number of clock loads on the second routed array clock
- r1 = Fixed capacitance due to first routed array clock
- r2 = Fixed capacitance due to second routed array clock
- C_{EQM} = Equivalent capacitance of logic modules in pF
- C_{EQI} = Equivalent capacitance of input buffers in pF
- C_{EQO} = Equivalent capacitance of output buffers in pF
- C_{EQCR} = Equivalent capacitance of routed array clock in pF
- C_L = Output lead capacitance in pF
- f_m = Average logic module switching rate in MHz
- f_n = Average input buffer switching rate in MHz
- f_p = Average output buffer switching rate in MHz
- f_{q1} = Average first routed array clock rate in MHz
- f_{q2} = Average second routed array clock rate in MHz

Table 2-7 • Fixed Capacitance Values for Microsemi FPGAs

| Device Type | r1, routed_Clk1 | r2, routed_Clk2 |
|-------------|-----------------|-----------------|
| A1225A | 106 | 106.0 |
| A1240A | 134 | 134.2 |
| A1280A | 168 | 167.8 |

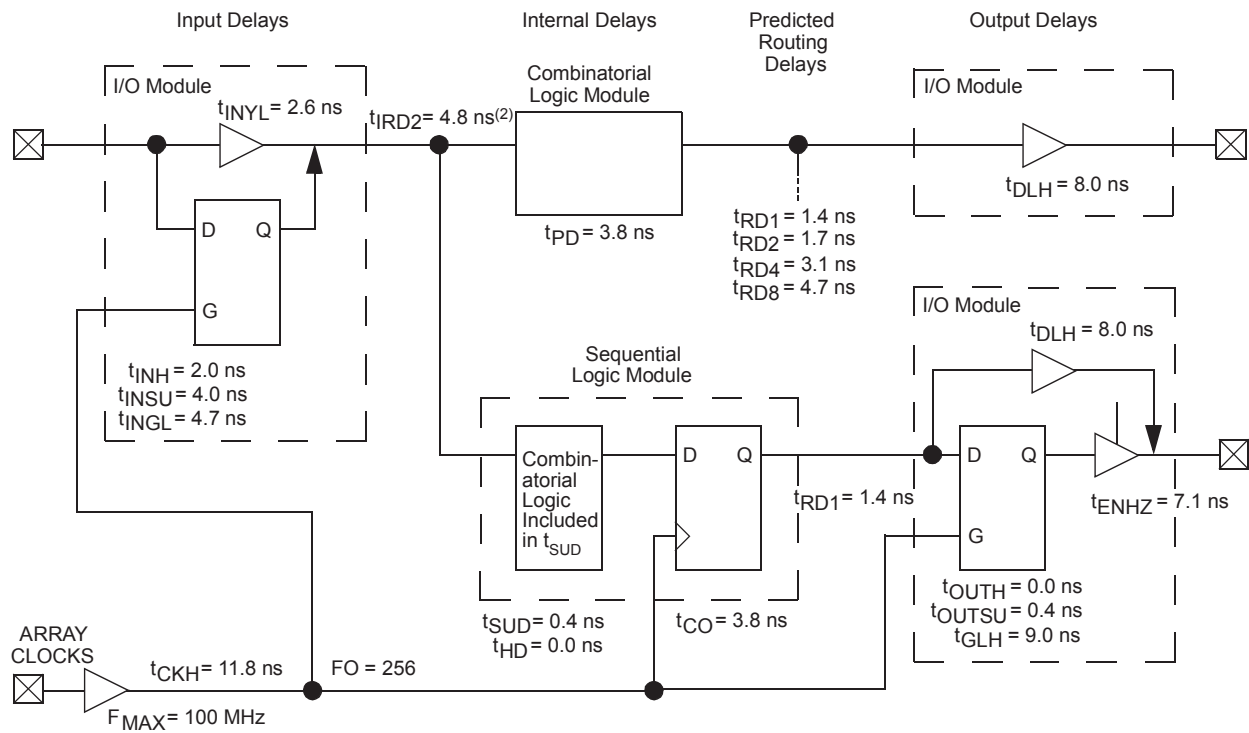
Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are given in Table 2-8.

Table 2-8 • Guidelines for Predicting Power Dissipation

| Data | Value |
|---|---------------------------|
| Logic Modules (m) | 80% of modules |
| Inputs switching (n) | # inputs/4 |
| Outputs switching (p) | # output/4 |
| First routed array clock loads (q1) | 40% of sequential modules |
| Second routed array clock loads (q2) | 40% of sequential modules |
| Load capacitance (C_L) | 35 pF |
| Average logic module switching rate (f_m) | F/10 |
| Average input switching rate (f_n) | F/5 |
| Average output switching rate (f_p) | F/10 |
| Average first routed array clock rate (f_{q1}) | F |
| Average second routed array clock rate (f_{q2}) | F/2 |

ACT 2 Timing Model¹



Notes:

1. Values shown for A1240A-2 at worst-case commercial conditions.
2. Input module predicted routing delay

Figure 2-1 • Timing Model

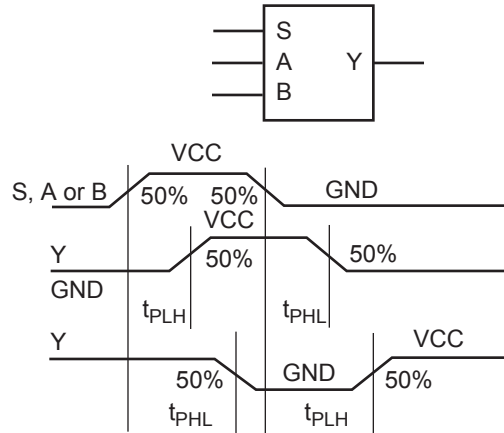
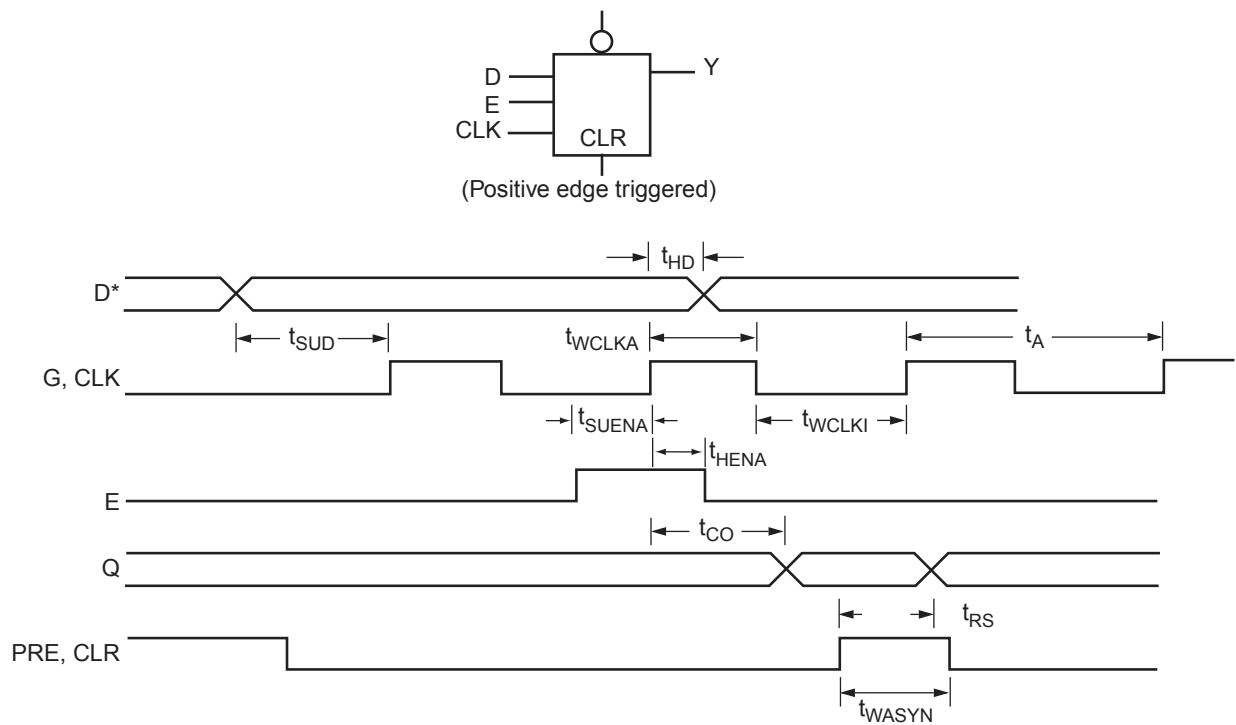


Figure 2-5 • Module Delays

Sequential Module Timing Characteristics



Note: D represents all data functions involving A, B, and S for multiplexed flip-flops.

Figure 2-6 • Flip-Flops and Latches

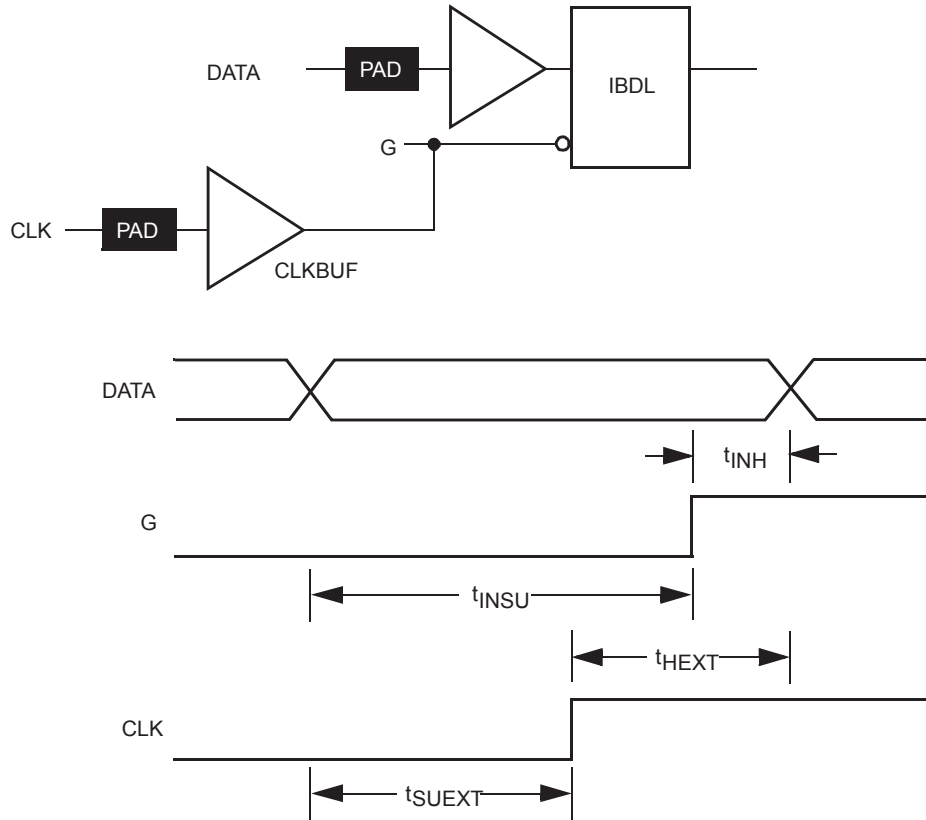


Figure 2-7 • Input Buffer Latches

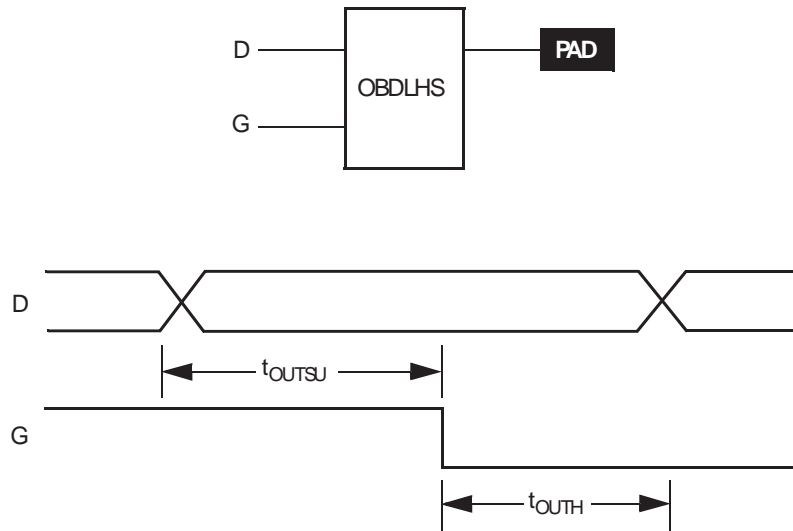


Figure 2-8 • Output Buffer Latches

Timing Derating Factor (Temperature and Voltage)

Table 2-9 • Timing Derating Factor (Temperature and Voltage)

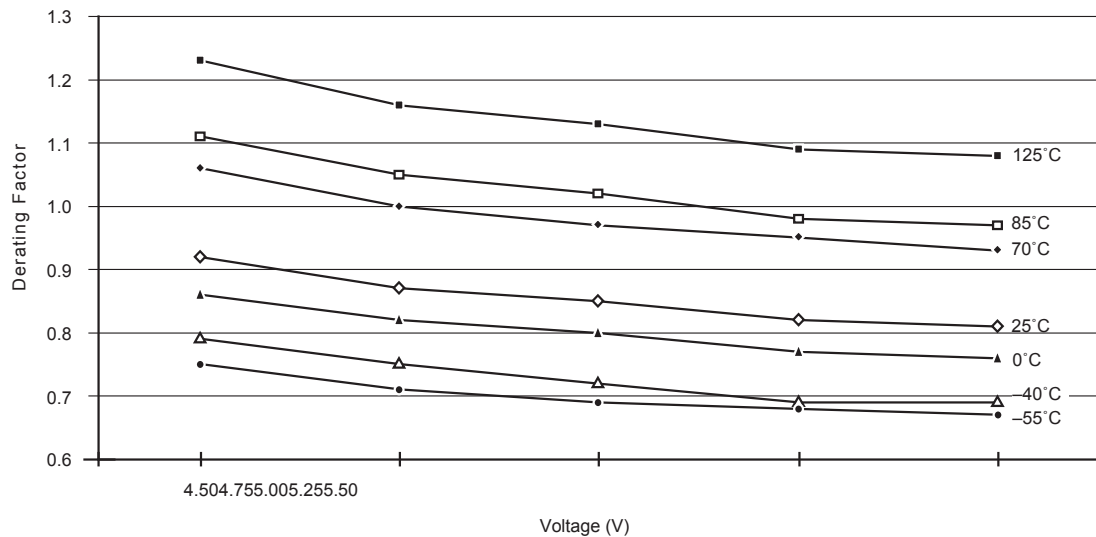
| | | | | |
|--|------------|------|----------|------|
| (Commercial Minimum/Maximum Specification) x | Industrial | | Military | |
| | Min. | Max. | Min. | Max. |
| | 0.69 | 1.11 | 0.67 | 1.23 |

Table 2-10 • Timing Derating Factor for Designs at Typical Temperature ($T_J = 25^\circ\text{C}$) and Voltage (5.0 V)

| | |
|--------------------------------------|------|
| (Commercial Maximum Specification) x | 0.85 |
|--------------------------------------|------|

Table 2-11 • Temperature and Voltage Derating Factors (normalized to Worst-Case Commercial, $T_J = 4.75\text{ V}, 70^\circ\text{C}$)

| | -55 | -40 | 0 | 25 | 70 | 85 | 125 |
|-------------|------|------|------|------|------|------|------|
| 4.50 | 0.75 | 0.79 | 0.86 | 0.92 | 1.06 | 1.11 | 1.23 |
| 4.75 | 0.71 | 0.75 | 0.82 | 0.87 | 1.00 | 1.05 | 1.13 |
| 5.00 | 0.69 | 0.72 | 0.80 | 0.85 | 0.97 | 1.02 | 1.13 |
| 5.25 | 0.68 | 0.69 | 0.77 | 0.82 | 0.95 | 0.98 | 1.09 |
| 5.50 | 0.67 | 0.69 | 0.76 | 0.81 | 0.93 | 0.97 | 1.08 |



Note: This derating factor applies to all routing and propagation delays.

Figure 2-9 • Junction Temperature and Voltage Derating Curves (normalized to Worst-Case Commercial, $T_J = 4.75\text{ V}, 70^\circ\text{C}$)

A1225A Timing Characteristics

Table 2-12 • A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

| Logic Module Propagation Delays ¹ | | -2 Speed ³ | | -1 Speed | | Std. Speed | | Units |
|--|--|-----------------------|-------|----------|------|------------|------|-------|
| Parameter/Description | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{PD1} | Single Module | | 3.8 | | 4.3 | | 5.0 | ns |
| t _{CO} | Sequential Clock to Q | | 3.8 | | 4.3 | | 5.0 | ns |
| t _{GO} | Latch G to Q | | 3.8 | | 4.3 | | 5.0 | ns |
| t _{RS} | Flip-Flop (Latch) Reset to Q | | 3.8 | | 4.3 | | 5.0 | ns |
| Predicted Routing Delays ² | | | | | | | | |
| t _{RD1} | FO = 1 Routing Delay | | 1.1 | | 1.2 | | 1.4 | ns |
| t _{RD2} | FO = 2 Routing Delay | | 1.7 | | 1.9 | | 2.2 | ns |
| t _{RD3} | FO = 3 Routing Delay | | 2.3 | | 2.6 | | 3.0 | ns |
| t _{RD4} | FO = 4 Routing Delay | | 2.8 | | 3.1 | | 3.7 | ns |
| t _{RD8} | FO = 8 Routing Delay | | 4.4 | | 4.9 | | 5.8 | ns |
| Sequential Timing Characteristics ^{3,4} | | | | | | | | |
| t _{SUD} | Flip-Flop (Latch) Data Input Setup | 0.4 | | 0.4 | | 0.5 | | ns |
| t _{HD} | Flip-Flop (Latch) Data Input Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{SUENA} | Flip-Flop (Latch) Enable Setup | 0.8 | | 0.9 | | 1.0 | | ns |
| t _{HENA} | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{WCLKA} | Flip-Flop (Latch) Clock Active Pulse Width | 4.5 | | 5.0 | | 6.0 | | ns |
| t _{WASYN} | Flip-Flop (Latch) Clock Asynchronous Pulse Width | 4.5 | | 5.0 | | 6.0 | | ns |
| t _A | Flip-Flop Clock Input Period | 9.4 | | 11.0 | | 13.0 | | ns |
| t _{INH} | Input Buffer Latch Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{INSU} | Input Buffer Latch Setup | 0.4 | | 0.4 | | 0.5 | | ns |
| t _{OUTH} | Output Buffer Latch Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{OUTSU} | Output Buffer Latch Setup | 0.4 | | 0.4 | | 0.5 | | ns |
| f _{MAX} | Flip-Flop (Latch) Clock Frequency | | 105.0 | | 90.0 | | 75.0 | MHz |

Notes:

- For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}—whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.
- Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1225A Timing Characteristics (continued)

Table 2-13 • A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

| I/O Module Input Propagation Delays | | | -2 Speed | | -1 Speed | | Std. Speed | | Units |
|---|----------------------------|----------|----------|-------|----------|-------|------------|-------|-------|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{INYH} | Pad to Y High | | 2.9 | | 3.3 | | 3.8 | ns | |
| t _{INYL} | Pad to Y Low | | 2.6 | | 3.0 | | 3.5 | ns | |
| t _{INGH} | G to Y High | | 5.0 | | 5.7 | | 6.6 | ns | |
| t _{INGL} | G to Y Low | | 4.7 | | 5.4 | | 6.3 | ns | |
| Input Module Predicted Input Routing Delays* | | | | | | | | | |
| t _{IRD1} | FO = 1 Routing Delay | | 4.1 | | 4.6 | | 5.4 | ns | |
| t _{IRD2} | FO = 2 Routing Delay | | 4.6 | | 5.2 | | 6.1 | ns | |
| t _{IRD3} | FO = 3 Routing Delay | | 5.3 | | 6.0 | | 7.1 | ns | |
| t _{IRD4} | FO = 4 Routing Delay | | 5.7 | | 6.4 | | 7.6 | ns | |
| t _{IRD8} | FO = 8 Routing Delay | | 7.4 | | 8.3 | | 9.8 | ns | |
| Global Clock Network | | | | | | | | | |
| t _{CKH} | Input Low to High | FO = 32 | | 10.2 | | 11.0 | | 12.8 | ns |
| | | FO = 256 | | 11.8 | | 13.0 | | 15.7 | |
| t _{CKL} | Input High to Low | FO = 32 | | 10.2 | | 11.0 | | 12.8 | ns |
| | | FO = 256 | | 12.0 | | 13.2 | | 15.9 | |
| t _{PWH} | Minimum Pulse Width High | FO = 32 | 3.4 | | 4.1 | | 4.5 | ns | |
| | | FO = 256 | 3.8 | | 4.5 | | 5.0 | | |
| t _{PWL} | Minimum Pulse Width Low | FO = 32 | 3.4 | | 4.1 | | 4.5 | ns | |
| | | FO = 256 | 3.8 | | 4.5 | | 5.0 | | |
| t _{CKSW} | Maximum Skew | FO = 32 | | 0.7 | | 0.7 | | 0.7 | ns |
| | | FO = 256 | | 3.5 | | 3.5 | | 3.5 | |
| t _{SUEXT} | Input Latch External Setup | FO = 32 | 0.0 | | 0.0 | | 0.0 | ns | |
| | | FO = 256 | 0.0 | | 0.0 | | 0.0 | | |
| t _{HEXT} | Input Latch External Hold | FO = 32 | 7.0 | | 7.0 | | 7.0 | ns | |
| | | FO = 256 | 11.2 | | 11.2 | | 11.2 | | |
| t _P | Minimum Period | FO = 32 | 7.7 | | 8.3 | | 9.1 | ns | |
| | | FO = 256 | 8.1 | | 8.8 | | 10.0 | | |
| f _{MAX} | Maximum Frequency | FO = 32 | | 130.0 | | 120.0 | | 110.0 | ns |
| | | FO = 256 | | 125.0 | | 115.0 | | 100.0 | |

Note: *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1225A Timing Characteristics (continued)

Table 2-14 • A1225A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

| TTL Output Module Timing ¹ | | -2 Speed | | -1 Speed | | Std. Speed | | Units |
|--|----------------------|----------|------|----------|------|------------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{DLH} | Data to Pad High | | 8.0 | | 9.0 | | 10.6 | ns |
| t _{DHL} | Data to Pad Low | | 10.1 | | 11.4 | | 13.4 | ns |
| t _{ENZH} | Enable Pad Z to High | | 8.9 | | 10.0 | | 11.8 | ns |
| t _{ENZL} | Enable Pad Z to Low | | 11.6 | | 13.2 | | 15.5 | ns |
| t _{ENHZ} | Enable Pad High to Z | | 7.1 | | 8.0 | | 9.4 | ns |
| t _{ENLZ} | Enable Pad Low to Z | | 8.3 | | 9.5 | | 11.1 | ns |
| t _{GLH} | G to Pad High | | 8.9 | | 10.2 | | 11.9 | ns |
| t _{GHL} | G to Pad Low | | 11.2 | | 12.7 | | 14.9 | ns |
| d _{TLH} | Delta Low to High | | 0.07 | | 0.08 | | 0.09 | ns/pF |
| d _{THL} | Delta High to Low | | 0.12 | | 0.13 | | 0.16 | ns/pF |
| CMOS Output Module Timing ¹ | | | | | | | | |
| t _{DLH} | Data to Pad High | | 10.1 | | 11.5 | | 13.5 | ns |
| t _{DHL} | Data to Pad Low | | 8.4 | | 9.6 | | 11.2 | ns |
| t _{ENZH} | Enable Pad Z to High | | 8.9 | | 10.0 | | 11.8 | ns |
| t _{ENZL} | Enable Pad Z to Low | | 11.6 | | 13.2 | | 15.5 | ns |
| t _{ENHZ} | Enable Pad High to Z | | 7.1 | | 8.0 | | 9.4 | ns |
| t _{ENLZ} | Enable Pad Low to Z | | 8.3 | | 9.5 | | 11.1 | ns |
| t _{GLH} | G to Pad High | | 8.9 | | 10.2 | | 11.9 | ns |
| t _{GHL} | G to Pad Low | | 11.2 | | 12.7 | | 14.9 | ns |
| d _{TLH} | Delta Low to High | | 0.12 | | 0.13 | | 0.16 | ns/pF |
| d _{THL} | Delta High to Low | | 0.09 | | 0.10 | | 0.12 | ns/pF |

Notes:

1. Delays based on 50 pF loading.
2. SSO information can be found at www.microsemi.com/soc/techdocs/appnotes/board_consideration.aspx.

A1240A Timing Characteristics

Table 2-15 • A1240A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

| Logic Module Propagation Delays ¹ | | -2 Speed ³ | | -1 Speed | | Std. Speed | | Units |
|--|--|-----------------------|-------|----------|------|------------|------|-------|
| Parameter/Description | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{PD1} | Single Module | | 3.8 | | 4.3 | | 5.0 | ns |
| t _{CO} | Sequential Clock to Q | | 3.8 | | 4.3 | | 5.0 | ns |
| t _{GO} | Latch G to Q | | 3.8 | | 4.3 | | 5.0 | ns |
| t _{RS} | Flip-Flop (Latch) Reset to Q | | 3.8 | | 4.3 | | 5.0 | ns |
| Predicted Routing Delays² | | | | | | | | |
| t _{RD1} | FO = 1 Routing Delay | | 1.4 | | 1.5 | | 1.8 | ns |
| t _{RD2} | FO = 2 Routing Delay | | 1.7 | | 2.0 | | 2.3 | ns |
| t _{RD3} | FO = 3 Routing Delay | | 2.3 | | 2.6 | | 3.0 | ns |
| t _{RD4} | FO = 4 Routing Delay | | 3.1 | | 3.5 | | 4.1 | ns |
| t _{RD8} | FO = 8 Routing Delay | | 4.7 | | 5.4 | | 6.3 | ns |
| Sequential Timing Characteristics^{3,4} | | | | | | | | |
| t _{SUD} | Flip-Flop (Latch) Data Input Setup | 0.4 | | 0.4 | | 0.5 | | ns |
| t _{HD} | Flip-Flop (Latch) Data Input Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{SUENA} | Flip-Flop (Latch) Enable Setup | 0.8 | | 0.9 | | 1.0 | | ns |
| t _{HENA} | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{WCLKA} | Flip-Flop (Latch) Clock Active Pulse Width | 4.5 | | 6.0 | | 6.5 | | ns |
| t _{WASYN} | Flip-Flop (Latch) Clock Asynchronous Pulse Width | 4.5 | | 6.0 | | 6.5 | | ns |
| t _A | Flip-Flop Clock Input Period | 9.8 | | 12.0 | | 15.0 | | ns |
| t _{INH} | Input Buffer Latch Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{INSU} | Input Buffer Latch Setup | 0.4 | | 0.4 | | 0.5 | | ns |
| t _{OUTH} | Output Buffer Latch Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{OUTSU} | Output Buffer Latch Setup | 0.4 | | 0.4 | | 0.5 | | ns |
| f _{MAX} | Flip-Flop (Latch) Clock Frequency | | 100.0 | | 80.0 | | 66.0 | MHz |

Notes:

- For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}—whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.
- Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1240A Timing Characteristics (continued)

Table 2-16 • A1240A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

| I/O Module Input Propagation Delays | | | -2 Speed | | -1 Speed | | Std. Speed | | Units |
|---|----------------------------|----------|----------|-------|----------|-------|------------|------|-------|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{INYH} | Pad to Y High | | 2.9 | | 3.3 | | 3.8 | ns | |
| t _{INYL} | Pad to Y Low | | 2.6 | | 3.0 | | 3.5 | ns | |
| t _{INGH} | G to Y High | | 5.0 | | 5.7 | | 6.6 | ns | |
| t _{INGL} | G to Y Low | | 4.7 | | 5.4 | | 6.3 | ns | |
| Input Module Predicted Input Routing Delays* | | | | | | | | | |
| t _{IRD1} | FO = 1 Routing Delay | | 4.2 | | 4.8 | | 5.6 | ns | |
| t _{IRD2} | FO = 2 Routing Delay | | 4.8 | | 5.4 | | 6.4 | ns | |
| t _{IRD3} | FO = 3 Routing Delay | | 5.4 | | 6.1 | | 7.2 | ns | |
| t _{IRD4} | FO = 4 Routing Delay | | 5.9 | | 6.7 | | 7.9 | ns | |
| t _{IRD8} | FO = 8 Routing Delay | | 7.9 | | 8.9 | | 10.5 | ns | |
| Global Clock Network | | | | | | | | | |
| t _{CKH} | Input Low to High | FO = 32 | | 10.2 | | 11.0 | | 12.8 | ns |
| | | FO = 256 | | 11.8 | | 13.0 | | 15.7 | |
| t _{CKL} | Input High to Low | FO = 32 | | 10.2 | | 11.0 | | 12.8 | ns |
| | | FO = 256 | | 12.0 | | 13.2 | | 15.9 | |
| t _{PWH} | Minimum Pulse Width High | FO = 32 | 3.8 | | 4.5 | | 5.5 | ns | |
| | | FO = 256 | 4.1 | | 5.0 | | 5.8 | | |
| t _{PWL} | Minimum Pulse Width Low | FO = 32 | 3.8 | | 4.5 | | 5.5 | ns | |
| | | FO = 256 | 4.1 | | 5.0 | | 5.8 | | |
| t _{CKSW} | Maximum Skew | FO = 32 | | 0.5 | | 0.5 | | 0.5 | ns |
| | | FO = 256 | | 2.5 | | 2.5 | | 2.5 | |
| t _{SUEXT} | Input Latch External Setup | FO = 32 | 0.0 | | 0.0 | | 0.0 | ns | |
| | | FO = 256 | 0.0 | | 0.0 | | 0.0 | | |
| t _{HEXT} | Input Latch External Hold | FO = 32 | 7.0 | | 7.0 | | 7.0 | ns | |
| | | FO = 256 | 11.2 | | 11.2 | | 11.2 | | |
| t _P | Minimum Period | FO = 32 | 8.1 | | 9.1 | | 11.1 | ns | |
| | | FO = 256 | 8.8 | | 10.0 | | 11.7 | | |
| f _{MAX} | Maximum Frequency | FO = 32 | | 125.0 | | 110.0 | | 90.0 | ns |
| | | FO = 256 | | 115.0 | | 100.0 | | 85.0 | |

Note: *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1240A Timing Characteristics (continued)

Table 2-17 • A1240A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

| TTL Output Module Timing ¹ | | -2 Speed | | -1 Speed | | Std. Speed | | Units |
|--|----------------------|----------|------|----------|------|------------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{DLH} | Data to Pad High | | 8.0 | | 9.0 | | 10.6 | ns |
| t _{DHL} | Data to Pad Low | | 10.1 | | 11.4 | | 13.4 | ns |
| t _{ENZH} | Enable Pad Z to High | | 8.9 | | 10.0 | | 11.8 | ns |
| t _{ENZL} | Enable Pad Z to Low | | 11.7 | | 13.2 | | 15.5 | ns |
| t _{ENHZ} | Enable Pad High to Z | | 7.1 | | 8.0 | | 9.4 | ns |
| t _{ENLZ} | Enable Pad Low to Z | | 8.4 | | 9.5 | | 11.1 | ns |
| t _{GLH} | G to Pad High | | 9.0 | | 10.2 | | 11.9 | ns |
| t _{GHL} | G to Pad Low | | 11.2 | | 12.7 | | 14.9 | ns |
| d _{TLH} | Delta Low to High | | 0.07 | | 0.08 | | 0.09 | ns/pF |
| d _{THL} | Delta High to Low | | 0.12 | | 0.13 | | 0.16 | ns/pF |
| CMOS Output Module Timing ¹ | | | | | | | | |
| t _{DLH} | Data to Pad High | | 10.2 | | 11.5 | | 13.5 | ns |
| t _{DHL} | Data to Pad Low | | 8.4 | | 9.6 | | 11.2 | ns |
| t _{ENZH} | Enable Pad Z to High | | 8.9 | | 10.0 | | 11.8 | ns |
| t _{ENZL} | Enable Pad Z to Low | | 11.7 | | 13.2 | | 15.5 | ns |
| t _{ENHZ} | Enable Pad High to Z | | 7.1 | | 8.0 | | 9.4 | ns |
| t _{ENLZ} | Enable Pad Low to Z | | 8.4 | | 9.5 | | 11.1 | ns |
| t _{GLH} | G to Pad High | | 9.0 | | 10.2 | | 11.9 | ns |
| t _{GHL} | G to Pad Low | | 11.2 | | 12.7 | | 14.9 | ns |
| d _{TLH} | Delta Low to High | | 0.12 | | 0.13 | | 0.16 | ns/pF |
| d _{THL} | Delta High to Low | | 0.09 | | 0.10 | | 0.12 | ns/pF |

Notes:

1. Delays based on 50 pF loading.
2. SSO information can be found at www.microsemi.com/soc/techdocs/appnotes/board_consideration.aspx.

A1280A Timing Characteristics

Table 2-18 • A1280A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

| Logic Module Propagation Delays ¹ | | -2 Speed ³ | | -1 Speed | | Std. Speed | | Units |
|--|--|-----------------------|------|----------|------|------------|------|-------|
| Parameter/Description | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{PD1} | Single Module | | 3.8 | | 4.3 | | 5.0 | ns |
| t _{CO} | Sequential Clock to Q | | 3.8 | | 4.3 | | 5.0 | ns |
| t _{GO} | Latch G to Q | | 3.8 | | 4.3 | | 5.0 | ns |
| t _{RS} | Flip-Flop (Latch) Reset to Q | | 3.8 | | 4.3 | | 5.0 | ns |
| Predicted Routing Delays ² | | | | | | | | |
| t _{RD1} | FO = 1 Routing Delay | | 1.7 | | 2.0 | | 2.3 | ns |
| t _{RD2} | FO = 2 Routing Delay | | 2.5 | | 2.8 | | 3.3 | ns |
| t _{RD3} | FO = 3 Routing Delay | | 3.0 | | 3.4 | | 4.0 | ns |
| t _{RD4} | FO = 4 Routing Delay | | 3.7 | | 4.2 | | 4.9 | ns |
| t _{RD8} | FO = 8 Routing Delay | | 6.7 | | 7.5 | | 8.8 | ns |
| Sequential Timing Characteristics ^{3,4} | | | | | | | | |
| t _{SUD} | Flip-Flop (Latch) Data Input Setup | 0.4 | | 0.4 | | 0.5 | | ns |
| t _{HD} | Flip-Flop (Latch) Data Input Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{SUENA} | Flip-Flop (Latch) Enable Setup | 0.8 | | 0.9 | | 1.0 | | ns |
| t _{HENA} | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{WCLKA} | Flip-Flop (Latch) Clock Active Pulse Width | 5.5 | | 6.0 | | 7.0 | | ns |
| t _{WASYN} | Flip-Flop (Latch) Clock Asynchronous Pulse Width | 5.5 | | 6.0 | | 7.0 | | ns |
| t _A | Flip-Flop Clock Input Period | 11.7 | | 13.3 | | 18.0 | | ns |
| t _{INH} | Input Buffer Latch Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{INSU} | Input Buffer Latch Setup | 0.4 | | 0.4 | | 0.5 | | ns |
| t _{OUTH} | Output Buffer Latch Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{OUTSU} | Output Buffer Latch Setup | 0.4 | | 0.4 | | 0.5 | | ns |
| f _{MAX} | Flip-Flop (Latch) Clock Frequency | | 85.0 | | 75.0 | | 50.0 | MHz |

Notes:

1. For dual-module macros, use t_{PD1} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}—whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.
4. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1280A Timing Characteristics (continued)

Table 2-19 • A1280A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

| I/O Module Input Propagation Delays | | | -2 Speed | | -1 Speed | | Std. Speed | | Units |
|---|----------------------------|----------|----------|-------|----------|------|------------|------|-------|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{INYH} | Pad to Y High | | 2.9 | | 3.3 | | 3.8 | ns | |
| t _{INYL} | Pad to Y Low | | 2.7 | | 3.0 | | 3.5 | ns | |
| t _{INGH} | G to Y High | | 5.0 | | 5.7 | | 6.6 | ns | |
| t _{INGL} | G to Y Low | | 4.8 | | 5.4 | | 6.3 | ns | |
| Input Module Predicted Input Routing Delays* | | | | | | | | | |
| t _{IRD1} | FO = 1 Routing Delay | | 4.6 | | 5.1 | | 6.0 | ns | |
| t _{IRD2} | FO = 2 Routing Delay | | 5.2 | | 5.9 | | 6.9 | ns | |
| t _{IRD3} | FO = 3 Routing Delay | | 5.6 | | 6.3 | | 7.4 | ns | |
| t _{IRD4} | FO = 4 Routing Delay | | 6.5 | | 7.3 | | 8.6 | ns | |
| t _{IRD8} | FO = 8 Routing Delay | | 9.4 | | 10.5 | | 12.4 | ns | |
| Global Clock Network | | | | | | | | | |
| t _{CKH} | Input Low to High | FO = 32 | | 10.2 | | 11.0 | | 12.8 | ns |
| | | FO = 256 | | 13.1 | | 14.6 | | 17.2 | |
| t _{CKL} | Input High to Low | FO = 32 | | 10.2 | | 11.0 | | 12.8 | ns |
| | | FO = 256 | | 13.3 | | 14.9 | | 17.5 | |
| t _{PWH} | Minimum Pulse Width High | FO = 32 | 5.0 | | 5.5 | | 6.6 | ns | |
| | | FO = 256 | 5.8 | | 6.4 | | 7.6 | | |
| t _{PWL} | Minimum Pulse Width Low | FO = 32 | 5.0 | | 5.5 | | 6.6 | ns | |
| | | FO = 256 | 5.8 | | 6.4 | | 7.6 | | |
| t _{CKSW} | Maximum Skew | FO = 32 | | 0.5 | | 0.5 | | 0.5 | ns |
| | | FO = 256 | | 2.5 | | 2.5 | | 2.5 | |
| t _{SUEXT} | Input Latch External Setup | FO = 32 | 0.0 | | 0.0 | | 0.0 | ns | |
| | | FO = 256 | 0.0 | | 0.0 | | 0.0 | | |
| t _{HEXT} | Input Latch External Hold | FO = 32 | 7.0 | | 7.0 | | 7.0 | ns | |
| | | FO = 256 | 11.2 | | 11.2 | | 11.2 | | |
| t _P | Minimum Period | FO = 32 | 9.6 | | 11.2 | | 13.3 | ns | |
| | | FO = 256 | 10.6 | | 12.6 | | 15.3 | | |
| f _{MAX} | Maximum Frequency | FO = 32 | | 105.0 | | 90.0 | | 75.0 | ns |
| | | FO = 256 | | 95.0 | | 80.0 | | 65.0 | |

Note: *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1280A Timing Characteristics (continued)

Table 2-20 • A1280A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

| TTL Output Module Timing ¹ | | -2 Speed | | -1 Speed | | Std. Speed | | Units |
|--|----------------------|----------|------|----------|------|------------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{DLH} | Data to Pad High | | 8.1 | | 9.0 | | 10.6 | ns |
| t _{DHL} | Data to Pad Low | | 10.2 | | 11.4 | | 13.4 | ns |
| t _{ENZH} | Enable Pad Z to High | | 9.0 | | 10.0 | | 11.8 | ns |
| t _{ENZL} | Enable Pad Z to Low | | 11.8 | | 13.2 | | 15.5 | ns |
| t _{ENHZ} | Enable Pad High to Z | | 7.1 | | 8.0 | | 9.4 | ns |
| t _{ENLZ} | Enable Pad Low to Z | | 8.4 | | 9.5 | | 11.1 | ns |
| t _{GLH} | G to Pad High | | 9.0 | | 10.2 | | 11.9 | ns |
| t _{GHL} | G to Pad Low | | 11.3 | | 12.7 | | 14.9 | ns |
| d _{TLH} | Delta Low to High | | 0.07 | | 0.08 | | 0.09 | ns/pF |
| d _{THL} | Delta High to Low | | 0.12 | | 0.13 | | 0.16 | ns/pF |
| CMOS Output Module Timing ¹ | | | | | | | | |
| t _{DLH} | Data to Pad High | | 10.3 | | 11.5 | | 13.5 | ns |
| t _{DHL} | Data to Pad Low | | 8.5 | | 9.6 | | 11.2 | ns |
| t _{ENZH} | Enable Pad Z to High | | 9.0 | | 10.0 | | 11.8 | ns |
| t _{ENZL} | Enable Pad Z to Low | | 11.8 | | 13.2 | | 15.5 | ns |
| t _{ENHZ} | Enable Pad High to Z | | 7.1 | | 8.0 | | 9.4 | ns |
| t _{ENLZ} | Enable Pad Low to Z | | 8.4 | | 9.5 | | 11.1 | ns |
| t _{GLH} | G to Pad High | | 9.0 | | 10.2 | | 11.9 | ns |
| t _{GHL} | G to Pad Low | | 11.3 | | 12.7 | | 14.9 | ns |
| d _{TLH} | Delta Low to High | | 0.12 | | 0.13 | | 0.16 | ns/pF |
| d _{THL} | Delta High to Low | | 0.09 | | 0.10 | | 0.12 | ns/pF |

Notes:

1. Delays based on 50 pF loading.
2. SSO information can be found at www.microsemi.com/soc/techdocs/appnotes/board_consideration.aspx.

Pin Descriptions

CLKA Clock A (Input)

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKB Clock B (Input)

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK Diagnostic Clock (Input)

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

GND Ground

Low supply voltage.

I/O Input/Output (Input, Output)

The I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven Low by the ALS software.

MODE Mode (Input)

The MODE pin controls the use of multifunction pins (DCLK, PRA, PRB, SDI). When the MODE pin is High, the special functions are active. When the MODE pin is Low, the pins function as I/Os. To provide Actionprobe capability, the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled High when required.

NC No Connection

This pin is not connected to circuitry within the device.

PRA Probe A (Output)

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

PRB Probe B (Output)

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

SDI Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

SDO Serial Data Output (Output)

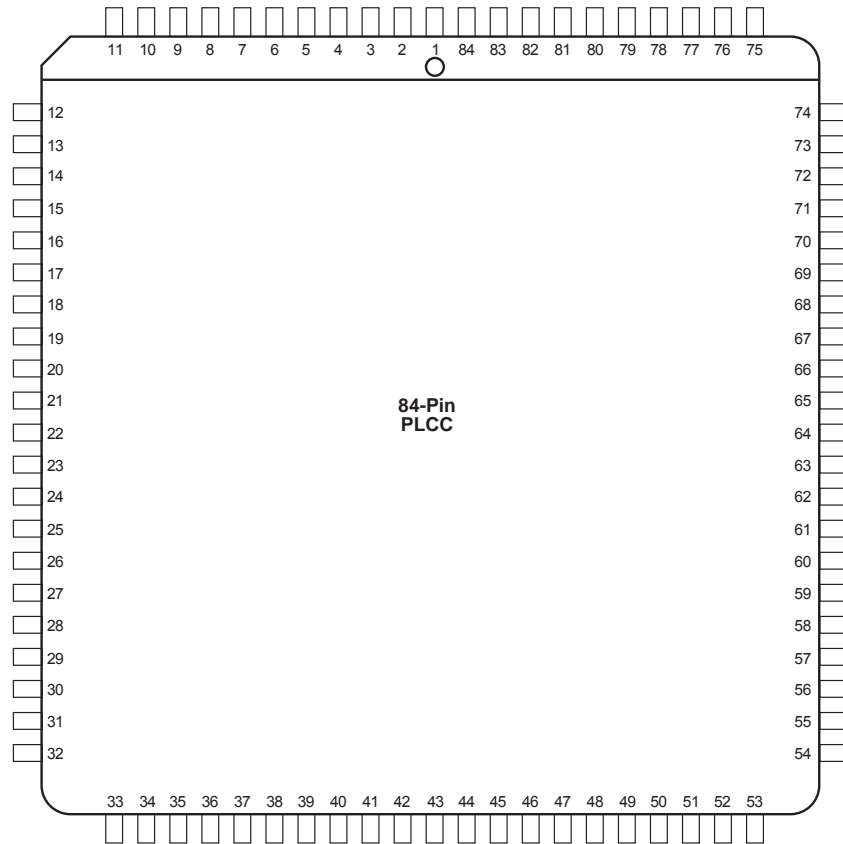
Serial data output for diagnostic probe. SDO is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

VCC 5.0 V Supply Voltage

High supply voltage.

3 – Package Pin Assignments

PL84



Note

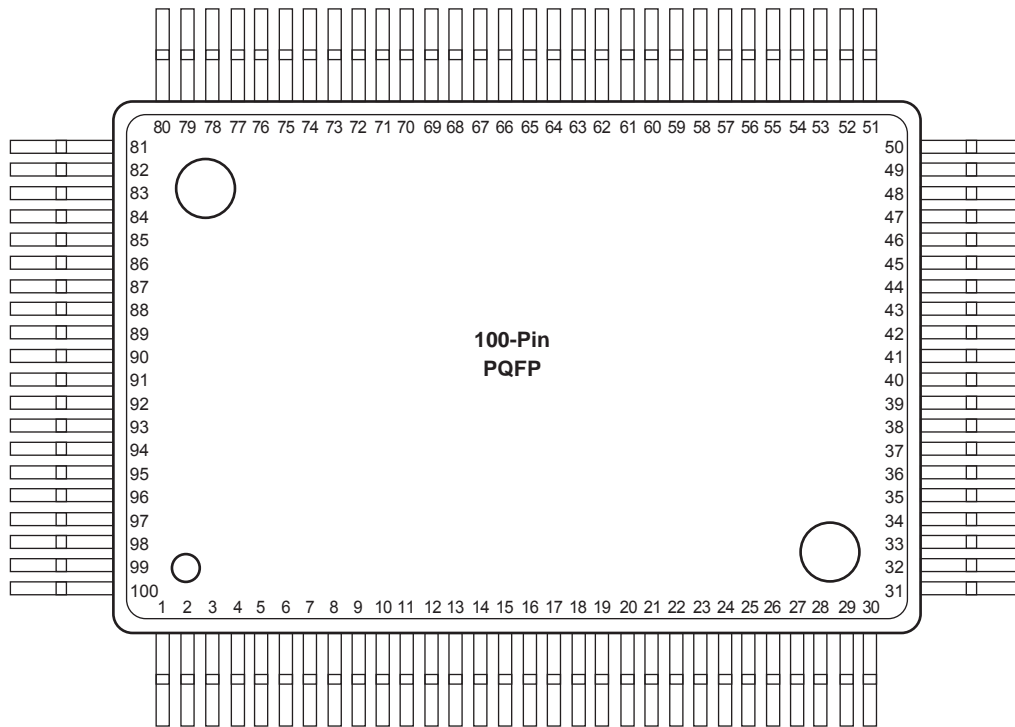
For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

| PL84 | | | |
|-------------------|------------------------|------------------------|------------------------|
| Pin Number | A1225A Function | A1240A Function | A1280A Function |
| 2 | CLKB, I/O | CLKB, I/O | CLKB, I/O |
| 4 | PRB, I/O | PRB, I/O | PRB, I/O |
| 6 | GND | GND | GND |
| 10 | DCLK, I/O | DCLK, I/O | DCLK, I/O |
| 12 | MODE | MODE | MODE |
| 22 | VCC | VCC | VCC |
| 23 | VCC | VCC | VCC |
| 28 | GND | GND | GND |
| 43 | VCC | VCC | VCC |
| 49 | GND | GND | GND |
| 52 | SDO | SDO | SDO |
| 63 | GND | GND | GND |
| 64 | VCC | VCC | VCC |
| 65 | VCC | VCC | VCC |
| 70 | GND | GND | GND |
| 76 | SDI, I/O | SDI, I/O | SDI, I/O |
| 81 | PRA, I/O | PRA, I/O | PRA, I/O |
| 83 | CLKA, I/O | CLKA, I/O | CLKA, I/O |
| 84 | VCC | VCC | VCC |

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PQ100



Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

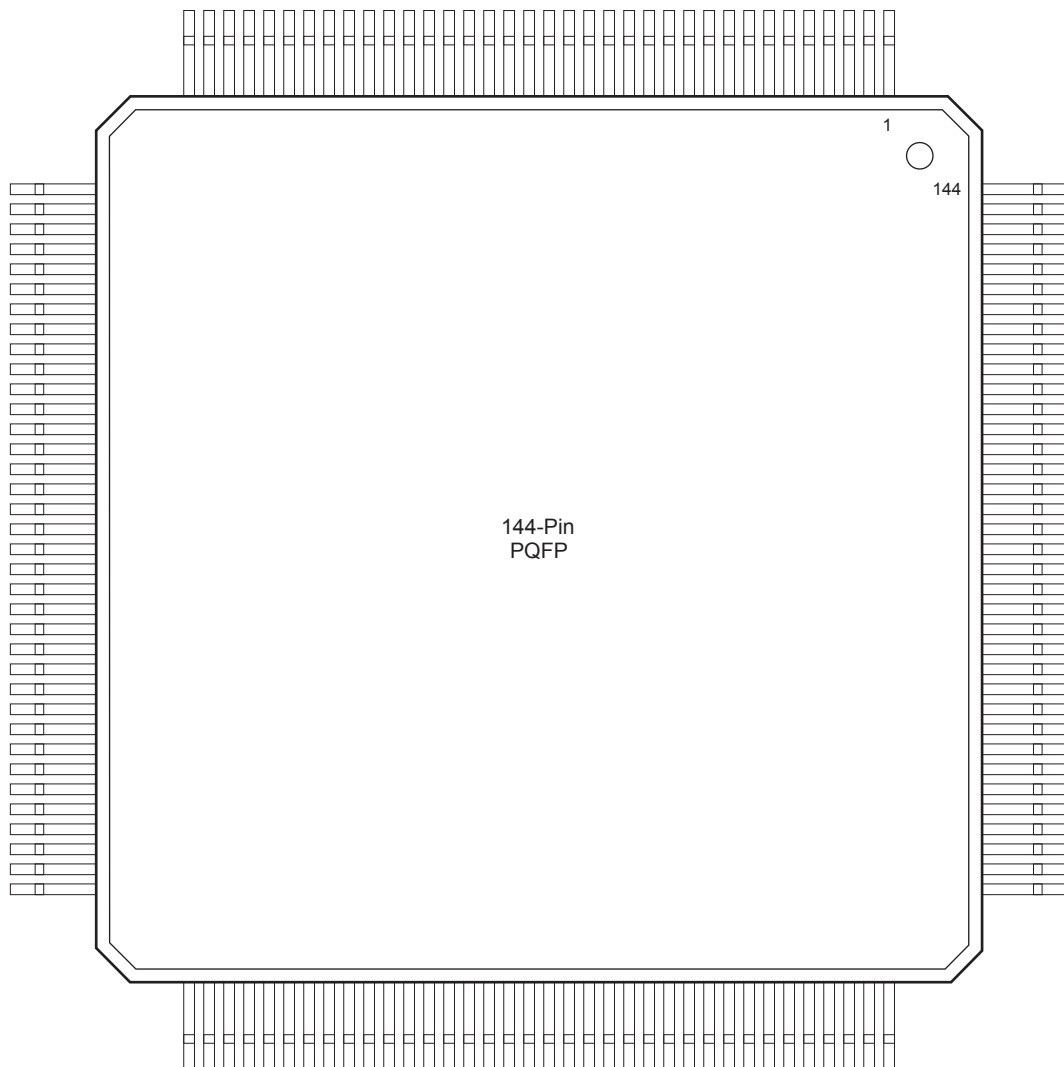
| PQ100 | |
|------------|-----------------|
| Pin Number | A1225A Function |
| 2 | DCLK, I/O |
| 4 | MODE |
| 9 | GND |
| 16 | VCC |
| 17 | VCC |
| 22 | GND |
| 34 | GND |
| 40 | VCC |
| 46 | GND |
| 52 | SDO |
| 57 | GND |
| 64 | GND |

| PQ100 | |
|------------|-----------------|
| Pin Number | A1225A Function |
| 65 | VCC |
| 66 | VCC |
| 67 | VCC |
| 72 | GND |
| 79 | SDI, I/O |
| 84 | GND |
| 87 | PRA, I/O |
| 89 | CLKA, I/O |
| 90 | VCC |
| 92 | CLKB, I/O |
| 94 | PRB, I/O |
| 96 | GND |

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PQ144



Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

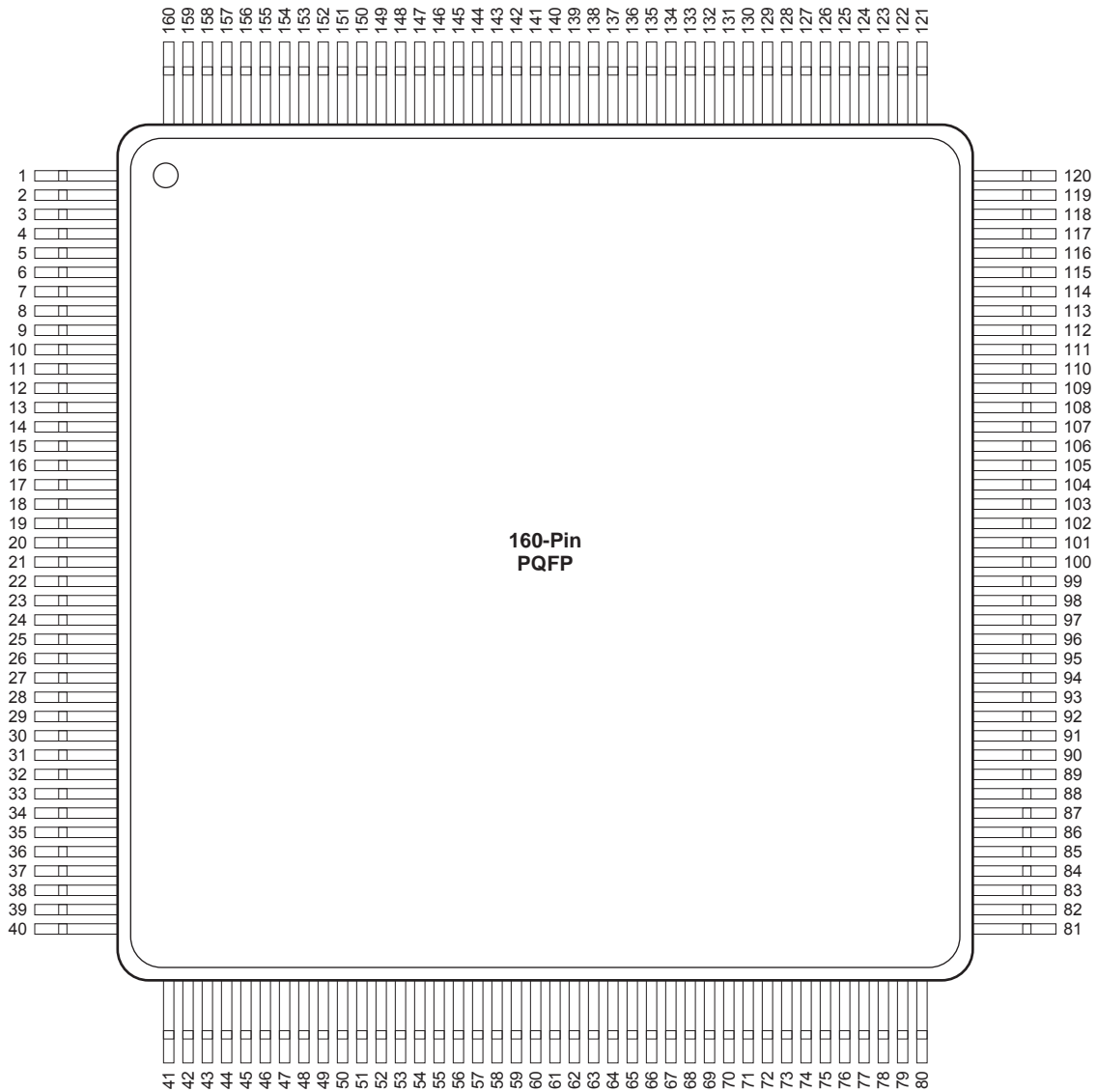
| PQ144 | |
|------------|-----------------|
| Pin Number | A1240A Function |
| 2 | MODE |
| 9 | GND |
| 10 | GND |
| 11 | GND |
| 18 | VCC |
| 19 | VCC |
| 20 | VCC |
| 21 | VCC |
| 28 | GND |
| 29 | GND |
| 30 | GND |
| 44 | GND |
| 45 | GND |
| 46 | GND |
| 54 | VCC |
| 55 | VCC |
| 56 | VCC |
| 64 | GND |
| 65 | GND |
| 71 | SDO |
| 79 | GND |
| 80 | GND |
| 81 | GND |
| 88 | GND |

| PQ144 | |
|------------|-----------------|
| Pin Number | A1240A Function |
| 89 | VCC |
| 90 | VCC |
| 91 | VCC |
| 92 | VCC |
| 93 | VCC |
| 100 | GND |
| 101 | GND |
| 102 | GND |
| 110 | SDI, I/O |
| 116 | GND |
| 117 | GND |
| 118 | GND |
| 123 | PRA, I/O |
| 125 | CLKA, I/O |
| 126 | VCC |
| 127 | VCC |
| 128 | VCC |
| 130 | CLKB, I/O |
| 132 | PRB, I/O |
| 136 | GND |
| 137 | GND |
| 138 | GND |
| 144 | DCLK, I/O |

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PQ160



Note: This is the top view of the package

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

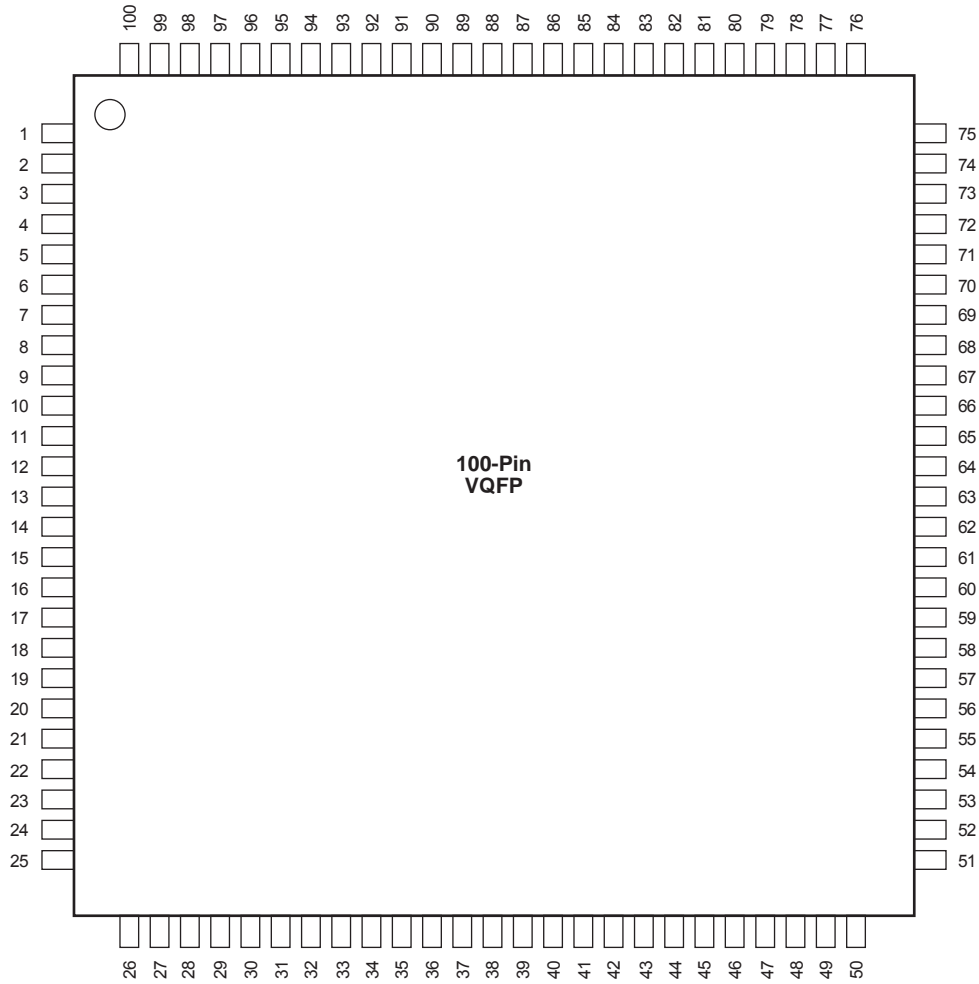
| PQ160 | |
|------------|-----------------|
| Pin Number | A1280A Function |
| 2 | DCLK, I/O |
| 6 | VCC |
| 11 | GND |
| 16 | PRB, I/O |
| 18 | CLKB, I/O |
| 20 | VCC |
| 21 | CLKA, I/O |
| 23 | PRA, I/O |
| 30 | GND |
| 35 | VCC |
| 38 | SDI, I/O |
| 40 | GND |
| 44 | GND |
| 49 | GND |
| 54 | VCC |
| 57 | VCC |
| 58 | VCC |
| 59 | GND |
| 60 | VCC |
| 61 | GND |
| 64 | GND |

| PQ160 | |
|------------|-----------------|
| Pin Number | A1280A Function |
| 69 | GND |
| 80 | GND |
| 82 | SDO |
| 86 | VCC |
| 89 | GN |
| 98 | GND |
| 99 | GND |
| 109 | GND |
| 114 | VCC |
| 120 | GND |
| 125 | GND |
| 130 | GND |
| 135 | VCC |
| 138 | VCC |
| 139 | VCC |
| 140 | GND |
| 145 | GND |
| 150 | VCC |
| 155 | GND |
| 159 | MODE |
| 160 | GND |

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

VQ100



Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

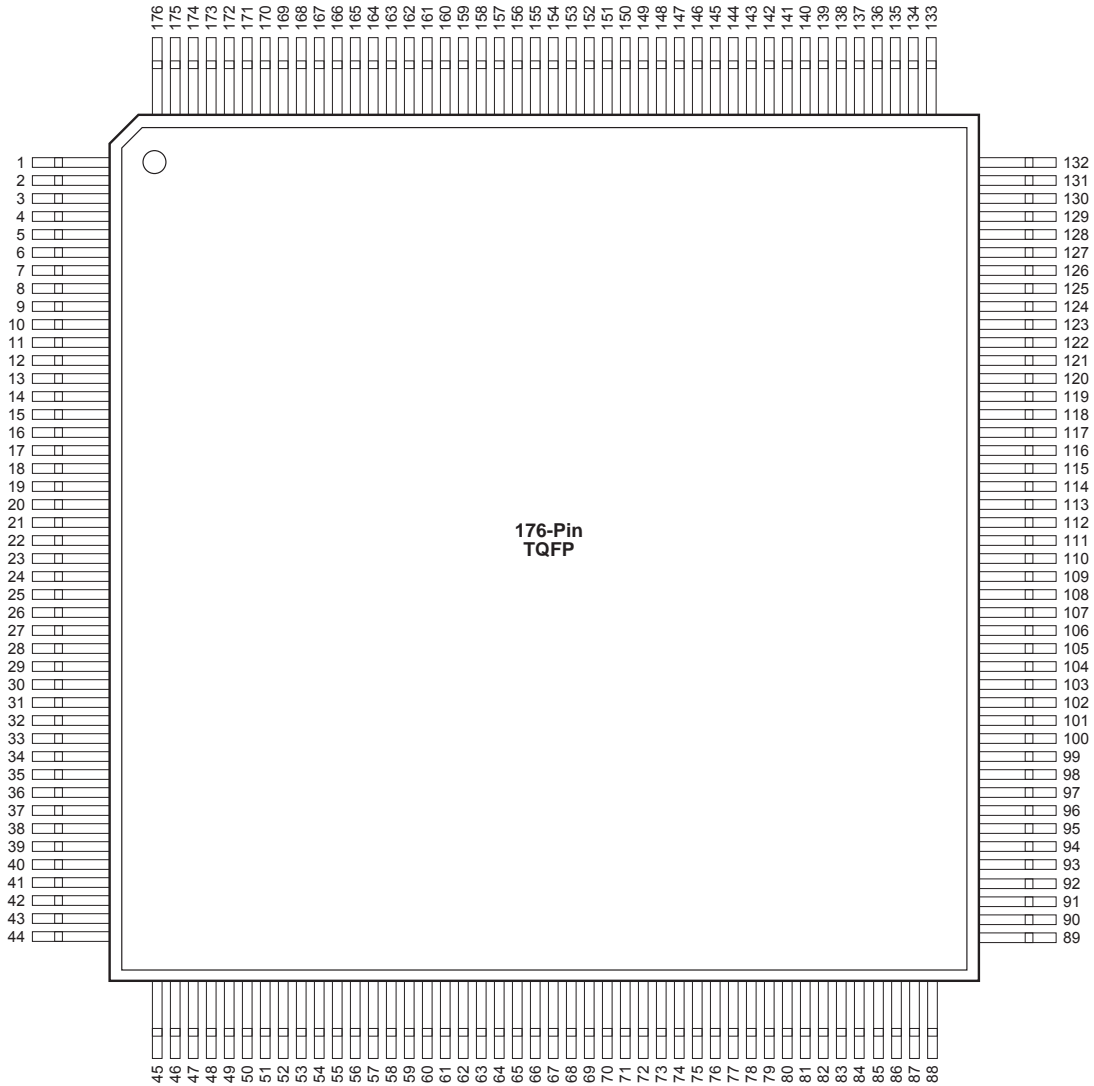
| VQ100 | |
|------------|-----------------|
| Pin Number | A1225A Function |
| 2 | MODE |
| 7 | GND |
| 14 | VCC |
| 15 | VCC |
| 20 | GND |
| 32 | GND |
| 38 | VCC |
| 44 | GND |
| 50 | SDO |
| 55 | GND |
| 62 | GND |
| 63 | VCC |

| VQ100 | |
|------------|-----------------|
| Pin Number | A1225A Function |
| 64 | VCC |
| 65 | VCC |
| 70 | GND |
| 77 | SDI, I/O |
| 82 | GND |
| 85 | PRA, I/O |
| 87 | CLKA, I/O |
| 88 | VCC |
| 90 | CLKB, I/O |
| 92 | PRB, I/O |
| 94 | GND |
| 100 | DCLK, I/O |

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

TQ176



Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

| TQ176 | | |
|------------|-----------------|-----------------|
| Pin Number | A1240A Function | A1280A Function |
| 1 | GND | GND |
| 2 | MODE | MODE |
| 8 | NC | NC |
| 10 | NC | I/O |
| 11 | NC | I/O |
| 13 | NC | VCC |
| 18 | GND | GND |
| 19 | NC | I/O |
| 20 | NC | I/O |
| 22 | NC | I/O |
| 23 | GND | GND |
| 24 | NC | VCC |
| 25 | VCC | VCC |
| 26 | NC | I/O |
| 27 | NC | I/O |
| 28 | VCC | VCC |
| 29 | NC | I/O |
| 33 | NC | NC |
| 37 | NC | I/O |
| 38 | NC | NC |
| 45 | GND | GND |
| 52 | NC | VCC |
| 54 | NC | I/O |
| 55 | NC | I/O |
| 57 | NC | NC |
| 61 | NC | I/O |
| 64 | NC | I/O |
| 66 | NC | I/O |
| 67 | GND | GND |
| 68 | VCC | VCC |
| 74 | NC | I/O |
| 77 | NC | NC |
| 78 | NC | I/O |
| 80 | NC | I/O |

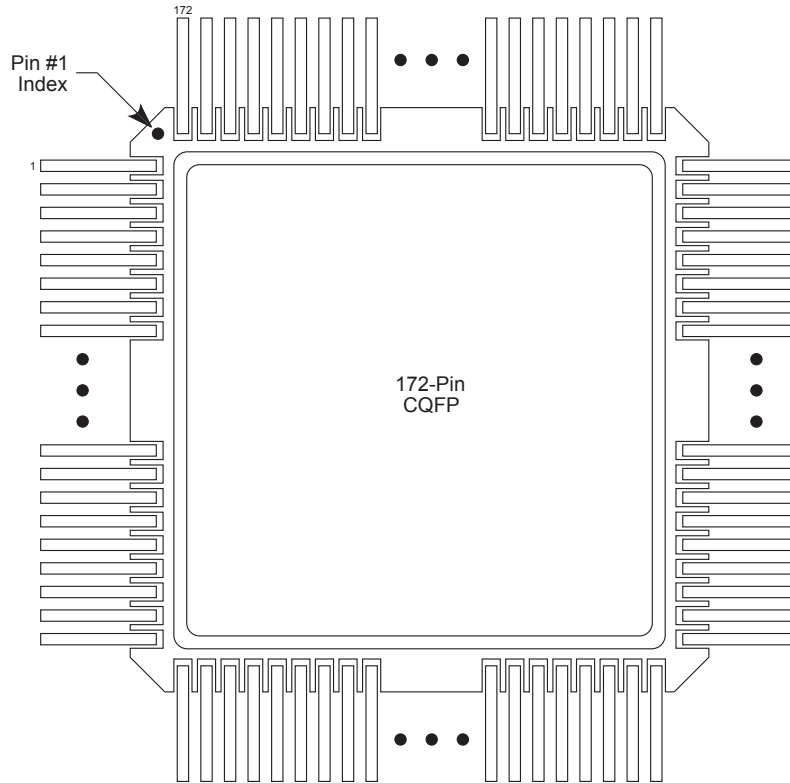
| TQ176 | | |
|------------|-----------------|-----------------|
| Pin Number | A1240A Function | A1280A Function |
| 82 | NC | VCC |
| 86 | NC | I/O |
| 87 | SDO | SDO |
| 89 | GND | GND |
| 96 | NC | I/O |
| 97 | NC | I/O |
| 101 | NC | NC |
| 103 | NC | I/O |
| 106 | GND | GND |
| 107 | NC | I/O |
| 108 | NC | I/O |
| 109 | GND | GND |
| 110 | VCC | VCC |
| 111 | GND | GND |
| 112 | VCC | VCC |
| 113 | VCC | VCC |
| 114 | NC | I/O |
| 115 | NC | I/O |
| 116 | NC | VCC |
| 121 | NC | NC |
| 124 | NC | I/O |
| 125 | NC | I/O |
| 126 | NC | NC |
| 133 | GND | GND |
| 135 | SDI, I/O | SDI, I/O |
| 136 | NC | I/O |
| 140 | NC | VCC |
| 143 | NC | I/O |
| 144 | NC | I/O |
| 145 | NC | NC |
| 147 | NC | I/O |
| 151 | NC | I/O |
| 152 | PRA, I/O | PRA, I/O |
| 154 | CLKA, I/O | CLKA, I/O |

| TQ176 | | |
|------------|-----------------|-----------------|
| Pin Number | A1240A Function | A1280A Function |
| 155 | VCC | VCC |
| 156 | GND | GND |
| 158 | CLKB, I/O | CLKB, I/O |
| 160 | PRB, I/O | PRB, I/O |
| 161 | NC | I/O |
| 165 | NC | NC |
| 166 | NC | I/O |
| 168 | NC | I/O |
| 170 | NC | VCC |
| 173 | NC | I/O |
| 175 | DCLK, I/O | DCLK, I/O |

Notes:

1. NC denotes no connection.
2. All unlisted pin numbers are user I/Os.
3. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

CQ172



Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

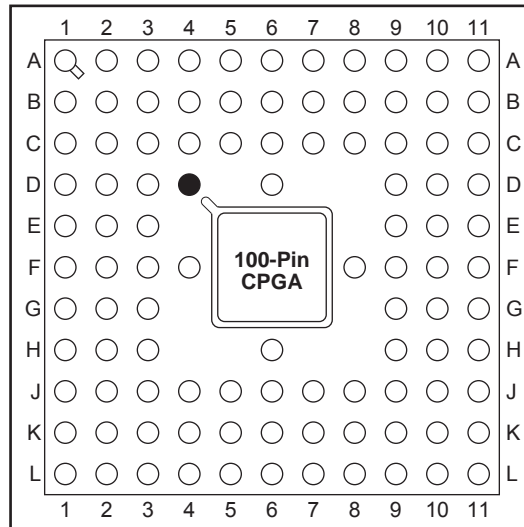
| CQ172 | |
|------------|-----------------|
| Pin Number | A1280A Function |
| 1 | MODE |
| 7 | GND |
| 12 | VCC |
| 17 | GND |
| 22 | GND |
| 23 | VCC |
| 24 | VCC |
| 27 | VCC |
| 32 | GND |
| 37 | GND |
| 50 | VCC |
| 55 | GND |
| 65 | GND |
| 66 | VCC |
| 75 | GND |
| 80 | VCC |
| 85 | SDO |
| 98 | GND |
| 103 | GND |
| 106 | GND |

| CQ172 | |
|------------|-----------------|
| Pin Number | A1280A Function |
| 107 | VCC |
| 108 | GND |
| 109 | VCC |
| 110 | VCC |
| 113 | VCC |
| 118 | GND |
| 123 | GND |
| 131 | SDI, I/O |
| 136 | VCC |
| 141 | GND |
| 148 | PRA, I/O |
| 150 | CLKA, I/O |
| 151 | VCC |
| 152 | GND |
| 154 | CLKB, I/O |
| 156 | PRB, I/O |
| 161 | GND |
| 166 | VCC |
| 171 | DCLK, I/O |

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PG100



● Orientation Pin

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

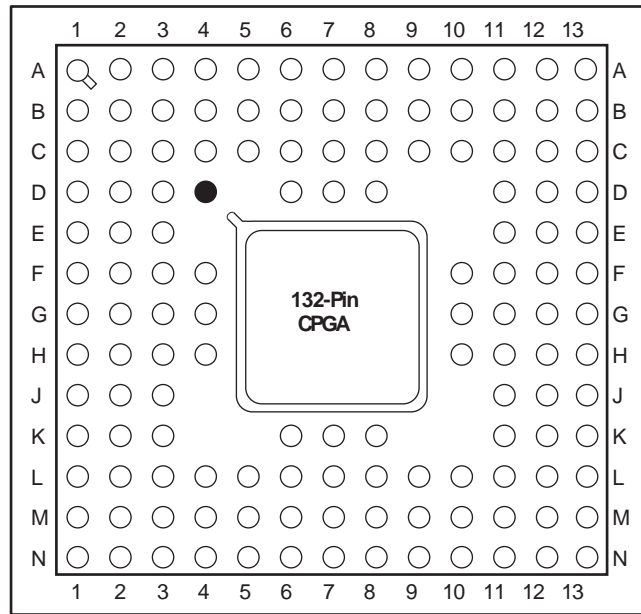
| PG100 | |
|------------|-----------------|
| Pin Number | A1225A Function |
| A4 | PRB, I/O |
| A7 | PRA, I/O |
| B6 | VCC |
| C2 | MODE |
| C3 | DCLK, I/O |
| C5 | GND |
| C6 | CLKA, I/O |
| C7 | GND |
| C8 | SDI, I/O |
| D6 | CLKB, I/O |
| D10 | GND |
| E3 | GND |

| PG100 | |
|------------|-----------------|
| Pin Number | A1225A Function |
| E11 | VCC |
| F3 | VCC |
| F9 | VCC |
| F10 | VCC |
| F11 | GND |
| G1 | VCC |
| G3 | GND |
| G9 | GND |
| J5 | GND |
| J7 | GND |
| J9 | SDO |
| K6 | VCC |

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PG132



● Orientation Pin

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

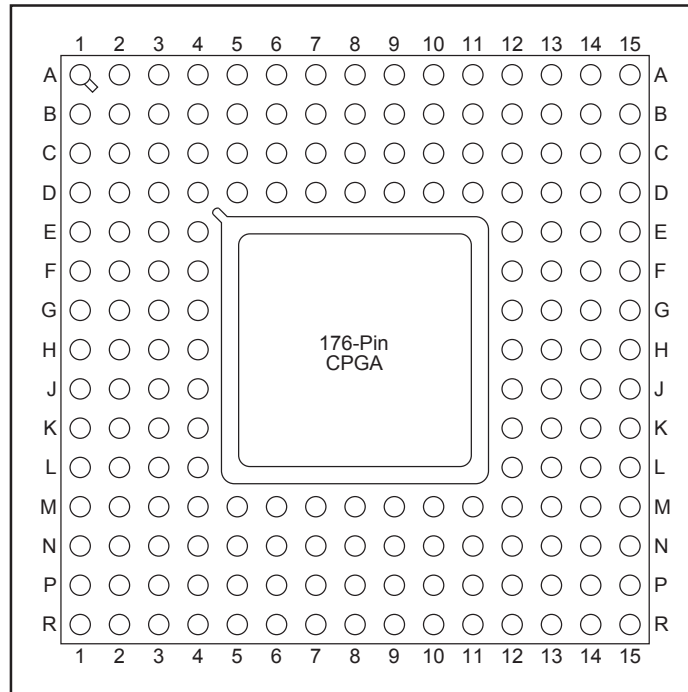
| PG132 | |
|------------|-----------------|
| Pin Number | A1240A Function |
| A1 | MODE |
| B5 | GND |
| B6 | CLKB, I/O |
| B7 | CLKA, I/O |
| B8 | PRA, I/O |
| B9 | GND |
| B12 | SDI, I/O |
| C3 | DCLK, I/O |
| C5 | GND |
| C6 | PRB, I/O |
| C7 | VCC |
| C9 | GND |
| D7 | VCC |
| E3 | GND |
| E11 | GND |
| E12 | GND |
| F4 | GND |
| G2 | VCC |

| PG132 | |
|------------|-----------------|
| Pin Number | A1240A Function |
| G3 | VCC |
| G4 | VCC |
| G10 | VCC |
| G11 | VCC |
| G12 | VCC |
| G13 | VCC |
| H13 | GND |
| J2 | GND |
| J3 | GND |
| J11 | GND |
| K7 | VCC |
| K12 | GND |
| L5 | GND |
| L7 | VCC |
| L9 | GND |
| M9 | GND |
| N12 | SDO |

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PG176



Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

| PG176 | |
|------------|-----------------|
| Pin Number | A1280A Function |
| A9 | CLKA, I/O |
| B3 | DCLK, I/O |
| B8 | CLKB, I/O |
| B14 | SDI, I/O |
| C3 | MODE |
| C8 | GND |
| C9 | PRA, I/O |
| D4 | GND |
| D5 | VCC |
| D6 | GND |
| D7 | PRB, I/O |
| D8 | VCC |
| D10 | GND |
| D11 | VCC |
| D12 | GND |
| E4 | GND |
| E12 | GND |
| F4 | VCC |
| F12 | GND |
| G4 | GND |
| G12 | VCC |
| H2 | VCC |

| PG176 | |
|------------|-----------------|
| Pin Number | A1280A Function |
| H3 | VCC |
| H4 | GND |
| H12 | GND |
| H13 | VCC |
| H14 | VCC |
| J4 | VCC |
| J12 | GND |
| J13 | GND |
| J14 | VCC |
| K4 | GND |
| K12 | GND |
| L4 | GND |
| M4 | GND |
| M5 | VCC |
| M6 | GND |
| M8 | GND |
| M10 | GND |
| M11 | VCC |
| M12 | GND |
| N8 | VCC |
| P13 | SDO |

Notes:

1. All unlisted pin numbers are user I/Os.
2. MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

4 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each version of the datasheet.

| Revision | Changes | Page |
|-------------------------------|--|------|
| Revision 8 (January 2012) | The ACT 2 datasheet was formatted newly in the style used for current datasheets. The same information is present (other than noted in the list of changes for this revision) but divided into chapters. | N/A |
| | Package names used in Table 1 • ACT 2 Product Family Profile and throughout the document were revised to match standards given in Package Mechanical Drawings (SAR 27395). | I |
| | The description for SDO pins had earlier been removed from the datasheet and has now been included again, in the "Pin Descriptions" section (SAR 35819). | 2-21 |
| | SDO pin numbers had earlier been removed from package pin assignment tables in the datasheet, and have now been restored to the pin tables (SAR 35819). | 3-2 |
| Revision 7 (June 2006) | The "Ordering Information" section was revised to include RoHS information. | II |
| Revision 6 (December 2000) | In the "PG176" package, pin A3 was incorrectly assigned as CLKA, I/O. A3 is a user I/O. Pin A9 is CLKA, I/O. | 3-21 |

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

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