THE DATASHEET OF

UCC28880DR

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TEXAS INSTRUMENTS

UCC28880

SLUSC05D – JULY 2014 – REVISED MAY 2016

UCC28880 700-V, 100-mA Low Quiescent Current Off-Line Converter

1 Features

- Integrated Power MOSFET (Switch) Rated to 700-V Drain-to-Source Voltage
- Integrated High-Voltage Current Source for Internal Low-Voltage Supply Generation
- Soft Start
- Self-Biased Switcher (Start Up and Operation Directly from Rectified Mains Voltage)
- Supports Buck, Buck-Boost and Flyback Topologies
- <100-µA Device Quiescent Current
- Robust Performance with Inductor Current Runaway Prevention
- Thermal Shutdown
- Protection
  - Current Limit
  - Overload and Output Short Circuit
- Create a Custom Design Using the UCC28880 with the WEBENCH Power Designer

2 Applications

- AC-to-DC Power Supplies (Output Current Up to 100 mA for CCM; 70 mA for DCM)
- Metering, Home Automation, Infrastructure SMPS
- Low-Side Buck Topology for TRIAC Driver
- Appliances, White Goods and LED Drivers

3 Description

The UCC28880 integrates the controller and a 700-V power MOSFET into one monolithic device. The device also integrates a high-voltage current source, enabling start up and operation directly from the rectified mains voltage.

The low quiescent current of the device enables excellent efficiency. With the UCC28880 the most common converter topologies, such as buck, buck-boost and flyback can be built using a minimum number of external components.

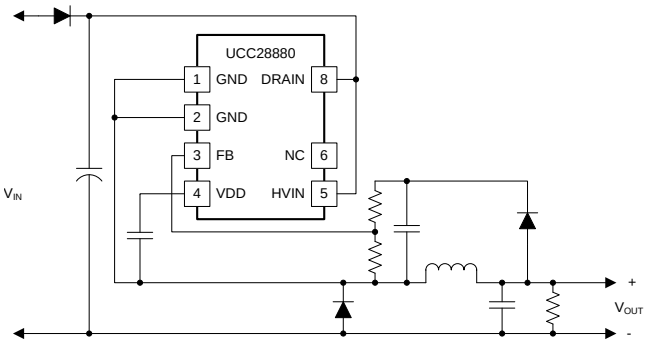
The UCC28880 incorporates a soft-start feature for controlled start up of the power stage which minimizes the stress on the power-stage components.

Device Information(1)

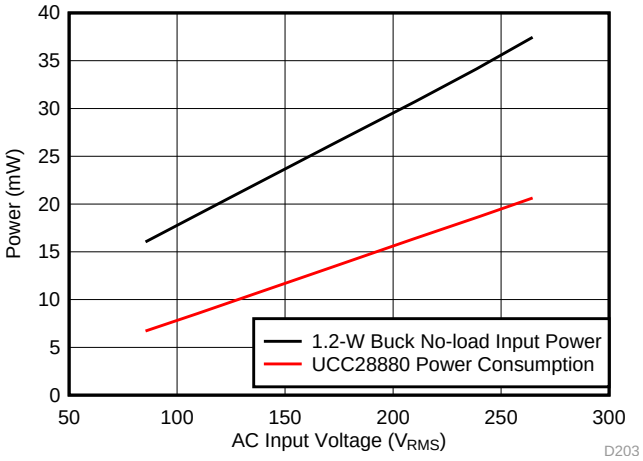
PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC28880	SOIC (7)	5.00 mm × 6.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Standby Power vs Input Voltage



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4 Revision History

Changes from Revision C (January 2016) to Revision D **Page**

- Changed HVIN off state current's MAX value from 12 µA to 36 µA. ... 8
- Changed Equation 2 ... 19

Changes from Revision B (September 2015) to Revision C **Page**

- Changed the documents title from, "UCC28880 700-V Lowest Quiescent Current Off-Line Switcher", to "700-V, 100-mA Low Quiescent Current Off-Line Converter". ... 1
- Changed Figure 16 image. ... 18
- Changed Equation 14. ... 22
- Changed Figure 19 image. ... 25
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- Changed Figure 26 image. ... 30
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- Changed Figure 28 image. ... 31

Changes from Revision A (October 2014) to Revision B **Page**

- Added Thermal Shutdown feature. ... 1
- Changed Applications features. ... 1
- Changed Power vs Input Voltage image. ... 1
- Changed Layout Guidelines section. ... 2
- Changed T_J specification and added note 4, 5 and 6. ... 6
- Added I_{VDD} ratings. ... 6
- Added HVIN pin exclusion. ... 6
- Added VDD clamp voltage specification. ... 8
- Changed Maximum switch on/off time specification. ... 8
- Added inductor current run away protection time threshold specification. ... 8
- Added $R_{TH}J_A$ vs Copper Area image. ... 10
- Changed Feature Description section. ... 12
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- Changed Universal Input, 12-V, 100-mA Output Low-Side Buck image. ... 18
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- Changed Equation 12. 22
- Changed Equation 14. 22
- Changed Equation 17. 23
- Changed Low-Side Buck-Boost Converter image. 29
- Changed Layout Guidelines section. 32

Changes from Original (August, 2014) to Revision A **Page**

- Added *Pin Configuration and Functions* section, *ESD table*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1
- Changed Simplified Schematic drawing. 1
- Changed Typical Characteristics graphs 1 through 7. 2
- Changed Typical Characteristics graphs 1 through 7. 9
- Changed Typical Characteristics graphs 1 through 7. 10
- Changed Equation 2 19

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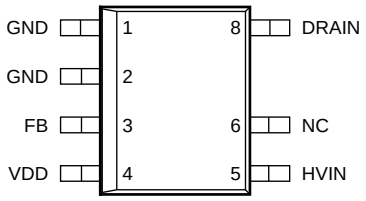
5 Pin Configuration and Functions

D package
8-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DRAIN	8	P	Drain pin
FB	3	I	Feedback terminal
GND	1	G	Ground
GND	2	G	Ground
HVIN	5	P	Supply pin
NC	6	N/C	Not internally connected
VDD	4	O	Supply pin, supply is provided by internal LDO

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)(3)

		MIN	MAX	UNIT
HVIN		–0.3	700 (4)	V
DRAIN		Internally clamped	700 (4)	V
I_{DRAIN}	Positive drain current single pulse, pulse max duration 25 µs		320 (5)	mA
I_{DRAIN}	Negative drain current	–320		mA
FB		–0.3	6	V
VDD	VDD is supplied from low impedance source	–0.3	6	V
I_{VDD}	VDD is supplied from high impedance source		400	µA
T_J (6)	Junction temperature		150	°C
	Lead temperature 1.6 mm (1/16 inch) from case 10 seconds		260	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. These ratings apply over the operating ambient temperature ranges unless otherwise noted.
(3) The device is not rated to withstand operating conditions when multiple parameters are at or near, absolute maximum ratings.
(4) T_A = 25°C
(5) The MOSFET drain to source voltage is less than 400V
(6) The thermal shutdown threshold can be beyond the absolute maximum rating of the junction temperature. Thermal shut down is designed to prevent thermal run away that could result in catastrophic failure. Prolonged operation above recommended maximum junction temperature can impact device life time

6.2 ESD Ratings

				UNIT
$V_{(ESD)}$	Electrostatic discharge	Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins except HVIN pin (1)	±2000	V
		Human Body Model (HBM) per ANSI/ESDA/JEDEC JS-001, HVIN pin (1)	±1500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VDD}	Voltage On VDD pin		5		V
V_{FB}	Voltage on FB pin	–0.2		5	V
T_A	Operating ambient temperature	–40		105	°C
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		UCC28880 D (SOIC) 7 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	134.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	85	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	76	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

V_{HVIN} = 30 V, T_A = T_J = –40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{HVIN(min)}$	Minimum Voltage to startup				30	V
I_{NL}	Internal supply current, no load	FB = 1.25 V (> V_{FB_TH})		58	100	µA
I_{FL}	Internal supply current, full load	FB = 0.75 V (> V_{FB_TH})		72	120	µA
I_{CH0}	Charging VDD Cap current	V_{VDD} = 0 V,	–3.8	–1.6	–0.4	mA
I_{CH1}	Charging VDD Cap current	V_{VDD} = 4.4V, V_{FB} = 1.25 V	–3.4	–1.3	–0.25	mA
V_{VDD}	Internally regulated low Voltage supply (supplied from HVIN pin)		4.5	5	5.5	V
V_{FB_TH}	FB pin reference threshold		0.94	1.02	1.1	V
$V_{VDD(on)}$	VDD turn-on threshold	VDD low-to-high	3.55	3.92	4.28	V
$\Delta V_{VDD(uvlo)}$	VDDON - VDD turn-off threshold	VDD high-to-low	0.28	0.33	0.38	V
D_{MAX}	Maximum Duty Cycle	FB = 0.75 V	45%		55%	
I_{LIMIT}	Current Limit	Static, T_A = –40°C			300	mA
		Static, T_A = 25°C	170	210	260	mA
		Static, T_A = 125°C	140			mA
$T_{J(stop)}$	Thermal Shutdown Temperature	Internal junction temperature		150		°C
$T_{J(hyst)}$	Thermal Shutdown Hysteresis	Internal junction temperature		50		°C
BV	Power MOSFET Breakdown Voltage	T_J = 25°C	700			V
$R_{DS(on)}$	Power MOSFET On-Resistance (includes internal sense-resistor)	I_D = 30 mA, T_J = 25°C		32	40	Ω
		I_D = 30 mA, T_J = 125°C		55	68	Ω
DRAIN_$I_{LEAKAGE}$	Power MOSFET off state leakage current	V_{DRAIN} = 700V, T_J = 25°C			5	µA
		V_{DRAIN} = 400 V, T_J = 125°C			20	µA
HVIN_I_{OFF}	HVIN off state current	V_{HVIN} = 700 V, T_J = 25°C, V_{VDD} = 5.8 V	4	7.5	36	µA
		V_{HVIN} = 400 V, T_J = 125°C, V_{VDD} = 5.8 V			20	µA
$V_{VDD(clamp)}$	VDD clamp voltage	I_{VDD} = 250 µA	6	6.7	7.5	V

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
$f_{SW(max)}$	Maximum switching frequency	52	62	75	kHz
t_{ON_MAX}	Maximum switch on time (current limiter not triggered), FB = 0.75 V	6.5	8.1	9.7	µs
t_{OFF_MIN}	Minimum switch off time follows every t_{ON} time, FB = 0.75 V	6.5	8.1	9.7	µs
t_{MIN}	Minimum on time	0.17	0.22	0.30	µs
$t_{OFF(ovl)}$	Max off time (OL condition), $t_{OFF(ovl)}$ = t_{SW} – $t_{ON(max)}$	130	200	270	µs
t_{on_TO}	Inductor current run away protection time threshold			500	ns

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6.7 Typical Characteristics

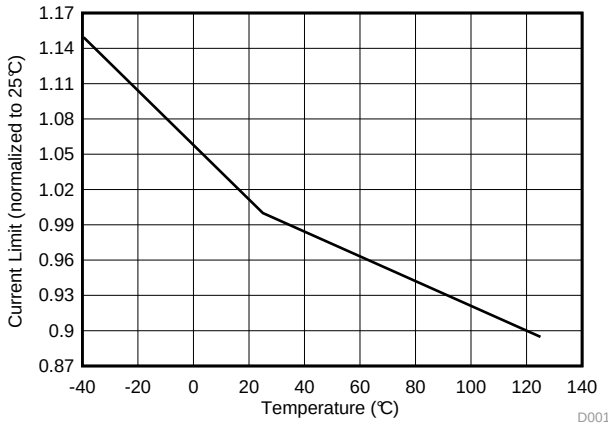

Figure 1. I_{LIMIT} vs Temperature

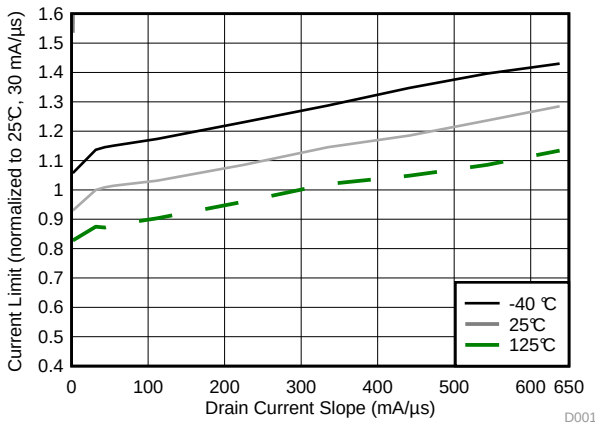

Figure 2. I_{LIMIT} vs Drain Current Slope

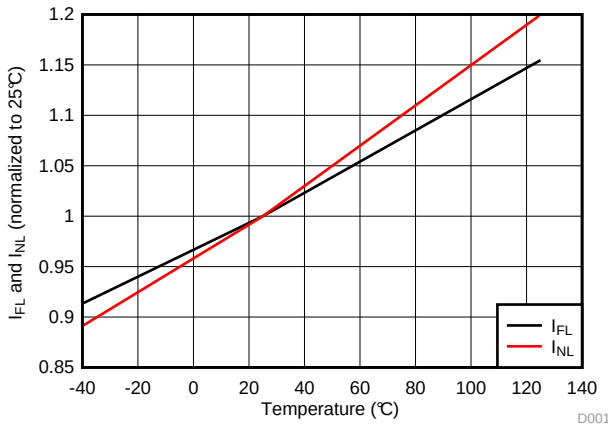

Figure 3. I_{NL} and I_{FL} vs Temperature

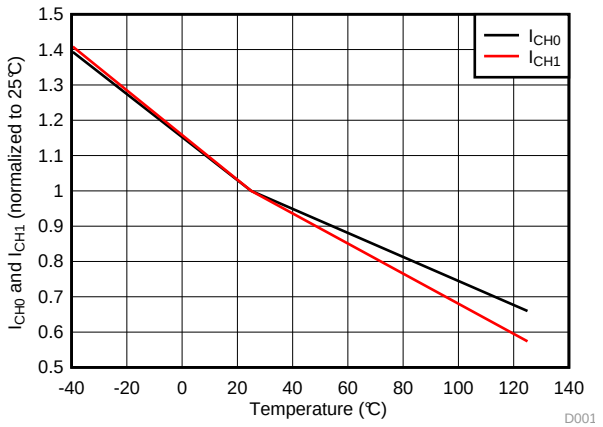

Figure 4. I_{CH0} and I_{CH1} vs Temperature

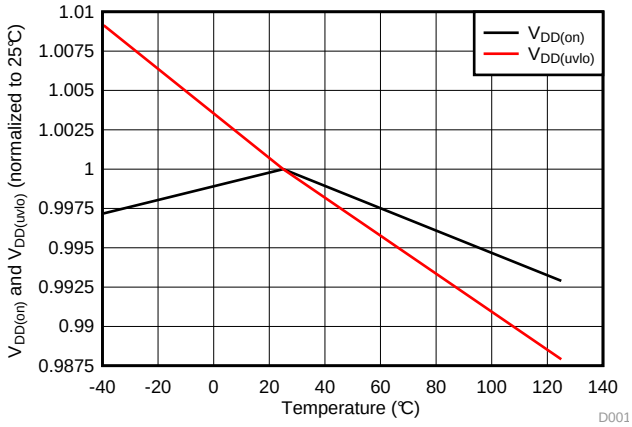

Figure 5. $V_{VDD(on)}$ and ΔV_{UVLO} vs Temperature

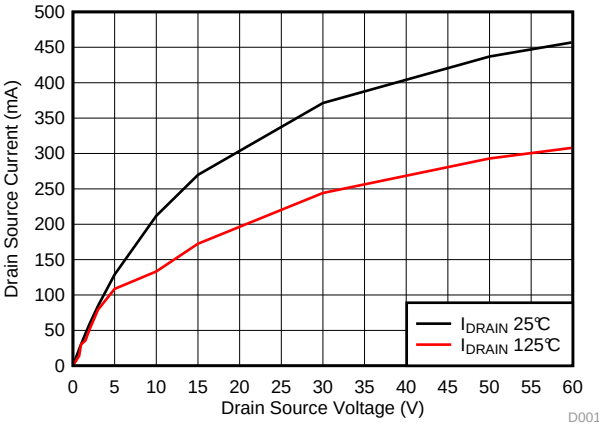

Figure 6. I_{DS} vs V_{DS} at 25°C and 125°C

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Typical Characteristics (continued)

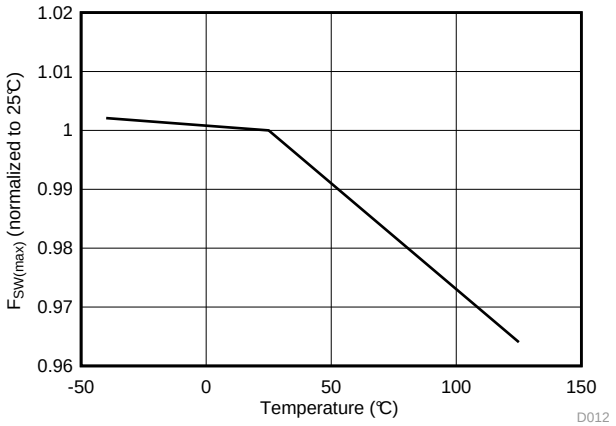

Figure 7. Maximum Switching Frequency vs Temperature

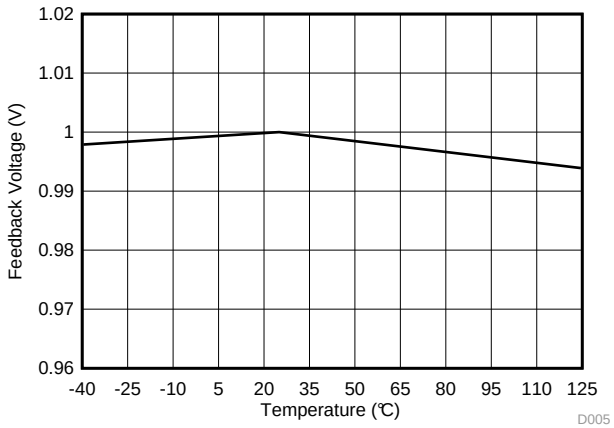

Figure 8. V_{FB_TH} vs Temperature

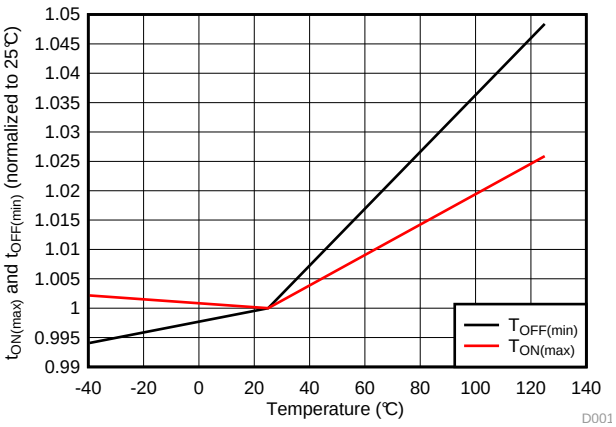

Figure 9. $t_{ON(max)}$ and $t_{OFF(min)}$ vs Temperature

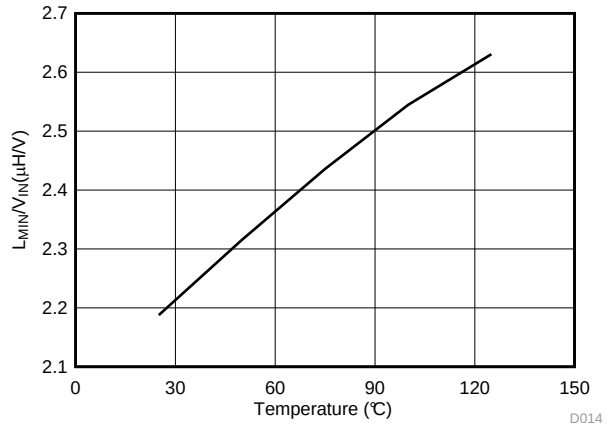

Figure 10. $(L_{MIN}/V_{IN})_{MIN}$ vs Temperature

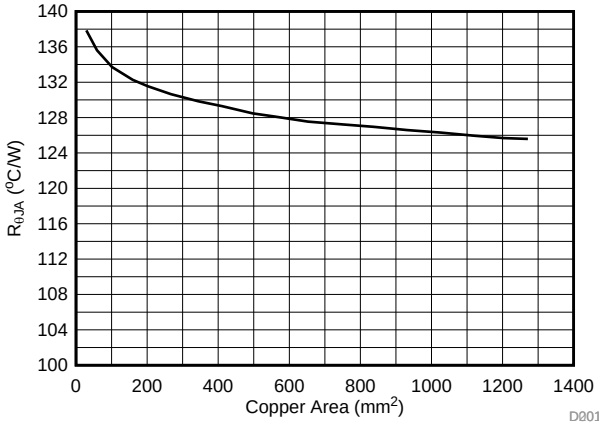

Figure 11. $R_{TH}J_A$ vs Copper Area

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7 Detailed Description

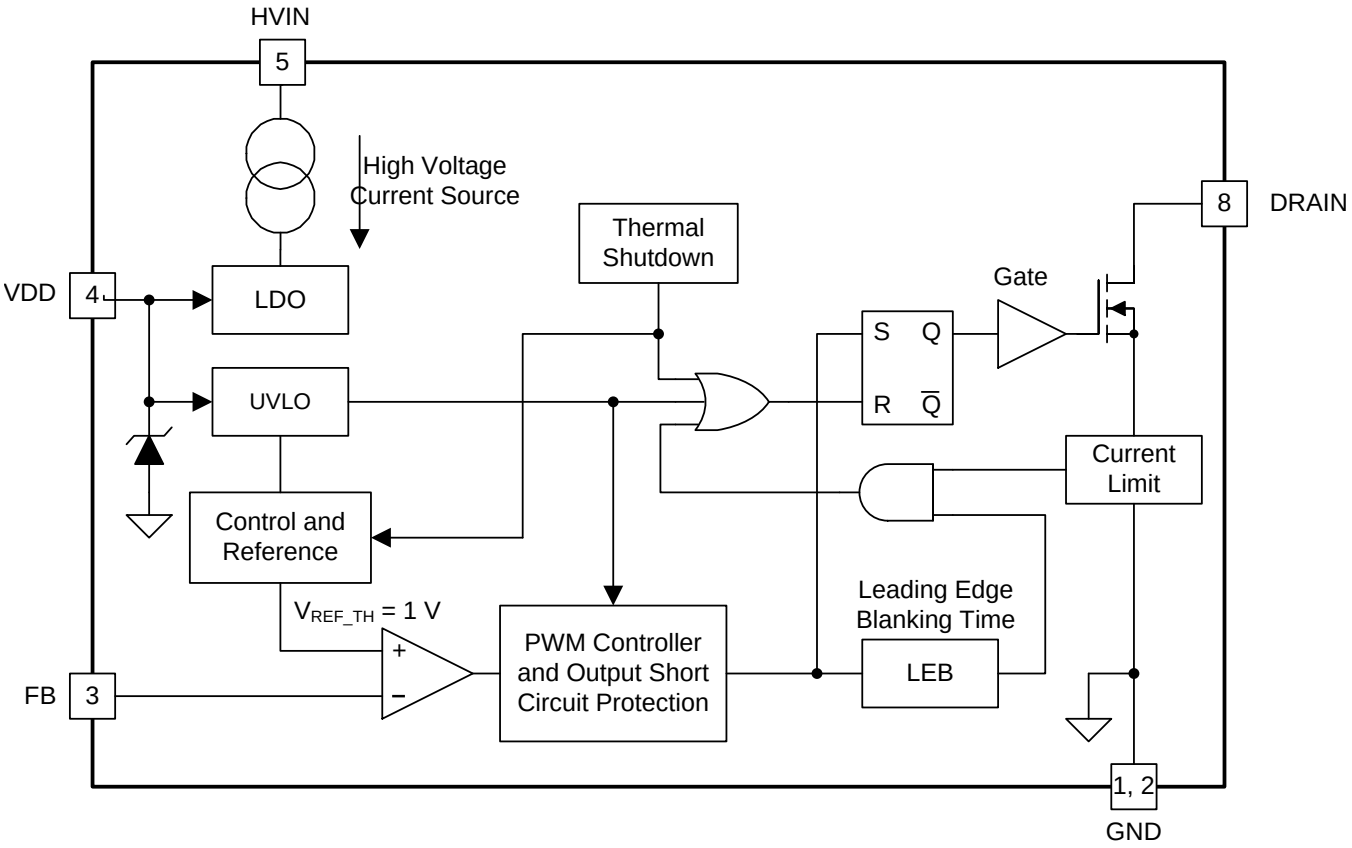
7.1 Overview

The UCC28880 integrates a controller and a 700-V power MOSFET into one monolithic device. The device also integrates a high-voltage current source, enabling start up and operation directly from the rectified mains voltage.

The low-quiescent current of the device enables excellent efficiency. The device is suitable for non-isolated AC-to-DC low-side buck and buck-boost configurations with level-shifted direct feedback, but also more traditional high-side buck, buck boost and low-power flyback converters with low standby power can be built using a minimum number of external components.

The device generates its own internal low-voltage supply (5 V referenced to the device's ground, GND) from the integrated high-voltage current source. The PWM signal generation is based on a maximum constant on-time, minimum off-time concept, with the triggering of the on-pulse depending on the feedback voltage level. Each on-pulse is followed by a minimum off-time to ensure that the power MOSFET is not continuously driven in an on-state. The PWM signal is AND-gated with the signal from a current limit circuit. No internal clock is required, as the switching of the power MOSFET is load dependent. A special protection mechanism is included to avoid runaway of the inductor current when the converter operates with the output shorted or in other abnormal conditions that can lead to an uncontrolled increase of the inductor current. This special protection feature keeps the MOSFET current at a safe operating level. The device is also protected from other fault conditions with thermal shutdown, under-voltage lockout and soft-start features.

7.2 Functional Block Diagram



7.3 Feature Description

The device integrates a 700-V rated power MOSFET switch, a PWM controller, a high-voltage current source to supply a low-voltage power supply regulator, a bias and reference block, thermal shutdown and the following protection features, current limiter, under voltage lockout (UVLO) and overload protection for situations like short circuit at the output.

In low-side buck and buck-boost topologies, the external level-shifted direct feedback circuit can be implemented by two resistors and a high-voltage PNP transistor.

The positive high-voltage input of the converter node (VIN+) functions as a system reference ground for the output voltage in low-side topologies. In the low-side buck topology the output voltage is negative with respect to the positive high-voltage input (VIN+), and in low-side buck-boost topology the output voltage is positive with respect to the positive high-voltage input (VIN+).

In high-side buck configuration, as well as in non-isolated flyback configuration, the output voltage is positive with respect to the negative high-voltage input (VIN-), which is the system reference ground.

UCC28880 can operate under continuous conduction mode (CCM) or discontinuous conduction mode (DCM) mode. CCM operation allows the converter to deliver more output power because of less current ripple. However, it requires a higher inductor value and generally results in lower efficiency due to the added losses associated with diode reverse recovery current. On the other hand, DCM mode operation uses a smaller inductor and achieves better efficiency, but the output current handling capability is reduced because of increased current ripple. The table below shows the current handling capability in DCM and CCM operation.

Table 1. Current Handling Capability

CURRENT HANDLING MODE	230 V_{AC} ±15%	85 V ~ 265 V_{AC}
Discontinuous Conduction Mode (DCM)	70 mA	70 mA
Continuous Conduction Mode (CCM)	100 mA	100 mA

When the bus voltage is higher than 400 V, it is recommended to limit operation to DCM mode only to avoid the diode reverse recovery current and the associated internal MOSFET stress. Due to the higher switching loss and device stresses at higher bus voltage, it is recommended to keep the converter input voltage less than 560 V for the buck applications.

UCC28880 power handling capability is reduced at higher ambient temperature, as a function of the power dissipation of the device, the device's recommended maximum operating junction temperature and the thermal dissipation capability of the total system. De-rating of the output current according to maximum ambient temperature can be estimated from Figure 12. The de-rating estimation assumes CCM operation, 7 µJ of switching loss and 135°C/W $R_{TH}J_A$ and 30-kHz full-load switching frequency. This is a conservative estimation. The thermal handling capability can be more accurately determined through experimental measurement. For more information on thermal evaluation methods see the IC Package and Thermal Metrics application report: SPRA953.

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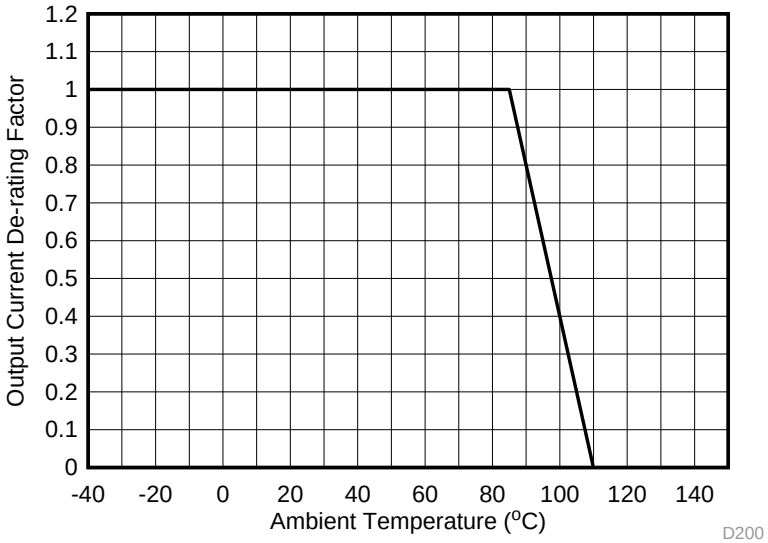

Figure 12. Output Current (De-Rating Factor) vs. Temperature

It is required to use fast recovery diode for the buck freewheeling diode. When designed in CCM, the diode reverse recovery time should be less than 35 ns to keep low reverse recovery current and the switching loss. For example, STTH1R06A provides 25-ns reverse recovery time. When designed in DCM, a slower diode can be used, but the reverse-recovery time should be kept less than 75 ns. MURS160 can fit the requirement.

The device has a low-standby power consumption (no-load condition), only 18 mW (typical) when connected to a 230-V_{AC} mains and 9 mW when connected to an 115-V_{AC} mains.

The standby power does not include the power dissipated in the external feedback path, the power dissipated in the external pre-load, the inductor in the freewheeling diode and the converter input stage (rectifiers and filter).

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7.4 Device Functional Modes

7.4.1 Startup Operation

The device includes a high-voltage current source connected between the HVIN pin and the internal supply for the regulator. When the voltage on the HVIN pin rises, the current source is activated and starts to supply current to the internal 5-V regulator. The 5-V regulator charges the external capacitor connected between VDD pin and GND pin. When the VDD voltage exceeds the VDD turn-on threshold, $V_{VDD(on)}$, device starts operations. The minimum voltage across HVIN and GND pins, to ensure enough current to charge the capacitance on VDD pin, is $V_{HVIN(min)}$. At the First switching cycle the minimum MOSFET off time is set to be >100 μs and cycle-by-cycle is progressively reduced up to $t_{OFF(min)}$ providing soft start.

7.4.2 Feedback and Voltage Control Loop

The feedback circuit consists of a voltage comparator with the positive input connected to an internal reference voltage (referenced to GND) and the negative input connected to FB pin. When the feedback voltage at the FB pin is below the reference voltage V_{FB_TH} logic high is generated at the comparator output. This logic high triggers the PWM controller, which generates the PWM signal turning on the MOSFET. When the feedback voltage at the FB pin is above the reference voltage, it indicates that the output voltage of the converter is above the targeted output voltage set by the external feedback circuitry and PWM is stopped.

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Device Functional Modes (continued)

7.4.3 PWM Controller

UCC28880 operates under on/off control. When the FB pin voltage is below internal reference 1 V, the converter is switching and sending power to the load. When the FB pin voltage is above internal reference 1 V, the converter shuts off and stops delivering power to the load.

The PWM controller does not need a clock signal. The PWM signal's frequency is set to $f_{SW(max)} = (1/(t_{ON(max)} + t_{OFF(min)}))$ which occurs when the voltage on the FB pin is continuously below V_{FB_TH}.

PWM duty cycle is determined by both the peak current and maximum on time. At each switching cycle, after turn on, the MOSFET is turned off if its current reaches the fixed peak-current threshold or its on time reaches the maximum value of on-time pulse $t_{ON(max)}$.

Normally the converter would operate under frequency control, which means the converter is only enabled one switching cycle and then disabled. Next switching cycle starts when output voltage decays and the feedback enable the converter again. This way, the converter appears to operate under variable switching frequency control.

The user might observe the converter operates in burst mode that converter is enabled for multiple switching cycles and then stopped for multiple switching cycles. This causes larger output voltage ripple. However, due to the infrequent switching it actually helps on the standby power at no load.

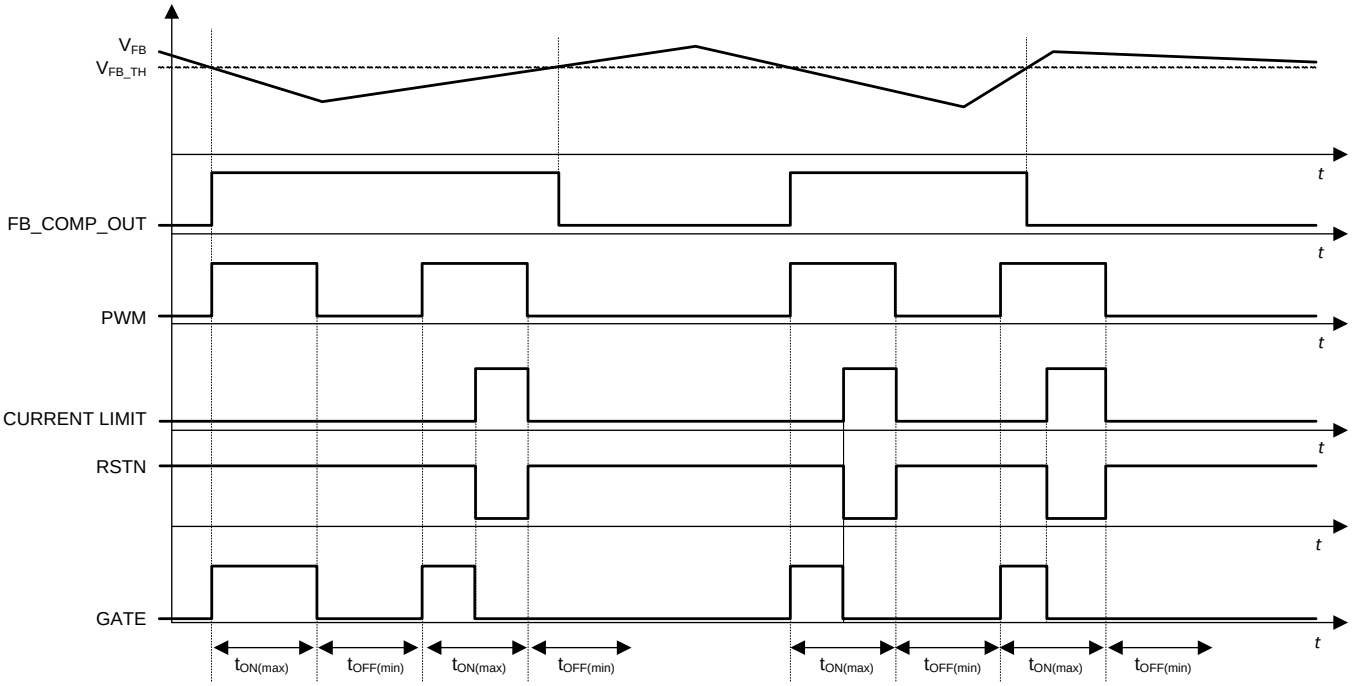

Figure 13. UCC28880 Timing Diagram

Device Functional Modes (continued)

7.4.4 Current Limit

The current limit circuit senses the current through the power MOSFET. The sensing circuit is located between the source of the power MOSFET and the GND pin. When the current in the power MOSFET exceeds the threshold I_{LIMIT}, the internal current limit signal goes high, which sets the internal RSTN signal low. This disables the power MOSFET by driving its gate low. The current limit signal is set back low after the falling edge of the PWM signal. After the rising edge of the GATE signal, there is a blanking time. During this blanking time, the current limit signal cannot go high. This blanking time and the internal propagation delay result in minimum on time, t_{MIN}.

7.4.5 Inductor Current Runaway Protection

To protect the device from overload conditions, including a short circuit at the output, the PWM controller incorporates a protection feature which prevents the inductor current from runaway. When the output is shorted the inductor demagnetization is very slow, low di/dt, and when the next switching cycle starts energy stored in the inductance is still high. After the MOSFET switches on, the current starts to rise from pre-existing DC value and reaches the current-limit value in a short duration of time. Because of the intrinsic minimum on-time of the device the MOSFET on-time cannot be lower than t_{MIN}, in an overload or output short circuit the energy inductance is not discharged sufficiently during MOSFET off-time, it is possible to lose control of the current leading to a runaway of the inductor current. To avoid this, if the on-time is less than t_{ON_TO} (t_{ON_TO} is a device internal time out), the controller increases the MOSFET off-time (t_{OFF}). If the MOSFET on-time is longer than t_{ON_TO} then t_{OFF} is decreased. The controller increases t_{OFF}, cycle-by-cycle, through discrete steps until the on-time continues to stay below t_{ON_TO}. The t_{OFF} is increased up to $t_{OFF(ovl)}$ after that, if the on-time is still below t_{ON_TO} the off-time is kept equal to $t_{OFF(ovl)}$. The controller decreases t_{OFF} cycle-by-cycle until the on-time continues to stay above t_{ON_TO} up to $t_{OFF(min)}$. This mechanism prevents control loss of the inductor current and prevents over stress of the MOSFET (see typical waveforms in Figure 14 and Figure 15). At start up, the t_{OFF} is set to $t_{OFF(ovl)}$ and reduced cycle-by-cycle (if the on-time is longer than t_{ON_TO}) up to $t_{OFF(min)}$ providing a soft start for the power stage.

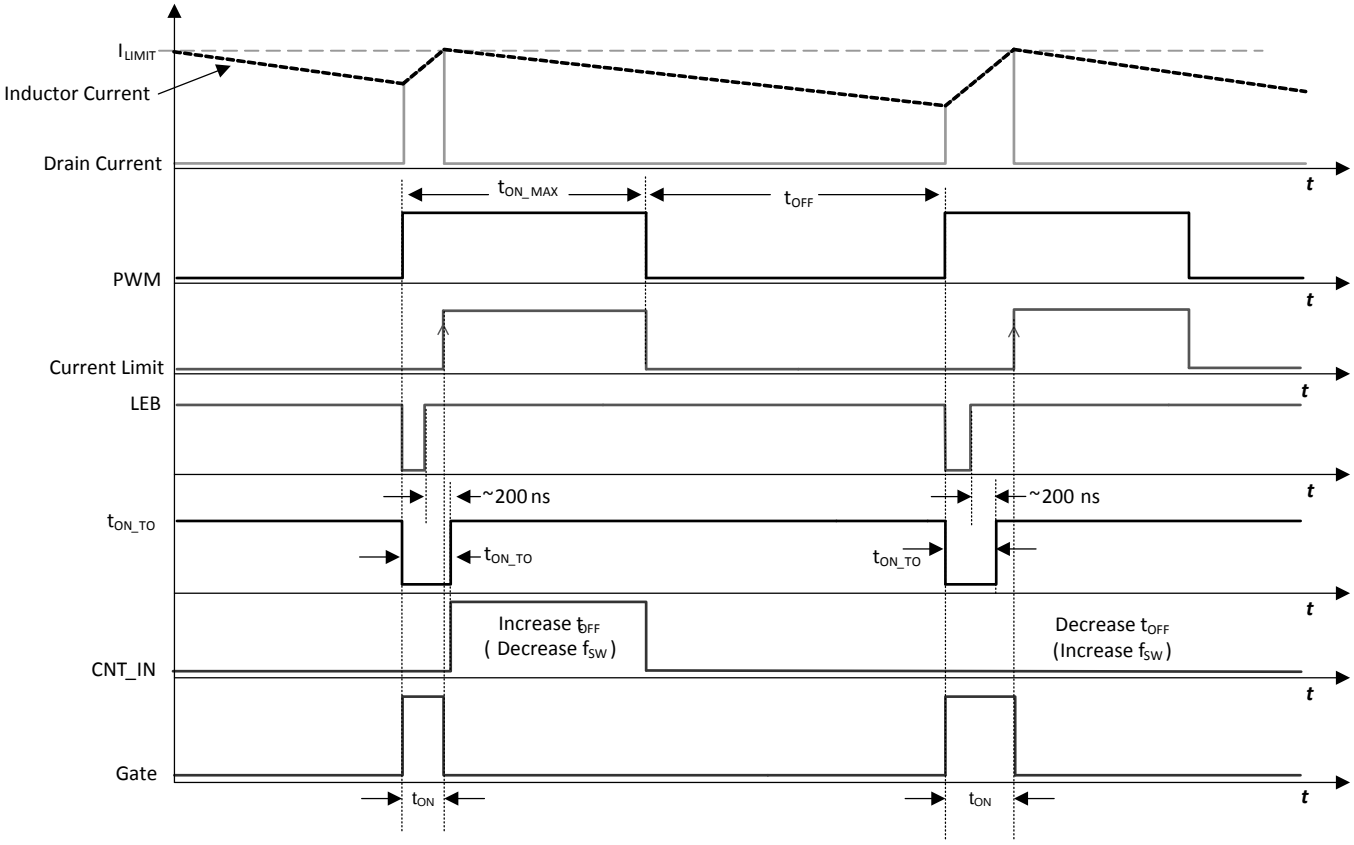

Figure 14. Current Runaway Protection Logic Timing Diagram

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Device Functional Modes (continued)

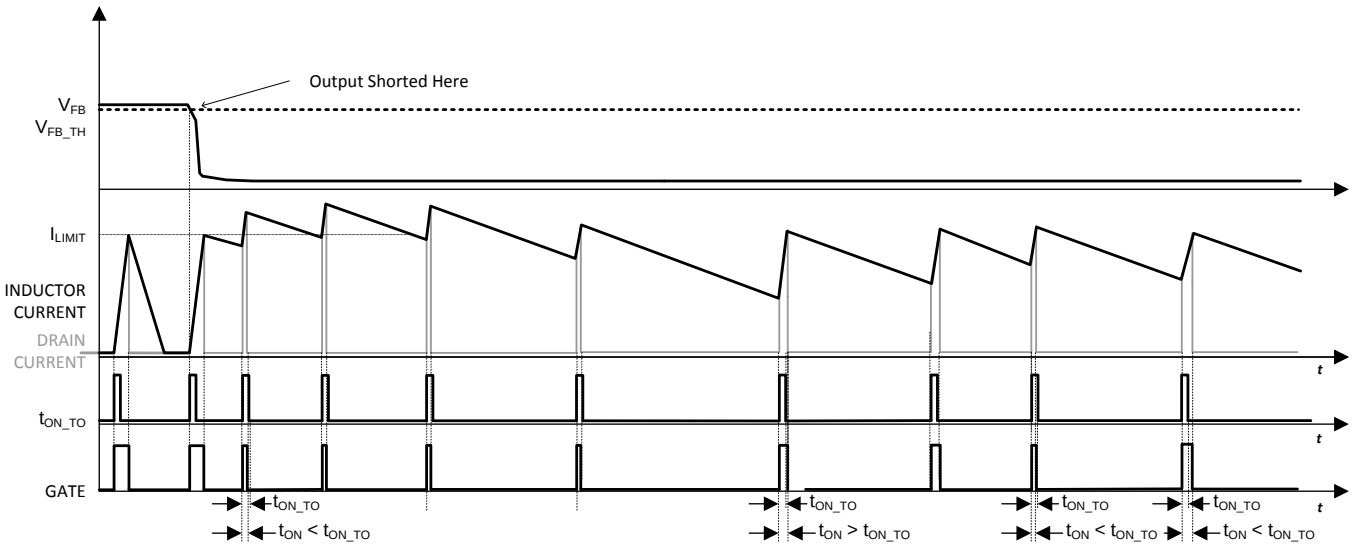

Figure 15. Current Runaway Protection, Inductor and MOSFET Current

A minimal value needs to be imposed on the inductance value to avoid nuisance tripping of the protection feature that prevents the loss of control of the inductor current. Inadvertent operation of the protection feature limits the output-power capability of the converter. This condition depends on the converter's maximum input operating voltage and temperature. Use Equation 1 to calculate your minimum inductance value.

$$L > \left[\left(\frac{L_{MIN}}{V_{IN}}\right)\right]\Big|_{T_J=T_{J(max)}} \times V_{IN(max)} = \frac{V_{IN(max)}}{I_{LIMIT}} \times t_{ON_TO} \quad (1)$$

The value of Equation 1 can be found by characterization graph of Figure 10. Pick the value at the desired maximum junction temperature

If the inductance value is too low, such that the MOSFET on-time is always less than t_{ON_TO} timeout and the device progressively increases the MOSFET off-time up to $t_{OFF(ovl)}$, the output power is reduced and the converter fails to supply the load.

7.4.6 Thermal Shutdown

If the junction temperature rises above $T_{J(stop)}$, the thermal shutdown is triggered. This disables the power MOSFET switching. To re-enable the switching of the MOSFET the junction temperature has to fall by $T_{J(hyst)}$ below the $T_{J(stop)}$ where the device moves out of over temperature.

According to the electrical specs, the thermal shutdown threshold can be beyond the device's rated absolute maximum junction temperature. Thermal shutdown is designed to prevent thermal run away that could result in catastrophic failure. Prolonged operation above the recommended maximum junction temperature can impact device lifetime.

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8 Application and Implementation

8.1 Application Information

The UCC28880 can be used in various application topologies with direct or isolated feedback. The device can be used in low-side buck, where the output voltage is negative, or as a low-side buck-boost configuration, where the output voltage is positive. In both configurations the common reference node is the positive input node (VIN+). The device can also be configured as a LED driver in either of the above mentioned configurations. If the application requires the AC-to-DC power supply output to be referenced to the negative input node (VIN-), the UCC28880 can also be configured as a traditional high-side buck as shown in Figure 19. In this configuration, the voltage feedback is sampling the output voltage VOUT, making the DC regulation less accurate and load dependent than in low-side buck configuration, where the feedback is always tracking the VOUT. However, high-conversion efficiency can still be obtained.

8.2 Typical Application

8.2.1 12-V, 100-mA Low-Side Buck Converter

Figure 16 shows a typical application example of a non-isolated power supply, where the UCC28880 is connected in a low-side buck configuration having an output voltage that is negative with respect to the positive input voltage (VIN+). The output voltage is set to 12 V in this example, but can easily be changed by changing the value of R_{FB1}. This application can be used for a wide variety of household appliances and automation, or any other applications where mains isolation is not required.

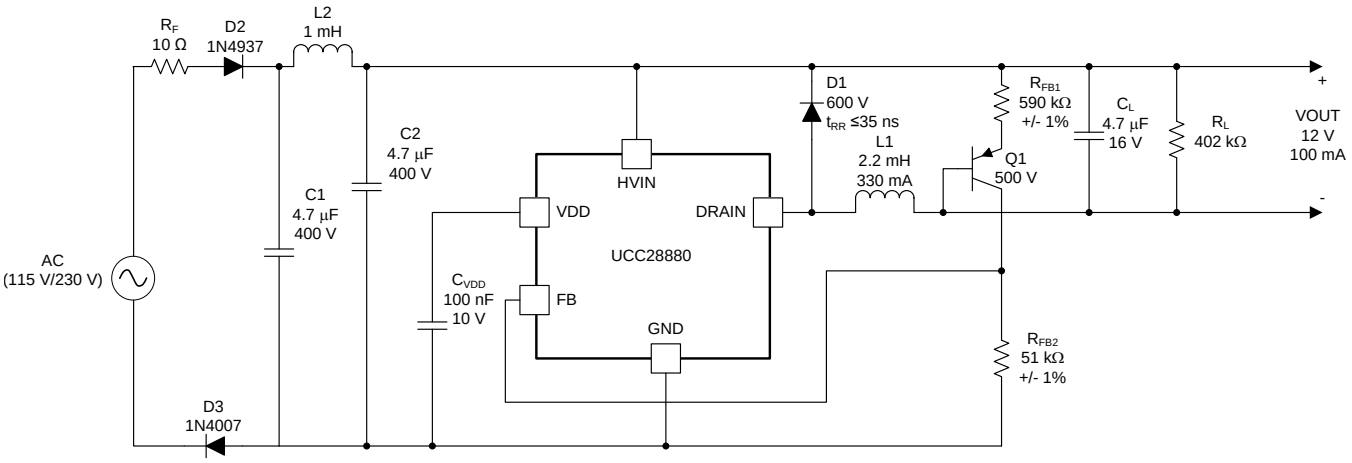

Figure 16. Universal Input, 12-V, 100-mA Output Low-Side Buck

8.2.1.1 Design Requirements

Table 2. Design Specification

DESCRIPTION		MIN	MAX	UNIT
DESIGN INPUT				
V_{IN}	AC input voltage	85	265	V_{RMS}
f_{LINE}	Line frequency	47	63	Hz
I_{OUT}	Output current	0	100	mA
DESIGN REQUIREMENTS				
P_{NL}	No-load input power		50	mW
V_{OUT}	Output voltage	12	13	V
ΔV_{OUT}	Output voltage ripple		350	mV
η	Converter efficiency	68%		

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8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the UCC28880 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   – Run electrical simulations to see important waveforms and circuit performance,
   – Run thermal simulations to understand the thermal performance of your board,
   – Export your customized schematic and layout into popular CAD formats,
   – Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

8.2.1.2.2 Input Stage (R_F, D2, D3, C1, C2, L2)

- Resistor R_F is a flame-proof fusible resistor. R_F limits the inrush current, and also provide protection in case any component failure causes a short circuit. Value for its resistance is generally selected between 4.7 Ω to 15 Ω.
- A half-wave rectifier is chosen and implemented by diode D2 (1N4937). It is a general purpose 1-A, 600-V rated diode. It has a fast reverse recovery time (200 ns) for improved differential-mode-conducted EMI noise performance. Diode D3 (1N4007) is a general purpose 1-A, 1-kV rated diode with standard reverse recovery time (>500 ns), and is added for improved common-mode-conducted EMI noise performance. D3 can be removed and replaced by a short if not needed.
- EMI filtering is implemented by using a single differential-stage filter (C1-L2-C2).

Capacitors C1 and C2 in the EMI filter also acts as storage capacitors for the high-voltage input DC voltage (VIN). The required input capacitor size can be calculated according Equation 2.

$$C_{BULK\,min} = \frac{\frac{2 \times P_{IN}}{f_{LINE(min)}} \times \left\{ \frac{1}{RCT} - \frac{1}{2 \times \pi} \times \arccos\left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}} \right) \right\}}{2 \times V_{IN(min)}^2 - V_{BULK(min)}^2} \quad (2)$$

where

- $C_{BULK(min)}$ is minimum value for the total input capacitor value (C1 + C2 in the schematic of Figure 16).
- RCT = 1 in case a half wave rectifier and RCT = 2 in case of full-wave rectifier (for the schematic reported in Figure 22 RCT = 1 because of a half-wave rectifier).
- P_{IN} is the converter input power.
- $V_{IN(min)}$ is the minimum RMS value of the AC input voltage.
- $V_{BULK(min)}$ is the minimum allowed voltage value across bulk capacitor during converter operation.
- $f_{LINE(min)}$ is the minimum line frequency when the line voltage is $V_{IN(min)}$.

The converter input power can be easily calculated as follow:

- The converter maximum output power is: $P_{OUT} = I_{OUT}$ x V_{OUT} = 0.1 A x 12.5 V = 1.25 W
- Assuming the efficiency η = 68.% the input power is $P_{IN} = P_{OUT}/\eta$ = 1.765 W

Using the following values for the other parameters

- $V_{BULK(min)}$ = 80 V
- $V_{IN(min)}$ = 85 V_{RMS} (from design specification table)
- $f_{LINE(min)}$ = 57 Hz

$C_{BULK(min)}$ = 6.96 µF. Considering that electrolytic capacitors, generally used as bulk capacitor, have 20% of tolerance in value, the minimum nominal value required for C_{BULK} is:

$$C_{BULKn(min)} > \frac{C_{BULK(min)}}{\left(1 - TOL_{CBULK}\right)} = 8.7\,\mu F \quad (3)$$

Select C1 and C2 to be 4.7 µF each (C_{BULK} = 4.7 µF + 4.7 µF = 9.4 µF > $C_{BULKn(min)}$).

By using a full-wave rectifier allows a smaller capacitor for C1 and C2, almost 50% smaller.

8.2.1.2.3 Regulator Capacitor (C_{VDD})

Capacitor C_{VDD} acts as the decoupling capacitor and storage capacitor for the internal regulator. A 100-nF, 10-V rated ceramic capacitor is enough for proper operation of the device's internal LDO.

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8.2.1.2.4 Freewheeling Diode (D1)

The freewheeling diode has to be rated for high-voltage with as short as possible reverse-recovery time (t_{rr}).

The maximum reverse voltage that the diode should experience in the application, during normal operation, is given by Equation 4.

$$V_{D1(max)} = \sqrt{2} \times V_{IN(max)} = \sqrt{2} \times 265\,V = 375\,V \tag{4}$$

A margin of 20% is generally considered.

The use of a fast recovery diode is required for the buck-freewheeling rectifier. When designed in CCM, the diode reverse recovery time should be less than 35 ns to keep low reverse recovery current and the switching loss. For example, STTH1R06A provides 25-ns reverse recovery time. When designed in DCM, slower diode can be used, but the reverse recovery time should be kept less than 75 ns. MURS160 can fit the requirement.

8.2.1.2.5 Output Capacitor (CL)

The value of the output capacitor impacts the output ripple. Depending on the combination of capacitor value and equivalent series resistor (R_{ESR}). A larger capacitor value also has an impact on the start-up time. For a typical application, the capacitor value can start from 47 μF, to hundreds of μF. A guide for sizing the capacitor value can be calculated by the following equations:

$$C_L > 4 \times \frac{I_{LIMIT} - I_{OUT}}{f_{SW(max)} \times \Delta V_{OUT}} = 4 \times \frac{260\,mA - 100\,mA}{350\,mV \times 66\,kHz} = 30\,\mu F \tag{5}$$

$$R_{ESR} < \frac{\Delta V_{OUT}}{I_{LIMIT}} = 1\,\Omega \tag{6}$$

Take into account that both C_L and R_{ESR} contribute to output voltage ripple. A first pass capacitance value can be selected and the contribution of C_L and R_{ESR} to the output voltage ripple can be evaluated. If the total ripple is too high the capacitance value has to increase or R_{ESR} value must be reduced. In the application example C_L was selected (47 μF) and it has an R_{ESR} of 0.3 Ω. So the R_{ESR} contributes for 1/3 of the total ripple. The formula that calculates C_L is based on the assumption that the converter operates in burst of four switching cycles. The number of bursts per cycle could be different, the formula for C_L is a first approximation.

8.2.1.2.6 Load Resistor (R_L)

The resistor should be chosen so that the output current in any standby/no-load condition is higher than the leakage current through the integrated power MOSFET. If the standby load current is ensured to always be larger than the specified $I_{LEAKAGE}$, the R_L is not needed. If OVP protection is required for safety reasons, then a zener could be placed across the output (not fitted in the application example). In the application example R_L = 402 kΩ. This ensures a minimum load current of at least ~30 μA when V_{OUT} = 12 V.

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8.2.1.2.7 Inductor (L1)

Initial calculations:

Half of the peak-to-peak ripple current at full load:

$$\Delta I_L = 2 \times \left(I_{LIMIT} - I_{OUT}\right) \tag{7}$$

When operating in DCM, the peak-to-peak current ripple is the peak current of the device.

Average MOSFET conduction minimum duty cycle at continuous conduction mode is:

$$D_{MIN} = \frac{V_{OUT} + V_d}{V_{IN(max)} - V_d} \tag{8}$$

If the converter operates in discontinuous conduction mode:

$$D_{MIN} = 2 \times \frac{I_{OUT}}{I_{LIMIT}} \frac{V_{OUT} + V_d}{V_{IN(max)} - V_d} \tag{9}$$

Maximum allowed switching frequency at $V_{IN(max)}$ and full load:

$$F_{SW_VIN(max)} = \frac{D_{MIN}}{t_{ON_TO}} \tag{10}$$

Switching frequency has a maximum value limit of $f_{SW(max)}$.

The worst case I_{LIMIT} = 140 mA, but assuming ΔI_L = 100 mA.

The converter works in continuous conduction mode ($\Delta I_L < I_{LIMIT}$) so the

$$D_{MIN} = \frac{V_{OUT} + V_d}{V_{IN(max)} - V_d} = 3.61\% \tag{11}$$

The maximum allowed switching frequency is 61.7 kHz because the calculated value exceeds it.

$$F_{SW_VIN(max)} = \frac{D_{MIN}}{t_{ON_TO}} = 72\,kHz > f_{SW(max)} = 61.7\,kHz \tag{12}$$

The duty cycle does not force the MOSFET on time to go below t_{ON_TO}. If $D_{MIN}/T_{ON_TO} < f_{SW(max)}$, the switching frequency is reduced by current runaway protection and the maximum average switching frequency is lower than $f_{SW(max)}$, the converter can't support full load.

The minimum inductance value satisfies both the following conditions:

$$L1 > \frac{V_{OUT} + V_d}{\Delta I_L \times F_{SW_VIN(max)}} = 2\,mH \tag{13}$$

$$L > \left[\left(\frac{L_{MIN}}{V_{IN}}\right)\right]\Big|_{T_J = T_{J(max)}} \times V_{IN(max)} = 2.65\,\frac{\mu H}{V} \times 375\,V \cong 1\,mH \tag{14}$$

In the application example, 2.2 mH is selected as the minimum standard value that satisfy Equation 13 and Equation 14. The value of Equation 14 can be found by characterization graph of Figure 10. Pick the value at the desired maximum junction temperature.

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8.2.1.2.8 Feedback Path (Q1, R_{FB1}, R_{FB2})

The feedback path of Q1, R_{FB1} and R_{FB2} implements a level-shifted direct feedback. R_{FB2} sets the current through the feedback path, and R_{FB1} sets the output voltage. Q1 acts as the level shifter and needs to be rated for high voltage. The output voltage is determined as follows:

$$V_{OUT} = V_{FB_TH} \times \frac{R_{FB1}}{R_{FB2}} + V_{BE}$$

where

- V_{OUT} is the output voltage.
- V_{FB_TH} is the FB pin voltage threshold = V_{FB_TH}.
- V_{BE} is the base-emitter saturation voltage of the external PNP transistor.
- R_{FB1} is the external resistor setting the output voltage (depending on the current set by R_{FB2}, and the V_{be}).
- R_{FB2} is the external resistor setting the current through the external feedback path. (15)

For the application example a target of ~20-μA of current is selected through the external feedback path (I_{FB}).

$$R_{FB2} = \frac{V_{FB_TH}}{I_{FB}} = \frac{1.0\,V}{\approx 20\,\mu A} = 50\,k\Omega \quad (16)$$

Choose a standard resistor size for R_{FB2} = 51 kΩ. For the high-voltage PNP transistor choose a 500-V rated transistor with a V_{BE} ≈ 0.5 V for the feedback current. To achieve the 12-V output voltage R_{FB1} needs to be:

$$R_{FB1} = \frac{V_{OUT} - V_{BE}}{V_{FB_TH}} \times R_{FB2} = \frac{12\,V - 0.5\,V}{1\,V} \times 51\,k\Omega = 586\,k\Omega \quad (17)$$

Choose a standard resistor size for R_{FB1} = 591 kΩ.

To change the output voltage, change the value for R_{FB1}. For example, to target a 5-V output voltage, R_{FB1} should be changed to a 230-kΩ resistor.

Accuracy of the output-voltage level depends proportionally on the variation of V_{FB_TH}, and on the absolute accuracy of V_{BE} according to Equation 16 and Equation 17.

The current through the feedback path is connected over the high voltage input (VIN), and this feedback current is always on. Higher current provides less noise-sensitive feedback, the feedback current should be minimized in order to minimize the total power consumption.

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8.2.1.3 Application Curves

Figure 17 shows the efficiency diagram of the converter, a design previous discussed. Figure 18 shows the output voltage vs output current diagram. The two diagrams were obtained by measuring efficiency (Figure 17), output current and output voltage (Figure 18) moving resistive load value from infinite (load disconnected) up to zero (output shorted). The different curves of the diagram correspond to different AC input voltage.

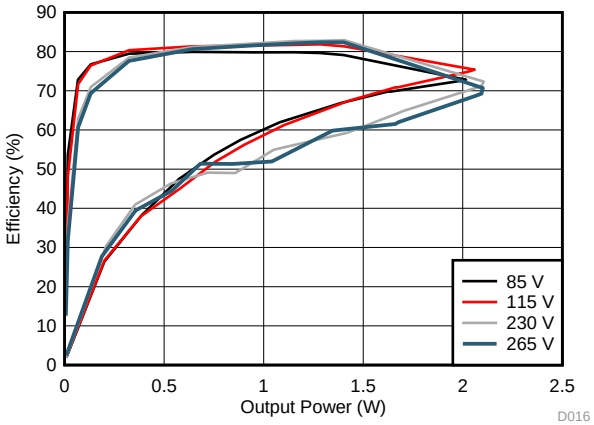

Figure 17. Efficiency vs Output Power Diagrams

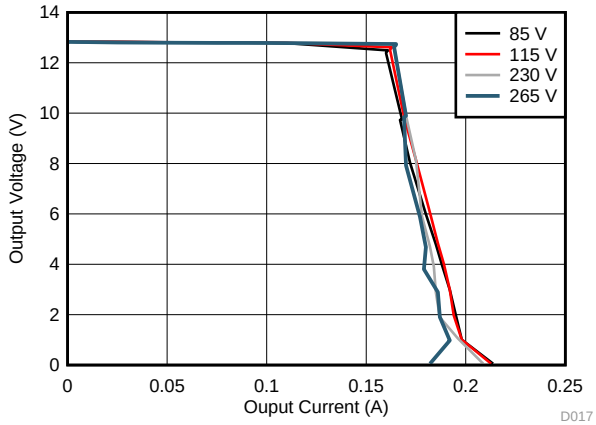

Figure 18. Output Voltage vs Output Current Diagram

Table 3 shows converter efficiency. Table 4 shows the converter input power in no-load conditions and output shorted conditions. The no-load condition shows the converter stand-by performance.

Table 3. Converter Efficiency

VIN_AC (V_{RMS})	LOAD (mA)	EFFICIENCY (%)	AVERAGE EFFICIENCY (%)
115	25	80.3	81.3
	50	81.4	
	75	81.6	
	100	81.9	
230	25	78.5	81.2
	50	81.1	
	75	82.1	
	100	82.7	

Table 4. No-Load and Output-Shorted Converter Input Power

V_{IN} (V_{RMS})	NO LOAD P_{IN} (mW)	OUTPUT SHORTED P_{IN} (mW)	OUTPUT SHORTED I_{OUT} (mA)
85	16	453	214
115	19.5	435	213
140	22.5	417	211
170	26	443	213
230	33	430	209
265	37.5	344	182

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8.2.2 12-V, 100-mA, High-Side Buck Converter

Figure 19 shows a typical application example of a non-isolated power supply, where the UCC28880 is connected in a high-side buck configuration having an output voltage that is positive with respect to the negative high-voltage input (VIN-).

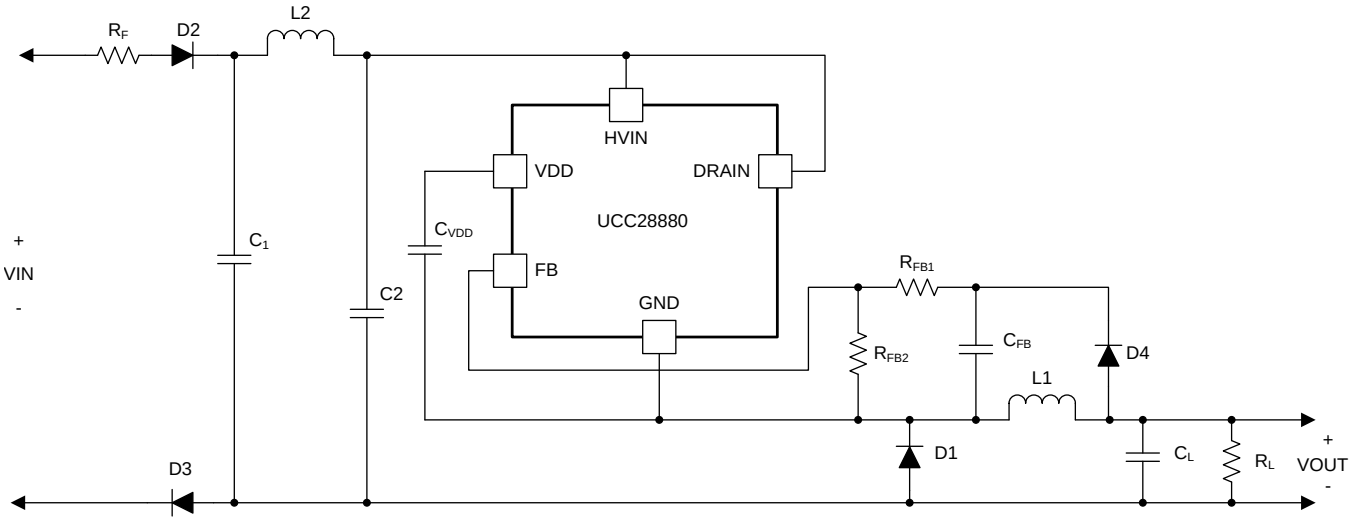

Figure 19. High-Side Buck Converter Schematic

8.2.2.1 Design Requirements

Table 5. Design specification

DESCRIPTION		MIN	MAX	UNIT
DESIGN INPUT				
V_{IN}	AC input Voltage	85	265	V_{RMS}
f_{LINE}	Line frequency	47	63	Hz
I_{OUT}	Output current	0	100	mA
DESIGN REQUIREMENTS				
P_{NL}	No-load input power		50	mW
V_{OUT}	Output voltage	12	14	V
ΔV_{OUT}	Output voltage ripple		250	mV
η	Converter efficiency	68%		

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8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Introduction

The low-side buck converter and high-side buck converter design procedures are very similar.

8.2.2.2.2 Feedback Path (C_{FB}, R_{FB1} and R_{FB2}) and Load Resistor (R_L)

In low-side buck converter the output voltage is always sensed by the FB pin and UCC28880 internal controller can turn on the MOSFET on VOUT. In high-side buck converter applications the information on the output voltage value is stored on C_{FB} capacitor. This information is not updated in real time. The information on C_{FB} capacitor is updated just after MOSFET turn-off event. When the MOSFET is turned off, the inductor current forces the freewheeling diode (D1 in Figure 19) to turn on and the GND pin of UCC28880 goes negative at $-V_{d1}$ (where V_{d1} is the forward drop voltage of diode D1) with respect to the negative terminal of bulk capacitor (C1 in Figure 19). When D1 is on, through diode D4, the C_{FB} capacitor is charged at $V_{OUT} – V_{d4} + V_{d1}$. Set the output voltage regulation level using Equation 18.

$$\frac{R_{FB1}}{R_{FB2}} = \frac{V_{OUT(T)} - V_{d4} + V_{d1} - V_{FB_TH}}{V_{FB_TH}} \cong \frac{V_{OUT(T)} - V_{FB_TH}}{V_{FB_TH}} \quad (18)$$

where

- V_{FB_TH} is the FB pin reference voltage.
- V_{OUT_T} is the target output voltage.
- R_{FB1}, R_{FB2} is the resistance of the resistor divider connected with FB pin (see Figure 19)
- The capacitor C_{FB} after D1 is discharged with a time constant that is $\tau fb = C_{FB} \times (R_{FB1} + R_{FB2})$.
- Select the time constant τ_{FB}, given in Equation 19

$$\tau_{FB} = C_{FB} \times \left(R_{FB1} + R_{FB2}\right) \cong \frac{1}{10} \times C_L \times R_L \quad (19)$$

The time constant selection leads to a slight output-voltage increase in no-load or light-load conditions. In order to reduce the output-voltage increase, increase τ_{FB}. The drawback of increasing τ_{FB} is t in high-load conditions V_{OUT} could drop.

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8.2.2.3 Application Curves

Figure 20 shows the output voltage vs output current. Different plots correspond to different converter AC input voltages. Figure 21 shows efficiency changes vs output power. Different plots correspond to different converter AC input voltages.

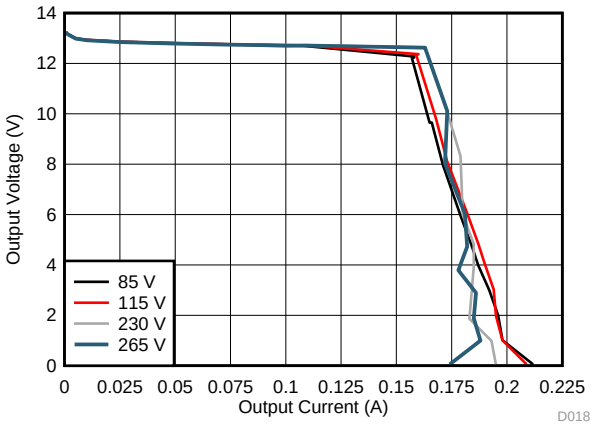

Figure 20. Output IV Characteristic

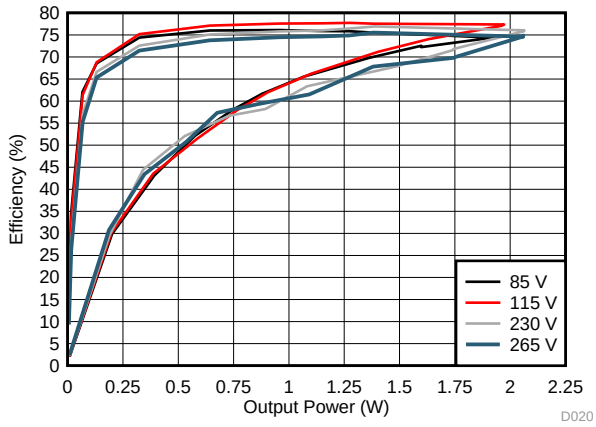

Figure 21. Efficiency vs P_{OUT}

Table 6. Converter Efficiency

V_{IN_AC} (V_{RMS})	LOAD (mA)	EFFICIENCY (%)	AVERAGE EFFICIENCY (%)
115	25	75.2	76.8
	50	77.1	
	75	77.6	
	100	77.7	
230	25	72.6	74.8
	50	75.1	
	75	75.7	
	100	76.3	

Table 7. No-Load and Output Shorted Converter Input Power

V_{IN} (V_{RMS})	NO LOAD P_{IN} (mW)	OUTPUT SHORTED P_{IN} (mW)	OUTPUT SHORTED I_{OUT} (mA)
85	31	415	212
115	34	399	209
140	36	414	211
170	38	401	208
230	44	394	195
265	47	333	174

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8.2.3 Additional UCC28880 Application Topologies

8.2.3.1 Low-Side Buck and LED Driver – Direct Feedback (Level Shifted)

Features include:

- Output Referenced to Input
- Negative Output (V_{OUT}) with Respect to VIN+
- Step Down: $V_{OUT} < V_{IN}$
- Direct Level-Shifted Feedback

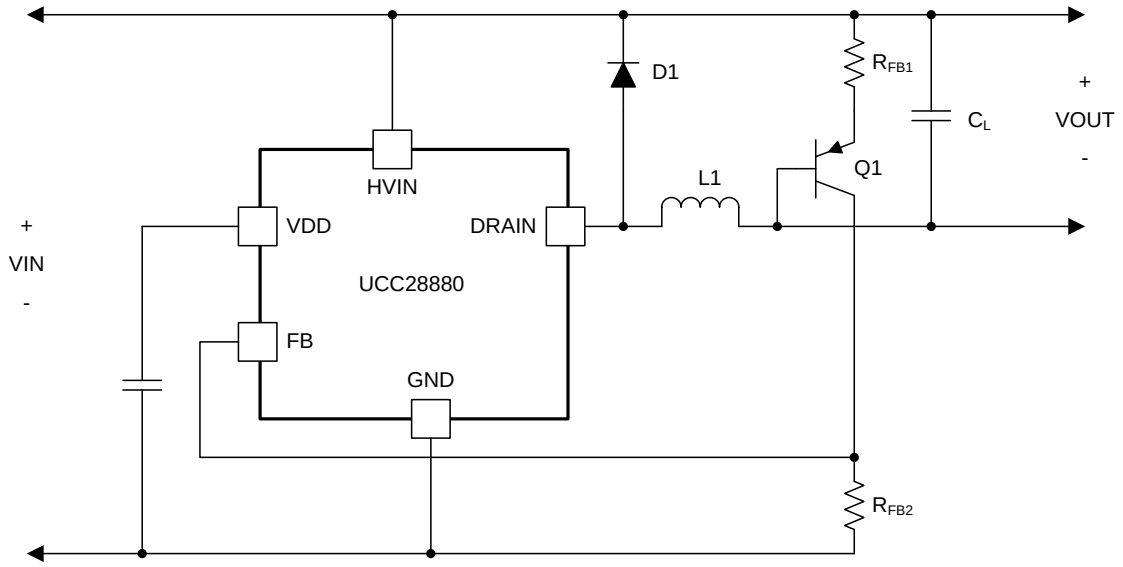

Figure 22. Low-Side Buck, Direct Feedback (Level Shifted)

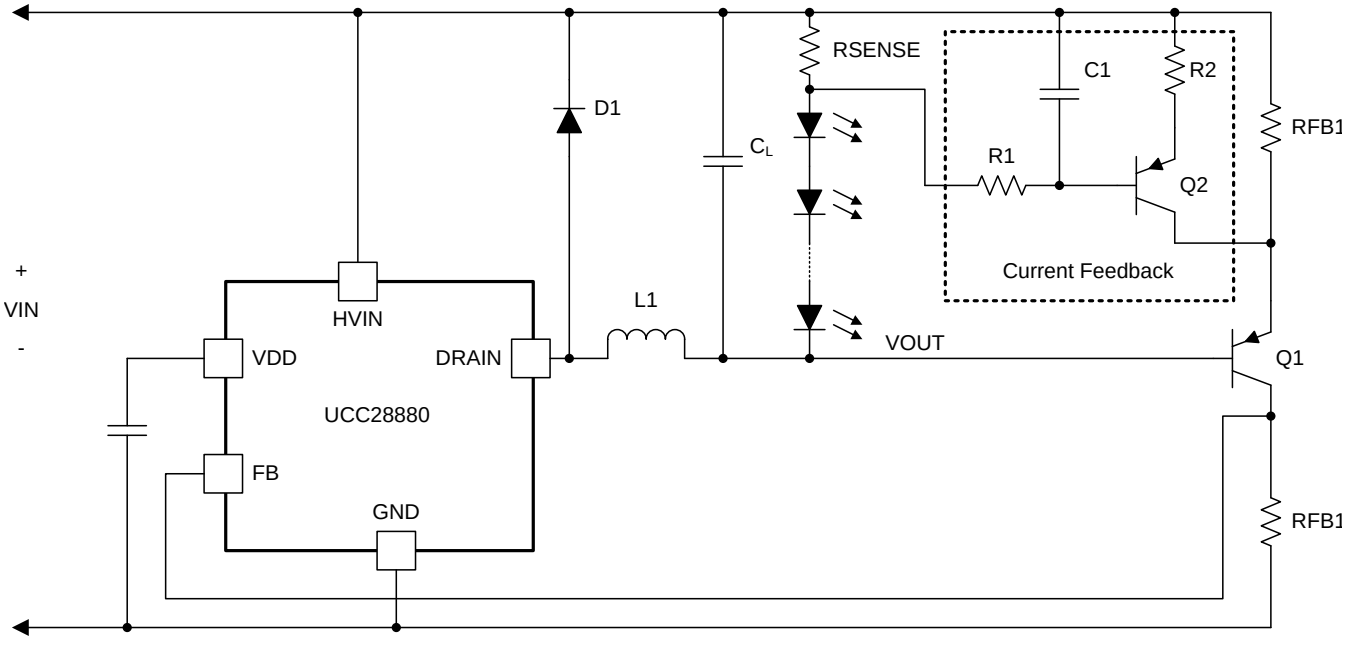

Figure 23. Low-Side Buck LED Driver, Direct Feedback (Level Shifted) image.

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8.2.3.2 12-V, 100-mA High-Side Buck Converter

Features include:

- Output Referenced to Input
- Positive Output (V) with Respect to VIN-
- Step Down (V_{OUT} < V_{IN})

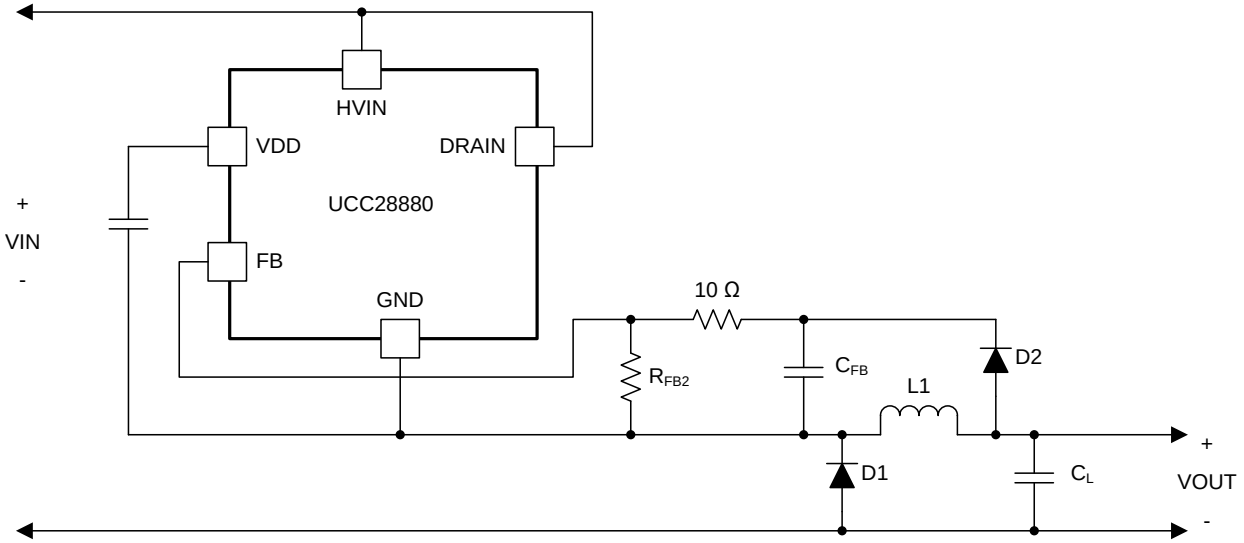

Figure 24. High-Side Buck Converter Schematic

8.2.3.3 Non-Isolated, Low-Side Buck-Boost Converter

Features Include:

- Output Referenced to Input
- Positive Output (V_{OUT}) with Respect to VIN+
- Step Up, Step Down: V_{OUT} </> V_{IN}
- Direct Level-Shifted Feedback

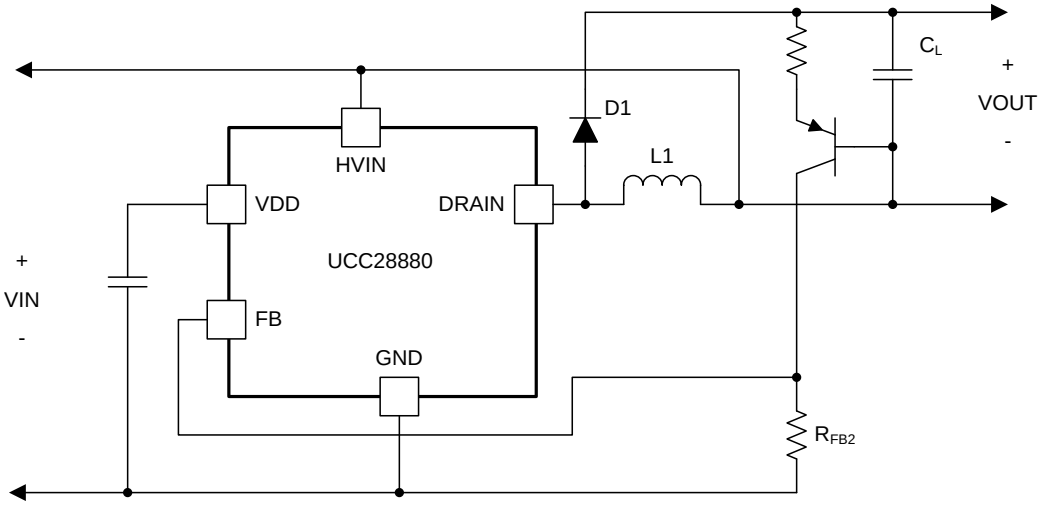

Figure 25. Low-Side Buck-Boost Converter

8.2.3.4 Non-Isolated, High-Side Buck-Boost Converter

Features include:

- Output Referenced to Input
- Positive Output (V_{OUT}) with Respect to VIN-
- Step Up, Step Down: V_{OUT} </> V_{IN}

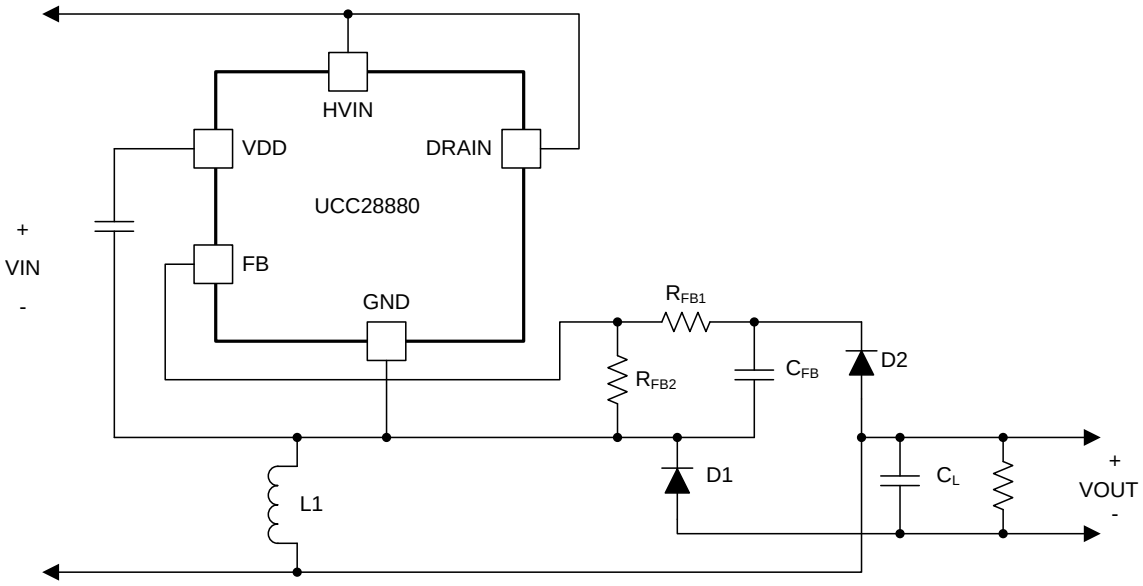

Figure 26. High-Side Buck-Boost Converter

8.2.3.5 Non-Isolated Flyback Converter

Features include:

- Output Referenced to Input
- Positive Output (V_{OUT}) with Respect VIN-
- Direct Feedback

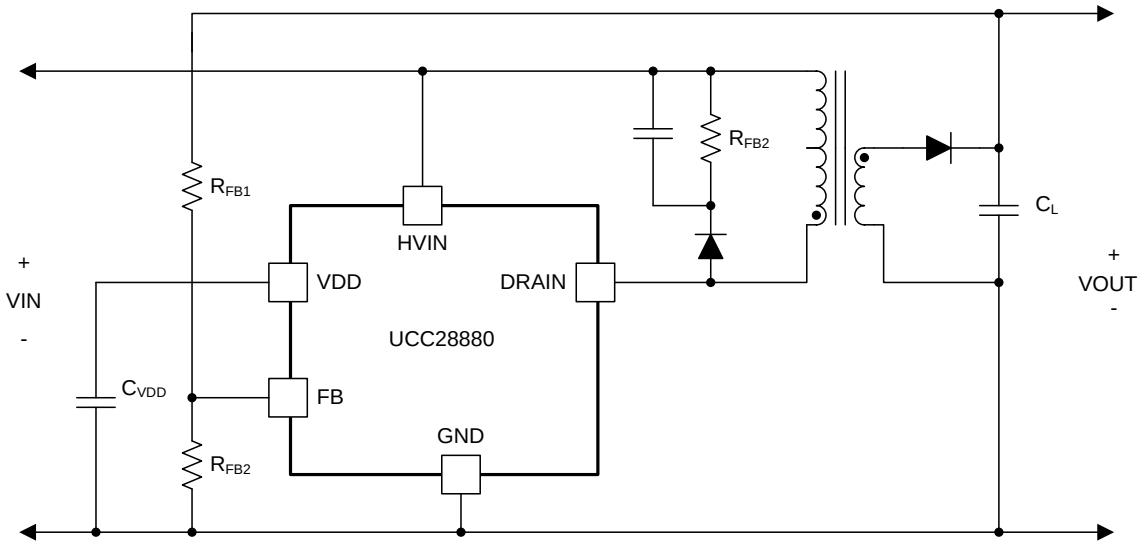

Figure 27. Non-Isolated Flyback Configuration

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8.2.3.6 Isolated Flyback Converter

Features include:

- Output Isolated from Input
- Direct Feedback

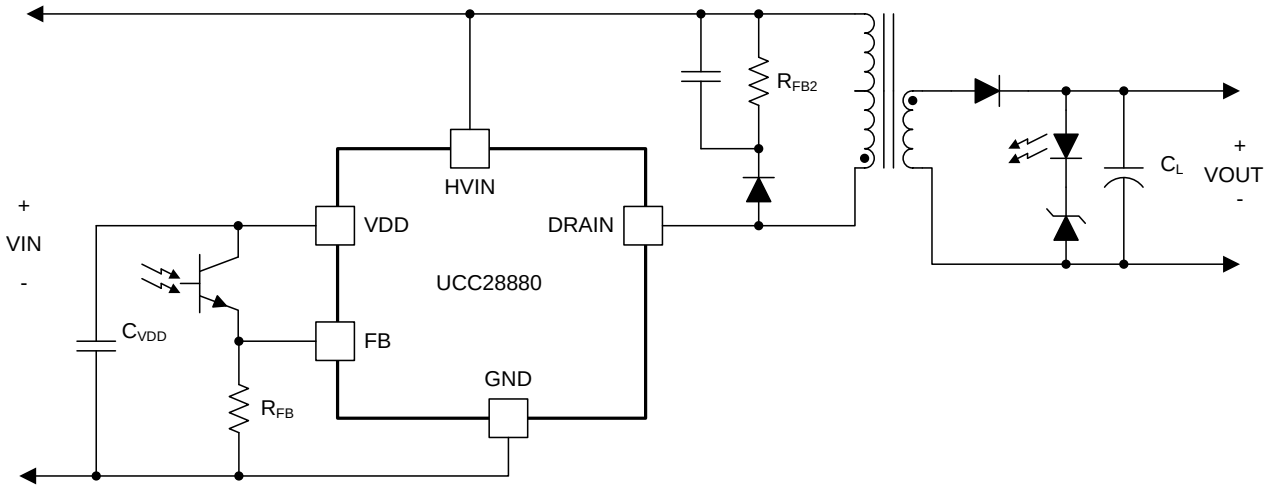

Figure 28. Isolated Flyback Converter

9 Power Supply Recommendations

The VDD capacitor recommended value is 100 nF to ensure high-phase margin of the internal 5-V regulator and it should be placed close to VDD pin and GND pins to minimize the series resistance and inductance.

The VDD pin provides a regulated 5-V output but it is not intended as a supply for external load. Do not supply VDD pin with external voltage source (for example the auxiliary winding of flyback converter).

Always keep GND pin 1 and GND pin 2 connected together with the shortest possible connection.

10 Layout

10.1 Layout Guidelines

- In both buck and buck-boost low-side configurations, the copper area of the switching node DRAIN should be minimized to reduce EMI.
- Similarly, the copper area of the FB pin should be minimized to reduce coupling to feedback path. Loop C_L, Q1, R_{FB1} should be minimized to reduce coupling to feedback path.
- In high-side buck and buck boost the GND, VDD and FB pins are all part of the switching node so the copper area connected with these pins should be optimized. Large copper area allows better thermal management, but it causes more common mode EMI noise. Use the minimum copper area that is required to handle the thermal dissipation.
- Minimum distance between 700-V coated traces is 1.41 mm (60 mils).

10.2 Layout Example

Figure 29 shows and example PCB layout for UCC28880 in low-side buck configuration.

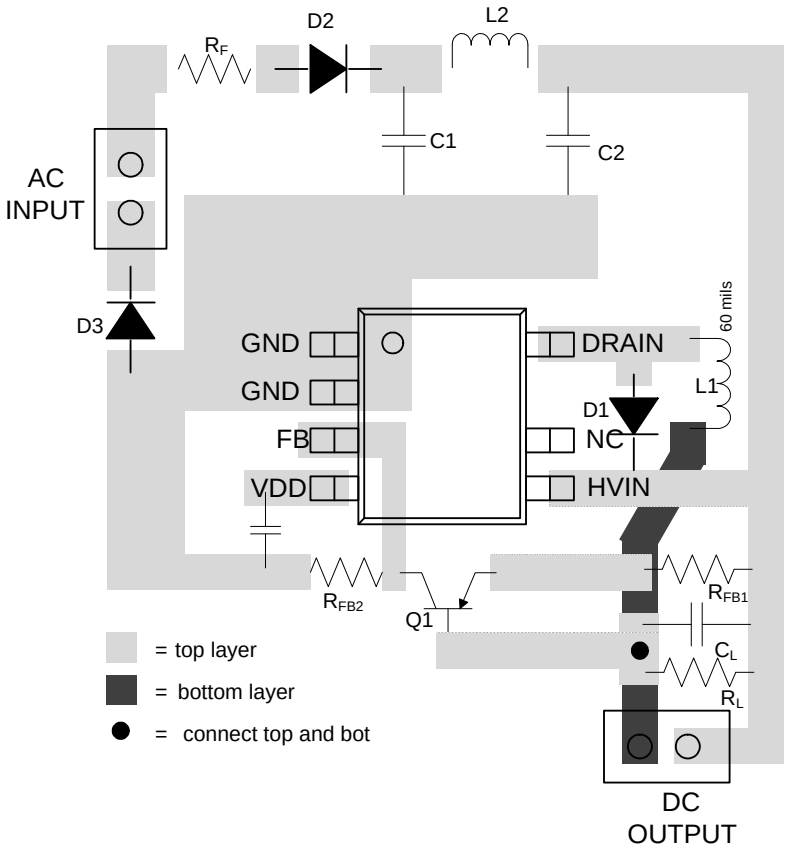

Figure 29. UCC28880 Layout Example

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11 Device and Documentation Support

11.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the UCC28880 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Trademarks

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All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC28880D	ACTIVE	SOIC	D	7	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	U28880	Samples
UCC28880DR	ACTIVE	SOIC	D	7	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	U28880	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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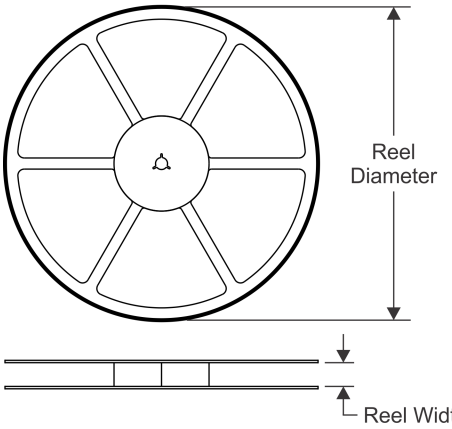
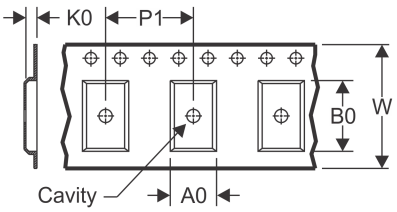
TAPE AND REEL INFORMATION

REEL DIMENSIONS

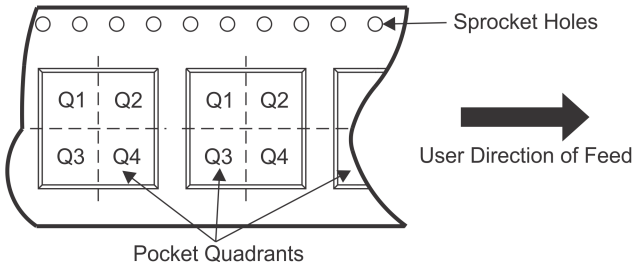


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

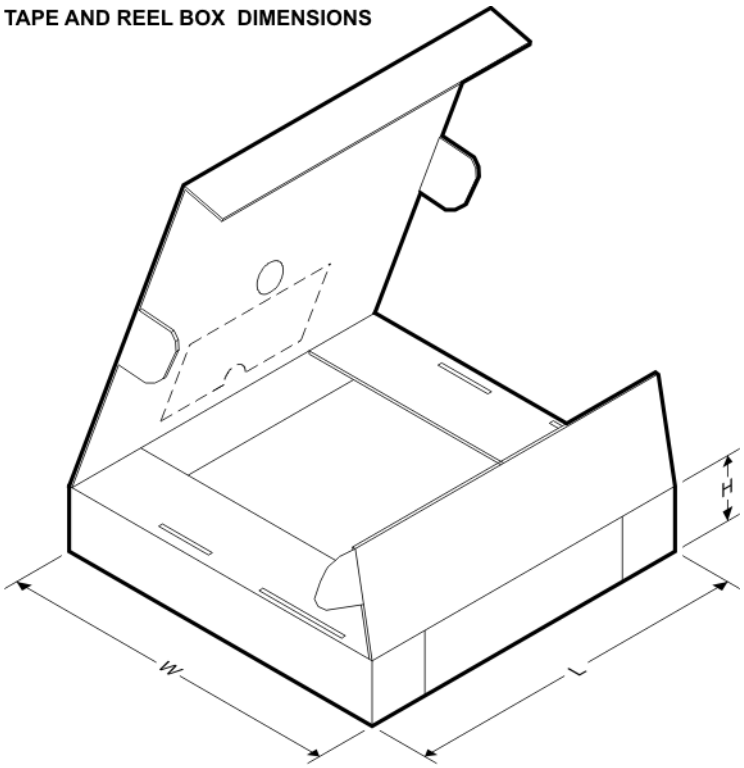
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

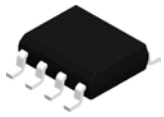
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28880DR	SOIC	D	7	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28880DR	SOIC	D	7	2500	367.0	367.0	35.0

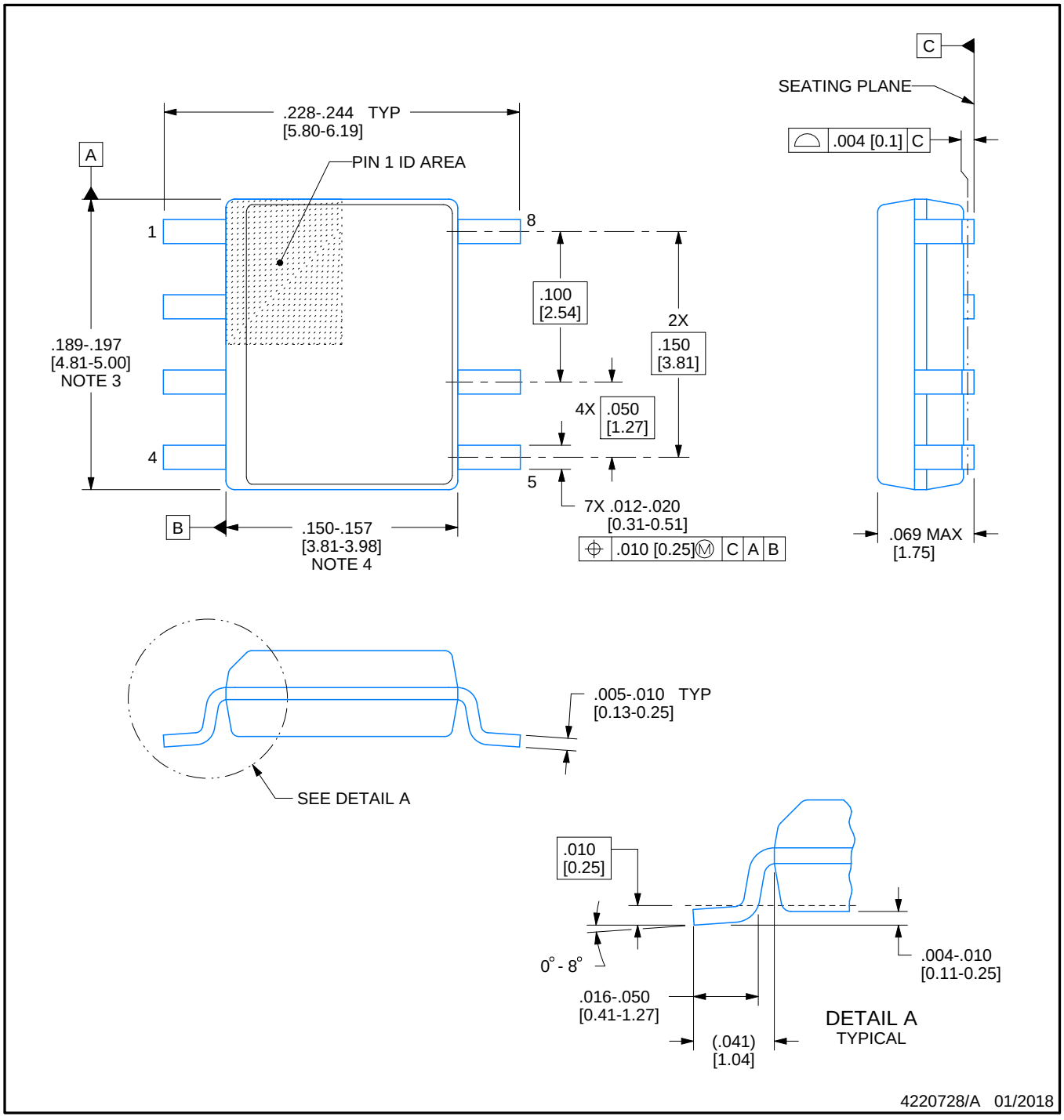


PACKAGE OUTLINE

D0007A

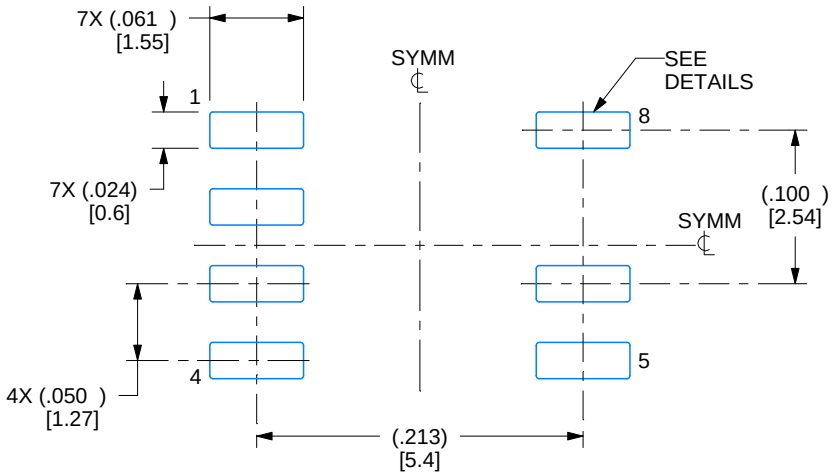
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

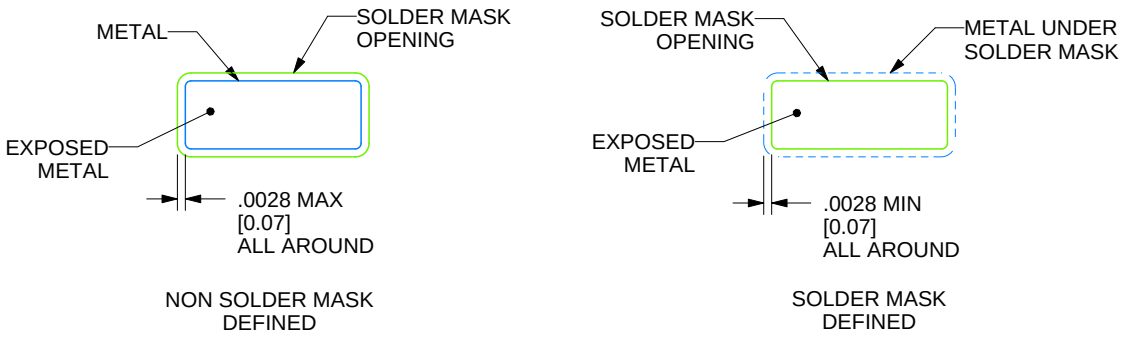


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4220728/A 01/2018

NOTES: (continued)

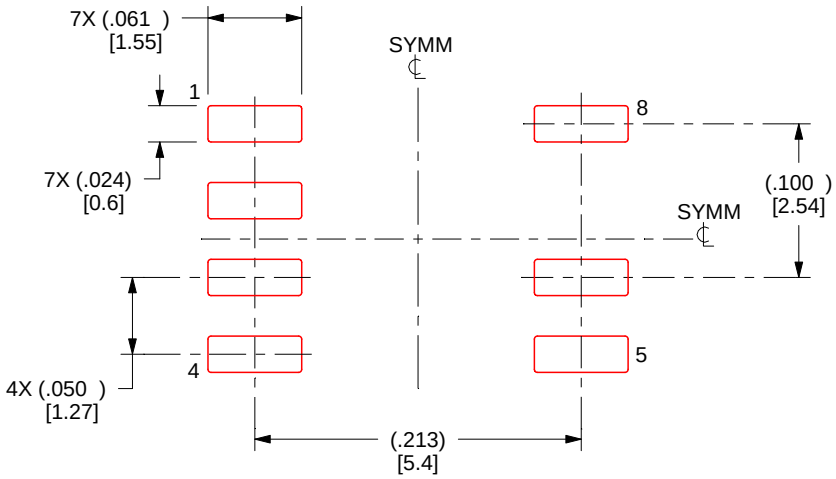
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0007A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4220728/A 01/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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