THE DATASHEET OF

UC3853D

UNITRODE

UC1853
UC2853
UC3853

High Power Factor Preregulator

FEATURES

- Complete 8-pin Power Factor Solution
- Reduced External Components
- RMS Line Voltage Compensation
- Precision Multiplier/Squarer/Divider
- Internal 75kHz Synchronizable Oscillator
- Average Current Mode PWM Control
- Overvoltage Protection Comparator
- High Current, Clamped Gate Driver

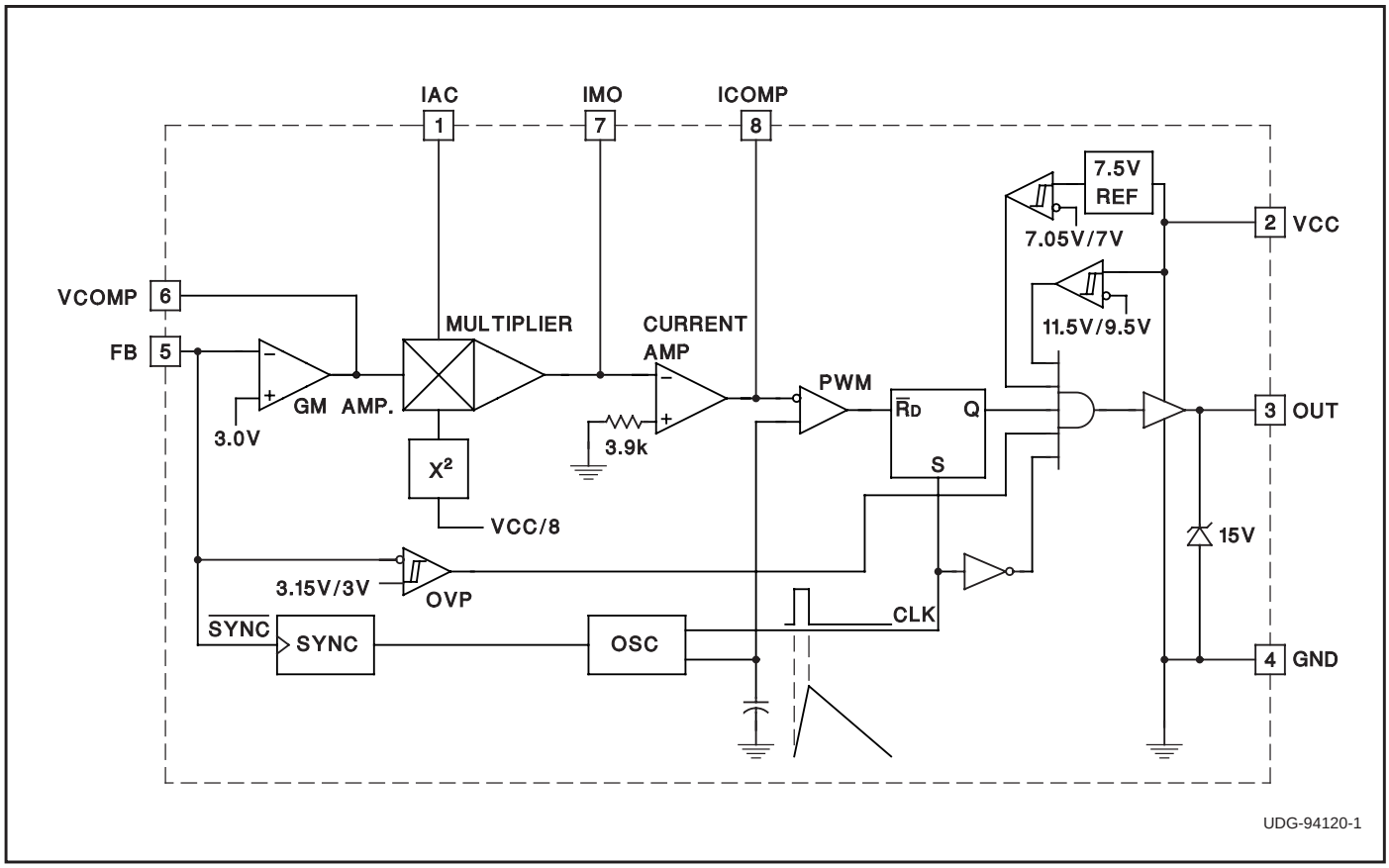
DESCRIPTION

The UC3853 provides simple, yet high performance active power factor correction. Using the same control technique as the UC1854, this 8-pin device exploits a simplified architecture and an internal oscillator to minimize external component count. The UC3853 incorporates a precision multiplier/squarer/divider circuit, voltage and current loop error amplifiers, and a precision voltage reference to implement average current mode control with RMS line voltage compensation. This control technique maintains constant loop gain with changes in input voltage, which minimizes input line current distortion over the worldwide input voltage range.

The internal 75kHz oscillator includes an external clock input, allowing synchronization to downstream converters. Additionally, the device features an overvoltage protection comparator, a clamped MOSFET gate driver which self-biases low during undervoltage lockout, and low startup and supply current.

These devices are available in 8-pin plastic and ceramic dual in-line (DIP) packages, and 8-lead small outline (SOIC) packages. The UC1853 is specified for operation from –55°C to +125°C, the UC2853 is specified for operation from –25°C to +85°C, and the UC3853 is specified for operation from 0°C to +70°C.

BLOCK DIAGRAM



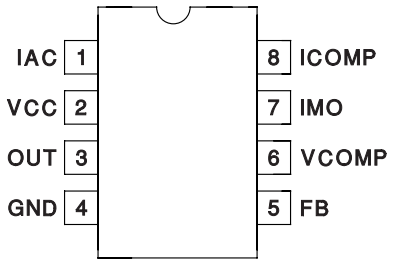
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC) 40V
Output Drive Current,
  Continuous 0.125A
  Peak 0.5A
Output Minimum Voltage . . . . . –0.3V
IAC Maximum Input Current 1mA
IMO Maximum Output Current . . . . . –2mA
IMO Minimum Voltage . . . . . –0.3V
FB Maximum Input Voltage 5V
VCOMP Maximum Voltage 6.2V
ICOMP Sourcing Current . . . . . Self-Limiting
ICOMP Sinking Current 20mA
ICOMP Maximum Voltage 7.2V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

All voltages with respect to GND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
J or N, D Package



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these parameters apply for T_A = –55°C to +125°C for the UC1853; –25°C to +85°C for the 2853; and 0°C to +70°C for the UC3853; VCC = 16V, V_{FB} = 3V, I_{AC} = 100µA, V_{VCOMP} = 3.75V, V_{ICOMP} = 3V, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout Section					
VCC Turn-on Threshold	V_{VCOMP}, V_{ICOMP} Open		11.5	13	V
Hysteresis		1.5	1.8	2.1	V
Supply Current Section					
I_{VCC} Startup	VCC = 8V, IAC = 100µA; V_{VCOMP}, V_{ICOMP} Open		250	500	µA
I_{VCC}	IAC = 0µA, V_{ICOMP} = 0V		10	15	mA
Voltage Loop Error Amplifier Section					
Transconductance	IOUT = ± 20µA 0-70C	300	450	575	µmho
	Temperature	135		640	µmho
Input Voltage	0-70C	2.925	3	3.075	V
	Temperature	2.9		3.1	V
AVOL	V_{VCOMP} = 1V – 4V	50	60		dB
Output Sink Current	V_{FB} = 3.2V, V_{VCOMP} = 3.75V	20	50		µA
Output Source Current	V_{FB} = 2.8V, V_{VCOMP} = 3.75V		–50	–20	µA
Output Voltage High		5.5	6		V
Output Voltage Low			0.6	0.9	V
Current Loop Error Amplifier Section					
Offset Voltage		0		6	mV
Voltage Gain	V_{ICOMP} = 1V – 4V		70		dB
Sink Current	V_{IMO} = 100mV, V_{ICOMP} = 3V	1			mA
Source Current	V_{IMO} = –0.1V, V_{ICOMP} = 3V		–150	–80	µA
Output High	I_{ICOMP} = –50mA	6	6.8		V
Output Low	I_{ICOMP} = 50µA		0.3	0.8	V
PWM Modulator Gain	V_{ICOMP} = 2V – 3V (Note 1)		20		%/V

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated, these parameters apply for T_A = –55°C to +125°C for the UC1853; –25°C to +85°C for the 2853; and 0°C to +70°C for the UC3853; VCC = 16V, V_{FB} = 3V, I_{AC} = 100µA, V_{VCOMP} = 3.75V, V_{ICOMP} = 3V, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Multiplier Section					
Output Current – IAC Limited	VCC = 11V, V_{VCOMP} = 6V	–230	–200	–170	µA
Output Current – Zero	IAC = 0µA	–2	–0.2	2	µA
Output Current – Power Limited	VCC = 12V, V_{VCOMP} = 5.5V	–236	–178	–168	µA
Output Current	VCC= 12V, V_{VCOMP} = 2V		–22		µA
	VCC= 12V, V_{VCOMP} = 5V		–156		µA
	VCC= 40V, V_{VCOMP} = 2V		–2		µA
	VCC= 40V, V_{VCOMP} = 5V		–14		µA
Multiplier Gain Constant	VCC= 12V, V_{VCOMP} = 5.5V (Note 2)	–1.05	–0.9	–0.75	V^{-1}
Oscillator Section					
Oscillator Initial Frequency	T_A = 25°C	67.5	75	82.5	kHz
Oscillator Frequency	Line, Load, Temperature	56	75	94	kHz
Synchronization Frequency Range				100	kHz
Synchronization Pulse Amplitude	Pulse slew rate = 100V/µsec (Note 3)		2		V
Output Driver Section					
Maximum Output Voltage	0mA load, VCC = 20V	12	15	17.5	V
Output High	0mA load, VCC = 12V, ref. to VCC	–2.7	–1.7		V
	–50mA load, VCC = 12V, ref. to VCC	–3	–2.2		V
Output Low (Device Inactive)	Vcc = 0V, 20mA load (Sinking)		0.9	2.0	V
Output Low (Device Active)	50mA load (Sinking)		0.5	1	V
OUT Rise Time	1nF from OUT to GND		55	100	ns
OUT Fall Time	1nF from OUT to GND		35	100	ns
OUT Maximum Duty Cycle	V_{ICOMP} = 0V	88	93		%
OVP Comparator Section					
Threshold Voltage	Volts Above EA Input V	90	150		mV
Hysteresis			80		mV

Note 1:

$$PWM\ modulator\ gain = \frac{\Delta DutyCycle}{\Delta V_{ICOMP}}$$

Note 2:

$$Gain\ constant\ (K) = \frac{IAC \bullet (VCOMP - 1.5V)}{IMO \bullet VCC \bullet \frac{VCC}{64}}\ ,\ VCC = 12V.$$

Note 3.
Synchronization is accomplished with a falling edge of 2V magnitude and 100V/µsec slew rate.

PIN DESCRIPTIONS

FB: Voltage Amplifier Inverting Input, Overvoltage Comparator Input, Sync Input. This pin serves three functions. FB accepts a fraction of the power factor corrected output voltage through a voltage divider, and is nominally regulated to 3V. FB voltages 5% greater than nominal will trip the overvoltage comparator, and shut down the output stage until the output voltage drops 5%. The internal oscillator can be synchronized through FB by injecting a 2V clock signal though a capacitor. To prevent false tripping of the overvoltage comparator, the clock signal must have a fast falling edge, but a slow rising edge. See Application Note U-159 for more information.

GND: Ground. All voltages are measured with respect to GND. The VCC bypass capacitor should be connected to ground as close to the GND pin as possible.

IAC: AC Waveform Input. This input provides voltage waveform information to the multiplier. The current loop will try to produce a current waveform with the same shape as the IAC signal. IAC is a low impedance input, nominally at 2V, which accepts a current proportional to the input voltage. Connect a resistor from the rectified input line to IAC which will conduct 500mA at maximum line voltage.

IMO: Multiplier Output and Current Sense Inverting Input. The output of the multiplier and the inverting input of the current amplifier are connected together at IMO. Avoid bringing this input below –0.5V to prevent the internal protection diode from conducting. The multiplier output is a current, making this a summing node and allowing a differential current error amplifier configuration to reject ground noise. The input resistance at this node should be 3.9k to minimize input bias current induced offset voltage. See the Applications section for the recommended circuit configuration.

OUT: Gate Driver Output. OUT provides high current gate drive for the external power MOSFET. A 15V clamp prevents excessive MOSFET gate-to-source voltage so that the UC3853 can be operated with VCC and high as 40V. A series gate resistor of at least 5 ohms should be used to minimize clamp voltage overshoot. In addition, a Schottky diode such as a 1N5818 connected between OUT and GND may be necessary to prevent parasitic substrate diode conduction.

ICOMP: Current Loop Error Amplifier Output. The current loop error amplifier is a conventional operational amplifier with a 150µA current source class A output stage. Compensate the current loop by placing an impedance between ICOMP and IMO. This output can swing above the oscillator peak voltage, allowing zero duty cycle when necessary.

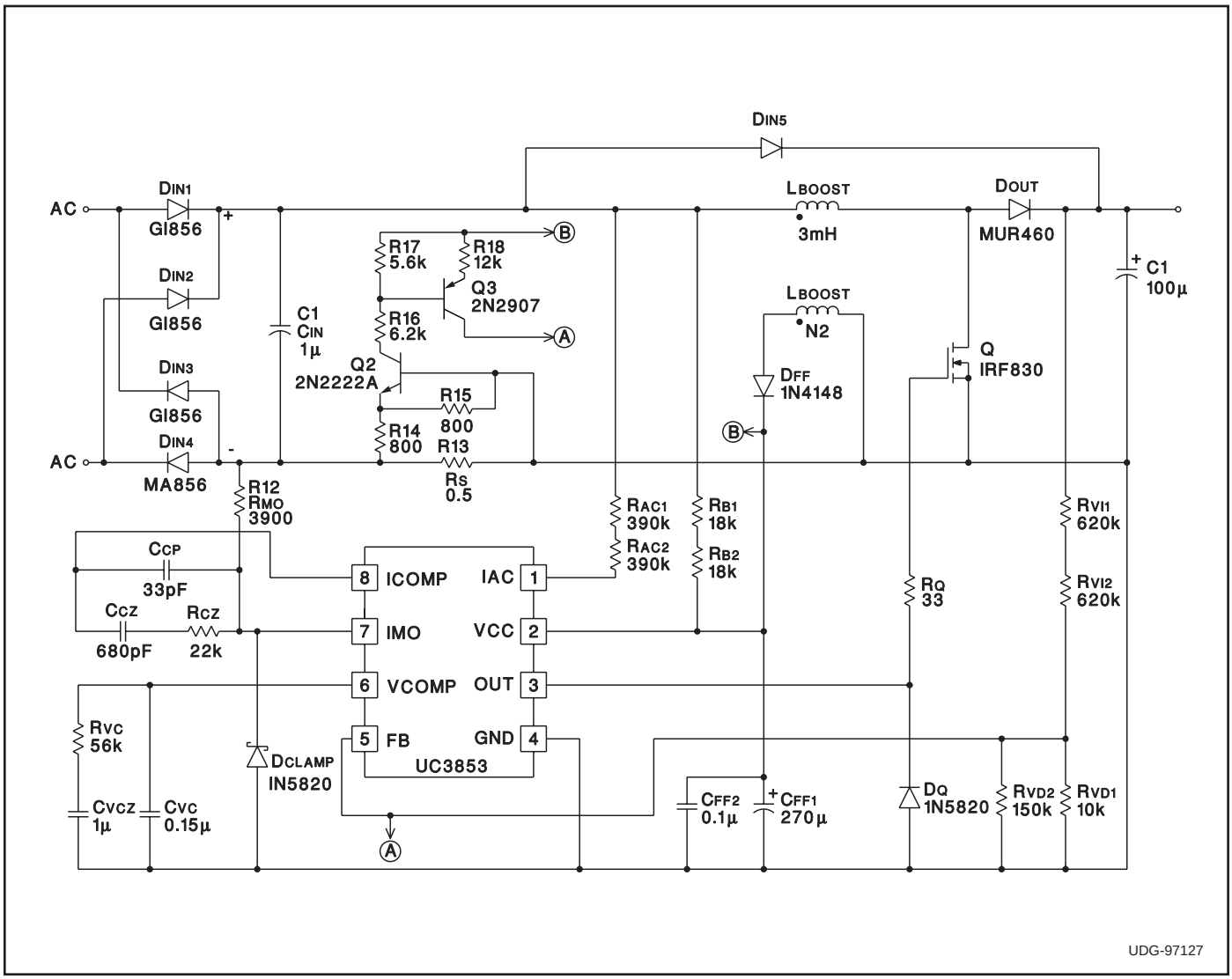
VCC: Input Supply Voltage. This pin serves two functions. It supplies power to the chip, and an input voltage level signal to the squarer circuit. When this input is connected to a DC voltage proportional to the AC input RMS voltage, the voltage loop gain is reduced by

$$\frac{64}{V_{CC}{}^2}.$$

This configuration maintains constant loop gain. The UC3853 input voltage range extends from 12V to 40V, allowing an AC supply voltage range in excess of 85VAC to 265VAC. Bypass VCC with at least a 0.1µF ceramic capacitor to ensure proper operation. See the Applications section for the recommended circuit configuration.

VCOMP: Voltage Loop Error Amplifier Output. The voltage loop error amplifier is a transconductance type operational amplifier. A feedback impedance between VCOMP and FB for loop compensation must be avoided to maintain proper operation of the overvoltage protection comparator. Instead, compensate the voltage loop with an impedance between VCOMP and GND. When VCOMP is below 1.5V, the multiplier output current is zero.

UC3853 TYPICAL APPLICATION



Note: the application circuit shown is a 100W, 75KHz design. Additional application information can be found in Application Note U–159 and Design Note DN–78.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2853D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	UC2853D	Samples
UC2853DTR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	UC2853D	Samples
UC2853N	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	UC2853N	Samples
UC3853D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3853D	Samples
UC3853DTR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3853D	Samples
UC3853N	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UC3853N	Samples
UC3853NG4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UC3853N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

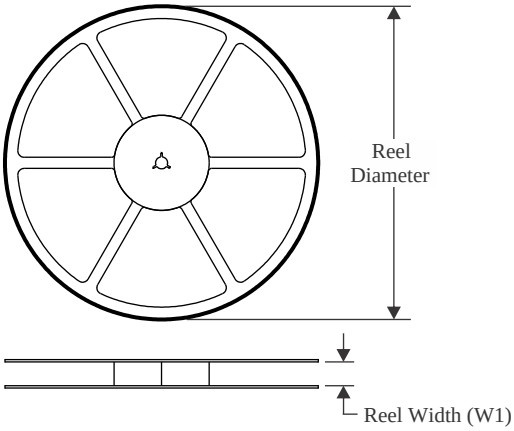
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

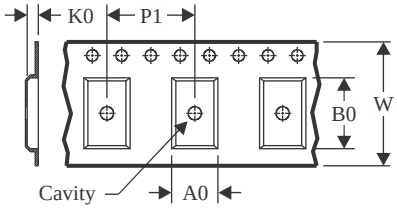
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

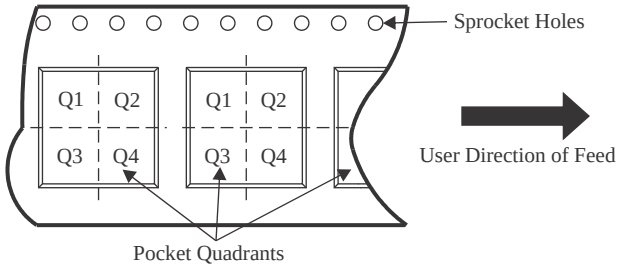


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

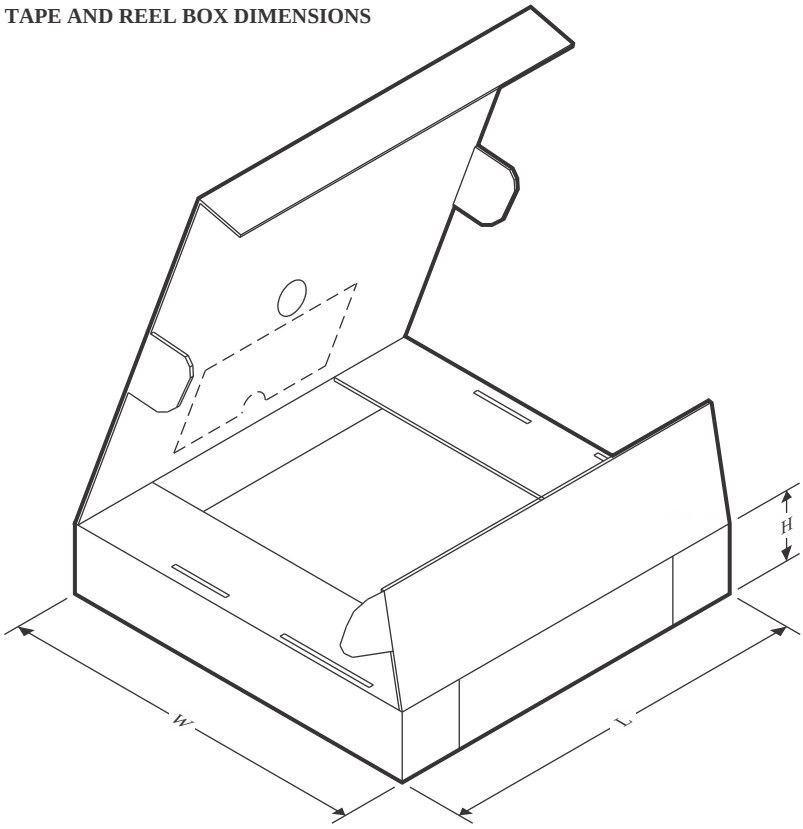
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2853DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3853DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

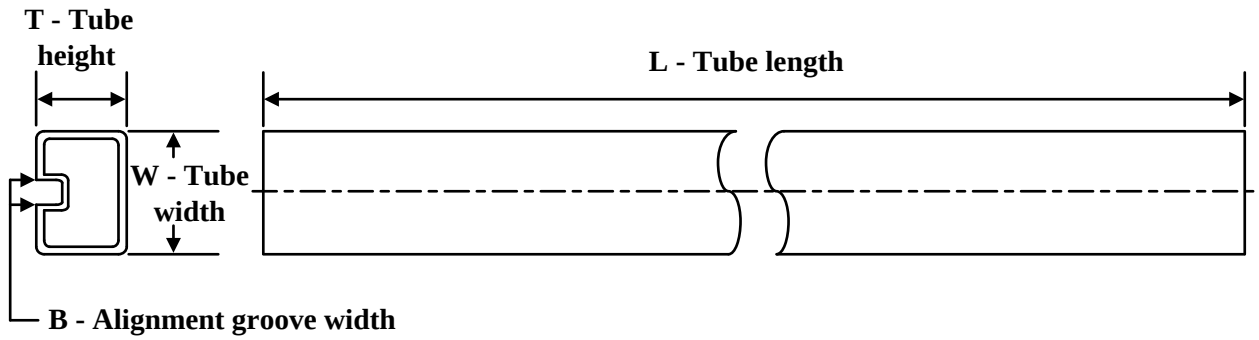
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2853DTR	SOIC	D	8	2500	356.0	356.0	35.0
UC3853DTR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UC2853D	D	SOIC	8	75	506.6	8	3940	4.32
UC2853N	P	PDIP	8	50	506	13.97	11230	4.32
UC3853D	D	SOIC	8	75	506.6	8	3940	4.32
UC3853N	P	PDIP	8	50	506	13.97	11230	4.32
UC3853NG4	P	PDIP	8	50	506	13.97	11230	4.32

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