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TW2864

4-Channel Video Decoders and Audio Codecs For Security Applications

FN7745
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The TW2864 includes four high quality NTSC/PAL/SECAM video decoders that convert analog composite video signal to digital component YCbCr data for security applications. The TW2864 contains four 10-bit ADC and proprietary clamp and gain controllers and utilizes 4H comb filter for separating luminance and chrominance to reduce cross noise artifacts. The TW2864 adopts the image enhancement techniques, such as IF compensation filter, CTI and programmable peaking. The TW2864 also includes audio CODEC, which has four audio Analog-to-Digital converters and one Digital-to-Analog converter. A built-in audio controller can generate digital outputs for recording/mixing and accepts digital input for playback.

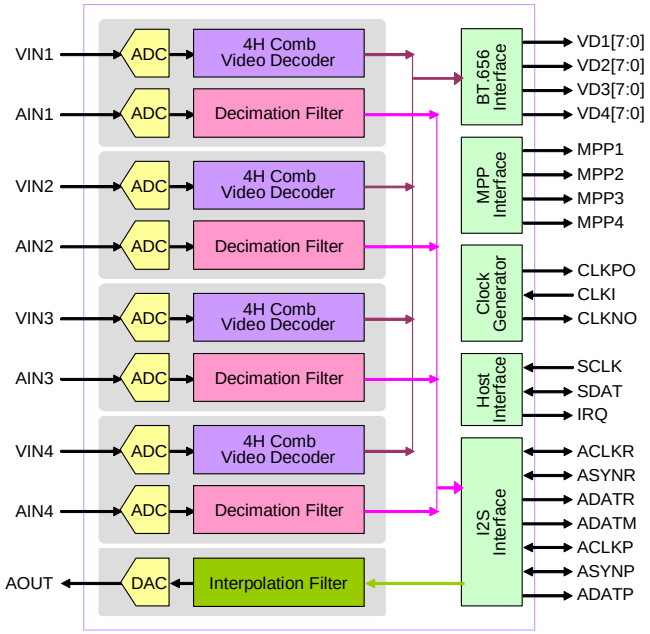
Features

- Accepts all NTSC(M/4.43) / PAL(B/D/G/H/I/K/L/M/N/60)/SECAM standards with auto detection
- Integrated four video analog anti-aliasing filters and 10-bit CMOS ADCs
- High performance adaptive 4H comb filters for all NTSC/PAL standards
- IF compensation filter for improvement of color demodulation
- Color Transient Improvement (CTI)
- Automatic white peak control
- Programmable hue, saturation, contrast, brightness and sharpness
- Proprietary fast video locking system for non-realtime applications
- Supports the standard ITU-R BT.656 format or time multiplexed output with 54/108MHz
- Provides simultaneous four channel Full D1 and CIF time-multiplexed outputs with 54MHz
- Integrated four audio ADCs and one audio DAC
- Provides multi-channel audio mixed analog output
- Supports I2S/DSP Master/Slave interface for record output and playback input
- PCM 8/16-bit and u-Law/A-Law 8-bit for audio word length
- Programmable audio sample rate that covers popular frequencies of 8/16/32/44.1/48kHz
- Supports a two-wire serial host interface
- Ultra low power consumption (Typical 388.5mW)
- 100 pin LQFP package

Device Type

PRODUCT TYPE	AUDIO FEATURES	DEFAULT CLOCK RATE
TW2864A	√	108MHz
TW2864B	√	54MHz
TW2864C	N/A	108MHz
TW2864D	N/A	54MHz

Block Diagram



Ordering Information

PART NUMBER	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
TW2864A-LD1-CR	TW2864A LD1-CR	100 LEAD LQFP (12mmx12mm)	Q100.12X12
TW2864A-LD1-GR	TW2864A LD1-GR	100 LEAD LQFP (12mmx12mm)	Q100.12X12
TW2864B-LC2-GR	TW2864B LC2-GR	100 LEAD LQFP (12mmx12mm)	Q100.12X12
TW2864B-LD1-CR	TW2864B LD1-CR	100 LEAD LQFP (12mmx12mm)	Q100.12X12
TW2864B-LD1-GR	TW2864B LD1-GR	100 LEAD LQFP (12mmx12mm)	Q100.12X12
TW2864C-LD1-CR	TW2864C LD1-CR	100 LEAD LQFP (12mmx12mm)	Q100.12X12
TW2864C-LD1-GR	TW2864C LD1-GR	100 LEAD LQFP (12mmx12mm)	Q100.12X12
TW2864D-LD1-GR	TW2864D LD1-GR	100 LEAD LQFP (12mmx12mm)	Q100.12X12
TW2864H-LD1-CR	TW2864H LD1-CR	100 LEAD LQFP (12mmx12mm)	Q100.12X12
TW2864H-LD1-GR	TW2864H LD1-GR	100 LEAD LQFP (12mmx12mm)	Q100.12X12
TW2864S-LD1-CR	TW2864S LD1-CR	100 LEAD LQFP (12mmx12mm)	Q100.12X12
TW2864S-LD1-GR	TW2864S LD1-GR	100 LEAD LQFP (12mmx12mm)	Q100.12X12

NOTE:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

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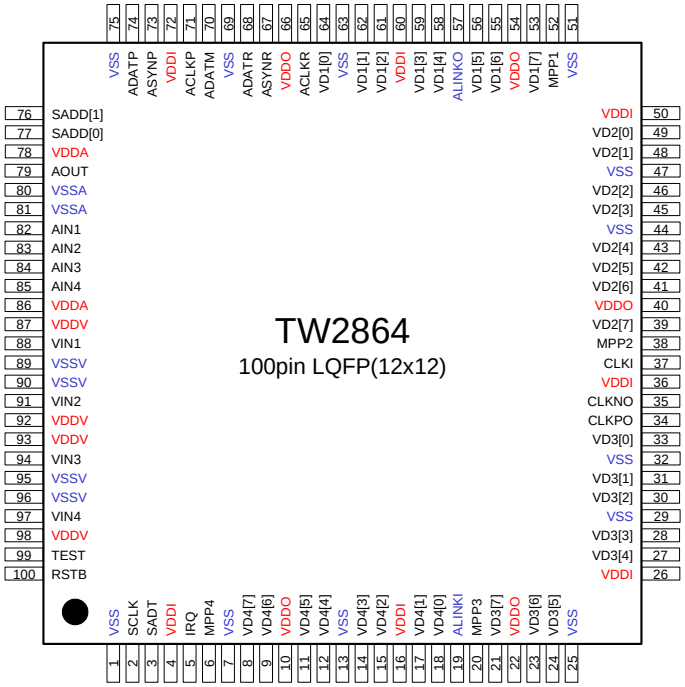
Pin Configuration



Pin Descriptions

Analog Video/Audio Interface Pins

NAME	NUMBER	TYPE	DESCRIPTION
VIN1	88	A	Composite video input of channel 1.
VIN2	91	A	Composite video input of channel 2.
VIN3	94	A	Composite video input of channel 3.
VIN4	97	A	Composite video input of channel 4.
AIN1	82	A	Audio input of channel 1.
AIN2	83	A	Audio input of channel 2.
AIN3	84	A	Audio input of channel 3.
AIN4	85	A	Audio input of channel 4.
AOUT	79	A	Audio mixing output.

Digital Video/Audio Interface Pins

NAME	NUMBER	TYPE	DESCRIPTION
VD1[7:0]	53, 55, 56, 58, 59, 61, 62, 64	O	Video data output of channel 1.
VD2[7:0]	39, 41, 42, 43, 45, 46, 48, 49	O	Video data output of channel 2.
VD3[7:0]	21, 23, 24, 27, 28, 30, 31, 33	O	Video data output of channel 3.
VD4[7:0]	8, 9, 11, 12, 14, 15, 17, 18	O	Video data output of channel 4.
MPP1	52	O	HS/VS/FLD/ACTIVE/NOVID of channel 1.
MPP2	38	O	HS/VS/FLD/ACTIVE/NOVID of channel 2.
MPP3	20	O	HS/VS/FLD/ACTIVE/NOVID of channel 3.
MPP4	6	O	HS/VS/FLD/ACTIVE/NOVID of channel 4.
ACLKR	65	IO	Audio serial clock input/output of record.
ASYNR	67	IO	Audio serial sync input/output of record.
ADATR	68	O	Audio serial data output of record.
ADATM	70	O	Audio serial data output of mixing.
ACLKP	71	IO	Audio serial clock input/output of playback.
ASYNP	73	IO	Audio serial sync input/output of playback.
ADATP	74	I	Audio serial data input of playback.
ALINKI	19	I	Audio Multi-chip operation serial input
ALINKO	57	IO	Audio Multi-chip operation serial output/test input

System Control Pins

NAME	NUMBER	TYPE	DESCRIPTION
RSTB	100	I	System reset.
CLKI	37	I	System clock input.27/54/108MHz
CLKPO	34	O	27/54/108MHz clock output.
CLKNO	35	O	27/54/108MHz clock output.
TEST	99	I	Test pin. Connect to ground.
SCLK	2	I	Serial control clock line.
SDAT	3	IO	Serial control data line.
SADD[1:0]	76,77	I	Serial control address.
IRQ	5	O	Interrupt request output.

Power and Ground Pins

NAME	NUMBER	TYPE	DESCRIPTION
VDDI	4,16,26, 36,50,60,72	P	1.8V Power for internal logic.
VDDO	10,22,40, 54,66	P	3.3V Power for output driver.
VSS	1,7,13,25,29,32,44,47,51, 63,69,75	G	Ground for internal logic and output driver.
VDDV	87,92,93,98	P	1.8V Power for analog video.
VSSV	89,90,95,96	G	Ground for analog video.
VDDA	78,86	P	1.8V Power for analog audio.
VSSA	80,81	G	Ground for analog audio.

Functional Description

Video Input Formats

The TW2864 has build-in automatic standard discrimination circuitry. The circuit uses burst-phase, burst-frequency and frame rate to identify NTSC, PAL or SECAM color signals. The standards that can be identified are NTSC (M), NTSC (4.43), PAL (B, D, G, H, I), PAL (M), PAL (N), PAL (60) and SECAM (M). Each standard can be included or excluded in the standard recognition process by software control. The exceptions are the base standard NTSC and PAL, which are always enabled. The identified standard is indicated by the Standard Selection (SDT) register. Automatic standard detection can be overridden by software controlled standard selection.

TW2864 supports all common video formats as shown in Table 1.

TABLE 1. VIDEO INPUT FORMATS SUPPORTED BY THE TW2864

FORMAT	LINES	FIELDS	FSC	COUNTRY
NTSC-M	525	60	3.579545 MHz	U.S., many others
NTSC-Japan (Note Note:)	525	60	3.579545 MHz	Japan
PAL-B, G, N	625	50	4.433619 MHz	Many
PAL-D	625	50	4.433619 MHz	China
PAL-H	625	50	4.433619 MHz	Belgium
PAL-I	625	50	4.433619 MHz	Great Britain, others
PAL-M	525	60	3.575612 MHz	Brazil
PAL-CN	625	50	3.582056 MHz	Argentina
SECAM	625	50	4.406MHz 4.250MHz	France, Eastern Europe, Middle East, Russia
PAL-60	525	60	4.433619 MHz	China
NTSC (4.43)	525	60	4.433619 MHz	Transcoding

NOTE:

2. NTSC-Japan has 0 IRE setup.

Analog Front-end

The TW2864 contains four 10-bit ADC (Analog to Digital Converters) to digitize the analog video inputs. The ADC can be put into power-down mode by the V_ADC_PWDN register. The TW2864 also contains an anti-aliasing filter to prevent out-of-band frequency in analog video input signal. So there is no need of external components in analog input pin except ac coupling capacitor and termination resistor. Figure 1 shows the frequency response of the anti-aliasing filter.

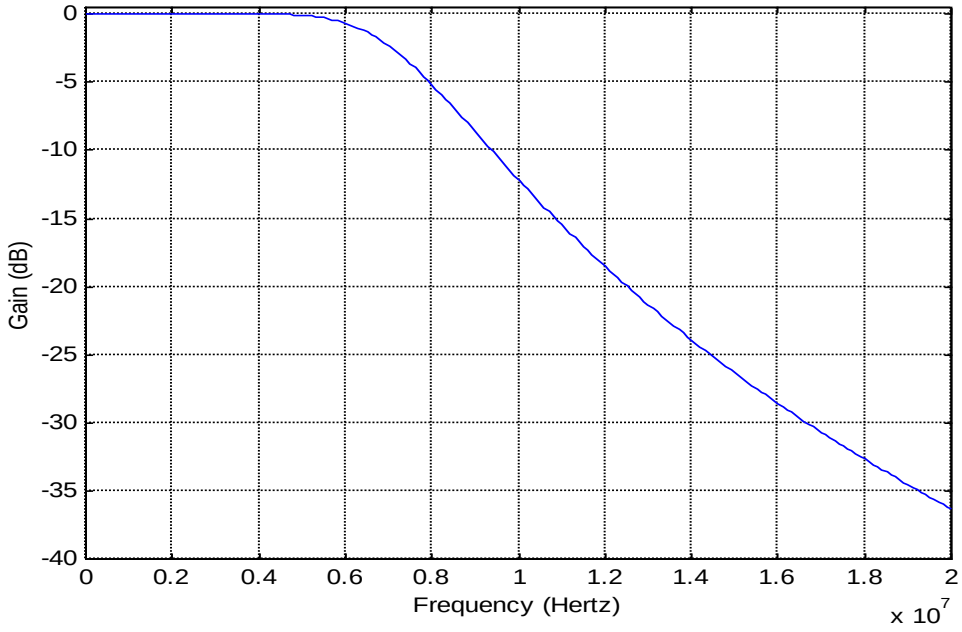


FIGURE 1. THE FREQUENCY RESPONSE OF ANTI-ALIASING FILTER

DECIMATION FILTER

The digitized composite video data are over-sampled to simplify the design of analog filter. The decimation filter is required to achieve optimum performance and prevent high frequency components from being aliased back into the video image when down-sampled. Figure 2 shows the characteristic of the decimation filter.

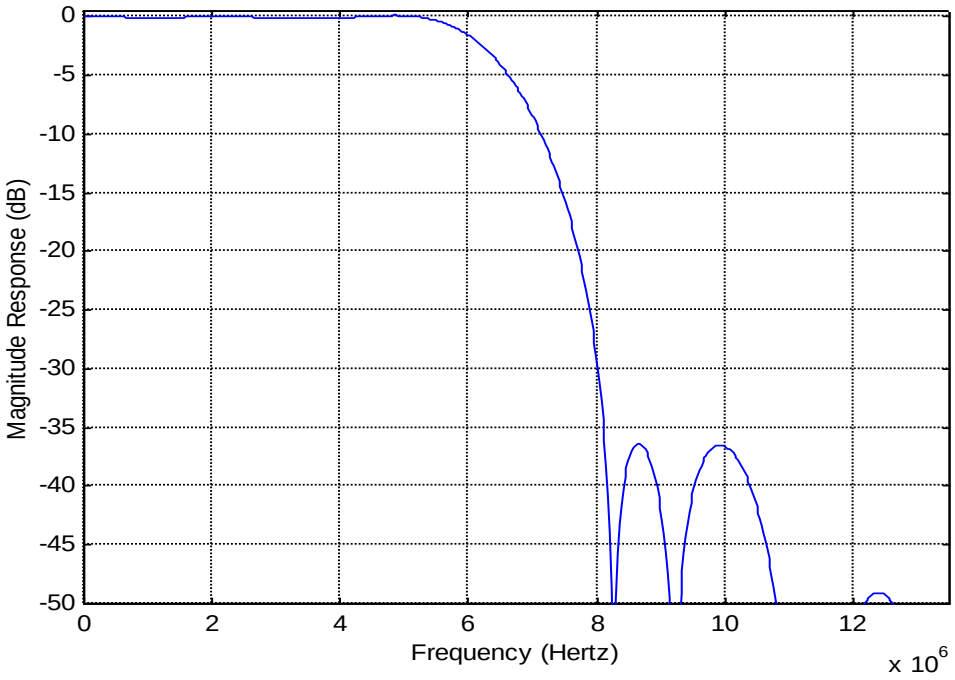


FIGURE 2. THE CHARACTERISTIC OF THE DECIMATION FILTER

Automatic Gain Control and Clamping

All four analog channels have built-in clamping circuit that restores the signal DC level. The Y channel restores the back porch of the digitized video to a level of 60. This operation is automatic through internal feedback loop. The Automatic Gain Control (AGC) of the Y channel adjusts input gain so that the sync tip is at a desired level. Programmable white peak protection logic is included to prevent saturation in the case of abnormal signal proportion between sync and white peak level.

Sync Processing

The sync processor of TW2864 detects horizontal synchronization and vertical synchronization signals in the composite video or in the Y signal of an S-video or component signal. The processor contains a digital phase-locked-loop and decision logic to achieve reliable sync detection in stable signal as well as in unstable signals such as those from VCR fast forward or backward.

The vertical sync separator detects the vertical synchronization pattern in the input video signals. In addition, the actual sync determination is controlled by a detection window to provide more reliable synchronization. An option is available to provide faster responses for certain applications. The field status is determined at vertical synchronization time. The field logic can also be controlled to toggle automatically while tracking the input

Y/C Separation

The color-decoding block contains the luma/chroma separation for the composite video signal and multi-standard color demodulation. For NTSC and PAL standard signals, the luma/chroma separation can be done either by comb filter or notch/band-pass filter combination. For SECAM standard signals, adaptive notch/band-pass filter is used. The default selection for NTSC/PAL is comb filter.

In the case of comb filter, the TW2864 separates luma (Y) and chroma (C) of a NTSC/PAL composite video signal using a proprietary 4H adaptive comb filter. The filter uses a four-line buffer. Adaptive logic combines the upper-comb and the lower-comb results based on the signal changes among the previous, current and next lines. This technique leads to excellent Y/C separation with small cross luma and cross color at both horizontal and vertical edges

Due to the line buffer used in the comb filter, there is always two lines processing delay at the output except for the component input mode which has only one line delay.

If notch/band-pass filter is selected, the characteristics of the filters are shown in the filter curve section.

Figure 3 shows the frequency response of notch filter for each system NTSC and PAL. Figure 4 shows the frequency response of Chroma Band Pass Filter Curves.

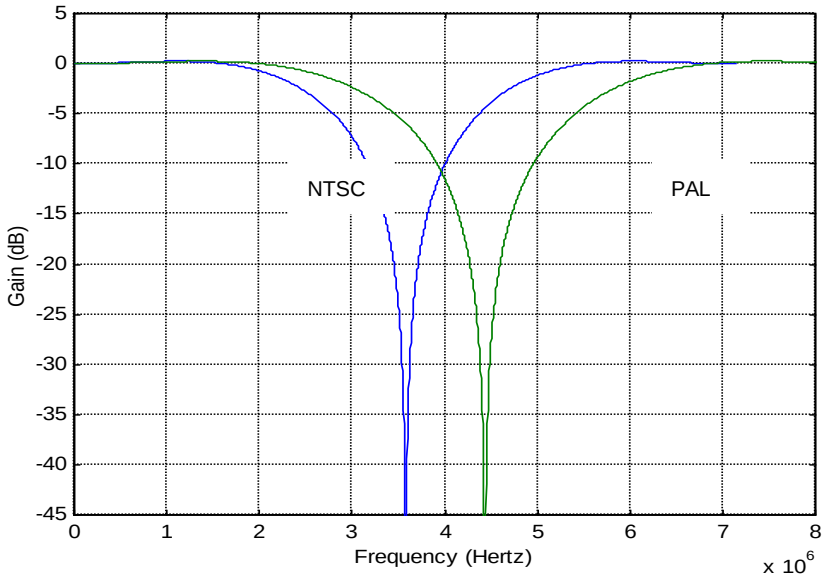


FIGURE 3. THE CHARACTERISTICS OF LUMINANCE NOTCH FILTER FOR PAL

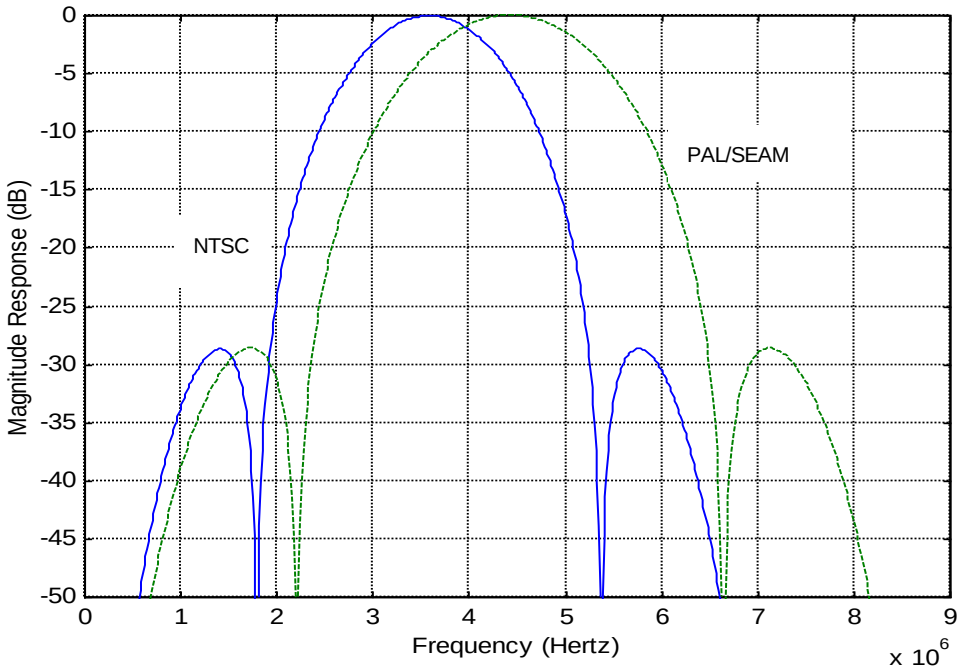


FIGURE 4. CHROMA BAND PASS FILTER CURVES

Color Decoding

CHROMINANCE DEMODULATION

The color demodulation for NTSC and PAL standard is done by first quadrature mixing the chroma signal to the base band. A low-pass filter is then used to remove carrier signal and yield chroma components. The low-pass filter characteristic can be selected for optimized transient color performance. For the PAL system, the PAL ID or the burst phase switching is identified to aid the PAL color demodulation.

For SECAM, the color information is FM modulated onto different carrier. The demodulation process therefore consists of FM demodulator and de-emphasis filter. During the FM demodulation, the chroma carrier frequency is identified and used to control the SECAM color demodulation.

The sub-carrier signal for use in the color demodulator is generated by direct digital synthesis PLL that locks onto the input sub-carrier reference (color burst). This arrangement allows any sub-standard of NTSC and PAL to be demodulated easily with single crystal frequency.

Figure 5 shows the frequency response of Chrominance Low-Pass Filter Curves.

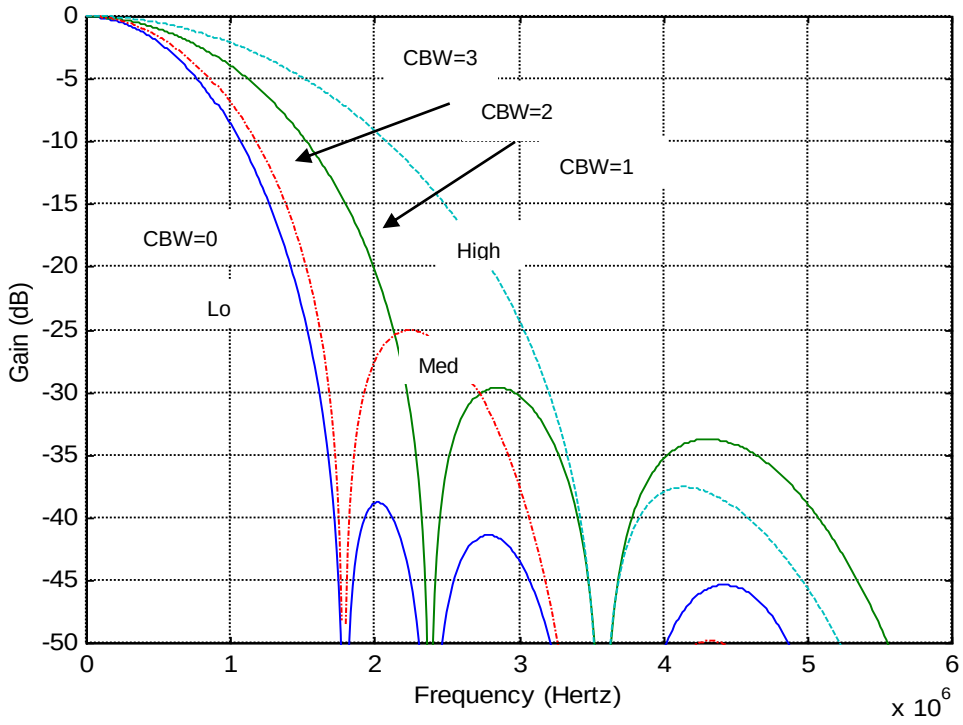


FIGURE 5. CHROMINANCE LOW-PASS FILTER CURVES

ACC (AUTOMATIC COLOR GAIN CONTROL)

The Automatic Chroma Gain Control (ACC) compensates for reduced amplitudes caused by high-frequency loss in video signal. In the NTSC/PAL standard, the color reference signal is the burst on the back porch. It is measured to control the chroma output gain. The range of ACC control is –6db to +24db.

Chrominance Processing

CHROMINANCE GAIN, OFFSET AND HUE ADJUSTMENT

When decoding NTSC signals, TW2864 can adjust the hue of the chroma signal. The hue is defined as a phase shift of the subcarrier with respect to the burst. This phase shift of NTSC decoding can be programmed through a control register. For the PAL standard, the PAL delay line is provided to compensate any hue error; therefore, there is no hue adjustment available. The color saturation can be adjusted by changing the gain of Cb and Cr signals for all NTSC, PAL and SECAM formats. The Cb and Cr gain can be adjusted independently for flexibility.

CTI (COLOR TRANSIENT IMPROVEMENT)

The TW2864 provides the Color Transient Improvement function to further enhance the image quality. The CTI enhance the color edge transient without any overshoot or under-shoot.

Luminance Processing

The TW2864 adjusts brightness by adding a programmable value (in register BRIGHTNESS) to the Y signal. It adjusts the picture contrast by changing the gain (in register CONTRAST) of the Y signal.

The TW2864 also provide programmable peaking function to further enhance the video sharpness. The peaking control has built-in coring function to prevent enhancement of noise.

Figure 6 shows the characteristics of the peaking filter for four different gain modes and different center frequencies.

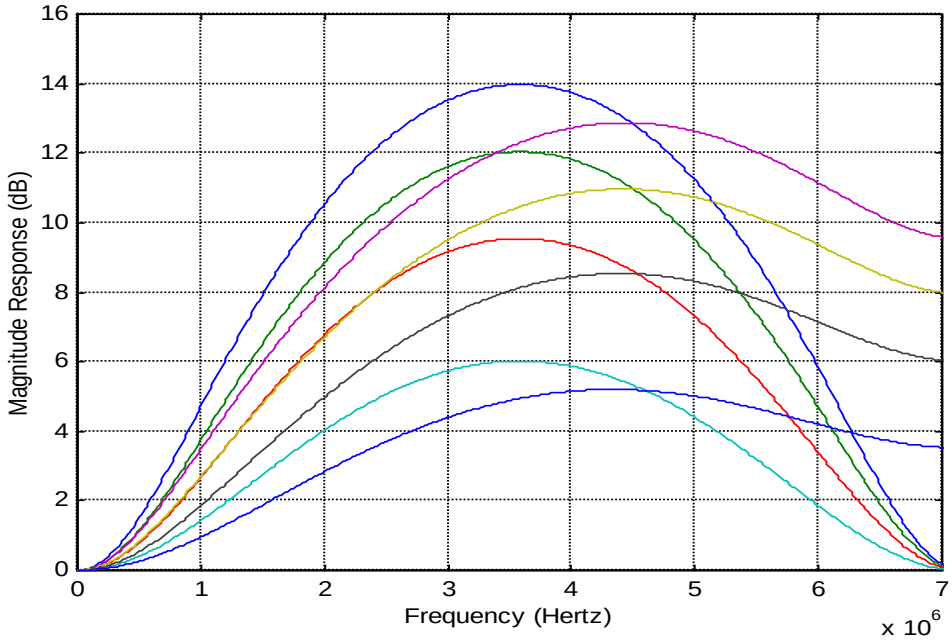


FIGURE 6. THE CHARACTERISTIC OF LUMINANCE PEAKING FILTER

Video Cropping

Cropping allows only subsection of a video image to be output. The active video region is determined by HDELAY, HACTIVE, VDELAY and VACTIVE register as illustrated in Fig7.The VACTIVE signal can be programmed to indicate the number of active lines to be displayed in a video field, and the HACTIVE signal can be programmed to indicate the number of active pixels to be displayed in a video line. The start of the field or frame in the vertical direction is indicated by the leading edge of VSYNC. The start of the line in the horizontal direction is indicated by the leading edge of the HSYNC. The start of the active lines from vertical sync edge is indicated by the VDELAY register. The start of the active pixels from the horizontal edge is indicated by the HDELAY register. The sizes and location of the active video are determined by HDELAY, HACTIVE, VDELAY, and VACTIVE registers. These registers are 8-bit wide, the lower 8-bits is, respectively, in HDELAY_LO, HACTIVE_LO, VDELAY_LO, and VACTIVE_LO. Their upper 2-bit shares the same register CROP_HI.

The Horizontal delay register (HDELAY) determines the number of pixels delay between the leading edge of HSYNC and the leading edge of the HACTIVE. Note that this value is referenced to the un-scaled pixel number. The Horizontal active register (HACTIVE) determines the number of active pixels to be output or scaled after the delay from the sync edge is met. This value is also referenced to the un-scaled pixel number. Therefore, if the scaling ratio is changed, the active video region used for scaling remain unchanged as set by the HACTIVE register, but the valid pixels output are equal or reduced due to down scaling. In order for the cropping to work properly, the following equation should be satisfied.

HDELAY + HACTIVE < Total number of pixels per line.

For NTSC output at 13.5 MHz pixel rate, the total number of pixels is 858.For PAL output at 13.5 MHz rate, the total number of pixels is 864. HACTIVE should be set to 720.

The Vertical delay register (VDELAY) determines the number of lines delay between the leading edge of the VSYNC and the start of the active video lines. It indicates number of lines to skip at the start of a frame before asserting the VACTIVE signal. This value is referenced to the incoming scan lines before the vertical scaling. The number of scan lines is 525 for the 60Hz systems and 625 for the 50Hz systems. The Vertical active register (VACTIVE) determines the number of lines to be used in the vertical scaling. Therefore, the number of scan lines output is equal or less than the value set in this register depending on the vertical scaling ratio. In order for the vertical cropping to work properly, the following equation should be observed.

VDELAY + VACTIVE < Total number of lines per field

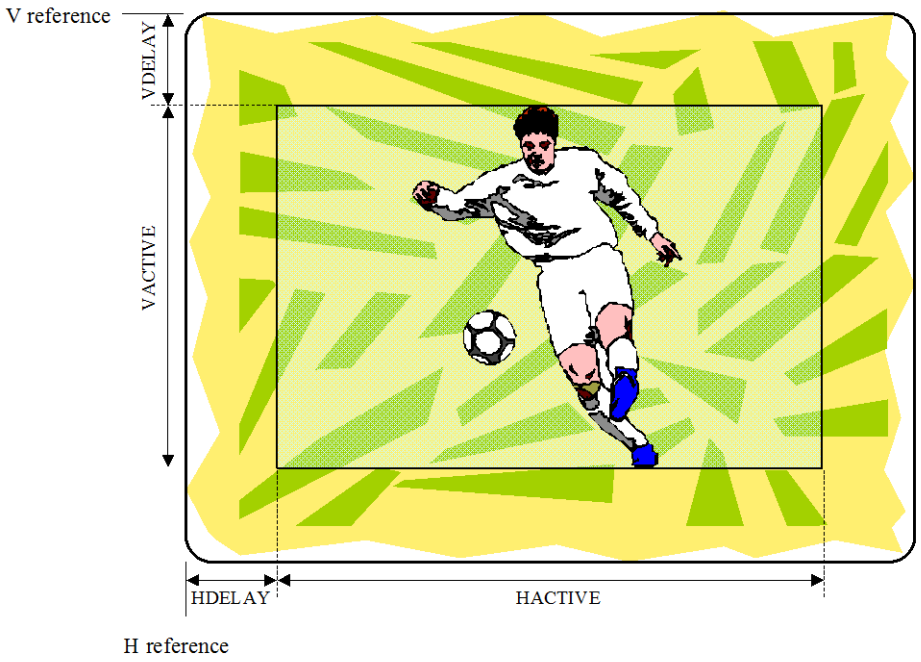


FIGURE 7. THE EFFECT OF CROPPING REGISTERS

Video Scaler

The TW2864 can independently reduce the output video image size in both horizontal and vertical directions using arbitrary scaling ratios up to 1/16 in each direction. The horizontal scaling employs a dynamic 6-tap 32-phase interpolation filter for luma and a 2-tap 8-phase interpolation filter for chroma because of the limited bandwidth of the chroma data. The vertical scaling uses simple line dropping algorithm. Therefore, the use of non-integer vertical scaling ration is not recommended.

Downscaling is achieved by programming the horizontal scaling ratio register (HSCALE) and vertical scaling ratio register (VSCALE). When outputting unscaled video, the TW2864 will output CCIR601 compatible 720 pixels per line or any number of pixels per line as specified by the HACTIVE register. The standard output for Square Pixel mode is 640 pixels for 60 Hz system and 768 pixels for 50 Hz systems. If the number of output pixels required is smaller than 720 in CCIR601 compatible mode or the number specified by the HACTIVE register, the 12-bit HSCALE register, which is the concatenation of two 8-bit registers SCALE_HI and HSCALE_LO, is used to reduce the output pixels to the desired number.

Following is an example using pixel ratio to determine the horizontal scaling ratio. These equations should be used to determine the scaling ratio to be written into the 12-bit HSCALE register assuming HACTIVE is programmed with 720 active pixels per line:

NTSC: $HSCALE = [720/N_{pixel_desired}] * 256$

PAL: $HSCALE = [(720/N_{pixel_desired})] * 256$

Where: $N_{pixel_desired}$ is the nominal number of pixel per line.

For example, to output a CCIR601 compatible NTSC stream at SIF resolution, the HSCALE value can be found as:

$HSCALE = [(720/320)] * 256 = 576 = 0x0240$

However, to output a SQ compatible NTSC stream at SIF resolution, the HSCALE value should be found as:

$HSCALE = [(640/320)] * 256 = 512 = 0x200$

In this case, with total resolution of 768 per line, the HACTIVE should have a value of 640.

The vertical scaling determines the number of vertical lines output by the TW2864. The vertical scaling register (VSCALE) is a 12-bit register, which is the concatenation of a 4-bit register SCALE_HI and an 8-bit register VSCALE_LO. The maximum scaling ratio is 16:1. Following equations should be used to determine the scaling ratio to be written into the 12-bit VSCALE register assuming VACTIVE is programmed with 240 or 288 active lines per field.

60Hz system: $VSCALE = [240/ N_{line_desired}] * 256$

50Hz system: $VSCALE = [288/ N_{line_desired}] * 256$

Where: $N_{line_desired\ is}$ the number of active lines output per field.

The scaling ratios for some popular formats are listed in

Table 2. **Error! Reference source not found.** shows Horizontal Scaler Pre-Filter Curves.

SCALING RATIO			FORMAT	TOTAL RESOLUTION	OUTPUT RESOLUTION	HSCALE VALUES	VSCALE (FRAME)
1:1			NTSC SQ	780x525	640x480	0x0100	0x0100
			NTSC CCIR601	858x525	720x480	0x0100	0x0100
			PAL SQ	944x625	768x576	0x0100	0x0100
			PAL CCIR601	864x625	720x576	0x0100	0x0100
2:1 (CIF)			NTSC SQ	390x262	320x240	0x0200	0x0200
			NTSC CCIR601	429x262	360x240	0x0200	0x0200
			PAL SQ	472x312	384x288	0x0200	0x0200
			PAL CCIR601	432x312	360x288	0x0200	0x0200
4:1 (QCIF)	NTSC SQ	195x131	160x120	0x0400	0x0400		
	NTSC CCIR601	214x131	180x120	0x0400	0x0400		
	PAL SQ	236x156	192x144	0x0400	0x0400		
	PAL CCIR601	216x156	180x144	0x0400	0x0400		

TABLE 2. HSCALE AND VSCALE VALUE FOR SOME POPULAR VIDEO FORMATS

SCALING RATIO			FORMAT	TOTAL RESOLUTION	OUTPUT RESOLUTION	HSCALE VALUES	VSCALE (FRAME)
1:1			NTSC SQ	780x525	640x480	0x0100	0x0100
			NTSC CCIR601	858x525	720x480	0x0100	0x0100
			PAL SQ	944x625	768x576	0x0100	0x0100
			PAL CCIR601	864x625	720x576	0x0100	0x0100
2:1 (CIF)			NTSC SQ	390x262	320x240	0x0200	0x0200
			NTSC CCIR601	429x262	360x240	0x0200	0x0200
			PAL SQ	472x312	384x288	0x0200	0x0200
			PAL CCIR601	432x312	360x288	0x0200	0x0200
4:1 (QCIF)	NTSC SQ	195x131	160x120	0x0400	0x0400		
	NTSC CCIR601	214x131	180x120	0x0400	0x0400		
	PAL SQ	236x156	192x144	0x0400	0x0400		
	PAL CCIR601	216x156	180x144	0x0400	0x0400		

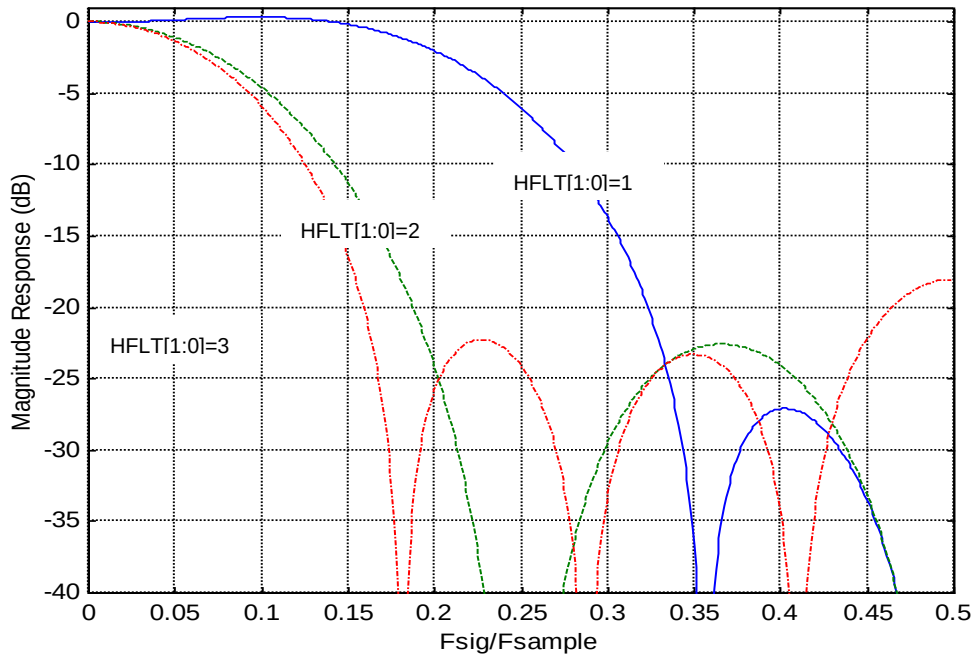


FIGURE 8. HORIZONTAL SCALER PRE-FILTER CURVES

Output Format

The TW2864 supports a standard ITU-R BT.656 format. All video data and timing signal of four channels are synchronous with the pins CLKPO or CLKNO output. Therefore, CLKPO or CLKNO can be connected to four channel interfaces for synchronizing data. And, the phase of CLKPO or CLKNO can be controlled by delay unit via the CLKP_DEL or CLKN_DEL registers and polarity inverse cell via the CLKP_POL or CLKN_POL registers independently.

ITU-R BT.656 FORMAT

In ITU-R BT.656 format, SAV and EAV sequences are inserted into the data stream to indicate the active video time. It is noted that the number of active pixels per line is constant in this mode regardless of the actual incoming line length. The output timing is illustrated in Figure 9. The SAV and EAV sequences are shown in Table 3.. An optional set of 656 SAV/EAV code sequence can be enabled to identify no-video status using the NOVID_656 bit.

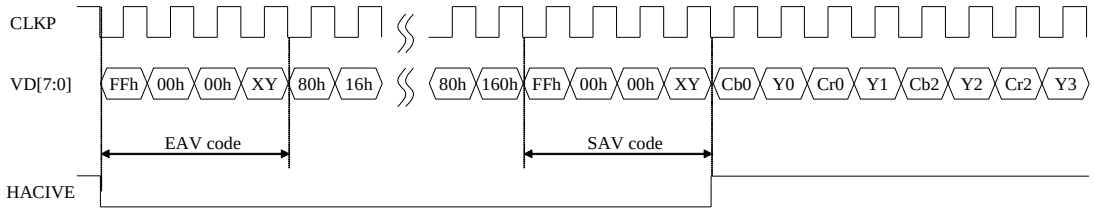


FIGURE 9. TIMING DIAGRAM OF ITU-R BT.656 FORMAT

TABLE 3. ITU-R BT.656 SAV AND EAV CODE SEQUENCE

CONDITION			656 FVH VALUE			SAV/EAV CODE SEQUENCE				
FIELD	V TIME	H TIME	FIELD	V TIME	H TIME	FIRST	SECOND	THIRD	FOURTH	
									NOMINAL	OPTION*
EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF1	0x71
EVEN	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xEC	0x6C
EVEN	Active	EAV	1	0	1	0xFF	0x00	0x00	0xDA	0x5A
EVEN	Active	SAV	1	0	0	0xFF	0x00	0x00	0xC7	0x47
ODD	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB6	0x36
ODD	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xAB	0x2B
ODD	Active	EAV	0	0	1	0xFF	0x00	0x00	0x9D	0x1D
ODD	Active	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x00

*Option includes video loss information in ITU-R BT.656

TWO CHANNEL ITU-R BT.656 TIME-MULTIPLEXED FORMAT WITH 54MHz

The TW2864 supports two channels ITU-R BT.656 time-multiplexed format with 54MHz that is useful to security application requiring two channel outputs through one channel video port. The DUAL_CH register enables the dual ITU-R BT.656 time-multiplexed format and the SEL_CH register selects another channel output to be multiplexed with its own channel on each VD pins. To de-multiplex the time-multiplexed data in the back end chip, the channel ID can be inserted in the data stream using the CHID register. Two kinds of channel ID format can be supported. One is horizontal blanking code with channel ID and the other is ITU-R BT.656 sync code with channel ID. Figure 10 illustrates the timing diagram in the case of CH1 and CH2 time-multiplexed output through CH1 video output port.

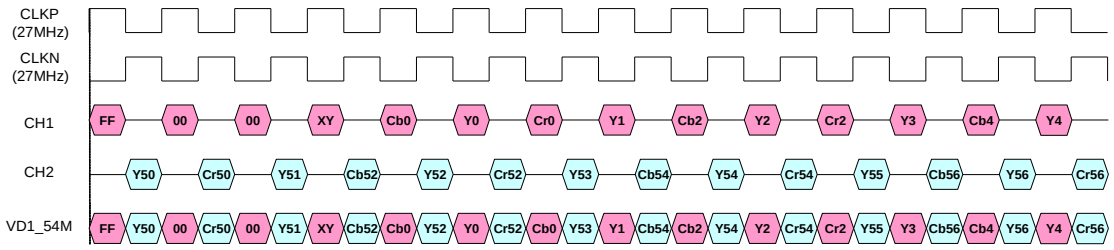


FIGURE 10. TIMING DIAGRAM OF TWO CHANNEL TIME-MULTIPLEXED FORMAT WITH 54MHZ

FOUR CHANNEL CIF TIME-MULTIPLEXED FORMAT WITH 54MHZ

Four channel CIF (360x480) time-multiplexed format is also provided for specific security application using the CIF_54M register. For this format, each channel ITU-R BT.656 data stream is down-sampled into 13.5MHz ITU-R BT.656 data stream except the sync code. Optionally, the vertical scaling can also be enabled to support Quad (360x240) format using the VSCALE(REV_ID=0 TW2864)/VSCL_ENA(REV_ID>=1 TW2864) register. Then, these four 13.5MHz ITU-R BT.656 data stream are time-multiplexed into 54MHz data stream. This format requires only one channel video port to transfer whole four channel CIF data independently.When CIF_54M register is set to 1,TW2864(REV_ID=0) output this four channel CIF (360x480) time-multiplexed format on all video ports.TW2864(REV_ID>=1) can support one channel video port to transfer whole four channel CIF data independently and the other video port to transfer two channel Full D1 ITU-R BT.656 time-multiplexed format simultaneously.To de-multiplex the time-multiplexed data in the back end chip, the channel ID can be inserted in the data stream using the CHID register. Two kinds of channel ID format can be supported. One is horizontal blanking code with channel ID and the other is ITU-R BT.656 sync code with channel ID. Optionally, when the vertical scaling is enabled, the ITU-R BT.656 sync code will be skipped in the invalid line through the VSCL_SYNC register. Figure 11 and Table 4 illustrate the timing diagram and detailed channel ID format for four channel CIF time-multiplexed format with 54MHz.

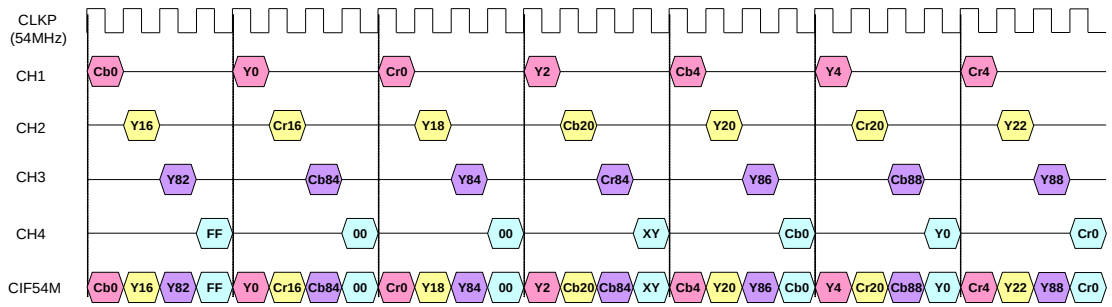


FIGURE 11. TIMING DIAGRAM OF 4 CH CIF TIME-MULTIPLEXED FORMAT WITH 54MHZ

TABLE 4. THE CHANNEL ID FORMAT FOR 4 CH CIF TIME-MULTIPLEXED FORMAT WITH 54MHZ

CONDITION			656 FVH VALUE			SAV/EAV CODE SEQUENCE						
FIELD	VTIME	HTIME	F	V	H	FIRST	SECOND	THIRD	FOURTH			
									CH1	CH2	CH3	CH4
EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF0	0xF1	0xF2	0xF3
EVEN	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xE0	0xE1	0xE2	0xE3
EVEN	Active	EAV	1	0	1	0xFF	0x00	0x00	0xD0	0xD1	0xD2	0xD3
EVEN	Active	SAV	1	0	0	0xFF	0x00	0x00	0xC0	0xC1	0xC2	0xC3
ODD	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB0	0xB1	0xB2	0xB3
ODD	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xA0	0xA1	0xA2	0xA3
ODD	Active	EAV	0	0	1	0xFF	0x00	0x00	0x90	0x91	0x92	0x93
ODD	Active	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x81	0x82	0x83

(a) ITU-R BT.656 Sync Code with Channel ID

CHANNEL	H BLANKING CODE WITH CHANNEL ID		
	Y	CB	CR
Ch1	8'h10	8'h80	8'h80
Ch2	8'h11	8'h81	8'h81
Ch3	8'h12	8'h82	8'h82
Ch4	8'h13	8'h83	8'h83

(b) Horizontal Blanking Code with Channel ID

FOUR CHANNEL D1 TIME-DIVISION-MULTIPLEXED FORMAT WITH 108MHZ

Four channel of D1 (720x480) at 27MHz video stream that are time-division-multiplexed at 108MHz data rate format is implemented in TW2864 for security surveillance application. In order to reduce pin counts (thus shrink chip size) on both decoder's digital output port and the input port of the back end compression Codec devices, TW2864 implements single 8 bit bus at 4 times the base band pixel clock rate of 27MHz. While quadrupling the data rate on a single bus to meet the new requirement, individually, each channel data arrangement still retains the base band 27MHz ITU-R BT.656 specification. For interface that can accept the new 108MHz clock bus, only one single clock at 108MHz is required. Embedded timing (SAV-EAV) code and Channel ID are inserted into each channel for de-multiplexing and separation of channel data.

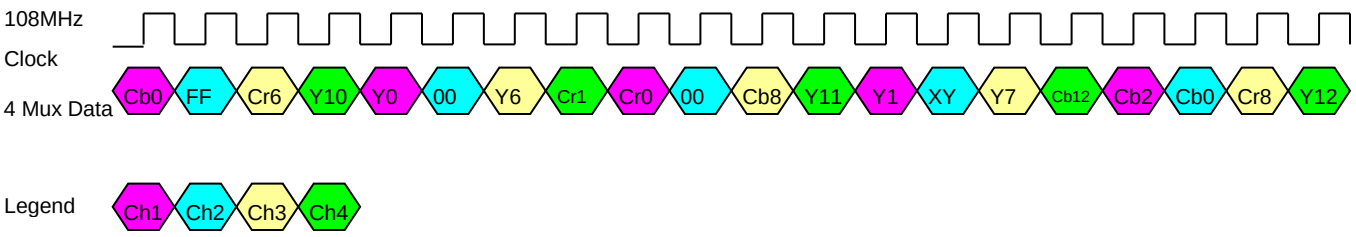


FIGURE 12. TIMING DIAGRAM OF 108MHZ 4 CH D1 TIME-DIVISION-MULTIPLEXED VIDEO DATA

Figure 12 depicts the temporal arrangement of the video data in 108MHz data rate. Each channel is byte level time-division multiplexed (TDM). Main clock is 108MHz clock.

TABLE 5. SPECIAL FORMAT OF ITU-R BT. 656 EMBEDDED TIMING CODE AND CHANNEL ID CODE

CONDITION			656 FVH VALUE			SAV-EAV CODE						
									FOURTH			
FIELD	V-TIME	H-TIME	F	V	H	FIRST	SECOND	THIRD	CH1	CH2	CH3	CH4
EVEN	BLANK	EAV	1	1	1	0xFF	0x00	0x00	0xF0	0xF1	0xF2	0xF3
EVEN	BLANK	SAV	1	1	0	0xFF	0x00	0x00	0xE0	0xE1	0xE2	0xE3
EVEN	ACTIVE	EAV	1	0	1	0xFF	0x00	0x00	0xD0	0xD1	0xD2	0xD3
EVEN	ACTIVE	SAV	1	0	0	0xFF	0x00	0x00	0xC0	0xC1	0xC2	0xC3
ODD	BLANK	EAV	0	1	1	0xFF	0x00	0x00	0xB0	0xB1	0xB2	0xB3
ODD	BLANK	SAV	0	1	0	0xFF	0x00	0x00	0xA0	0xA1	0xA2	0xA3
ODD	ACTIVE	EAV	0	0	1	0xFF	0x00	0x00	0x90	0x91	0x92	0x93
ODD	ACTIVE	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x81	0x82	0x83

OUTPUT ENABLING ACT

After power-up, the TW2864 registers have unknown values. The RSTB pin must be asserted and released to bring all registers to its default values. After reset, the TW2864 data outputs are tri-stated. The OE register should be written after reset to enable outputs desired.

VIDEO OUTPUT CHANNEL SELECTION

If CHMDn[1:0] in Reg0xCA is set to 0hex,MAINCHn[1:0] in Reg0xCD selects one number of Video Channels to be output on VDn[7:0] pin as Single Channel ITU-R BT.656(D1) Format output.If CHMDn[1:0] in Reg0xCA is set to 1hex,MAINCHn[1:0] in Reg0xCD and SELCHn[1:0] in Reg0xCC select two numbers of Video Channels to be output on VDn[7:0] pin as Two Channel ITU-R BT.656(D1) Time-multiplexed Format output.If CHMDn[1:0] in Reg0xCA is set to 2hex, Four Channel ITU-R BT.656(D1) Time-multiplexed Format is output on VDn[7:0] pin.

EXTRA SYNC OUTPUT

The additional timing information such as syncs and field flag are also supported through the MPP pins. The video output timing is illustrated in Fig13 and Fig14 TW2864 HS/VS/FLD output function is compatible to TW9907 Video decoder HSYNC/VSYNC/FIELD output function. Start of VS timing is controlled by VSHT register(V timing) and OVSDLY register(H timing).End of VS timing is controlled by OVSEND register(V Timing).Start of FLD timing is controlled by OFDLY register(V timing).Start of HS timing is controlled by HSBEGIN register and End of HS timing is controlled by HSEND register.

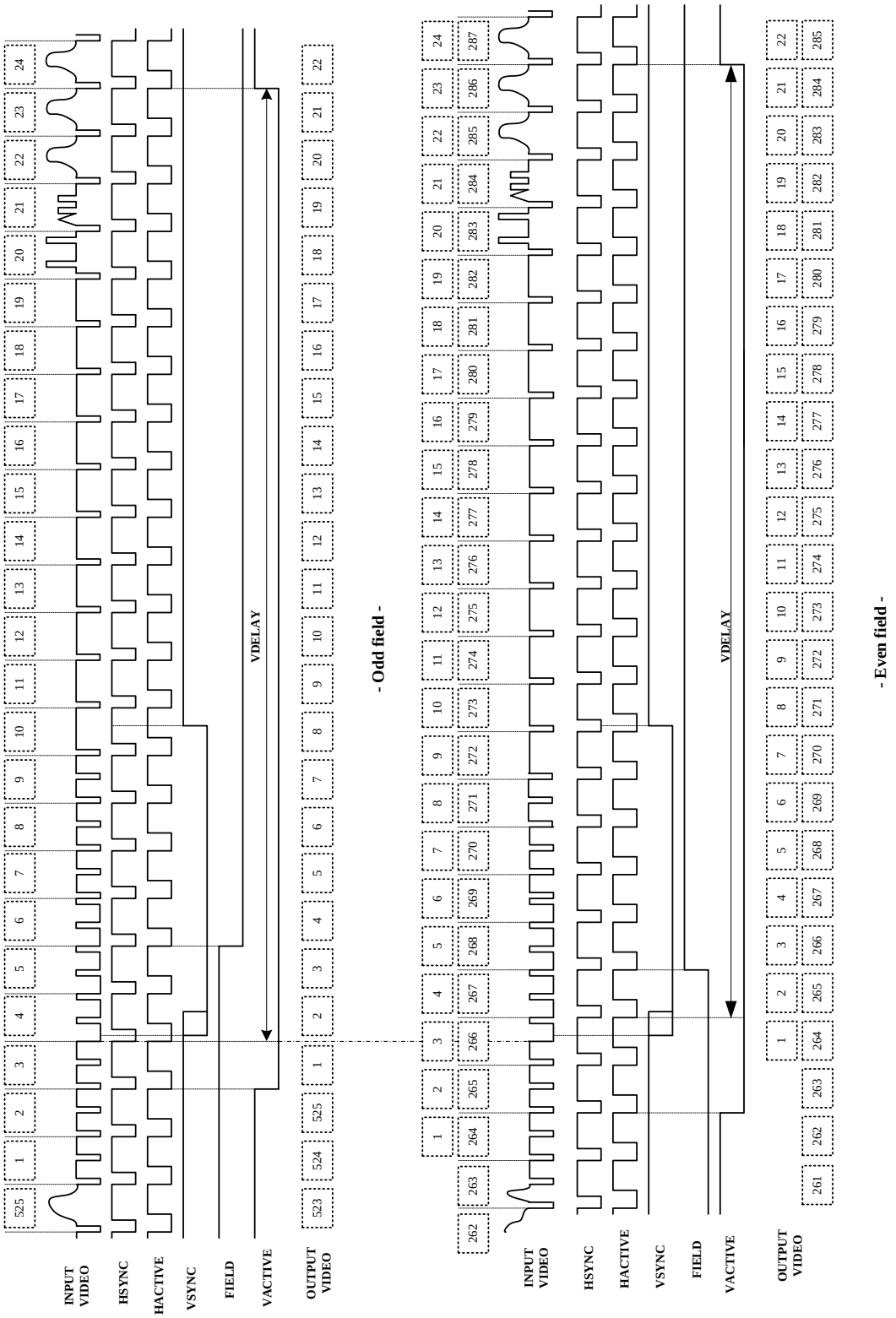


FIGURE 13. VERTICAL TIMING DIAGRAM FOR 60Hz/525 LINE SYSTEM

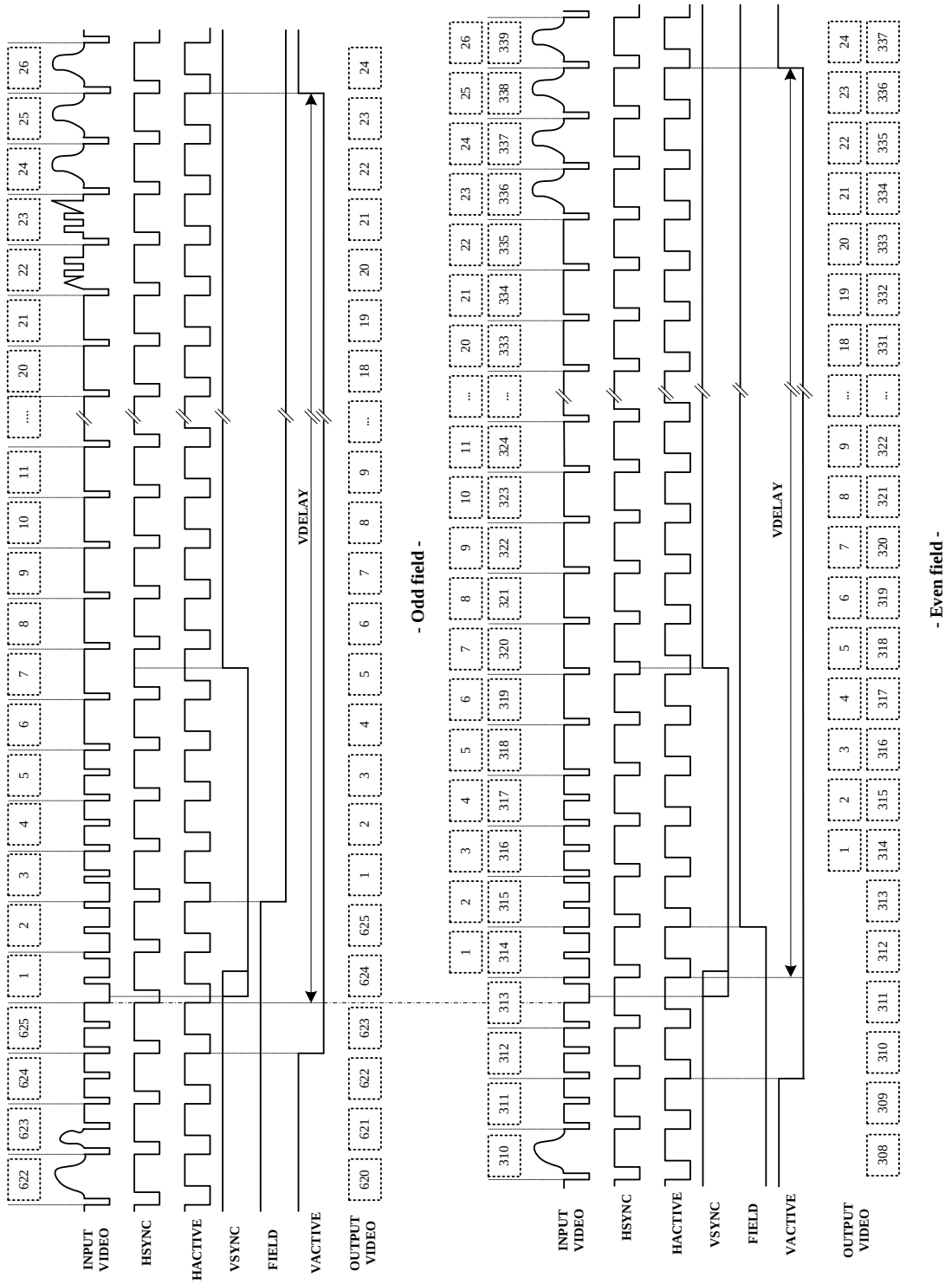


FIGURE 14. VERTICAL TIMING DIAGRAM FOR 50HZ/625 LINE SYSTEM

AUDIO CODEC

The audio codec in the TW2864 is composed of 4 audio Analog-to-Digital converters, 1 Digital-to-Analog converter, audio mixer, digital serial audio interface and audio detector, as shown in Figure 15. The TW2864 can accept 4 analog audio signals and 1 digital serial audio data and produce 1 mixing analog audio signal and 2 digital serial audio data.

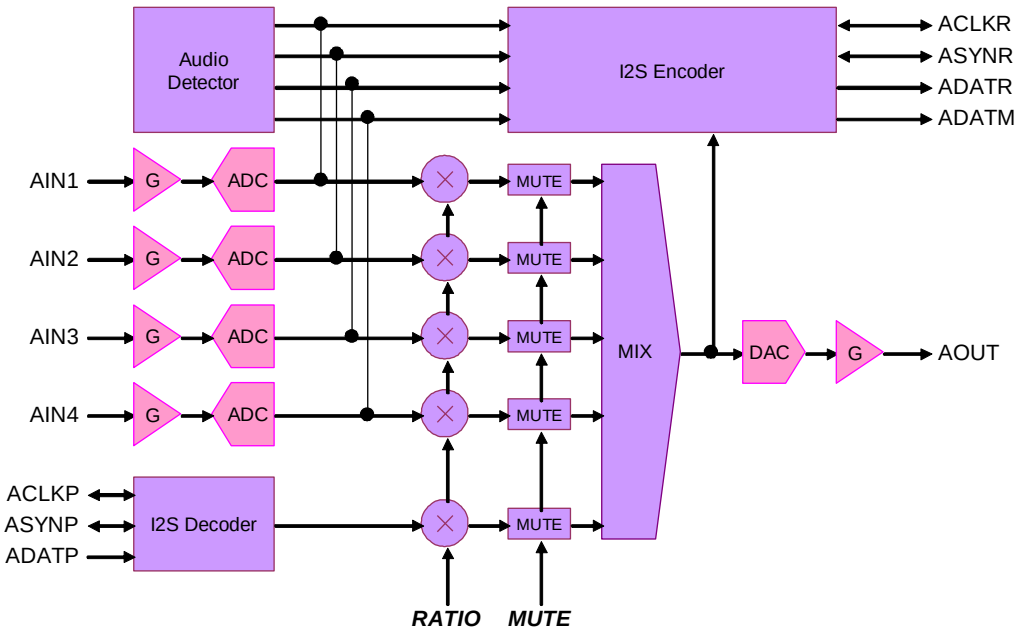


FIGURE 15. BLOCK DIAGRAM OF AUDIO CODEC

The level of analog audio input signal AIN0 ~ AIN4 can be adjusted respectively by internal programmable gain amplifiers that are defined via the AIGAIN1, AIGAIN2, AIGAIN3 and AIGAIN4 registers and then sampled by each Analog-to-Digital converters. The digital serial audio input data through the ACLKP, ASYNP and ADATP pin are used for playback function. To record audio data, the TW2864 provides the digital serial audio output via the ACLKR, ASYNR and ADATR pin.

The TW2864 can mix all of audio inputs including analog audio signal and digital audio data according to the predefined mixing ratio for each audio via the MIX_RATIO1 ~ MIX_RATIO4 and MIX_RATIOP registers. This mixing audio output can be provided through the analog and digital interfaces. The embedded audio Digital-to-Analog converter supports the analog mixing audio output whose level can be controlled by programmable gain amplifier via the AOGAIN register. The ADATM pin supports the digital mixing audio output and its digital serial audio timings are provided through the ACLKR and ASYNR pins that are shared with the digital serial audio record timing pins.

AUDIO CLOCK MASTER/SLAVE MODE

The TW2864 has two types of Audio Clock modes. If ACLKRMASTER register is set to 1,fs audio sample date is processed from 256xfs audio clock internal ACKG (Audio Clock Generator) generates. In this master mode, ACLKR/ASYNR pins are output mode. ASYNROEN register for ASYNR pin should be set to 0(output enable mode).If ACLKRMASTER register is set to 0,fs audio sample rate is processed from 256xfs audio clock on ACLKR pin input.256xfs audio clock should be connected to ACLKR pin from external master clock source in this slave mode.

ASYNR pin can be input or output by external Audio clock master in slave mode. ASYNR signal should change per fs audio sample rate in both master and slave mode.

AUDIO DETECTION

The TW2864 has an audio detector for individual 4 channels. There are 2 kinds of audio detection method defined by the ADET_MTH. One is the detection of absolute amplitude and the other is of differential amplitude. For both detection methods, the accumulating period is defined by the ADET_FILT register and the detecting threshold value is defined by the ADET_TH1 ~ ADET_TH4 registers. The status for audio detection is read by the STATE_AVDET register and it also makes the interrupt request through the IRQ pin with the combination of the status for video loss detection.

MULTI-CHIP OPERATION

TW2864 can output 16 channel audio data on ACLKR/ASYNR/ADATR output simultaneously. Therefore, up to 4 chips should be connected on most Multi-Chip application cases. SMD register selects Audio cascade serial interface mode. If SMD register is set to 1, IRQ pin is audio cascade serial output and ADATP pin is audio cascade serial input.This is IRQ cascade mode. If SMD register is set to 2, ALINKI pin is audio cascade serial input and ALINKO pin is audio cascade serial output mode. It's ALINK cascade mode. If SMD register is set to 0, ALINKO pin is input.ALINKO pin default is also input.

Each stage chip can accept 4 analog audio signals so that four cascaded chips through the ADATP and IRQ pin will be 16-channel audio controller. The first stage chip provides 16ch digital serial audio data for record. Even though the first stage chip has only 1 digital serial audio data pin ADATR for record, the TW2864 can generate 16 channel data simultaneously using multi-channel method. Also, each stage chip can support 4 channel record outputs that are corresponding with analog audio inputs. This first stage chip can also output 16 channel mixing audio data by the digital serial audio data and analog audio signal. The last stage chip accepts the digital serial audio data for playback. The digital playback data can be converted to analog signal by Digital-to-Analog Converter in the last stage chip.

In Multi-Chip Audio operation mode,one same Oscillator clock source(108MHz or 54MHz) need to be connected to all CLKI pins.One 27MHz clock source can be connected if needed,too.

Several Master/Slave mode configurations are available.The Fig16-1/Fig16-2/Fig16-3/Fig16-4/Fig16-5/Fig16-6 show all possible systems of 16 channel audio connection using 4 chips with Clock Master mode(ACLKRMASTER=1).Fig16-7 is the most recommended and demanded system with Clock Master mode(ACLKRMASTER=1).Fig16-8 is the most recommended system with Clock Slave Sync Master mode(ACLKRMASTER=0,ASYNROEN=0).Fig16-9 is the most recommended system with Clock Slave Sync Slave mode(ACLKRMASTER=0,ASYNROEN=1) .

If All Clock Sync is required in system,one same RSTB reset# signal needs to be connected to all RSTB pins.If ALINK cascade mode,in this All Clock Sync system,all ACLKR pins and all ACLKP pins should be connected. Also,all ASYNR pins and all ASYNP pins should be connected.If IRQ cascade mode, in this All Clock Sync system,all ACLKR pins and LastStage ACLKP pin should be connected.Also,all ASYNR pins and LastStage ASYNP pin should be connected.

In following each Fig,Mix1-16-Pb1-Pb4 means Mix output of AIN1-16 and Playback1-4.AIN1-16 means one selected Audio output in AIN1-16.Pb1-Pb4 means one selected Audio output in Playback1-4.Mix1-16-Pb4 means Mix output of

AIN1-16 and Playback4.Mix13-16-Pb4 means Mix output of AIN13-16 and Playback4.AIN13-16 means one selected Audio output in AIN13-16.

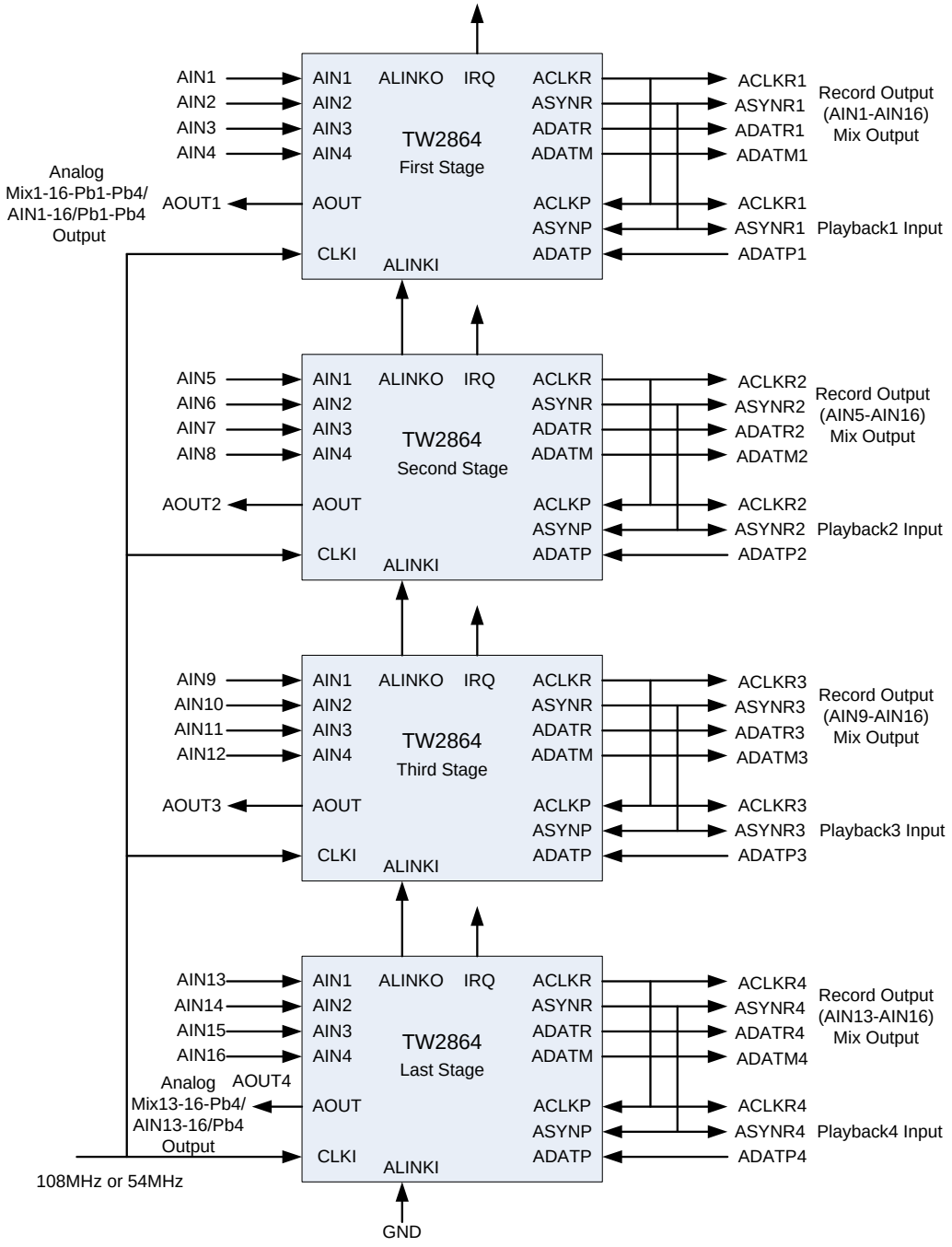


FIGURE 16. CONNECTION FOR MASTER MULTI-CHIP OPERATION ON ALINK CASCADE MODE

All chips have SMD = 2;ACLKRMASTER=1;ASYNROEN=0;PB_MASTER=0

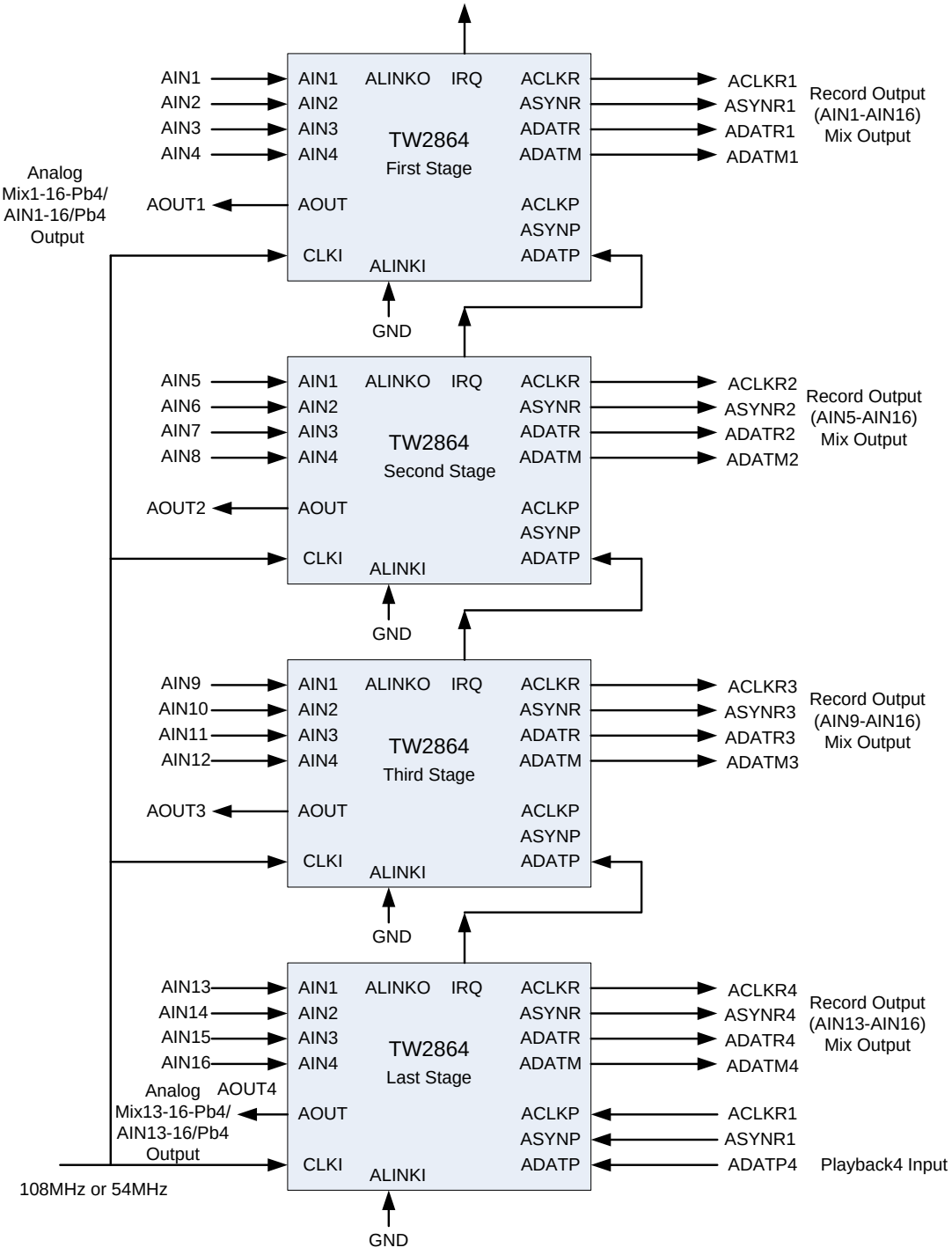


FIGURE 17. CONNECTION FOR MASTER MULTI-CHIP OPERATION ON IRQ CASCADE MODE

All chips have SMD = 1;ACLKRMASTER=1;ASYNROEN=0; Last Stage FIRSTCNUM=0,Other Stage FIRSTCNUM=3;PB_MASTER=0

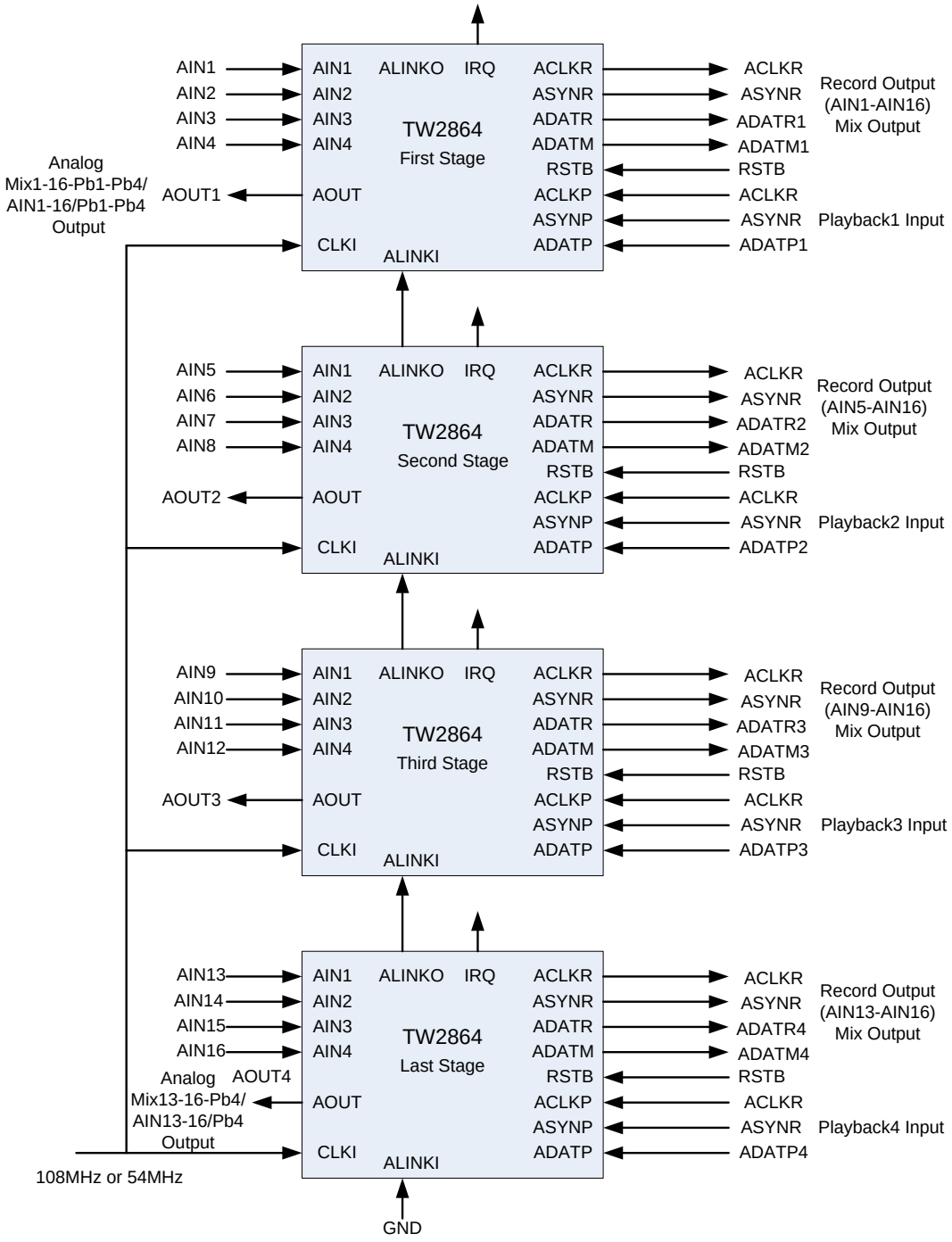


FIGURE 18. CONNECTION FOR MASTER ALL CLOCK SYNC MULTI-CHIP OPERATION ON ALINK CASCADE MODE

All chips have SMD = 2;ACLKRMASTER=1;ASYNROEN=0;PB_MASTER=0

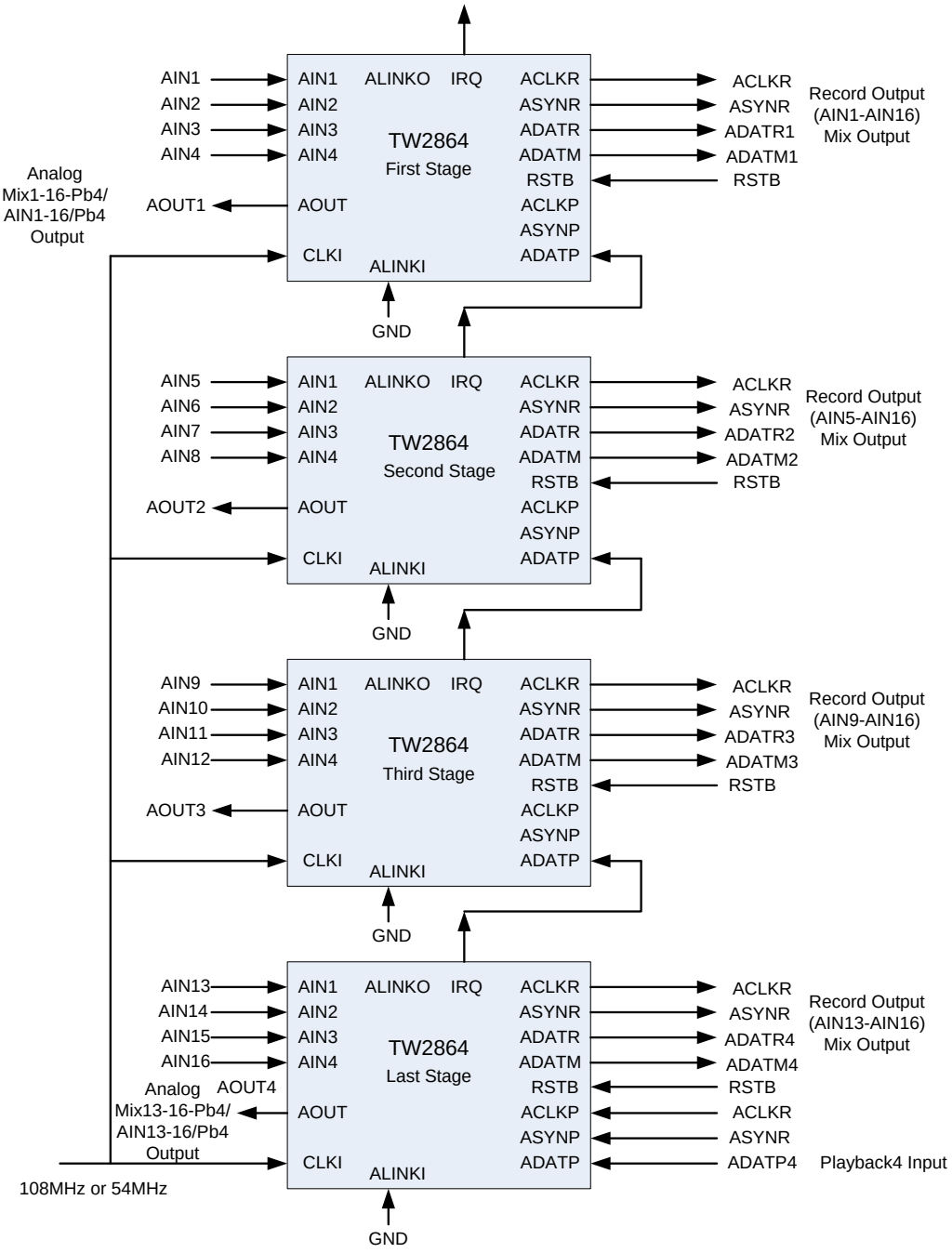


FIGURE 19. CONNECTION FOR MASTER ALL CLOCK SYNC MULTI-CHIP OPERATION ON IRQ CASCADE MODE

All chips have SMD = 1;ACLKRMASTER=1;ASYNROEN=0;

Last Stage FIRSTCNUM=0,Other Stage FIRSTCNUM=3;PB_MASTER=0

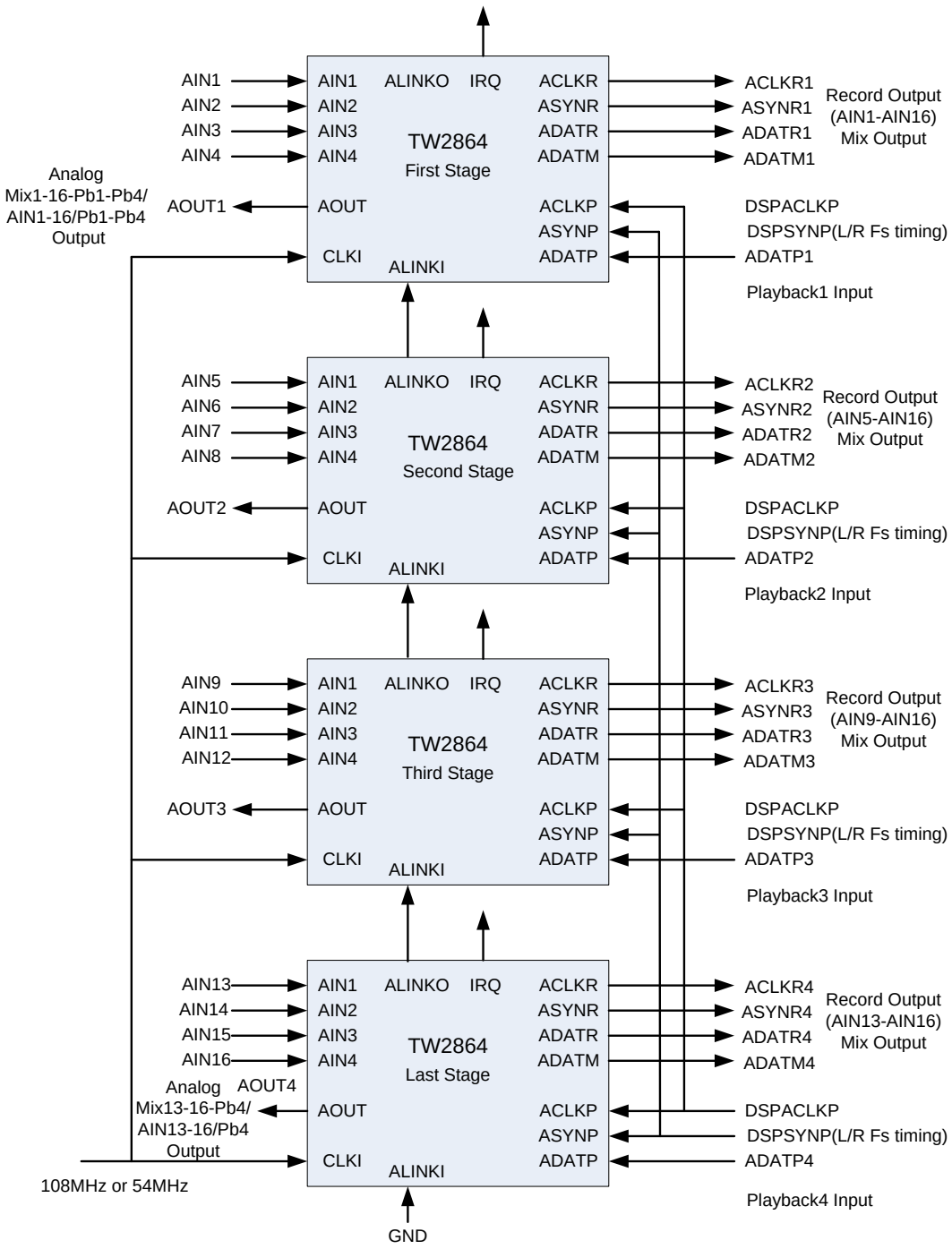


FIGURE 20. CONNECTION FOR PLAYBACK SLAVE LOCK MULTI-CHIP OPERATION ON ALINK CASCADE MODE

(REV_ID>=1 TW2864 only)

All chips have SMD = 2;ACLKRMASTER=1;ASYNROEN=0;PB_MASTER=0

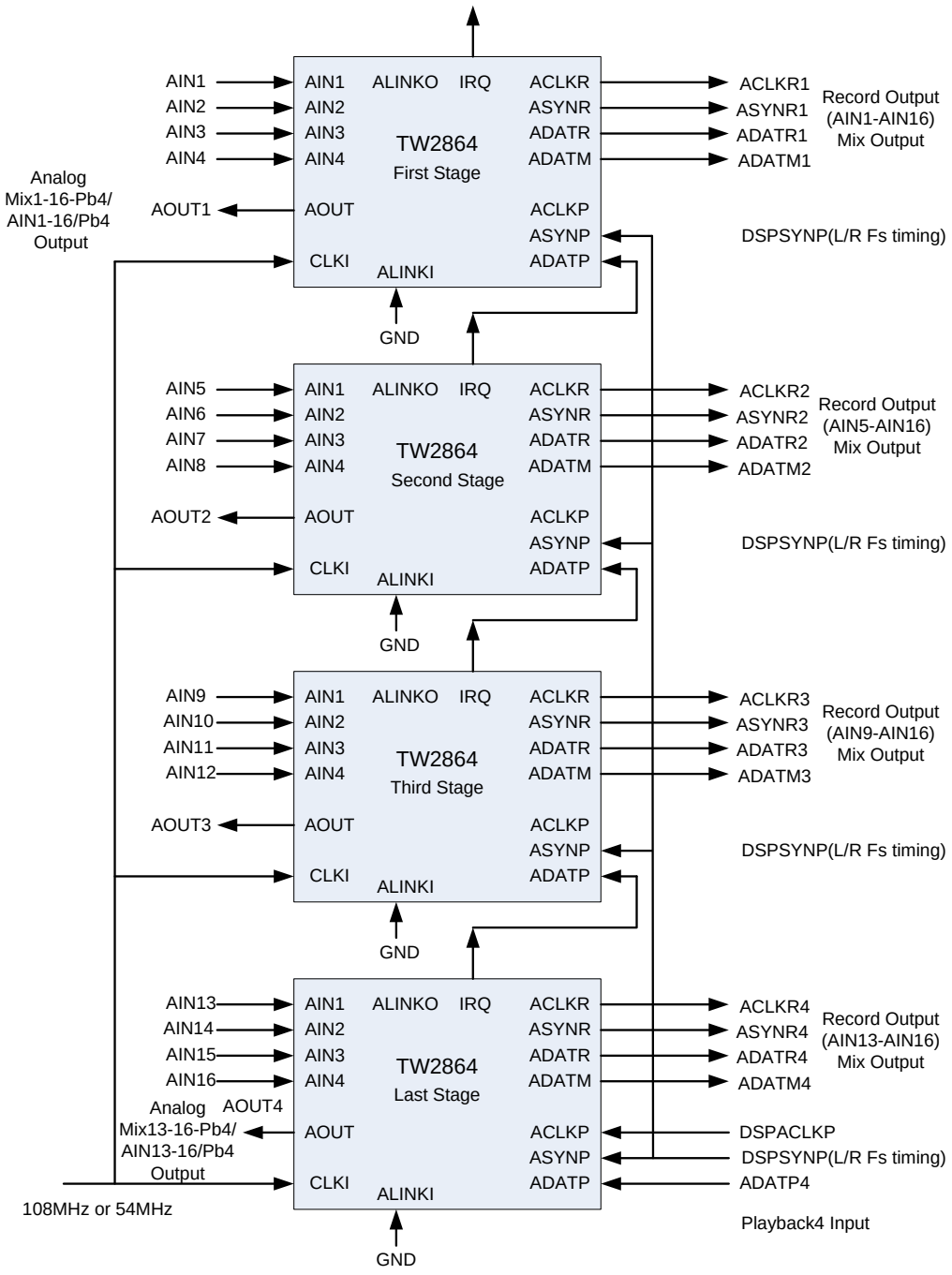


FIGURE 21. CONNECTION FOR PLAYBACK SLAVE LOCK MULTI-CHIP OPERATION ON IRQ CASCADE MODE

(REV_ID>=1 TW2864 only) All chips have SMD = 1;ACLKRMASTER=1;ASYNROEN=0; Last Stage FIRSTCNUM=0,Other Stage FIRSTCNUM=3;PB_MASTER=0

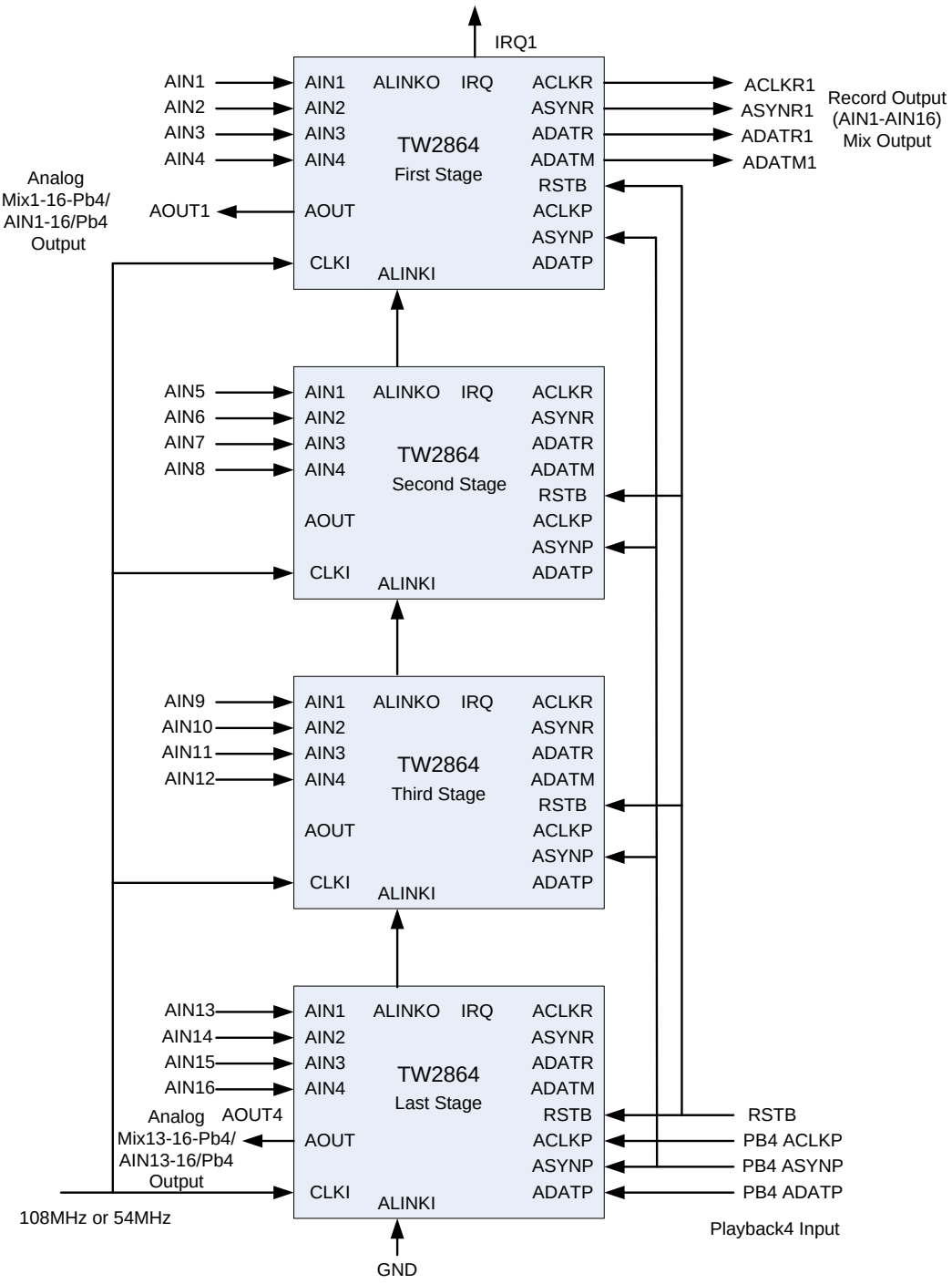


FIGURE 22. RECOMMENDED CLOCK MASTER CASCADE MODE SYSTEM

All chips have SMD = 2;ACLKRMASTER=1;ASYNROEN=0;PB_MASTER=0

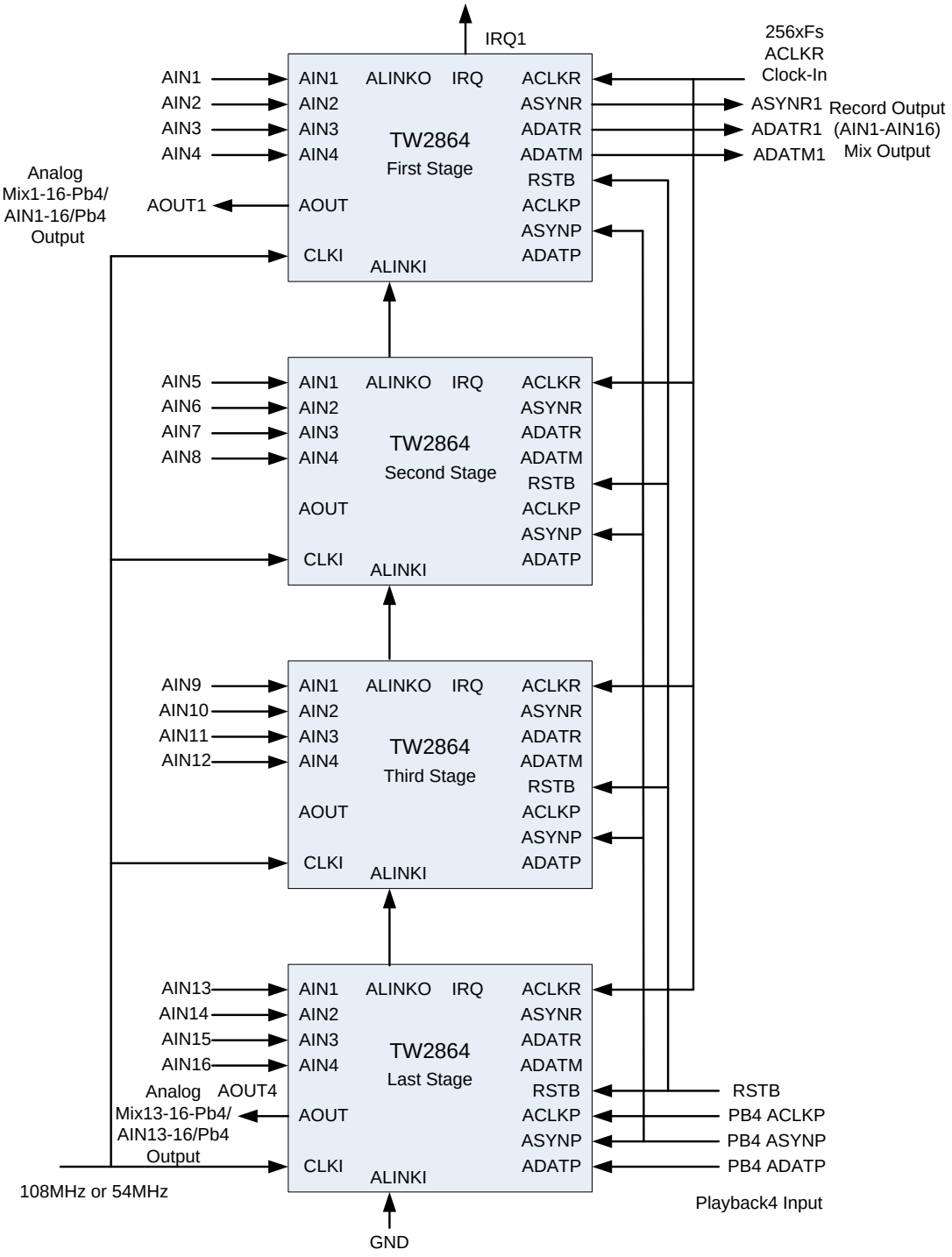


FIGURE 23. RECOMMENDED CLOCK SLAVE SYNC MASTER CASCADE MODE SYSTEM

All chips have SMD = 2;ACLKRMASTER=0;ASYNROEN=0;PB_MASTER=0

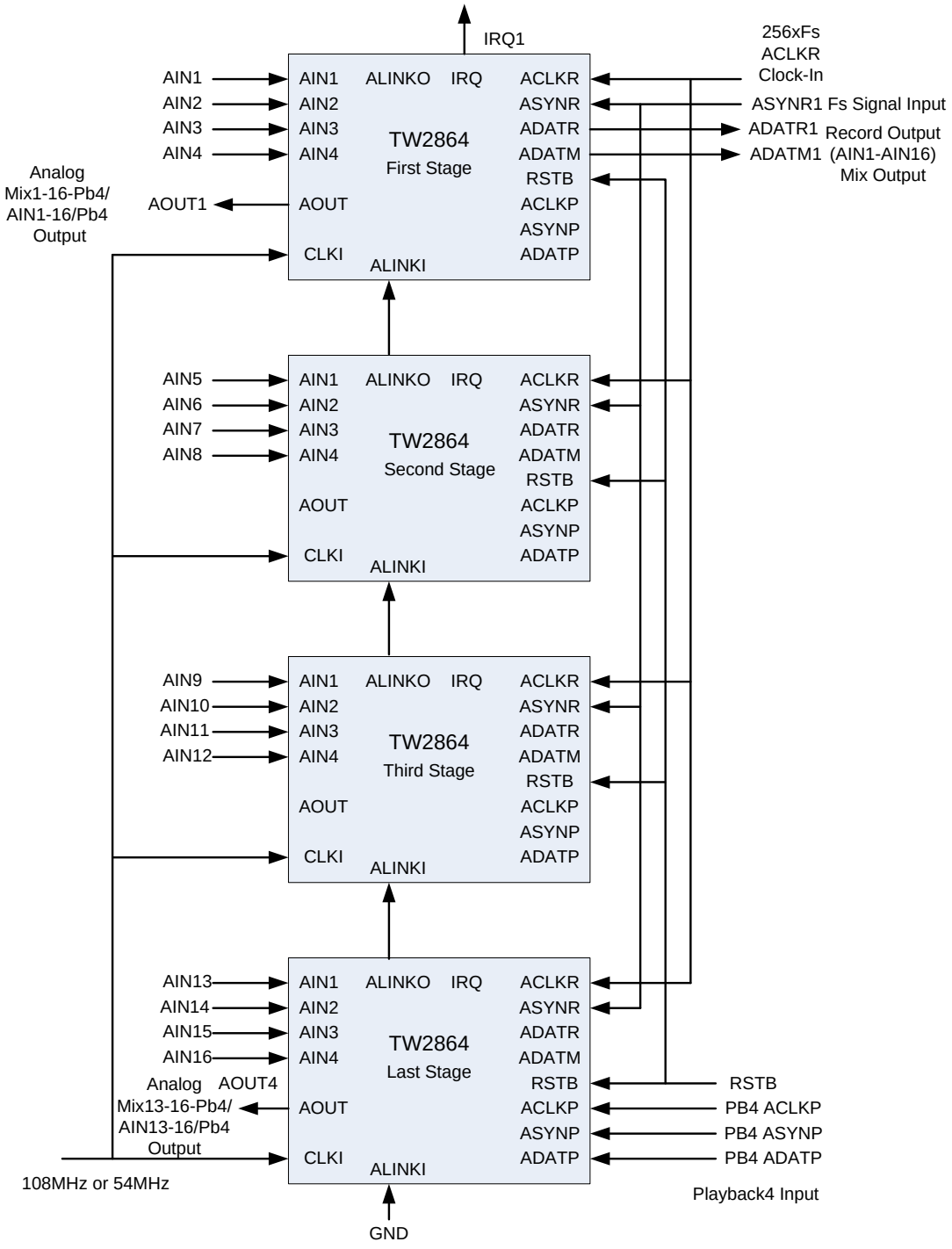
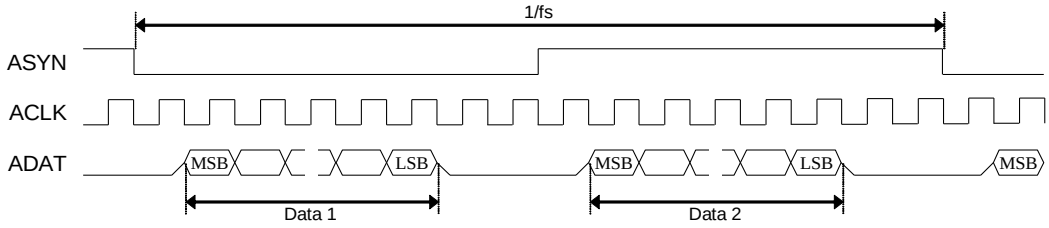


FIGURE 24. RECOMMENDED CLOCK SLAVE SYNC SLAVE CASCADE MODE SYSTEM

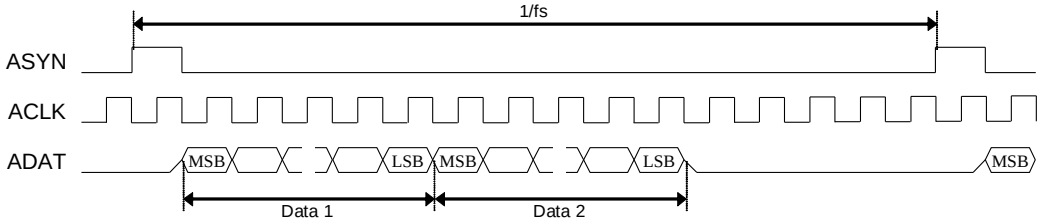
All chips have SMD = 2;ACLKRMASTER=0;ASYNROEN=1;PB_MASTER=0

SERIAL AUDIO INTERFACE

There are 3 kinds of digital serial audio interfaces in the TW2864, the first is a recording output, the second is a mixing output and the third is a playback input. These 3 digital serial audio interfaces follow a standard I2S or DSP interface, as shown in Figure 25.



(a) I2S Format



(b) DSP Format

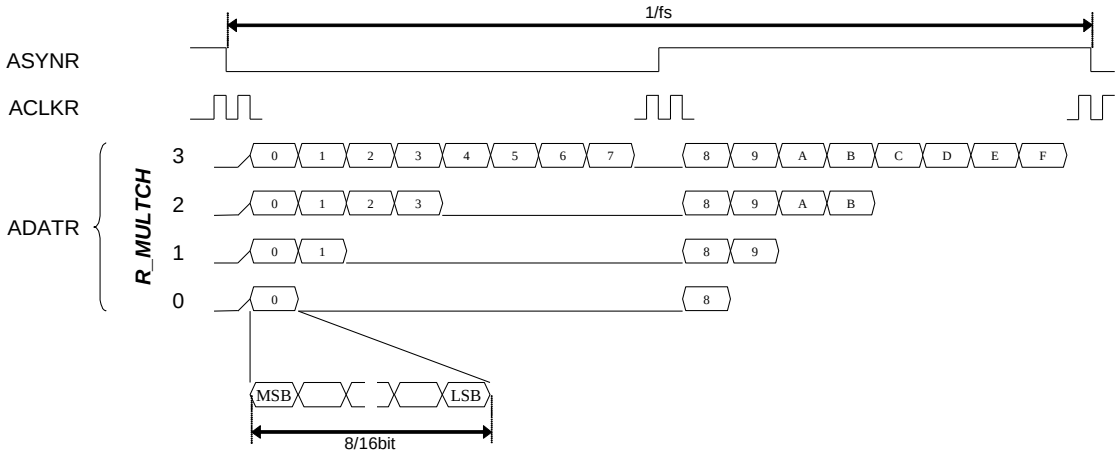
FIGURE 25. TIMING CHART OF SERIAL AUDIO INTERFACE

PLAYBACK INPUT

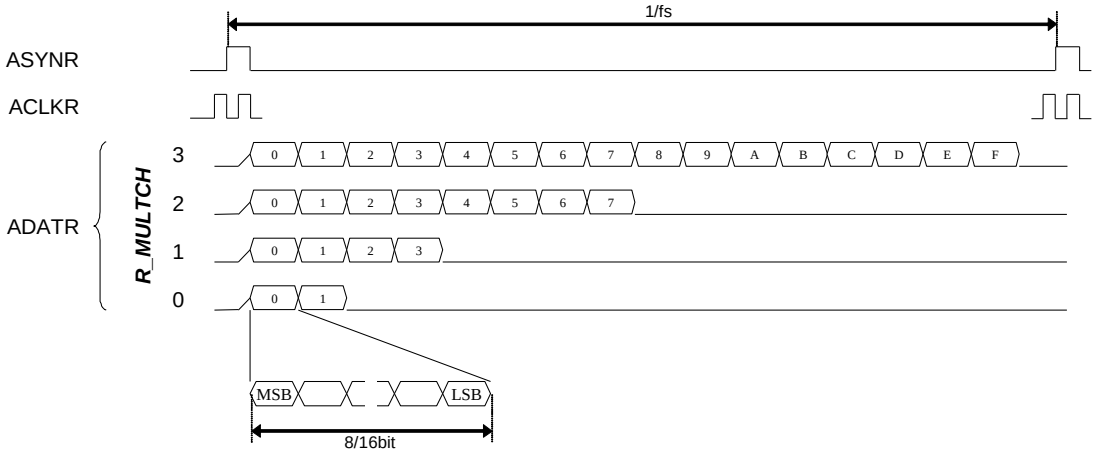
The serial interface using the ACLKP, ASYNP and ADATP pins accepts the digital serial audio data for the playback purpose. The ACLKP and ASYNP pins can be operated as master or slave mode. For master mode, these pins work as output pin and generate the standard audio clock and synchronizing signal. For slave mode, these pins are input mode and accept the standard audio clock and synchronizing signal. The ADATP pin is always input mode regardless of operating mode. One of audio data in left or right channel should be selected for playback audio by the PB_LRSEL.

RECORD OUTPUT

To record audio data, the TW2864 provides the digital serial audio data through the ACLKR, ASYNR and ADATR pins. Sampling frequency comes from 256xfs audio system clock setting. Even though the standard I2S and DSP format can have only 2 audio data on left and right channel, the TW2864 can provide an extended I2S and DSP format, which can have 16 channel audio data through ADATR pin. The R_MULTCH defines the number of audio data to be recorded by the ADATR pin. ASYNR signal is always fs frequency rate. One ASYNR period is always equal to 256 ACLKR clock length. Figure 26 shows the digital serial audio data organization for multi-channel audio. 8-bit mode has only DSP format. 16-bit mode has both I2S format and DSP format.



(a) I2S Format



(b) DSP Format

FIGURE 26. TIMING CHART OF MULTI-CHANNEL AUDIO RECORD

Table 6 shows the sequence of audio data to be recorded for each mode of the R_MULTCH register. The sequences of 0 ~ F do not mean actual audio channel number but represent sequence only. The actual audio channel should be assigned to sequence 0 ~ F by the R_SEQ_0 ~ R_SEQ_F register. When the ADATM pin is used for record via the R_ADATM register, the audio sequence of ADATM is also shown in Table 6.

TABLE 6. SEQUENCE OF MULTI-CHANNEL AUDIO RECORD

(a) I2S Format

R_MULTCH	PIN	LEFT CHANNEL								RIGHT CHANNEL							
0	ADATR	0								8							
	ADATM	F								7							
1	ADATR	0	1							8	9						
	ADATM	F	E							7	6						
2	ADATR	0	1	2	3					8	9	A	B				
	ADATM	F	E	D	C					7	6	5	4				
3	ADATR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	ADATM	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

(b) DSP Format

R_MULTCH	PIN	LEFT/RIGHT CHANNEL															
0	ADATR	0	1														
	ADATM	F	E														
1	ADATR	0	1	2	3												
	ADATM	F	E	D	C												
2	ADATR	0	1	2	3	4	5	6	7								
	ADATM	F	E	D	C	B	A	9	8								
3	ADATR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	ADATM	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

MIX OUTPUT

The digital serial audio data on the ADATM pin has 2 different audio data which are mixing audio and playback audio. The mixing digital serial audio data is the same as analog mixing output. The sampling frequency, bit width and number of audio for the ADATM pin are same as the ADATR pin because the ACLKR and ASYNR pins are shared with the ADATR and ADATM pins.

AUDIO CLOCK SLAVE MODE DATA OUTPUT TIMING

TW2864 always outputs ASYNR/ADATR/ADATM by ACLKR falling edge triggered timing.
ADATR/ADATM output data are always changing at next ACLKR falling edge triggered timing after ASYNR signal changes. If ASYNR is output, ADATR/ADATM outputs are always fixed to one ACLKR falling edge timing. However, if ASYNR is input, ADATR/ADATM output timing changes by ASYNR input timing.

ASYNR is ACLKR Falling Edge Triggered Input/Output

If ASYNR is input and ASYNR input is ACLKR falling edge triggered input as ASYNR input signal is changing after ACLKR falling edge,or if ASYNR is output, TW2864 output ADATR/ADATM by ACLKR falling edge triggered timing, as shown in the following figures. ASYNR signal is changing during ACLKR = 0.TW2864 output ADATR/ADATM data after next ACLKR falling edge triggered timing with more than half ACLKR clock delay.

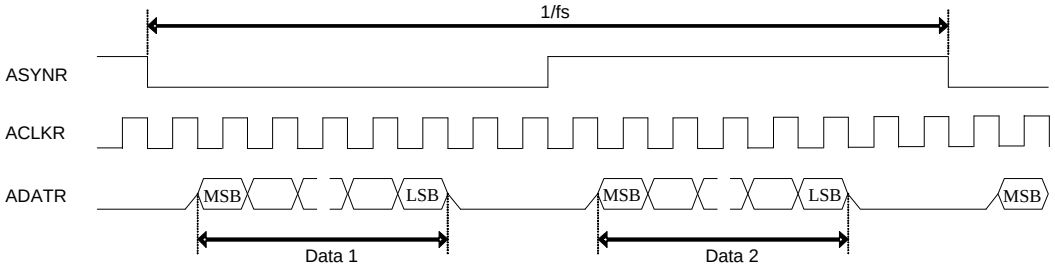


FIGURE 27. ACLKMASTER=0,RM_SYNC=0

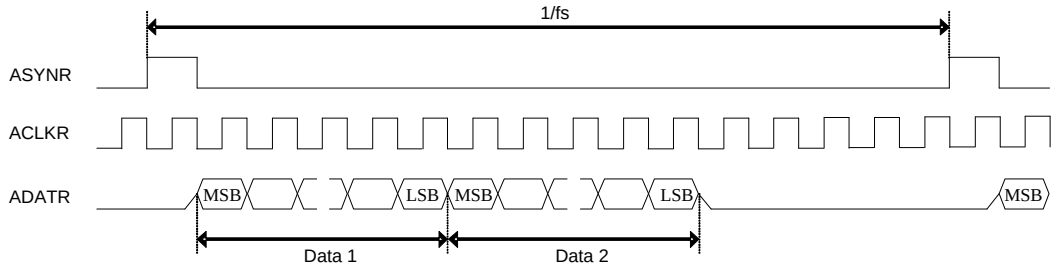


FIGURE 28. ACLKMASTER=0,RM_SYNC=1

ASYNR is ACLKR Rising Edge Triggered Input

If ASYNR is input and ASYNR input is ACLKR rising edge triggered input as ASYNR input signal is changing after ACLKR rising edge, TW2864 outputs ADATR/ADATM by ACLKR falling edge triggered timing, as shown in the following figures. ASYNR signal is changing during ACLKR = 1. TW2864 output ADATR/ADATM data after next ACLKR falling edge triggered timing with less than half ACLKR clock delay.

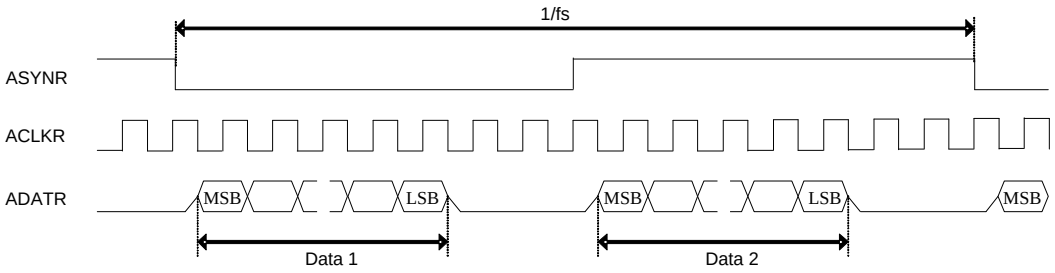


FIGURE 29. ACLKMASTER=0,RM_SYNC=0,ASYNROEN=1

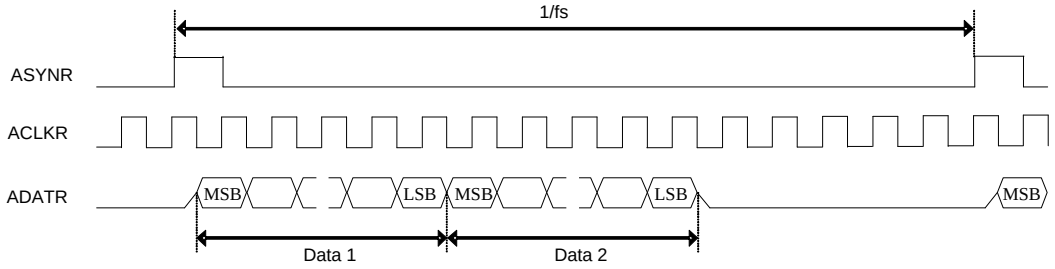


FIGURE 30. ACLKMASTER=0,RM_SYNC=1,ASYNROEN=1

AUDIO CLOCK SLAVE MODE DATA INPUT TIMING

ADATP data input has two kind of delay timings according to ACLKP/ASYNP input timing. ADATP data needs to be input from next ACLKP falling edge after ASYNP signal changes.

ASYNP is ACLKP falling edge triggered input

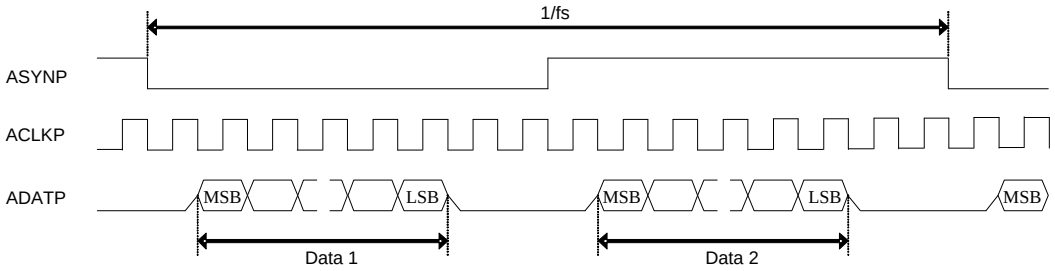


FIGURE 31. ACLKMASTER=0,RM_SYNC=0,PB_MASTER=0

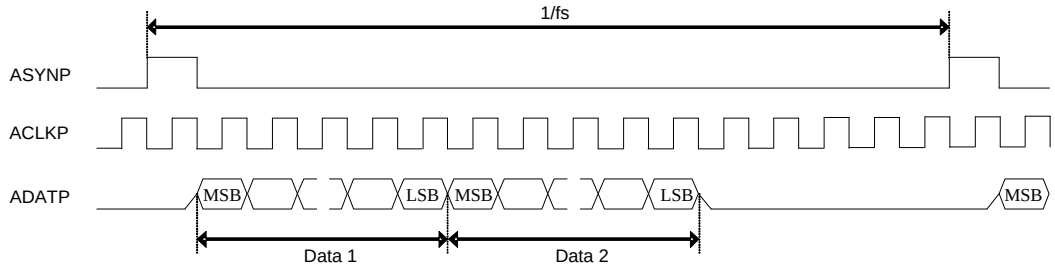


FIGURE 32. ACLKMASTER=0,RM_SYNC=1,PB_MASTER=0

ASYNP is ACLKP rising edge triggered input

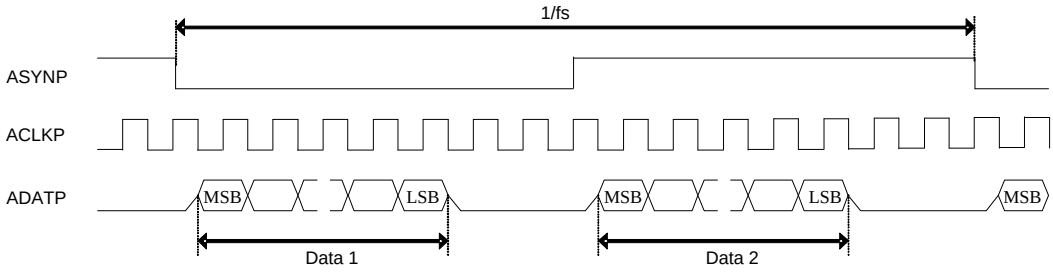


FIGURE 33. ACLKMASTER=0,RM_SYNC=0,PB_MASTER=0

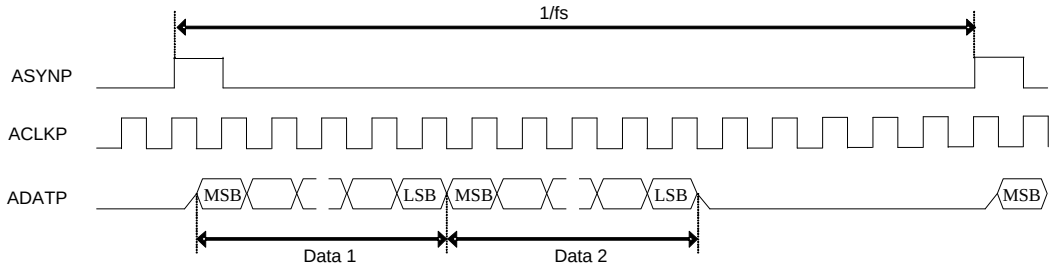


FIGURE 34. ACLKMASTER=0,RM_SYNC=1,PB_MASTER=0

ASYNP/ADATP signal need following input timing at this ACLKP rising edge triggered input.

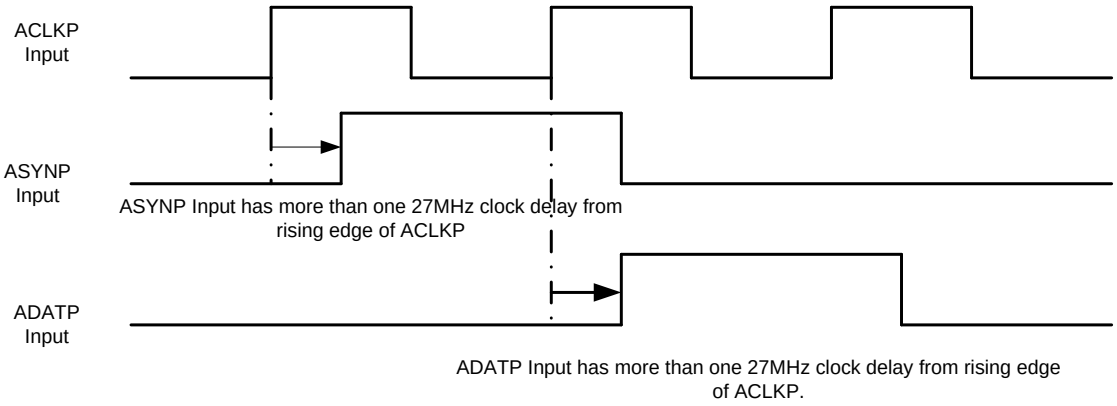


FIGURE 35. ASYNP/ADATP ACLKP RISING EDGE TRIGGERED INPUT TIMING

AUDIO CLOCK GENERATION

TW2864 has built-in field locked audio clock generator for use in video capture applications. The circuitry will generate the same pre-defined number of audio sample clocks per field to ensure synchronous playback of video and audio after digital recording or compression. The audio clock is digitally synthesized from the crystal clock input with reference to the incoming video. The master audio clock frequency is programmable through ACKN and ACKI register based on the following two equations.

ACKN = round (F AMCLK / F field), it gives the Audio master Clock Per Field.
ACKI = round (F AMCLK / F 27MHz * 2^23),it gives the Audio master Clock Nominal increment.

The following table provides setting examples of some commonly used audio frequencies, assuming a Video Decoder system clock frequency of 27MHz.

AMCLK(MHZ)	FIELD[HZ]	ACKN [DEC]	ACKN [HEX]	ACKI [DEC]	ACKI [HEX]
256 x 48 KHz					
12.288	50	245760	3-C0-00	3817749	3A-41-15
12.288	59.94	205005	3-20-CD	3817749	3A-41-15
256 x 44.1KHz					
11.2896	50	225792	3-72-00	3507556	35-85-65
11.2896	59.94	188348	2-DF-BC	3507556	35-85-65
256 x 32 KHz					
8.192	50	163840	2-80-00	2545166	26-D6-0E
8.192	59.94	136670	2-15-DE	2545166	26-D6-0E
256 x 16 KHz					
4.096	50	81920	1-40-00	1272583	13-6B-07
4.096	59.94	68335	1-0A-EF	1272583	13-6B-07
256 x 8 KHz					
2.048	50	40960	A0-00	636291	9-B5-83
2.048	59.94	34168	85-78	636291	9-B5-83

If ACLKRMASTER register bit is set to 1, this AMCLK(256xfs) is used as audio system clock inside TW2864 chip. [REV_ID>=1 TW2864 only]

If Slave Playback-in lock mode is required, ACKN=00100hex and PBREFEN=1 needs to be set up. The number of AMCLK clock per one ASYNP input cycle is locked (fixed) to 256 in this mode.

The frequency equation is “AMCLK(Freq) = 256 x ASYNP(Freq)”.

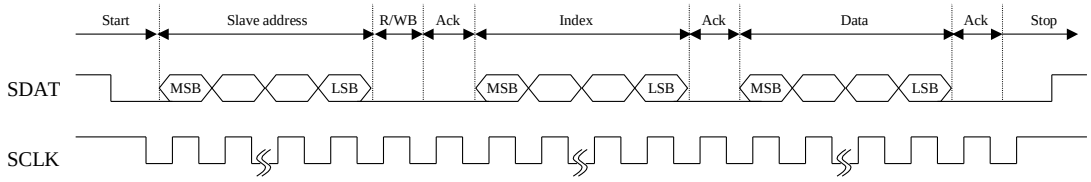
Host Interface

Serial Interface

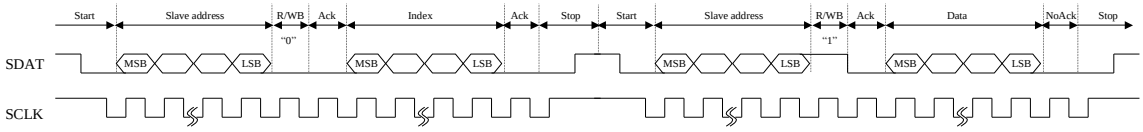
The two wire serial bus interface is used to allow an external micro-controller to write to or read from the data through the TW2864 register. The SCLK is the serial clock and SDAT is the data line. Both lines are pulled high by the resistors connected to VDD. The SADD[1:0] defines two LSB of the slave device address by tying the SADD pins either to VDD or GND.

SLAVE ADDRESS							R/W
0	1	0	1	0	SADD[1]	SADD[0]	1 = Read 0 = Write

The TW2864 supports auto index increments in write/read mode if the data are in sequential order. Data transfer rate on the bus is up to 400 Kbits/s.



(a) Write Mode

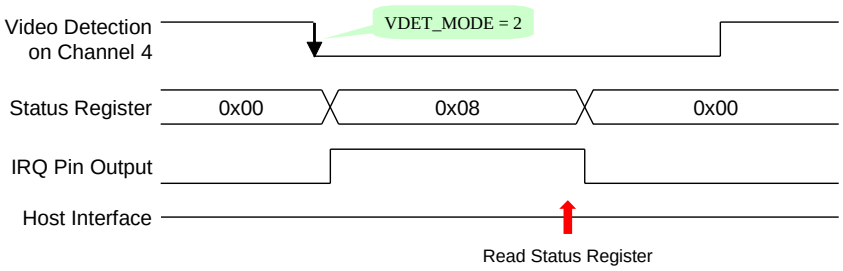


(b) Read Mode

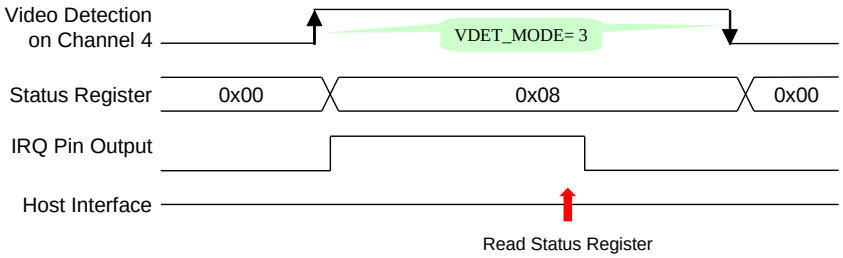
FIGURE 36. TIMING CHART OF SERIAL INTERFACE

Interrupt Interface

The TW2864 provides the interrupt request function using an IRQ pin so that the host does not need to waste much resource to detect video or audio signal from TW2864. To use interrupt request function, the interrupt request should be enabled by the IRQENA and polarity of the IRQ pin should be selected by the IRQPOL. Also, each channel of video and audio detection should be enabled by the AVDET_ENA. Then, the interrupt mode should be defined by the VDET_MODE and ADET_MODE that control the time to request interrupt and set the status register AVDET_STATE. The Figure 37 shows operation of interrupt when the VDET_MODE and/or ADET_MODE are 2 and 3. The IRQ pin is cleared automatically by reading the AVDET_STATE. When the VDET_MODE and/or ADET_MODE is 1 or 2, the status register AVDET_STATE will also be cleared automatically by reading AVDET_STATE. However, when the VDET_MODE and/or ADET_MODE are 3, the status register AVDET_STATE will not be cleared automatically, but has the same value as actual status of video and audio detection flag.



(a) Status Register of Automatic Cleared Mode



(b) Status Register same as Video and Audio Detection Flag Mode

FIGURE 37. TIMING DIAGRAM OF INTERRUPT INTERFACE

Single Channel Clock-In Mode

[REV_ID>=1 TW2864 only]

If TEST pin is 1 and ALINKI pin is 0, TW2864 works under CLKI pin Single Channel Clock-In mode. In this mode, if FC27 register is 1, a 27MHz clock needs to be connected to the CLKI pin; if FC27 register is 0, a 29.5MHz clock for PAL-SQ or 24.543MHz clock for NTSC-SQ needs to be connected to the CLKI pin. Also, SADD[1:0]=0/2/3 values are available for Serial Interface Slave Address. If Audio function is used with FC27=0 squared pixel mode, ACKI register equation is as follows.

ACKI = round (Faudio/CLKI input clock Frequency * 2^23)

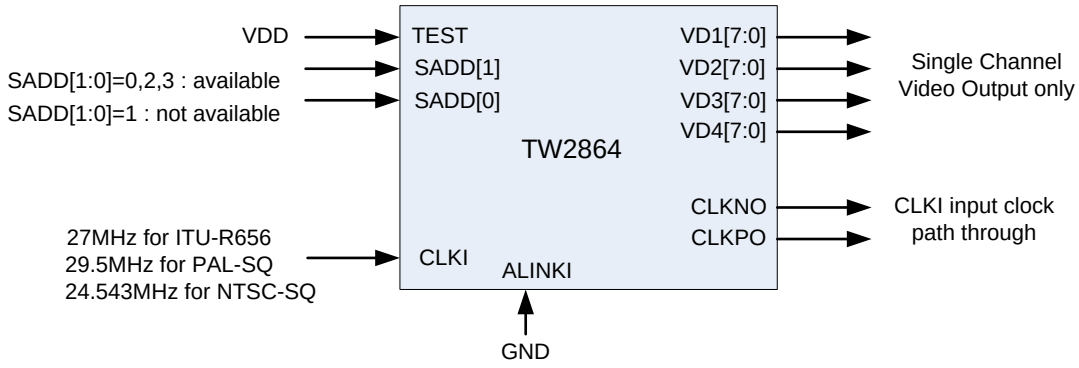


FIGURE 38. SINGLE CHANNEL CLOCK-IN MODE

Squared Pixel Mode Operation

If FC27 register bit is set to 0, TW2864 works under Squared Pixel mode operation. If Single Channel Clock-In mode is not selected, CLKI pin input on PAL-SQ mode should have either 118MHz(=29.5MHzx4) for TW2864A/TW2864C or 59MHz(=29.5MHzx2) for TW2864B/TW2864D. Also,CLKI pin input on NTSC-SQ mode should have either 98.172MHz(=24.543MHzx4) for TW2864A/TW2864C or 49.086MHz(=24.543MHzx2) for TW2864B/TW2864D. If Single Channel Clock-In mode is selected (REV_ID>=1 TW2864 only), CLKI pin input should have either 29.5MHz for PAL-SQ or 24.543MHz for NTSC-SQ. HACTIVE register value should be 0x300 (768dec) for PAL-SQ and 0x280 (640dec) for NTSC-SQ. If Audio function is used with this Squared Pixel mode, ACKI register equations are as follows.

ACKI = round (F audio / 29.5MHz * 2^23)……for PAL-SQ

ACKI = round (F audio / 24.543MHz * 2^23)……for NTSC-SQ

Control Registers

REGISTER MAP

Address				Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH1	CH2	CH3	CH4									
0x00	0x10	0x20	0x30	VIDSTAT *	VDLOSS*	HLOCK*	SLOCK*	FLD*	VLOCK*	Reserved*	MONO*	DET50*
0x01	0x11	0x21	0x31	BRIGHT	BRIGHTNESS							
0x02	0x12	0x22	0x32	CONTRAST	CONTRAST							
0x03	0x13	0x23	0x33	SHARPNESS	SCURVE	VSF	CTI		SHARPNESS			
0x04	0x14	0x24	0x34	SAT_U	SAT_U							
0x05	0x15	0x25	0x35	SAT_V	SAT_V							
0x06	0x16	0x26	0x36	HUE	HUE							
0x07	0x17	0x27	0x37	CROP_HI	VDELAY[9:8]		VACTIVE[9:8]		HDELAY[9:8]		HACTIVE[9:8]	
0x08	0x18	0x28	0x38	VDELAY_LO	VDELAY[7:0]							
0x09	0x19	0x29	0x39	VACTIVE_LO	VACTIVE[7:0]							
0x0A	0x1A	0x2A	0x3A	HDELAY_LO	HDELAY[7:0]							
0x0B	0x1B	0x2B	0x3B	HACTIVE_LO	HACTIVE[7:0]							
0x0C	0x1C	0x2C	0x3C	MVSN*	SF*	PF*	FF*	KF*	CSBAD*	MCVSN*	CSTRIPE*	CTYPE*
0x0D	0x1D	0x2D	0x3D	STATUS2*	VCR*	WKAIR*	WKAIR1*	VSTD*	NINTL*	0	0	0
0x0E	0x1E	0x2E	0x3E	SDT	DETSTUS*	STDNOW*			ATREG	STANDARD		
0x0F	0x1F	0x2F	0x3F	SDTR	ATSTART	PAL60EN	PALCNEN	PALMEN	NTSC44EN	SECAMEN	PALBEN	NTSCEN
0xE4	0xE7	0xEA	0xED	VSCALE_LO	VSCALE[7:0]							
0xE5	0xE8	0xEB	0xEE	SCALE_HI	VSCALE[11:8]				HSACLE[11:8]			
0xE6	0xE9	0xEC	0xEF	HSCALE_LO	HSCALE[7:0]							
0xA4	0xA5	0xA6	0xA7	IDCNTL	IDX		NSEN/SSEN/PSEN/WKTH					
0xC4	0xC5	0xC6	0xC7	HREF*	HREF							

NOTE: *** READ ONLY REGISTERS**

Address				Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH1	CH2	CH3	CH4									
0x7B				Reserved	0	0	0	1	0	1	0	1
0x7C				Reserved	0	0	0	1	0	1	0	1
0x7E				Reserved	1	0	1	0	0	0	1	1
0x80				SRST	0	0	AUDIORST	VOUTRST	VDEC4RST	VDEC3RST	VDEC2RST	VDEC1RST
0x81				ACNTL	0	IREF	VREF	0	CLKPDN	0	YFLEN	YSV
0x82				ACNTL2	CTEST	YCLEN	0	AFLTEN	GTEST	VLPF	CKLY	CKLC
0x83				CNTRL1	PBW	DEM	PALSW	SET7	COMB	HCOMP	YCOMB	PDLY
0x84				CKHY	GMEN	CKHY			HSDLY			
0x85				SHCOR	SHCOR				0	0	0	0
0x86				CORING	CTCOR		CCOR		VCOR		CIF	
0x87				CLMPG	CLPEND				CLPST			
0x88				IAGC	NMGAIN				WPGAIN			0
0x89				Reserved	0	0	0	0	0	0	0 or 1	0 or 1
0x8A				PEAKWT	PEAKWT							
0x8B				CLMPL	CLMPLD	CLMPL						
0x8C				SYNCT	SYNCTD	SYNCT						
0x8D				MISSCNT	MISSCNT				HSWIN			
0x8E				PCLAMP	PCLAMP							
0x8F				VCNTL1	VLCKI		VLCKO		VMODE	DETV	AFLD	VINT
0x90				VCNTL2	BSHT			VSHT				
0x91				CKILL	CKILMAX		CKILMIN					
0x92				COMB	COMBMD	HTL			VTL			
0x93				LDLY	CKLM	YDLY			HPF_RES			
0x94				MISC1	HPLC	ENCNT	PALC	SDET	TBCEN	BYPASS	SYOUT	0
0x95				LOOP	HPM		ACCT		SPM		CBW	
0x96				MISC2	NKILL	PKILL	SKILL	CBAL	FCS	LCS	CCS	BST
0x97				CLMD	FRM		YNR		CLMD		PSP	
0x98				HSLOWCTL	0	HSBEGIN[2:0]			0	HSEND[2:0]		
0x99				HSBEGIN	HSBEGIN[10:3]							
0x9A				HSEND	HSEND[10:3]							
0x9B				OVSDLY	OVSDLY							

NOTE: **: * READ ONLY REGISTERS**

Address				Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH1	CH2	CH3	CH4									
0x9C				OVSEND	HASYNC	OFDLY			VSMODE	OVSEND		
0x9D				HBLEN	HBLEN							
0x9E				NOVID	0	FC27	CHID_MD		NOVID_656	EAVSWAP	VIPCFG	NTSC656
0x9F				CLK_MD	CLKN_DEL				CLKP_DEL			
0xA8				HFLT21	HFLT2				HFLT1			
0xA9				HFLT43	HFLT4				HFLT3			
0xAA				AGCEN	AGCEN4	AGCEN3	AGCEN2	AGCEN1	AGCGAIN4[8]	AGCGAIN3[8]	AGCGAIN2[8]	AGCGAIN1[8]
0xAB				AGCGAIN1	AGCGAIN1[7:0]							
0xAC				AGCGAIN2	AGCGAIN2[7:0]							
0xAD				AGCGAIN3	AGCGAIN3[7:0]							
0xAE				AGCGAIN4	AGCGAIN4[7:0]							
0xAF				VSHP21	0	VSHP2			0	VSHP1		
0xB0				VSHP43	0	VSHP4			0	VSHP3		
0xB1				CLKCURRENT	0	0	NOVIDMODE or 0		CLKN2OEB or 0	CLKN1OEB or 0	CLKP2OEB or 0	CLKP1OEB or 0
0xB2				Reserved	Reserved							
0xB3				AADC4OFS_H	AADC4OFS[9:8]		AADC3OFS[9:8]		AADC2OFS[9:8]		AADC1OFS[9:8]	
0xB4				AADC1OFS_L	AADC1OFS[7:0]							
0xB5				AADC2OFS_L	AADC2OFS[7:0]							
0xB6				AADC3OFS_L	AADC3OFS[7:0]							
0xB7				AADC4OFS_L	AADC4OFS[7:0]							
0xB8				AUDADC_H*	AUD4ADC[9:8]		AUD3ADC[9:8]		AUD2ADC[9:8]		AUD1ADC[9:8]	
0xB9				AUD1ADC_L*	AUD1ADC[7:0]							
0xBA				AUD2ADC_L*	AUD2ADC[7:0]							
0xBB				AUD3ADC_L*	AUD3ADC[7:0]							
0xBC				AUD4ADC_L*	AUD4ADC[7:0]							
0xBD				ADJAADC_H*	ADJAADC4[9:8]		ADJAADC3[9:8]		ADJAADC2[9:8]		ADJAADC1[9:8]	
0xBE				ADJAADC1_L*	ADJAADC1[7:0]							
0xBF				ADJAADC2_L*	ADJAADC2[7:0]							
0xC0				ADJAADC3_L*	ADJAADC3[7:0]							
0xC1				ADJAADC4_L*	ADJAADC4[7:0]							

NOTE: *** READ ONLY REGISTERS**

Address				Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH1	CH2	CH3	CH4									
0xC8				CLK_DEL1	GPP_VAL2	MPP_MODE2			GPP_VAL1	MPP_MODE1		
0xC9				CLK_DEL2	GPP_VAL4	MPP_MODE4			GPP_VAL3	MPP_MODE3		
0xCA				CHMD	CHMD4		CHMD3		CHMD2		CHMD1	
0xCB				CIF54M	POLMPP4	POLMPP3	POLMPP2	POLMPP1	CIF54M4	CIF54M3	CIF54M2	CIF54M1
0xCC				SELCH	SELCH4		SELCH3		SELCH2		SELCH1	
0xCD				MAINCH	MAINCH4		MAINCH3		MAINCH2		MAINCH1	
0xCE				ANAPWDN	AAUTOMUTE	HPF_RES	A_DAC_PWDN	A_ADC_PWDN	V4_ADC_PWDN	V3_ADC_PWDN	V2_ADC_PWDN	V1_ADC_PWDN
0xCF				SMD	SMD		VRSTSEL		FIRSTCNUM			
0xD0				AIGAIN21	AIGAIN2				AIGAIN1			
0xD1				AIGAIN43	AIGAIN4				AIGAIN3			
0xD2				R_MULTCH	M_RLSWAP	RM_SYNC	RM_PBSEL		0	R_ADATM	R_MULTCH	
0xD3				R_SEQ10	R_SEQ_1				R_SEQ_0			
0xD4				R_SEQ32	R_SEQ_3				R_SEQ_2			
0xD5				R_SEQ54	R_SEQ_5				R_SEQ_4			
0xD6				R_SEQ76	R_SEQ_7				R_SEQ_6			
0xD7				R_SEQ98	R_SEQ_9				R_SEQ_8			
0xD8				R_SEQBA	R_SEQ_B				R_SEQ_A			
0xD9				R_SEQDC	R_SEQ_D				R_SEQ_C			
0xDA				R_SEQFE	R_SEQ_F				R_SEQ_E			

NOTE: *** READ ONLY REGISTERS**

Address				Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH1	CH2	CH3	CH4									
0xDB				AMASTER	ADACEN	AADCEN	PB_MASTER	PB_LRSEL	PB_SYNC	RM_8BIT	ASYNROEN	ACLKRMASTER
0xDC				MIX_MUTE	LAWMD		MIX_DERATIO	MIX_MUTE				
0xDD				MIX_RATIO21	MIX_RATIO2				MIX_RATIO1			
0xDE				MIX_RATIO43	MIX_RATIO4				MIX_RATIO3			
0xDF				AOGAIN	AOGAIN				MIX_RATIOP			
0xE0				MIX_OUTSEL	VADCCKPOL	AADCCKPOL	ADACCKPOL	MIX_OUTSEL				
0xE1				ADET	AAMPMD	ADET_FILT			ADET_TH4[4]	ADET_TH3[4]	ADET_TH2[4]	ADET_TH1[4]
0xE2				ADET_TH21	ADET_TH2[3:0]				ADET_TH1[3:0]			
0xE3				ADET_TH43	ADET_TH4[3:0]				ADET_TH3[3:0]			
0xF0				ACKI_L	ACKI[7:0]							
0xF1				ACKI_M	ACKI[15:8]							
0xF2				ACKI_H	0	0	ACKI[21:16]					
0xF3				ACKN_L	ACKN[7:0]							
0xF4				ACKN_M	ACKN[15:8]							
0xF5				ACKN_H	0	0	0	0	0	0	ACKN[17:16]	
0xF6				SDIV	0	0	SDIV					
0xF7				LRDIV	0	0	LRDIV					
0xF8				ACCNTL	0 or APZ	APZ or APG[2]	APG		0	ACPL	SRPH	LRPH
0xF9				VMISC	0 or LIM16	0 or PBREFEN	YCBCR422	HA656MD	VBI_FRAM	CNTL656	VSCL_SYNC	HA_EN
0xFA				CLKOCTL	0 or VSCL_ENA	OE	CLKN_OEB	CLKP_OEB	CLKN_MD		CLKP_MD	
0xFB				AVDET_MODE	CLKN_POL	CLKP_POL	IRQENA	IRQPOL	ADET_MODE		VDET_MODE	
0xFC				AVDET_ENA	AVDET_ENA							
0xFD				AVDET_STATE*	AVDET_STATE							
0xFE				TEST	DEV_ID[6:5]* : 0h		0	0	0	TEST		
0xFF				DEV_ID*	DEV_ID[4:0] : 6h					REV_ID		

Note : * Read only registers

REGISTER DESCRIPTIONS

0X00(CH1)/0X10(CH2)/0X20(CH3)/0X30(CH4) – VIDEO STATUS REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	VDLOSS	R	1 = Video not present. (sync is not detected in number of consecutive line periods specified by MISSCNT register) 0 = Video detected.	0
6	HLOCK	R	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	0
5	SLOCK	R	1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked.	0
4	FIELD	R	0 = Odd field is being decoded. 1 = Even field is being decoded.	0
3	VLOCK	R	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	0
2	Reserved	R	Reserved	0
1	MONO	R	1 = No color burst signal detected. 0 = Color burst signal detected.	0
0	DET50	R	0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked for decoding.	0

0X01(CH1)/0X11(CH2)/0X21(CH3)/0X31(CH4) – BRIGHTNESS CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	BRIGHT	R/W	These bits control the brightness. They have value of –128 to 127 in 2's complement form. Positive value increases brightness. A value 0 has no effect on the data.	00

0X02(CH1)/0X12(CH2)/0X22(CH3)/0X32(CH4) – CONTRAST CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	CNTRST	R/W	These bits control the luminance contrast gain. A value of 100 (64h) has a gain of 1. The range of adjustment is from 0% to 255% at 1% per step.	5C

0X03(CH1)/0X13(CH2)/0X23(CH3)/0X33(CH4) – SHARPNESS CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	SCURVE	R/W	This bit controls the center frequency of the peaking filter. The corresponding gain adjustment is HFLT. 0 = low 1 = center	0
6	VSF	R/W	This bit is for internal used.	0
5-4	CTI	R/W	CTI level selection. 0 = None. 3 = highest.	1
3-0	SHARP	R/W	These bits control the amount of sharpness enhancement on the luminance signals. There are 16 levels of control with '0' having no effect on the output image. 1 through 15 provides sharpness enhancement with 'F' being the strongest.	1

0X04(CH1)/0X14(CH2)/0X24(CH3)/0X34(CH4) – CHROMA (U) GAIN REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	SAT_U	R/W	These bits control the digital gain adjustment to the U (or Cb) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%. A value of 128 (80h) has gain of 100%.	80

0X05(CH1)/0X15(CH2)/0X25(CH3)/0X35(CH4) – CHROMA (V) GAIN REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	SAT_V	R/W	These bits control the digital gain adjustment to the V (or Cr) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%. A value of 128 (80h) has gain of 100%.	80

0X06(CH1)/0X16(CH2)/0X26(CH3)/0X36(CH4) – HUE CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HUE	R/W	These bits control the color hue as 2's complement number. They have value from +90° (7Fh) to -90° (80h) with an increment of 2.8°. The 2 LSB has no effect. The positive value gives greenish tone and negative value gives purplish tone. The default value is 0° (00h). This is effective only on NTSC and PAL system.	00

0X07(CH1)/0X17(CH2)/0X27(CH3)/0X37(CH4) – CROPPING REGISTER, HIGH

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	VDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Vertical Delay register.	0
5-4	VACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit VACTIVE register. Refer to description on Reg09 for its shadow register.	1
3-2	HDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Horizontal Delay register.	0
1-0	HACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit HACTIVE register.	2

0X08(CH1)/0X18(CH2)/0X28(CH3)/0X38(CH4) – VERTICAL DELAY REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	VDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Delay register. The two MSBs are in the CROP_HI register. It defines the number of lines between the leading edge of VSYNC and the start of the active video.	12

0X09(CH1)/0X19(CH2)/0X29(CH3)/0X39(CH4) – VERTICAL ACTIVE REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	VACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Active register. The two MSBs are in the CROP_HI register. It defines the number of active video lines per frame output. The VACTIVE register has a shadow register for use with 50Hz source when ATREG of Reg0x1C is not set. This register can be accessed through the same index address by first changing the format standard to any 50Hz standard.	20

0X0A(CH1)/0X1A(CH2)/0X2A(CH3)/0X3A(CH4) – HORIZONTAL DELAY REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Delay register. The two MSBs are in the CROP_HI register. It defines the number of pixels between the leading edge of the HSYNC and the start of the image cropping for active video. The HDELAY_LO register has two shadow registers for use with PAL and SECAM sources respectively. These register can be accessed using the same index address by first changing the decoding format to the corresponding standard.	0A

0X0B(CH1)/0X1B(CH2)/0X2B(CH3)/0X3B(CH4) – HORIZONTAL ACTIVE REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Active register. The two MSBs are in the CROP_HI register. It defines the number of active pixels per line output.	D0

0X0C(CH1)/0X1C(CH2)/0X2C(CH3)/0X3C(CH4) – MACROVISION DETECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	SF	R	This bit is for internal use.	0
6	PF	R	This bit is for internal use.	0
5	FF	R	This bit is for internal use.	0
4	KF	R	This bit is for internal use.	0
3	CSBAD	R	1 = Macrovision color stripe detection un-reliable	0
2	MVCSN	R	1 = Macrovision AGC pulse detected. 0 = Not detected.	0
1	CSTRIPE	R	1 = Macrovision color stripe protection burst detected. 0 = Not detected.	0
0	CTYPE	R	This bit is valid only when color stripe protection is detected, i.e. CSTRIPE=1. 1 = Type 2 color stripe protection 0 = Type 3 color stripe protection	0

0X0D(CH1)/0X1D(CH2)/0X2D(CH3)/0X3D(CH4) – CHIP STATUS II

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	VCR	R	VCR signal indicator.	0
6	WKAIR	R	Weak signal indicator 2.	0
5	WKAIR1	R	Weak signal indicator controlled by WKTH.	0
4	VSTD	R	1 = Standard signal 0 = Non-standard signal	0
3	NINTL	R	1 = Non-interlaced signal 0 = interlaced signal	0
2-0	Reserved	R	Reserved	0h

0X0E(CH1)/0X1E(CH2)/0X2E(CH3)/0X3E(CH4) – STANDARD SELECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	DETSTUS	R	0 = Idle 1 = detection in progress	0
6-4	STDNOW	R	Current standard invoked 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Not valid	0
3	ATREG	R/W	1 = Disable the shadow registers. 0 = Enable VACTIVE and HDELAY shadow registers value depending on standard	0
2-0	STD	R/W	Standard selection 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Auto detection	7

0X0F(CH1)/0X1F(CH2)/0X2F(CH3)/0X3F(CH4) – STANDARD RECOGNITION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	ATSTART	R/W	Writing 1 to this bit will manually initiate the auto format detection process. This bit is a self-resetting bit.	0
6	PAL6_EN	R/W	1 = enable recognition of PAL60. 0 = disable recognition.	1
5	PALN_EN	R/W	1 = enable recognition of PAL (CN). 0 = disable recognition.	1
4	PALM_EN	R/W	1 = enable recognition of PAL (M). 0 = disable recognition.	1
3	NT44_EN	R/W	1 = enable recognition of NTSC 4.43. 0 = disable recognition.	1
2	SEC_EN	R/W	1 = enable recognition of SECAM. 0 = disable recognition.	1
1	PALB_EN	R/W	1 = enable recognition of PAL (B,D,G,H,I). 0 = disable recognition.	1
0	NTSC_EN	R/W	1 = enable recognition of NTSC (M). 0 = disable recognition.	1

0XE4(CH1)/0XE7(CH2)/0XEA(CH3)/0XED(CH4) – VERTICAL SCALING REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	VSCALE_LO	R/W	These bits are bit 7 to 0 of the 12-bit vertical scaling ratio register	00

0XE5(CH1)/0XE8(CH2)/0XEB(CH3)/0XEE(CH4) – SCALING REGISTER, HIGH

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	VSCALE_HI	R/W	These bits are bit 11 to 8 of the 12-bit vertical scaling ratio register.	1
3-0	HSCALE_HI	R/W	These bits are bit 11 to 8 of the 12-bit horizontal scaling ratio register.	1

0XE6(CH1)/0XE9(CH2)/0XEC(CH3)/0XEF(CH4) – HORIZONTAL SCALING REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HSCALE_LO	R/W	These bits are bit 7 to 0 of the 12-bit horizontal scaling ratio register.	00

0XA4(CH1)/0XA5(CH2)/0XA6(CH3)/0XA7(CH4) – ID DETECTION CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	IDX	R/W	These two bits indicate which of the four lower 6-bit registers is currently being controlled. The write sequence is a two steps process unless the same register is written. A write of {ID,000000} selects one of the four registers to be written. A subsequent write will actually write into the register.	0
5-0	NSEN / SSEN / PSEN / WKTH	R/W	IDX = 0 controls the NTSC color carrier detection sensitivity (NSEN). IDX = 1 controls the SECAM ID detection sensitivity (SSEN). IDX = 2 controls the PAL ID detection sensitivity (PSEN). IDX = 3 controls the weak signal detection sensitivity (WKTH).	1A / 20 / 1C / 2A

0XC4(CH1)/0XC5(CH2)/0XC6(CH3)/0XC7(CH4) – H MONITOR

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HFREF	R	Horizontal line frequency indicator (Test purpose only)	X

0X80 – SOFTWARE RESET CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	Reserved	R	Reserved	00b
5	AUDIORST	W	A 1 written to this bit resets the Audio portion to its default state but all register content remains unchanged. This bit is self-resetting.	0
4	VOUTRST	W	A 1 written to this bit resets Video data mux output logic to its default state but all register content remain unchanged. This bit is self-resetting.	0
3	VDEC4RST	W	A 1 written to this bit resets the Video4 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0
2	VDEC3RST	W	A 1 written to this bit resets the Video3 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0
1	VDEC2RST	W	A 1 written to this bit resets the Video2 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0
0	VDEC1RST	W	A 1 written to this bit resets the Video1 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0

0X81 – ANALOG CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R	Reserved	0
6	IREF	R/W	0 = Internal current reference 1. 1 = Internal current reference increase 30%.	0
5	VREF	R/W	0 = Internal voltage reference. 1 = Internal voltage reference shut down.	0
4	Reserved	R/W	0 = Normal operation(must be 0), 1 = AIGAINTEST	0
3	CLKPDN	R/W	0 = Normal clock operation. 1 = All 4Ch Video Decoder System clock in power down mode, but the MPU INTERFACE module and output clocks (CLKP and CLKN) are still active.	0

BIT	FUNCTION	R/W	DESCRIPTION	RESET
2	Reserved	R/W	0 = Normal operation(must be 0), 1 = AINSWTEST	0
1	YFLEN	R/W	Analog Video CH1/CH2/CH3/CH4 anti-alias filter control 1 = enable 0 = disable	1
	YSV	R/W	Analog Video CH1/CH2/CH3/CH4 Reduced power mode 1 = enable 0 = disable	0

0X82 – ANALOG CONTROL REISTER2

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CTEST	R/W	Clamping control for debugging use.(Test purpose only)	0
6	YCLEN	R/W	1 = Y channel clamp disabled (Test purpose only) 0 = Enabled.	0
5	CKIPOL	R/W	[REV_ID>=2 only] 27MHz clock output signal rise/fall timing. 0: change by 54MHz clock output falling edge. 1: change by 54MHz clock output rising edge.	0
4	AFLTEN	R/W	1 = Analog Audio input Anti-Aliasing Filter enabled (REV_ID=0/1/2 TW2864 default) 0 = Disabled.(**must be 0 for no Audio Input cross-talk**) (REV_ID=3 TW2864 default)	0
3	GTEST	R/W	1 = Internal test.(Test purpose only) 0 = Normal operation.	0
2	VLPF	R/W	Clamping filter control.	0
1	CKLY	R/W	Clamping current control 1.	0
0	CKLC	R/W	Clamping current control 2.	0

0X83 – CONTROL REGISTER I

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	PBW	R/W	1 = Wide Chroma BPF BW 0 = Normal Chroma BPF BW	1
6	DEM	R/W	Reserved	1
5	PALSW	R/W	1 = PAL switch sensitivity low. 0 = PAL switch sensitivity normal.	0
4	SET7	R/W	1 = The black level is 7.5 IRE above the blank level. 0 = The black level is the same as the blank level.	0
3	COMB	R/W	1 = Adaptive comb filter for NTSC and PAL (recommended). Not for SECAM. 0 = Notch filter. For SECAM.	1
2	HCOMP	R/W	1 = operation mode 1. (recommended) 0 = mode 0.	1
1	YCOMB	R/W	1 = Bypass Comb filter when there is no burst presence 0 = No bypass	0
0	PDLY	R/W	PAL delay line. 0 = enabled. 1 = disabled.	0

0X84 – COLOR KILLER HYSTERESIS CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET

7	GMEN	R/W	Reserved.	0
6-5	CKHY	R/W	Color killer hysteresis. 0 – fastest 1 – fast 2 – medium 3 - slow	00b
4-0	HSDLY	RW	Reserved for test.	00h

0X85 – VERTICAL SHARPNESS

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	SHCOR	R/W	These bits provide coring function for the sharpness control.	8
3-0	Reserved	R	Reserved	0

0X86 – CORING CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	CTCOR	R/W	These bits control the coring for CTI.	1
5-4	CCOR	R/W	These bits control the low level coring function for the Cb/Cr output.	0
3-2	VCOR	R/W	These bits control the coring function of vertical peaking.	1
1-0	CIF	R/W	These bits control the chrominance IF compensation level. 0 = None 1 = 1.5dB 2 = 3dB 3 = 6dB	0

0X87 – CLAMPING GAIN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	CLPEND	R/W	These 4 bits set the end time of the clamping pulse. Its value should be larger than the value of CLPST.	5
3-0	CLPST	R/W	These 4 bits set the start time of the clamping. It is referenced to PCLAMP position.	0

0X88 – INDIVIDUAL AGC GAIN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	NMGAIN	R/W	The normal AGC loop gain control. Larger value reduce the loop response time.	2
3-1	WPGAIN	R/W	Peak AGC loop gain control.	1
0	Reserved	R	Reserved	0

0X8A – WHITE PEAK THRESHOLD

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	PEAKWT	R/W	These bits control the white peak detection threshold. Setting 'FF' disables this function.	D8

0X8B– CLAMP LEVEL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CLMPLD	R/W	0 = Clamping level is set by CLMPL. 1 = Clamping level preset at 60d.	1
6-0	CLMPL	R/W	These bits determine the clamping level of the Y channel.	3C

0X8C– SYNC AMPLITUDE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	SYNCTD	R/W	0 = Reference sync amplitude is set by SYNCT. 1 = Reference sync amplitude is preset to 38h.	1
6-0	SYNCT	R/W	These bits determine the standard sync pulse amplitude for AGC reference.	38

0X8D – SYNC MISS COUNT REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	MISSCNT	R/W	These bits set the threshold for horizontal sync miss count threshold.	4
3-0	HSWIN	R/W	These bits determine the VCR mode detection threshold.	4

0X8E – CLAMP POSITION REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	PCLAMP	R/W	These bits set the clamping position from the internal PLL sync edge	38

0X8F – VERTICAL CONTROL I

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	VLCKI	R/W	Vertical lock in time. 0 = fastest 3 = slowest.	0
5-4	VLCKO	R/W	Vertical lock out time. 0 = fastest 3 = slowest.	0
3	VMODE	R/W	This bit controls the vertical detection window. 1 = search mode. 0 = vertical count down mode.	0
2	DETV	R/W	1 = recommended for special application only. 0 = Normal Vsync logic	0
1	AFLD	R/W	Auto field generation control 0 = Off 1 = On	0
0	VINT	R/W	Vertical integration time control. 1 = short 0 = normal	0

0X90 – VERTICAL CONTROL II

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-5	BSHT	R/W	Burst PLL center frequency control.	0
5-0	VSHT	R/W	Vsync output delay control in the increment of half line length.	00

0X91 – COLOR KILLER LEVEL CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	CKILMAX	R/W	These bits control the amount of color killer hysteresis. The hysteresis amount is proportional to the value.	1
5-0	CKILMIN	R/W	These bits control the color killer threshold. Larger value gives lower killer level.	38

0X92 – COMB FILTER CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	HTL	R/W	0 = adaptive mode 1 = fixed comb	0
6-4	HTL	R/W	Adaptive Comb filter threshold control 1.	4
3-0	VTL	R/W	Adaptive Comb filter threshold control 2.	4

0X93 – LUMA DELAY AND H FILTER CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CKLM	R/W	Color Killer mode. 0 = normal 1 = fast (for special application)	0
6-4	YDLY	R/W	Luma delay fine adjustment. This 2's complement number provides –4 to +3 unit delay control.	3
3-0	HPF_RES	R/W	REV_ID=3 TW2864 only. Eh is recommended. Audio ADC High Pass Filter Resistance Control	Dh

0X94 – MISCELLANEOUS CONTROL I

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	HPLC	R/W	Reserved for internal use.	0
6	EVCNT	R/W	1 = Even field counter in special mode. 0 = Normal operation	0
5	PALC	R/W	Reserved for future use.	0
4	SDET	R/W	ID detection sensitivity. A '1' is recommended.	1
3	TBC_EN	R/W	1 = Internal TBC enabled. Total pixel per line on Video active line is always 858x2 for NTSC/PAL-M(60Hz) and 864x2 for PAL/SECAM(50Hz). 0 = TBC off.	0
2	BYPASS	R/W	It controls the standard detection and should be set to '1' in normal use.	1
1	SYOUT	R/W	1 = Hsync output is disabled when video loss is detected 0 = Hsync output is always enabled	0
0	Reserved	R	Reserved	0

0X95 – LOOP CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	HPM	R/W	Horizontal PLL acquisition time. 3 = Fast 2 = Auto1 1 = Auto2 0 = Normal	2
5-4	ACCT	R/W	ACC time constant 0 = No ACC 1 = slow 2 = medium 3 = fast	2
3-2	SPM	R/W	Burst PLL control. 0 = Slowest 1 = Slow 2 = Fast 3 = Fastest	1
1-0	CBW	R/W	Chroma low pass filter bandwidth control. Refer to filter curves.	1

0X96 – MISCELLANEOUS CONTROL II

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	NKILL	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL	R/W	0 = Normal output 1 = special output mode.	0
3	FCS	R/W	1 = Force decoder output value determined by CCS. 0 = Disabled.	0
2	LCS	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled.	0
1	CCS	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0X97 – CLAMP MODE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	FRM	R/W	Free run mode control 0 = Auto 2 = default to 60Hz 3 = default to 50Hz	0
5-4	YNR	R/W	Y HF noise reduction 0 = None 1 = smallest 2 = small 3 = medium	0
3-2	CLMD	R/W	Clamping mode control. 0 = Sync top 1 = Auto 2 = Pedestal 3 = N/A	1
1-0	PSP	R/W	Slice level control 0 = low 1 = medium 2 = high	1

0X98 – HSLOWCTL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R/W		0
6-4	HSBEGIN[2:0]	R/W	HSYNC Start position Control Bit2-0.	00
3	Reserved	R/W		0
2-0	HSEND[2:0]	R/W	HSYNC End position Control Bit2-0.	00

0X99 – HSBEGIN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HSBEGIN[10:3]	R/W	HSYNC Start position Control Bit10-3.	28

0X9A – HSEND

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HSEND[10:3]	R/W	HSYNC End position Control Bit10-3.	44

0X9B – OVSDLY

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	OVSDLY	R/W	VSYNC Start position. Control H position on VSYNC start.	44

0X9C – OVSEND

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	HASYNC	R/W	1:the length of EAV to SAV is set up and fixed by HBLEN registers. 0:the length of SAV to EAV is set up and fixed by HACTIVE registers.	0
6-4	OFDLY	R/W	FIELD output delay. 0h:0H line delay FIELD output.(601 mode only) 1h-6h: 1H-6H line delay FIELD output. 7h:Reserved.	2
3	VSMODE	R/W	1:VSYNC output is HACTIVE-VSYNC mode. 0:VSYNC output is HSYNC-VSYNC mode.	0
2-0	OVSEND	R/W	Line delay for VSYNC end position.	0

0X9D – HBLEN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HBLEN	R/W	These bits are effective when HASYNC bit is set to 1. These bits set up the length of EAV to SAV code when HASYNC bit is 1.Normal value is (Total pixel per line – HACTIVE) value. NTSC/PAL-M(60Hz): 8Ah(138dec)=858-720 PAL/SECAM(50Hz): 90h(144dec)=864-720 If Reg0x0E[3](ATRIG for CH1) is set to 0,this value changes into 8Ah or 90h at auto video format detection initial time automatically according to CH1 video detection status.	90h

0X9E – NOVID

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R	Reserved	0
6	FC27	R/W	1:normal ITU-R656 operation 0:Squared Pixel mode.	1
5-4	CHID_MD	R/W	Select the Channel ID format for time-multiplexed output 0 No channel ID (default) 1 CHID with the specific ITU-R BT.656 sync Code 2 CHID with the specific horizontal blanking code 3 CHID with the specific ITU-R BT.656 sync & horizontal blanking code	0
3	NOVID_656	R/W	0:Normal ITU-R BT.656 SA/EAV(default) 1:AN optional set of ITU-R BT.656 SAV/EAV code for No-video status	0
2	EAVSWAP	R/W	1:EAV-SAV code is swapped. 0:EAV-SAV code is not swapped(standard 656 output mode)	0
1	VIPCFG	R/W	Set up Bit7 in 4th byte of EAV/SAV code. 1:Standard ITU-R656 code format.(It's also VIP task-A code format.) 0:Old VIP task-B code format.	1
0	NTSC656	R/W	1:Number of Even Field Video output line is (the number of Odd field Video output line – 1).This bit is required for ITU-R BT.656 output for 525 line system standard. 0: Number of Even Field Video output line is same as the number of Odd field Video output line.	0

Index	Clock Output Delay Control							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x9F	CLKN_DEL				CLKP_DEL			

*) CLKN_POL/CLKP_POL controls have more better&easy clock margin adjustment.Use CLKN_POL/CLKP_POL at first normally,especially for 27MHz/54MHz data output application.CLKN_DEL/CLKP_DEL are sometimes required for 108MHz data output interface. CLKN_DEL/CLKP_DEL are not required for 27MHz/54MHz data output in most cases.

CLKN_DEL Control the clock delay of CLKNO pin.
0h/1h/3h/7h/Fh values are effective..The default value is "0".
[REV_ID=0 TW2864]
1h:about 0.3ns more delay, 3h:about 0.6ns more delay,
7h:about 1.0ns more delay, Fh:about 1.3ns more delay
[REV_ID>=1 TW2864]
1h:about 2ns more delay, 3h:about 4ns more delay,
7h:about 6ns more delay, Fh:about 7ns more delay

CLKP_DEL Control the clock delay of CLKPO pin.
0h/1h/3h/7h/Fh values are effective. The default value is "0".
[REV_ID=0 TW2864]
1h:about 0.3ns more delay, 3h:about 0.6ns more delay,
7h:about 1.0ns more delay, Fh:about 1.3ns more delay
[REV_ID>=1 TW2864]
1h:about 2ns more delay, 3h:about 4ns more delay,
7h:about 6ns more delay, Fh:about 7ns more delay

Index	Horizontal Scaler Pre-filter Control							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xA8	HFLT2				HFLT1			
0xA9	HFLT4				HFLT3			

HFLT Pre-filter selection for Video CH1/CH2/CH3/CH4 horizontal scaler
If HSCALE[11-8]=1,HFLT [3:0] controls the peaking function.
If HSCALE[11-8]>1,HFLT [2:0] function is bellow.
1** = Bypass
000 = Auto selection based on Horizontal scaling ratio. (default)
001 = Recommended for CIF size image
010 = Recommended for QCIF size image
011 = Recommended for ICON size image

Index	Video AGC Control							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xAA	AGCEN4	AGCEN3	AGCEN2	AGCEN1	AGCGAIN4[8]	AGCGAIN3[8]	AGCGAIN2[8]	AGCGAIN1[8]
0xAB	AGCGAIN1[7:0]							
0xAC	AGCGAIN2[7:0]							
0xAD	AGCGAIN3[7:0]							
0xAE	AGCGAIN4[7:0]							

AGCEN Select Video AGC loop function on AIN1 ~ AIN4.

0 AGC loop function enabled.(recommended for most application cases)
[REV_ID>=1 TW2864] default.

1 AGC loop function disabled. Gain is set by AGCGAIN1~4
[REV_ID=0 TW2864] default

AGCGAIN These registers control the AGC gain when AGC loop is disabled.
Default value is 0F0h.

Index	Vertical Peaking Level Control							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xAF	0	VSHP2			0	VSHP1		
0xB0	0	VSHP4			0	VSHP3		

VSHP Select Video Vertical peaking level. (*)

0 none. (default)

7 highest

*Note: VSHP must be set to '0' if Reg0x83 COMB = 0.

Index	CLK Output Current Control							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xB1	0	0	NOVIDMODE		CLKN2OEB	CLKN1OEB	CLKP2OEB	CLKP1OEB

[REV_ID=0 TW2864] These functions don't exist.These bits are always 0.
[REV_ID>=1 TW2864 only]

NOVIDMODE Select NOVID_656 output mode status.When NOVID_656 is set to 1,
NOVID_656 code is being output when following status is active in Video Decoding logic.
0 Video lost(vdloss).(default)
1 No Video(novideo)
2 Video lost or No video(vdloss or novideo)
3 NOVID_656 code is not being output at anytime.

CLKN2OEB Control 4mA drive current on CLKN output.
0 4mA drive enable.
1 4mA drive disable.(default)

CLKN1OEB Control 8mA drive current on CLKN output.
0 8mA drive enable. (default)
1 8mA drive disable.

CLKP2OEB Control 4mA drive current on CLKP output.
0 4mA drive enable.
1 4mA drive disable.(default)

CLKP1OEB Control 8mA drive current on CLKP output.
0 8mA drive enable. (default)
1 8mA drive disable.

Index	Audio ADC Digital Input Offset Control							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xB3	AADC4OFS[9:8]		AADC3OFS[9:8]		AADC2OFS[9:8]		AADC1OFS[9:8]	
0xB4	AADC1OFS[7:0]							
0xB5	AADC2OFS[7:0]							
0xB6	AADC3OFS[7:0]							
0xB7	AADC4OFS[7:0]							

[REV_ID=0 TW2864] These functions don't exist.These bits are always 0.

[REV_ID>=1 TW2864]

Digital ADC input data offset control.Digital ADC input data is adjusted by

ADJAADCn = AUDnADC + AADCnOFS.

AUDnADC is 2's formatted Analog Audio ADC output.

AADCnOFS is adjusted offset value by 2's format.

Index	Analog Audio ADC Digital Output Value							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xB8	AUD4ADC[9:8]		AUD3ADC[9:8]		AUD2ADC[9:8]		AUD1ADC[9:8]	
0xB9	AUD1ADC[7:0]							
0xBA	AUD2ADC[7:0]							
0xBB	AUD3ADC[7:0]							
0xBC	AUD4ADC[7:0]							

[REV_ID=0 TW2864] These functions don't exist.These bits are always 0.

[REV_ID>=1 TW2864] These bits are read only.

AUDnADC shows current Analog Audio n ADC Digital Output Value by 2's fomat.

Index	Adjusted Analog Audio ADC Digital Input Value							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xBD	ADJAADC4[9:8]		ADJAADC3[9:8]		ADJAADC2[9:8]		ADJAADC1[9:8]	
0xBE	ADJAADC1[7:0]							
0xBF	ADJAADC2[7:0]							
0xC0	ADJAADC3[7:0]							
0xC1	ADJAADC4[7:0]							

[REV_ID=0 TW2864] These functions don't exist.These bits are always 0.

[REV_ID>=1 TW2864] These bits are read only.

ADJAADCn shows current adjusted Audio ADC Digital input data value by 2's format.These value show the first input data value in front of Digital Audio Decimation Filtering process.

Index	MPP Pin Output Mode Control							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xC8	GPP_VAL2	MPP_MODE2			GPP_VAL1	MPP_MODE1		
0xC9	GPP_VAL4	MPP_MODE4			GPP_VAL3	MPP_MODE3		

GPP_VAL

Select the general purpose value through the MPP pin

0 "0" value (default)

1 "1" value

MPP_MODE

Select the output mode for MPP pins.Followings show the status when eash POLMPP1-4 register are set to 0. If each POLMPP1-4 register is set to 1,following values have inversed status.

0 Horizontal sync output.Low is H-sync active. (default)

1 Vertical sync output.Low is V-sync active.

2 Field flag output.Low is field1(Odd),High is field2(Even).

3 Horizontal active signal output.High is H-active.

4 Vertical active & horizontal active signal output.High is VH-active.

5 No video flag.High is No-video,Low is Video.

6 Digital serial audio mixing data same as ADATM pin

7 GPP_VAL.Same as GPP_VAL4-1 register value.

Index	Video Channel Output Control							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xCA	CHMD4		CHMD3		CHMD2		CHMD1	

CHMD

Select video bus output mode on 8bit VD1/VD2/VD3/VD4 pins.

0 Single Channel ITU-R BT.656 format output (default)

1 Two Channel ITU-R BT.656 Time-multiplexed format output

2 Four Channel ITU-R BT.656 Time-multiplexed format output

Index	Four Channel CIF Time-multiplxed Format							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xCB	POLMPP4	POLMPP3	POLMPP2	POLMPP1	CIF_54M4	CIF_54M3	CIF_54M2	CIF_54M1

POLMPP

Select MPP1~4 pin output polarity

0 normal (default)

1 inverse polarity

CIF_54M

Enable four channel CIF time-multiplexed format with 54MHz

CIF_54M1~4 stands for CH1 to CH4.

When CHMD4/CHMD3/CHMD2/CHMD1 registers have 0h or 1h,this function is effective on all Video ports.

When CHMD4/CHMD3/CHMD2/CHMD1 registers have 2h value,all video ports are always four channel D1 Time-division-multiplexed Format with 108MHz.

0 output format is controlled by CHMD4/CHMD3/CHMD2/CHMD1 registers and it's not four channel CIF time-multiplexed format with 54MHz.(default)

1 Four channel CIF time-multiplexed format with 54MHz

[REV_ID=0 TW2864]

CIF_54M4=1;CIF_54M3=1;CIF_54M2=1;CIF_54M1=1;

Bit3-0 must be set to Fh in this mode.

[REV_ID>=1 TW2864]

CIF_54M4=1 : Output this Four channel CIF time-multiplexed format on VD4[7:0] port.

CIF_54M3=1 : Output this Four channel CIF time-multiplexed format on VD3[7:0] port.

CIF_54M2=1 : Output this Four channel CIF time-multiplexed format on VD2[7:0] port.

CIF_54M1=1 : Output this Four channel CIF time-multiplexed format on VD1[7:0] port.

Index	2nd Channel Selection							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xCC	SELCH4		SELCH3		SELCH2		SELCH1	

SELCH4 Select 2nd video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD4 pin

0 CH1 video output (default)
1 CH2 video output
2 CH3 video output
3 CH4 video output

SELCH3 Select 2nd video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD3 pin

0 CH1 video output
1 CH2 video output
2 CH3 video output
3 CH4 video output (default)

SELCH2 Select 2nd video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD2 pin

0 CH1 video output
1 CH2 video output
2 CH3 video output (default)
3 CH4 video output

SELCH1 Select 2nd video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD1 pin

0 CH1 video output
1 CH2 video output (default)
2 CH3 video output
3 CH4 video output

Index	1st Channel Selection							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xCD	MAINCH4		MAINCH3		MAINCH2		MAINCH1	

MAINCH4 Select 1st video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD4 pin

0 CH1 video output
1 CH2 video output
2 CH3 video output
3 CH4 video output (default)

MAINCH3 Select 1st video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD3 pin

0 CH1 video output
1 CH2 video output
2 CH3 video output (default)
3 CH4 video output

MAINCH2 Select 1st video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD2 pin

0 CH1 video output
1 CH2 video output (default)
2 CH3 video output
3 CH4 video output

MAINCH1 Select 1st video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD1 pin

0 CH1 video output (default)
1 CH2 video output
2 CH3 video output
3 CH4 video output

Index	Analog Power Down							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xCE	AAUTOMUTE	HPF_RES	A_DAC_ PWDN	A_ADC_ PWDN	V_ADC_PWDN			

AAUTOMUTE

1. When input Analog data is less than ADET_TH level,output PCM data will be 0x0000(0x00).Audio DAC data input is 0x200. (REV_ID>=1 TW2864 only)

0 No effect.(default)

HPF_RES

Audio ADC High Pass Filter Resistance Selection.

0 20Kohm(default)

1 10Kohm

REV_ID=3 TW2864 doesn't have this function.Instead of this, HPF_RES[3:0] Reg0x93[3:0] is used.

A_DAC_PWDN

Power down the audio DAC.

0 Normal operation (default)

1 Power down

A_ADC_PWDN

Power down the audio ADC.

0 Normal operation (default)

1 Power down

V_ADC_PWDN

Power down the video ADC.

V_ADC_PWDN[3:0] stands for CH4 to CH1.

0 Normal operation (default)

1 Power down

Index	Serial Mode Control							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xCF	SMD		VRSTSEL		FIRSTCNUM			

SMD

Set up cascade Audio Serial mode.

When SMD=2hex or 3hex,ALINKO pin is output pin.When SMD=0hex or 1hex,ALINKO pin is input. TW2815 chip can be replaced with 54MHz clock-in TW2864B/TW2864D chip under SMD=0hex/1hex setting.

00 No Serial mode. ALINKO pin is test input mode.(default)

01 TW2815 Serial mode. IRQ pin is Serial out pin. ADATP pin is Serial input pin.

10 ALINKO pin is Serial out pin. ALINKI pin is Serial input pin.

VRSTSEL

Select VRST(V reset) signal on ACKG (Audio Clock Generator) refin input .

0 Ch1 VRST (default)

1 Ch2 VRST

2 Ch3 VRST

3 Ch4 VRST

FIRSTCNUM

This function is only effective in SMD=01h mode.

Set up 0h on Last(Bottom)Stage chip.

If 4 chip cascade mode,set up 3h on FirstStage/SecondStage/ThirdStage chips and 0h on LastStage chip.

If 3 chip cascade mode,set up 2h on FirstStage/SecondStage and 0h on ThirdStage chip.

If 2 chip cascade mode,set up 1h on FirstStage chip and 0h on SecondStage chip.

If single chip application mode, this register doesn't need to be set up.

0 (default)

Index	Analog Audio Input Gain							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD0	AIGAIN2				AIGAIN1			
0xD1	AIGAIN4				AIGAIN3			

AIGAIN Select the amplifier's gain for each analog audio input AIN1 ~ AIN4.

0 0.25
1 0.31
2 0.38
3 0.44(REV_ID=3 TW2864 default)
4 0.50
5 0.63
6 0.75
7 0.88
8 1.00 (REV_ID=0/1/2 TW2864 default)
9 1.25
10 1.50
11 1.75
12 2.00
13 2.25
14 2.50
15 2.75

REV_ID=0/1/2 TW2864 : Typical case setting is AIGAIN<=3.

REV_ID=3 TW2864 : Typical recommended value is AIGAIN=3.

8kHz/16kHz control range AIGAIN<=8
32kHz control range AIGAIN<=5
44.1kHz/48kHz control range AIGAIN<=3

Index	Number of Audio to be Recorded							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD2	M_RLSWAP	RM_SYNC	RM_PBSEL		0	R_ADATM	R_MULTCH	

M_RLSWAP Define the sequence of mixing and playback audio data on the ADATM pin.
If RM_SYNC=0 : I2S format
0 Mixing audio on position 0 and playback audio on position 8 (default)
1 Playback audio on position 0 and mixing audio on position 8
If RM_SYNC=1 : DSP format
0 Mixing audio on position 0 and playback audio on position 1 (default)
1 Playback audio on position 0 and mixing audio on position 1

RM_SYNC Define the digital serial audio data format for record and mixing audio on the ACLKR, ASYNR, ADATR and ADATM pin.
0 I2S format (default)
1 DSP format

RM_PBSEL Select the output PlayBackIn data for the ADATM pin.
0 First Stage PalyBackIn audio (default)
1 Second Stage PalyBackIn audio
2 Third Stage PalyBackIn audio
3 Last Stage PalyBackIn audio

R_ADATM Select the output mode for the ADATM pin.
0 Digital serial data of mixing audio (default)
1 Digital serial data of record audio

R_MULTCH Define the number of audio for record on the ADATR pin.
0 2 audios (default)
1 4 audios
2 8 audios
3 16 audios
Number of output data are limited as shown on Sequence of Multi-channel Audio Record table.Also,each output position data are selected by R_SEQ_0/R_SEQ_1/.../R_SEQ_F registers.

Index	Sequence of Audio to be Recorded							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD3	R_SEQ_1				R_SEQ_0			
0xD4	R_SEQ_3				R_SEQ_2			
0xD5	R_SEQ_5				R_SEQ_4			
0xD6	R_SEQ_7				R_SEQ_6			
0xD7	R_SEQ_9				R_SEQ_8			
0xD8	R_SEQ_B				R_SEQ_A			
0xD9	R_SEQ_D				R_SEQ_C			
0xDA	R_SEQ_F				R_SEQ_E			

R_SEQ

Define the sequence of record audio on the ADATR pin.

Refer to the Fig17 and Table5 for the detail of the R_SEQ_0 ~ R_SEQ_F.

The default value of R_SEQ_0 is “0”, R_SEQ_1 is “1”, ... and R_SEQ_F is “F”.

0 AIN1

1 AIN2

: :

: :

14 AIN15

15 AIN16

Index	Master Control							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xDB	ADACEN	AADCEN	PB_MASTER	PB_LRSEL	PB_SYNC	RM_8BIT	ASYNROEN	ACLKRMASTER

ADACEN Audio DAC Function mode

0 Audio DAC function disable(test purpose only)

1 Audio DAC function enable(default)

AADCEN Audio ADC Function mode

0 Audio ADC function disable(test purpose only)

1 Audio ADC function enable(default)

PB_MASTER Define the operation mode of the ACLKP and ASYNP pin for playback.

0 All type I2S/DSP Slave mode(ACLKP and ASYNP is input) (default)

1 TW2864 type I2S/DSP Master mode (ACLKP and ASYNP is output)

PB_LRSEL Select audio data to be used for playback input.

If PB_SYNC=0 I2S format,

0: 1st Left channel audio data (default), 1: 1st Right channel audio data.

If PB_SYNC=1 DSP format,

0 1st input audio data. 1: 2nd input audio data

PB_SYNC Define the digital serial audio data format for playback audio on the ACLKP, ASYNP and ADATP pin.

0 I2S format (default)

1 DSP format

RM_8BIT Define output data format per one word unit on ADATR pin.

0 16bit one word unit output(default)

1 8bit one word unit packed output

ASYNROEN Define input/output mode on the ASYNR pin.

1 ASYNR pin is input(default)

0 ASYNR pin is output

ACLKRMASTER Define input/output mode on the ACLKR pin and set up audio 256xfs system processing.

0 ACLKR pin is input.External 256xfs clock should be connected to ACLKR pin.(default)

1 ACLKR pin is output. Internal ACKG generates 256xfs clock.

Index	Mix Mute Control							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xDC	LAWMD		MIX_ DERATIO	MIX_MUTE				

LAWMD — Select u-Law/A-Law/PCM/SB data output format on ADATR and ADATM pin.

0 PCM output (default)

1 SB(Signed MSB bit in PCM data is inverted) output

2 u-Law output

3 A-Law output

MIX_DERATIO — Disable the mixing ratio value for all audio.

0 Apply individual mixing ratio value for each audio (default)

1 Apply nominal value for all audio commonly

MIX_MUTE — Enable the mute function for each audio. It effects only for mixing.

MIX_MUTE[0] : Audio input AIN1.

MIX_MUTE[1] : Audio input AIN2.

MIX_MUTE[2] : Audio input AIN3.

MIX_MUTE[3] : Audio input AIN4.

MIX_MUTE[4] : Playback audio input.

It effects only for single chip or the last stage chip

0 Normal (default)

1 Muted

Index	Mix Ratio Value							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xDD	MIX_RATIO2				MIX_RATIO1			
0xDE	MIX_RATIO4				MIX_RATIO3			
0xDF	AOGAIN				MIX_RATIOP			

MIX_RATIO Define the ratio values for audio mixing.

MIX_RATIO1 : Audio input AIN1.

MIX_RATIO2 : Audio input AIN2.

MIX_RATIO3 : Audio input AIN3.

MIX_RATIO4 : Audio input AIN4.

MIX_RATIOP : Playback audio input.

It effects only for single chip or the last stage chip.

0 0.25(Recommended for more than 4x AIN1/AIN2/AIN3/AIN4/PBIN)

1 0.31

2 0.38

3 0.44

4 0.50

5 0.63

6 0.75

7 0.88

8 1.00(default for REV_ID=0 TW2864)

9 1.25

10 1.50

11 1.75

12 2.00

13 2.25

14 2.50

15 2.75

REV_ID>=1 TW2864 default is 0.

Index	Analog Audio Output Gain							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xDF	AOGAIN				MIX_RATIOP			

AOGAIN Define the amplifier gain for analog audio output.

0 0.25
1 0.31
2 0.38
3 0.44
4 0.50
5 0.63
6 0.75
7 0.88
8 1.00 (default)
9 1.25
10 1.50
11 1.75
12 2.00
13 2.25
14 2.50
15 2.75

REV_ID=0/1/2 TW2864 : Typical case setting is AOGAIN<=8.

REV_ID=3 TW2864 : Typical recommended value is AOGAIN=8.
Control range AOGAIN<=13

Index	Mix Output Selection							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xE0	VADCCKPOL	AADCCKPOL	ADACCKPOL	MIX_OUTSEL				

VADCCKPOL Test purpose only. 0 (default)

AADCCKPOL 0 (default)

ADACCKPOL Test purpose only. 0 (default)

MIX_OUTSEL Define the final audio output for analog and digital mixing out.

0 Select record audio of channel 1
1 Select record audio of channel 2
2 Select record audio of channel 3
3 Select record audio of channel 4
4 Select record audio of channel 5
5 Select record audio of channel 6
6 Select record audio of channel 7
7 Select record audio of channel 8
8 Select record audio of channel 9
9 Select record audio of channel 10
10 Select record audio of channel 11
11 Select record audio of channel 12
12 Select record audio of channel 13
13 Select record audio of channel 14
14 Select record audio of channel 15
15 Select record audio of channel 16
16 Select playback audio of the first stage chip
17 Select playback audio of the second stage chip
18 Select playback audio of the third stage chip
19 Select playback audio of the last stage chip
20 Select mixed audio (default)
21 Test purpose only.

Index	Audio Detection Period							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xE1	AAMPMD	ADET_FILT			ADET_ TH4[4]	ADET_ TH3[4]	ADET_ TH2[4]	ADET_ TH1[4]

AAMPMD Define the audio detection method.

0 Detect audio if absolute amplitude is greater than threshold (default)

1 Detect audio if differential amplitude is greater than threshold

ADET_FILT Select the filter for audio detection

0 Wide LPF (default)

. .

. .

7 Narrow LPF

Index	Audio Detection Threshold							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xE1	AAMPMD	ADET_FILT			ADET_ TH4[4]	ADET_ TH3[4]	ADET_ TH2[4]	ADET_ TH1[4]
0xE2	ADET_TH2[3:0]				ADET_TH1[3:0]			
0xE3	ADET_TH4[3:0]				ADET_TH3[3:0]			

ADET_TH Define the threshold value for audio detection.

ADET_TH1 : Audio input AIN1.

ADET_TH2 : Audio input AIN2.

ADET_TH3 : Audio input AIN3.

ADET_TH4 : Audio input AIN4.

0 Low value (default)

. .

. .

31 High value

If fs=8kHz Audio Clock setting mode,

Reg0xE1=0xC0,Reg0xE2=0xAA,Reg0xE3=0xAA are typical setting value.

If fs=16kHz/32kHz/44.1kHz/48kHz Audio Clock setting mode,

Reg0xE1=0xE0,Reg0xE2=0xBB,Reg0xE3=0xBB are typical setting value.

Index	Audio Clock Increment							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xF0	ACKI[7:0]							
0xF1	ACKI[15:8]							
0xF2	0	0	ACKI[21:16]					

ACKI These bits control ACKI Clock Increment in ACKG block.
09B583h for fs = 8kHz is default

Index	Audio Clock Number							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xF3	ACKN[7:0]							
0xF4	ACKN[15:8]							
0xF5	0	0	0	0	0	0	ACKN[17:16]	

ACKN These bits control ACKN Clock Number in ACKG block..
[REV_ID=0 TW2864] 08578h for fs = 8kHz is default.
[REV_ID>=1 TW2864] 000100h for Playback Slave-in lock is default.

Index	Serial Clock Divider							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xF6	0	0	SDIV					

SDIV Reserved. 01h is default.

Index	Left/Right Clock Divider							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xF7	0	0	LRDIV					

LRDIV Reserved.20h is default.

[REV_ID=0 TW2864]

Index	Audio Clock Control							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xF8	0	APZ	APG		0	ACPL	SRPH	LRPH

[REV_ID>=1 TW2864]

Index	Audio Clock Control							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xF8	APZ	APG			0	ACPL	SRPH	LRPH

APZ These bits control Loop in ACKG block.
1 is default

APG These bits control Loop in ACKG block.
[REV_ID=0 TW2864] 2 is default
[REV_ID>=1 TW2864] 4 is default

ACPL These bits control Loop closed/open in ACKG block.
0 Loop closed(default)
1 Loop open(recommended on most application case)

SRPH Reserved.
0 (default)

LRPH Reserved.
0 (default)

Index	Video Miscellaneous Function Control							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xF9	LIM16	PBREFEN	YCBCR422	HA656MD	VBI_FRAM	CNTL656	VSCL_SYNC	HA_EN

LIM16 [REV_ID=0 TW2864] This function doesn't exist.This bit is always 0.
[REV_ID>=1 TW2864]
Output ranges are limited to 2~254(default)
Output ranges are limited to 16~235 for Y and 16~239 for CbCr

PBREFEN [REV_ID=0 TW2864] This function doesn't exist.This bit is always 0.
[REV_ID>=1 TW2864] Audio ACKG Reference(refin) input select
ACKG has video VRST refin input selected by VRSTSEL register
ACKG has audio ASYNP refin input.(default)

YCBCR422 Control YCbCr 4:2:2 output mode
0 Normal 4:2:2 output mode (default)
1 Averaging 4:2:2 output mode

HA656MD Control HACTIVE signal output on H-Down Scaling output mode.
0 HACTIVE signal is always HACTIVE register's length
(REV_ID=0 TW2864 default)
1 HACTIVE signal is same as DVALID signal in H-Down Scaled video output(TW2834 need 1).
(REV_ID>=1 TW2864 default)

VBI_FRAM Test purpose only. 0 default

CNTL656 Select invalid data value.
0 0x80 and 0x10 code will be output as invalid data during active video line(default)
1 0x00 code will be output as invalid data during active video line.

VSCL_SYNC Enable the optional ITU-R.656 sync code format.
0 Skip ITU-R BT.656 sync code for non-valid vertical line (default)
1 Standard ITU-R BT.656 sync code on any vertical line.

HA_EN Control HACTIVE output during vertical blanking period.
0 HACTIVE output is disabled during vertical blanking period
1 HACTIVE output is enabled during vertical blanking period (default)

Index	Clock Output Control							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xFA	VSCL_ENA	OE	CLKN_ OEB	CLKP_ OEB	CLKN_MD		CLKP_MD	

VSCL_ENA(REV_ID>=1 TW2864 only)

Enable the vertical scaler for 4x CIF time-multiplexed format with 54MHz.

0 Full size for vertical direction (default)

1 Half size for vertical direction

OE

Control the tri-state of output pin

0 Outputs are Tri-state except clock output (CLKPO, CLKNO) pin (default)

1 Outputs are enabled

CLKN_OEB

Control the tri-state of CLKNO pin

0 Output is enabled (default)

1 Output is Tri-state

CLKP_OEB

Control the tri-state of CLKPO pin

0 Output is enabled (default)

1 Output is Tri-state

CLKN_MD

CLKP_MD

Control the clock frequency of CLKNO/CLKPO pin

0 CLKI Input Freq / 4 Clock for TW2864A/TW2864C(default)
CLKI Input Freq / 2 Clock for TW2864B/TW2864D(default)

1 CLKI Input Freq / 2 Clock for TW2864A/TW2864C
CLKI Input Freq Clock for TW2864B/TW2864D

2 CLKI Input Freq Clock for TW2864A/TW2864B/TW2864C/TW2864D

3 always 0 value

[REV_ID>=1 TW2864 only]

If Single Channel Clock-In mode is selected,

0,1,2 CLKI Input Freq Clock for TW2864A/TW2864B/TW2864C/TW2864D

3 always 0 value

Index	Video and Audio Detection Mode							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xFB	CLKN_POL	CLKP_POL	IRQENA	IRQPOL	ADET_MODE		VDET_MODE	

CLKN_POL — Polarity inverse control on output CLKNO signal just before CLKNO pin.
- 0 not inversed. (default)
- 1 Polarity inverse. good for 27MHz/54MHz clock output.

CLKP_POL — Polarity inverse control on output CLKPO signal just before CLKPO pin.
- 0 not inversed. good for 27MHz/54MHz clock output.(default)
- 1 Polarity inverse.

IRQENA — Enable/Disable the interrupt request through the IRQ pin.
- 0 Disable (default)
- 1 Enable

IRQPOL — Select the polarity of interrupt request through the IRQ pin.
- 0 Falling edge requests the interrupt and keeps its state until cleared (default)
- 1 Rising edge requests the interrupt and keeps its state until cleared

ADET_MODE — Define the polarity of state register and interrupt request for audio detection.
- 0 No interrupt request by the audio detection
- 1 Make the interrupt request rising only when the audio signal comes in
- 2 Make the interrupt request falling only when the audio signal goes out
- 3 Make the interrupt request rising and falling when the audio comes in and goes out (default)

VDET_MODE — Define the polarity of state register and interrupt request for video detection.
- 0 No interrupt request by the video detection
- 1 Make the interrupt request rising only when the video signal comes in
- 2 Make the interrupt request falling only when the video signal goes out
- 3 Make the interrupt request rising and falling when the video comes in and goes out (default)

Index	Enable Video and Audio Detection							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xFC	AVDET_ENA							

AVDET_ENA Enable state register updating and interrupt request of video and audio detection for each input.

[0] : Video input VIN1.

[1] : Video input VIN2.

[2] : Video input VIN3.

[3] : Video input VIN4.

[4] : Audio input AIN1.

[5] : Audio input AIN2.

[6] : Audio input AIN3.

[7] : Audio input AIN4.

0 Disable state register updating and interrupt request

1 Enable state register updating and interrupt request (default)

Index	State of Video and Audio Detection							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xFD	AVDET_STATE							

AVDET_STATE

State of Video and Audio detection.

These bit is activated according VDET_MODE and ADET_MODE.

[0] : Video input VIN1.

[1] : Video input VIN2.

[2] : Video input VIN3.

[3] : Video input VIN4.

[4] : Audio input AIN1.

[5] : Audio input AIN2.

[6] : Audio input AIN3.

[7] : Audio input AIN4.

0 Inactivated

1 Activated

Index	Device and Revision ID Flag							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xFE	DEV_ID*[6:5]		0	0	0	TEST		
0xFF	DEV_ID*[4:0]					REV_ID*		

TEST

Test purpose only. This must be 0 in normal mode. default is 0.

DEV_ID

The TW2864 product ID code.*(Read only)*

All REV_ID=3'h0 chips have DEV_ID=7'h06.

REV_ID=1/2

108MHz clock-in TW2864A/TW2864C : DEV_ID=7'h0C.

54MHz clock-in TW2864B/TW2864D : DEV_ID=7'h0D.

REV_ID=3

TW2864A : DEV_ID=7'h0C. TW2864B : DEV_ID=7'h0D.

TW2864C : DEV_ID=7'h0E. TW2864D : DEV_ID=7'h0F.

REV_ID

The revision number. *(Read only)*

REV_ID=3'h0 1st TW2864A/ TW2864B/ TW2864C/ TW2864D

REV_ID=3'h1 2nd TW2864A/ TW2864B/ TW2864C/ TW2864D

REV_ID=3'h2 3rd TW2864A/ TW2864B/ TW2864C/ TW2864D

REV_ID=3'h3 4th TW2864A/ TW2864B/ TW2864C/ TW2864D

REV_ID=3 TW2864 Test Purpose

Index	Test Registers							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x73	0	0	0	0	0	0	0	0
0x7B	0	0	0	1	0	1	0	1
0x7C	0	0	0	1	0	1	0	1
0x7E	1	0	1	0	0	0	1	1

These registers are test purpose only.Above register 0x7B 0x7C 0x7E default values need to be set up on normal mode.Register0x73[0] need to be set up 0 if IRQ signal output is needed with Video/Audio detection.Register0x73 default is 01h.

Index	CKIMD Registers							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x89	0	0	0	0	0	0	CKIMD	

Reserved bits must have above 0 values.

CKIMD CLKI pin Clock Input mode.

0: 27MHz Clock Input.

1: 54MHz Clock Input.(TW2864B/TW2864D default)

2: 108MHz Clock Input.(TW2864A/TW2864C default)

3: All Clock off mode except register block.All functions are in power down mode except register block.

REV_ID=3 TW2864 Recommended Setting

Following register need to be set up after RSTB pin changes into 1 in typical system.

HPF_RES[3:0]=Eh.

If Audio 8kHz mode,AADCCKPOL=1.

If Audio 16kHz/32kHz/44.1kHz/48kHz mode,AADCCKPOL=0(default).

TW2864 REV_ID=2(LC2) and REV_ID=3(LD1) Register difference

	Default Value		Recommended Value for software compatible.
	REV_ID=2	REV_ID=3	
Reg0x82	0x10	0x00	Both 0x00
Reg0x93	0x30	0x3D	Both 0x3E,REV_ID=2 doesn't have bit3-0.
Reg0xCE	0x00	0x00	Both 0x40,Bit6 is REV_ID=2 only function.
Reg0xD0	0x88	0x33	Both 0x33
Reg0xD1	0x88	0x33	Both 0x33

DEV_ID and REV_ID are different between REV_ID=2 and REV_ID=3.

Reg0xFF Value:

	REV_ID=2	REV_ID=3
TW2864A	0x62	0x63
TW2864B	0x6A	0x6B
TW2864C	0x62	0x73
TW2864D	0x6A	0x7B

Electrical Specifications

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
VDDV (Measured to VSSV)	VDD_{VM}	-0.5		2.3	V
VDDA (Measured to VSSA)	VDD_{AM}	-0.5		2.3	V
VDDI (Measured to VSS)	VDD_{IM}	-0.5		2.3	V
VDDO (Measured to VSS)	VDD_{OM}	-0.5		4.5	V
Digital Input/Output Voltage	-	–0.5		4.5	V
Analog Input Voltage	-	–0.5		2.0	V
Storage Temperature	T_S	–65		150	°C
Junction Temperature	T_J	0		125	°C
Reflow Soldering (10-30 Seconds)	T_{PEAK}			255-260	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
VDDV (Measured to VSSV)	VDD_V	1.62	1.8	1.98	V
VDDA (Measured to VSSA)	VDD_A	1.62	1.8	1.98	V
VDDI (Measured to VSS)	VDD_I	1.62	1.8	1.98	V
VDDO (Measured to VSS)	VDD_O	3.0	3.3	3.6	V
Analog Input Voltage (AC Coupling Required)	V_{AIN}	0.5	1.0	1.35	V
Ambient Operating Temperature	T_A	-40		85	°C

DC Electrical Parameters

PARAMETER	SYMBOL (NOTE 1)	MIN	TYP	MAX (NOTE 1)	UNITS
DIGITAL INPUTS					
Input High Voltage (TTL)	V_{IH}	2.0		5.5	V
Input Low Voltage (TTL)	V_{IL}	-0.3		0.8	V
Input Leakage Current (@V_I = 2.5V or 0V)	I_L			±10	µA
Input Capacitance	C_{IN}		6		pF
DIGITAL OUTPUTS					
Output High Voltage	V_{OH}	2.4			V
Output Low Voltage	V_{OL}			0.4	V
High Level Output Current (@V_{OH} = 2.4V)	I_{OH}	6.3	12.8	21.2	mA
Low Level Output Current (@V_{OL} = 0.4V)	I_{OL}	4.9	7.4	9.8	mA
Tri-state Output Leakage Current (@V_O = 2.5V or 0V)	I_{OZ}			±10	µA
Output Capacitance	C_O		6		pF
Analog Pin Input Capacitance	C_A		6		pF
SUPPLY CURRENT					
Analog Video Supply Current (VDDV, 1.8V)	I_{DDV}		44		mA
Analog Audio Supply Current (VDDA, 1.8V)	I_{DDA}		16		mA
Digital Internal Supply Current (VDDI, 1.8V)	I_{DDI}		110		mA
Digital I/O Supply Current (VDDO, 3.3V)	I_{DDO}		25		mA
Total Power Dissipation	P		388.5		mW

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

AC Electrical Parameters

CLKI AND VIDEO DATA/SYNC TIMING

PARAMETER	SYMBOL	MIN (NOTE 1)	TYP	MAX (NOTE 1)	UNITS
Delay from CLKI to CLKPO (27MHz)	1	1		5	Ns
Hold from CLKPO to Video Data/Sync (27MHz)	2a	18			Ns
Delay from CLKPO to Video Data/Sync (27MHz)	2b			19	Ns
Delay from CLKI to CLKPO (54MHz)	3	0.1		5	Ns
Hold from CLKPO to Video Data/Sync (54MHz)	4a	9			Ns
Delay from CLKPO to Video Data/Sync (54MHz)	4b			10	Ns
Delay from CLKI to CLKPO (108MHz)	5	3			Ns
Hold from CLKPO to Video Data/Sync (108MHz)	6a	5			Ns
Delay from CLKPO to Video Data/Sync (108MHz)	6b			6	Ns

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
2. CLKPO timing is related with CLKP_DEL register value. The following timing diagram is illustrated in the case that the CLKP_DEL is set to 0hex and CLKP_POL is se to 0.
   CLKNO timing is almost inversed CLKPO timing as default setting.

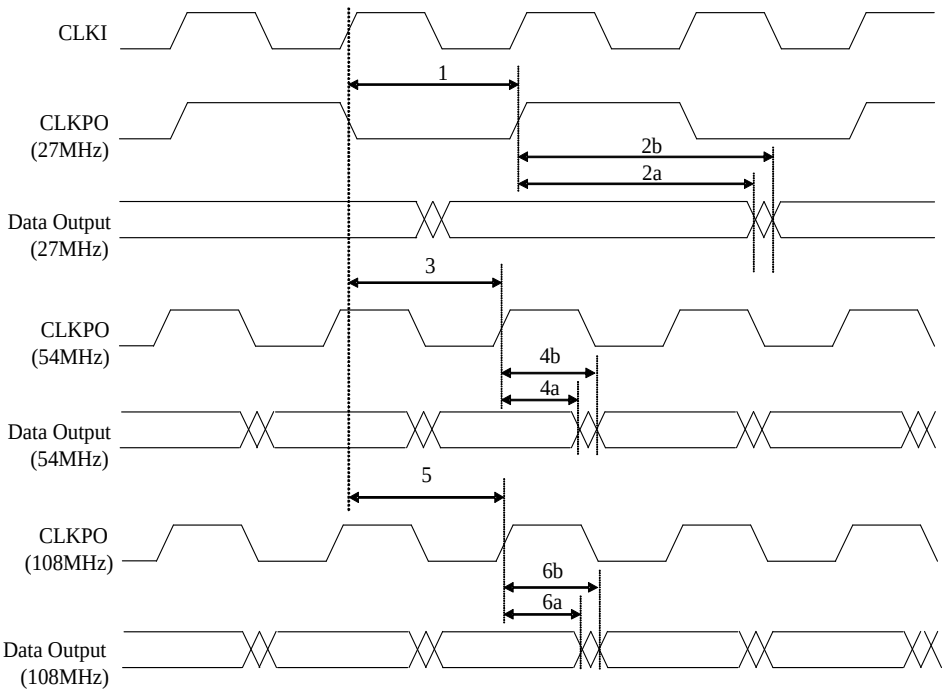


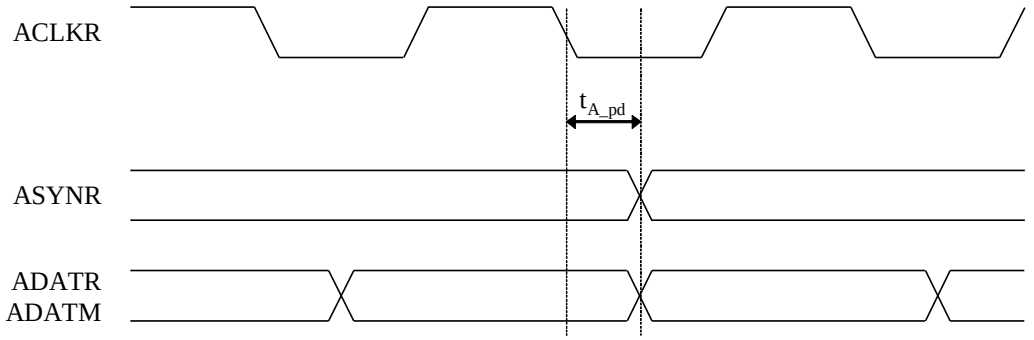
FIGURE 39. CLKI AND VIDEO DATA TIMING DIAGRAM

DIGITAL SERIAL AUDIO INTERFACE TIMING

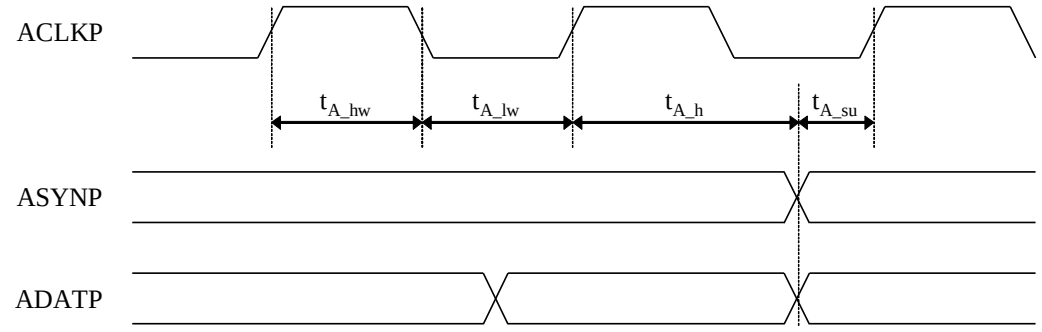
PARAMETER	SYMBOL	MIN (NOTE 1)	TYP	MAX (NOTE 1)	UNITS
ASYNR, ADATR, ADATM Propagation Delay	T_{A_pd}	0.6		2	ns
ACLKP High Pulse Duration	T_{A_hw}	37			ns
ACLKP Low Pulse Duration	T_{A_lw}	74			ns
ASYNP, ADATP Setup Time	T_{A_su}	36			ns
ASYNP, ADATP Hold Time	T_{A_h}	35			ns

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
2. T_{A_lw} Min value and T_{A_su} Min value are Fs = 48KHz mode only. If Fs < 48KHz, these Min values are more bigger. High period of ACLKR/ACLKP is 27MHz one clock period.



(a) Record and Mix Audio(Master mode)



(b) Playback Audio(Master mode)

FIGURE 40. TIMING DIAGRAM OF DIGITAL SERIAL AUDIO INTERFACE

SERIAL HOST INTERFACE TIMING

PARAMETER	SYMBOL	MIN (NOTE 1)	TYP	MAX (NOTE 1)	UNITS
Bus Free Time between STOP and START	t_{BF}	740			ns
SDAT Setup Time	t_{sSDAT}	100			ns
SDAT Hold Time	t_{hSDAT}	50			ns
Setup Time for START Condition	t_{sSTA}	370			ns
Setup Time for STOP Condition	t_{sSTOP}	370			ns
Hold Time for START Condition	t_{hSTA}	74			ns
Rise Time for SCLK and SDAT	t_R			300	ns
Fall Time for SCLK and SDAT	t_F			300	ns
Capacitive Load for Each Bus Line	C_{BUS}			400	pF
LOW Period of SCL	t_{LOW}	0.5			µs
HIGH Period of SCL	t_{HIGH}	0.5			µs
SCLK Clock Frequency	f_{SCLK}			400	KHz

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

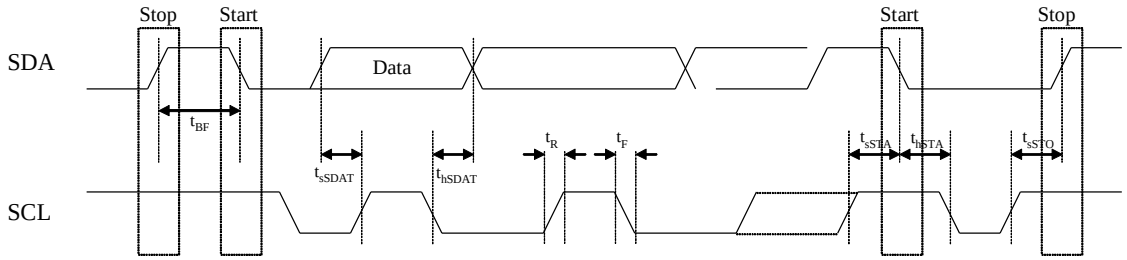


FIGURE 41. SERIAL HOST INTERFACE TIMING

This Serial Host Interface is also supporting old µs (MicroSecond) unit timing chip's Serial Host Interface by more higher speed logic design.

All REV_ID chips have an equal Serial Host Interface timing.

Video Decoder Parameter 1

PARAMETER	SYMBOL	MIN (NOTE 1)	TYP	MAX (NOTE 1)	UNITS
ADCS					
ADC Resolution	ADCR		10		Bits
ADC Integral Non-linearity	AINL		±1		LSB
ADC Differential Non-Linearity	ADNL		±1		LSB
ADC Clock Rate	f_{ADC}	24	27	30	MHz
Video Bandwidth (-3db)	BW		10		MHz
HORIZONTAL PLL					
Line Frequency (50Hz)	f_{LN}		15.625		KHz
Line Frequency (60Hz)	f_{LN}		15.734		KHz
Static Deviation	Δf_H			6.2	%
SUBCARRIER PLL					
Subcarrier Frequency (NTSC-M)	f_{SC}		3579545		Hz
Subcarrier Frequency (PAL-BDGHI)	f_{SC}		4433619		Hz
Subcarrier Frequency (PAL-M)	f_{SC}		3575612		Hz
Subcarrier Frequency (PAL-N)	f_{SC}		3582056		Hz
Lock In Range	Δf_H	±450			Hz
OSCILLATOR INPUT					
Nominal Frequency			27		MHz
Deviation				±50	ppm
Duty Cycle				55	%

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Video Decoder Parameter 2

PARAMETER	SYMBOL	MIN (NOTE 1)	TYP	MAX (NOTE 1)	UNITS
LOCK SPECIFICATION					
Sync Amplitude Range		1		200	%
Color Burst Range		5		200	%
Horizontal Lock Range		-5		5	%
Vertical Lock Range		45		65	Hz
Fsc Lock Range			±700		Hz
Color Burst Position Range			±2.2		μs
Color Burst Width Range		1			cycle
VIDEO BANDWIDTH					
B/W			6		MHz
NOISE SPECIFICATION					
SNR (Luma Flat Field)			57		dB
NONLINEAR SPECIFICATION					
Y Nonlinearity			0.5	0.7	%
Differential Phase	DP		0.4	0.6	°
Differential Gain	DG		0.6	0.8	%
CHROMA SPECIFICATION					
Hue Accuracy			1		°
Chroma ACC Range				400	%
Chroma Amplitude Error			1		%
Chroma Phase Error			0.3		%
Chroma Luma Intermodulation			0.2		%
K-FACTOR					
K_{2T}			0.5		%
$K_{pulse/bar}$			0.5		%

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

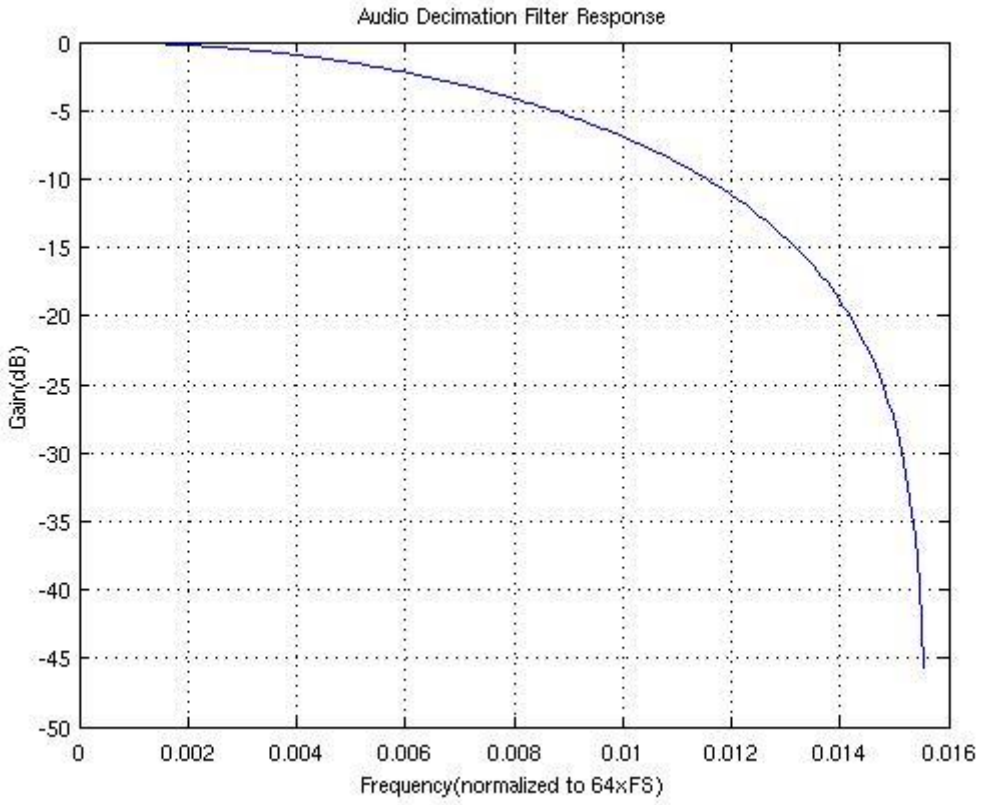
Analog Audio Parameters

PARAMETER	SYMBOL	MIN (NOTE 4)	TYP	MAX (NOTE 4)	UNITS
ANALOG AUDIO INPUT CHARACTERISTICS					
AIN1-4 Input Impedance	RINX	10			KΩ
Interchannel Gain Mismatch			0.2		dB
Input Voltage Range				1.5	Vpp
Full Scale Input Voltage (Note 1)	V_{IFULL}		1		Vpp
Interchannel Isolation (Note 2)			90		dB
ANALOG AUDIO OUTPUT CHARACTERISTICS					
AOUT Output Load Resistance	RLAO	300			ohm
AOUT Load Capacitance	CLAO			1	nF
AOUT Offset Voltage	VOSAO			100	mV
Full Scale Output Voltage (Note 3)	V_{OFULL}		1.4		Vpp

NOTE:

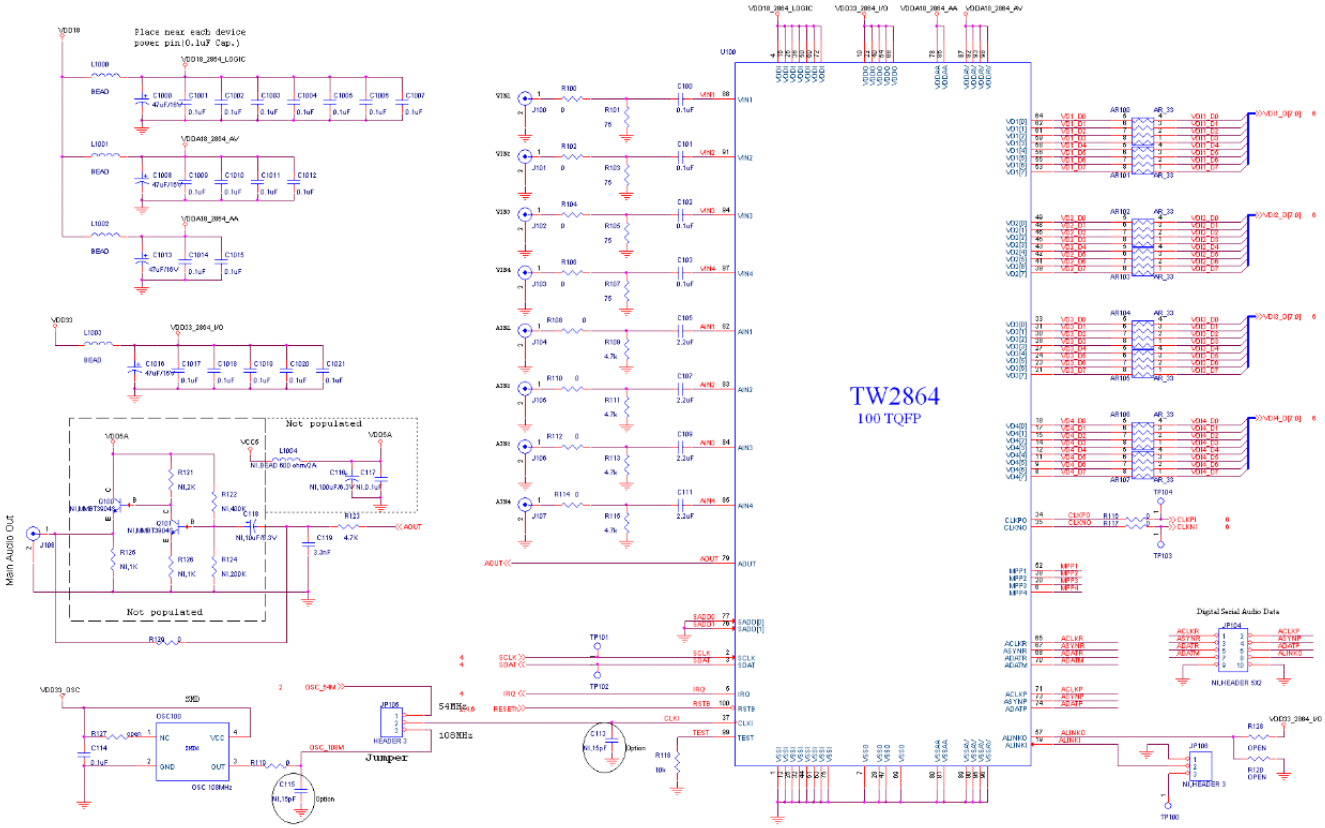
1. Tested at input gain of 0 dB, Fin = 1KHz.
2. Tested at input gain of 0 dB, Fs=8 KHz and 16KHz.
3. Tested at output gain of 0 dB, Fout = 1KHz.
4. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Audio Decimation Filter Response



(*) 0.016 line = 0.016x64xFs

Application Schematic

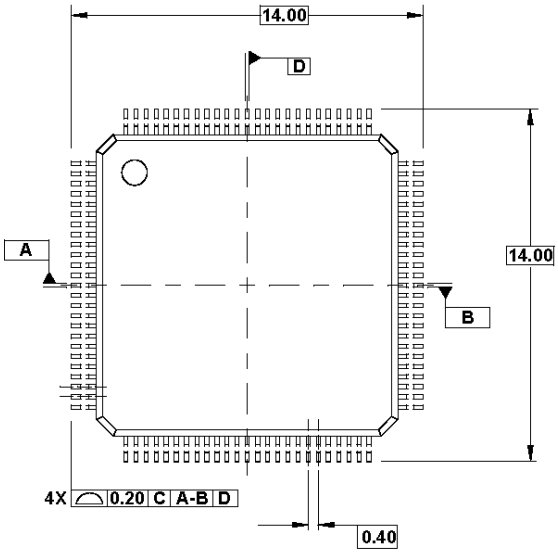


Package Outline Drawing

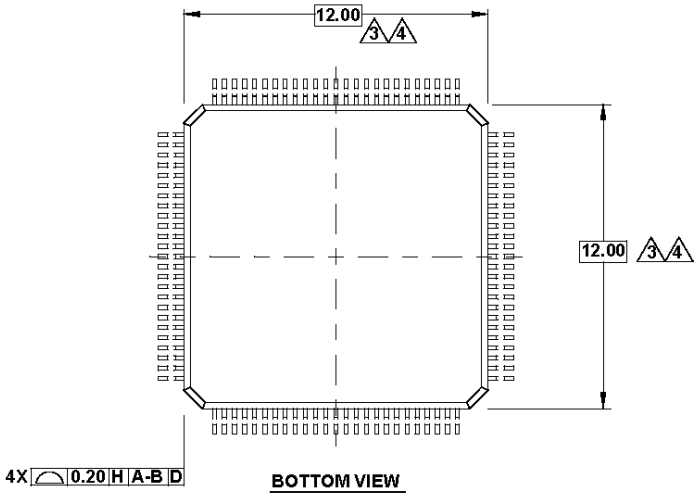
Q100.12X12

100 LEAD LOW PLASTIC QUAD FLATPACK PACKAGE (LQFP)

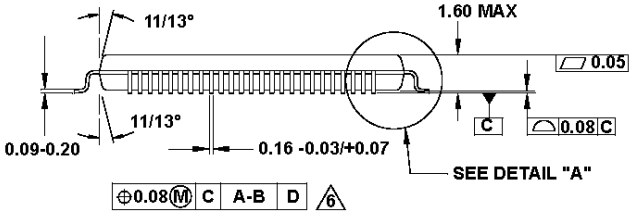
Rev 1, 6/11



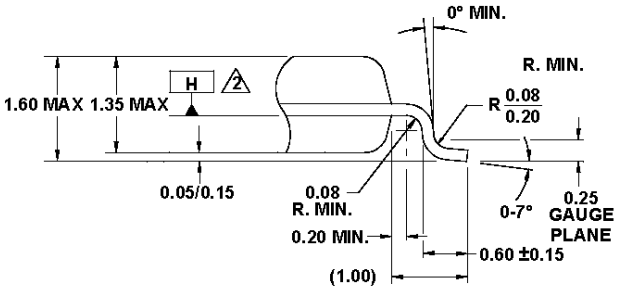
TOP VIEW



BOTTOM VIEW

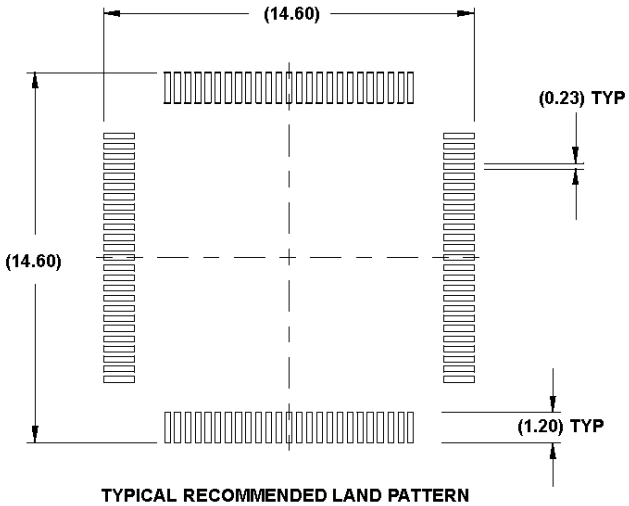


SIDE VIEW



DETAIL "A"

SCALE: NONE



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. All dimensioning and tolerancing conform to ANSI Y14.5-1982.
2. Datum plane H located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Dimensions do not include mold protrusion. Allowable mold protrusion is 0.25mm per side.
4. These dimensions to be determined at datum plane H.
5. Package top dimensions are smaller than bottom dimensions and top of package will not overhang bottom of package.
6. Dimension does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of the dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
7. Controlling dimension: millimeter.
8. This outline conforms to JEDEC publication 95 registration MS-026, variation ADE.
9. Dimensions in ( ) are for reference only.

Datasheet Revision History

VERSION	DATE	DESCRIPTION
FN7745.0	August 23, 2012	Initial release.

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