# THE DATASHEET OF

# TSI578-10GCLY

Integrated Device Technology

# IDT Serial RapidIO Switch Feature Comparison Chart

| FEATURES | RXS2448 | RXS1632 | CPS-1848 | CPS-1432 | CPS/SPS-1616 | CPS-8 | /10Q | / 16 | Tsi572 | / 574 | / 578 | Tsi577 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Performance and Configurability** | | | | | | | | | | | | |
| Serial RapidIO® specifications | 3.2 | 3.2 | 2.1 | 2.1 | 2.1 | 1.3 | 1.3 | 1.3 | 1.3 | 1.3 | 1.3 | 1.3 |
| Aggregate peak throughput (Gbps) | 600 | 400 | 240 | 160 | 80 | 20 | 100 | 40 | 30 | 40 | 80 | 40 |
| Maximum Port Throughput | 50 | 50 | 20 | 20 | 20 | 10 | 10 | 10 | 10 | 10 | 10 | 10 |
| Full mesh non-blocking fabric | √ | √ | √ | √ | √ | √ | | √ | √ | √ | √ | √ |
| Maximum of number of x4 ports | 12 | 8 | 12 | 8 | 4 | 2 | 10 | 4 | 2 | 4 | 8 | 4 |
| Maximum of number of x2 ports | 24 | 16 | 18 | 14 | 8 | | | | | | | |
| Maximum of number of x1 port | 24 | 16 | 18 | 14 | 16 | 8 | 16 | 16 | 8 | 8 | 16 | 16 |
| Cut-through latency (ns) | 100 | 100 | 100 | 100 | 100 | 190 | 190 | 190 | 110 | 110 | 110 | 110 |
| Store and forward mode | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ |
| Configurable by speed | Each Port | Each Port | Each Quad | Each Quad | CPS/SPS - Each Lane | Each Lane Pair | Each Quad | Each Lane Pair | Each MAC | | | Each Quad |
| **SerDes and Power** | | | | | | | | | | | | |
| Power per 10 Gbps link (typical, mW) | <250 | <250 | <300 | <385 | CPS/SPS <440 | <500 | | <500 | <500 | | | <500 |
| Per port power down | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ |
| Programmable transmit drive strength and pre-emphasis | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ |
| Programmable receive equalization | √ | √ | √ | √ | √ | | | | √ | √ | √ | √ |
| On-die scope capability | √ | √ | | | | | | | √ | √ | √ | √ |
| **Multicast and Routing** | | | | | | | | | | | | |
| Per port multicast architecture | √ | √ | √ | √ | √ | √ | √ | √ | | | | |
| Per port multicast masks/groups | 256 | 256 | 40 | 40 | 40 | 10 | 40 | 10 | 8 | 8 | 8 | 8 |
| 8- and 16-bit addressing | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ |
| 32-bit addressing | √ | √ | | | | | | | | | | |
| Programmable watermarks on ingress buffers | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ |
| **RapidIO Standard and Non-Standard Features** | | | | | | | | | | | | |
| Packet filter & capture | √ | √ | √ | √ | √ | √ | √ | √ | | | | |
| Traffic management through user selectable scheduling algorithms | √ | √ | √ | √ | √ | | | | √ | √ | √ | √ |
| Receiver controlled flow control | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ |
| Transmitter controlled flow control | | | √ | √ | √ | | | | | | | |
| Performance counters/monitors | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ |
| Error Management features exceeding S-RIO specification | √ | √ | √ | √ | √ | | | | √ | √ | √ | √ |
| Error log (history) and broad error detection coverage | √ | √ | √ | √ | √ | √ | √ | √ | | | | |
| Link-layer AES-128 encryption | | | | | SPS on 4 1x Ports | | | | | | | |
| **BOM Reduction and Clocking Options** | | | | | | | | | | | | |
| Clocking options (MHz) | 156.25 or 100 | | 156 | 156 | 156 | 156 | | 156 | 156 or 125 | | | |
| Lane swap for board design simplification | √ | √ | | | | | | | √ | √ | √ | √ |
| Debug packet generator | √ | √ | √ | √ | √ | | | | √ | √ | √ | √ |
| Debug error insertion | √ | √ | | | | | | | | | | |
| Package (mm) | 33 X 33 | 29 X 29 | 29 X 29 | 25 x 25 | 21 X 21 | 19 X 19 | 27 X 27 | 19 X 19 | 21 X 21 | 21 X 21 | 27 X 27 | 21 X 21 |

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