



# THE DATASHEET OF TSH344IDT



## 340MHz single-supply triple video buffer

### Features

- Bandwidth: 340MHz
- 5V single-supply operation
- Low output rail guaranteed at 60mV max
- Internal gain of 6dB for a matching between 3 channels
- Very low harmonic distortion
- Slew rate: 740V/ms
- Specified for 150Ω and 100Ω loads
- Tested on 5V power supply
- Min. and max. data tested during production

### Applications

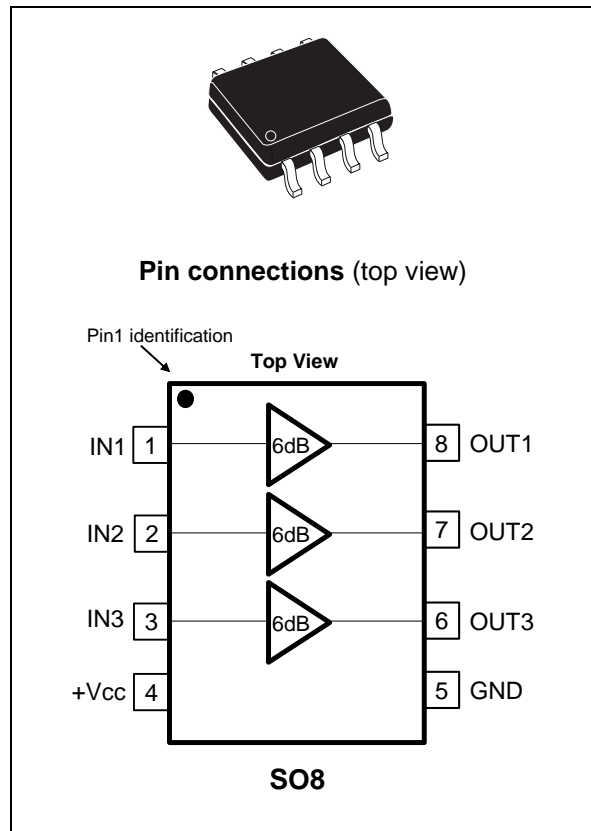
- High-end video systems
- High definition TV (HDTV)
- Broadcast and graphic video
- Multimedia products

### Description

The TSH344 is a triple single-supply video buffer featuring an internal gain of 6dB and a large bandwidth of 340MHz.

The main advantage of this buffer is its very low output rail very close to GND when supplied in single supply 0/5V. This output rail is guaranteed by test at 60mV from GND on 150Ω. This datasheet gives technical information on using the TSH344 as an RGB driver for video DAC output on a video line. See the TSH343 datasheet for Y-Pb-Pr signals.

The TSH344 is available in the compact SO8 plastic package for optimum space-saving.



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# 1 Absolute maximum ratings and operating conditions

**Table 1. Absolute maximum ratings (AMR)**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage <sup>(1)</sup>	6	V
$V_{in}$	Input voltage range <sup>(2)</sup>	0 to +2	V
$T_{oper}$	Operating free air temperature range	-40 to +85	°C
$T_{stg}$	Storage temperature	-65 to +150	°C
$T_j$	Maximum junction temperature	150	°C
$R_{thjc}$	SO8 thermal resistance junction to case	28	°C/W
$R_{thja}$	SO8 thermal resistance junction to ambient area	157	°C/W
$P_{max}$	Maximum power dissipation (@ $T_{amb}=25^{\circ}C$ ) for $T_j=150^{\circ}C$	800	mW
ESD	CDM: charged device model	2	kV
	HBM: human body model	1.5	kV
	MM: machine model	200	V

1. All voltage values, except differential voltage, are with respect to network terminal.

2. The magnitude of input and output voltage must never exceed  $V_{CC} + 0.3V$ .

**Table 2. Operating conditions**

Symbol	Parameter	Value	Unit
$V_{CC}$	Power supply voltage <sup>(1)</sup>	3 to 5.5	V

1. Tested in full production at 0V/5V single power supply.

## 2 Electrical characteristics

Table 3.  $V_{CC} = +5V$  single supply,  $T_{amb} = 25^{\circ}C$  (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
$V_{OS}$	Output offset voltage <sup>(1)</sup>	No load, $T_{amb}$	-35	-8	+35	mV
		$-40^{\circ}C < T_{amb} < +85^{\circ}C$		-8.6		
$I_{ib}$	Input bias current	$T_{amb}$ , input to GND		5.5	16	$\mu A$
		$-40^{\circ}C < T_{amb} < +85^{\circ}C$		6		
$R_{in}$	Input resistance	$T_{amb}$		4		G $\Omega$
$C_{in}$	Input capacitance	$T_{amb}$		1		pF
PSRR	Power supply rejection ratio $20 \log (\Delta V_{CC} / \Delta V_{out})^{(2)}$	Input to GND, $F=1MHz$ , $\Delta V_{CC}=200mV$		-90		dB
ICC	Supply current per buffer	No load, input to GND		10.1	13	mA
		$-40^{\circ}C < T_{amb} < +85^{\circ}C$		10.3		
G	DC voltage gain	$R_L = 150\Omega$ , $V_{in}=1V$	1.92	2	2.05	V/V
MG1	Gain matching between 3 channels	Input = 1V		0.5	2	%
MG0.3	Gain matching between 3 channels	Input = 0.3V		0.5	2	%
<b>Dynamic performance and output characteristics</b>						
Bw	-3dB bandwidth	Small signal $V_{out}=20mVp$ $V_{icm}=0.6V$ , $R_L = 150\Omega$	190	340		MHz
	Gain flatness @ 0.1dB	Small signal $V_{out}=20mVp$ $V_{icm}=0.6V$ , $R_L = 150\Omega$		65		
FPBW	Full power bandwidth	$V_{icm}=0.6V$ , $V_{out} = 2Vp-p$ , $R_L = 150\Omega$	130	200		MHz
D	Delay between each channel	0 to 30MHz		0.5		ns
SR	Slew rate <sup>(3)</sup>	$V_{icm}=0.6V$ , $V_{out} = 2Vp-p$ , $R_L = 150\Omega$	500	740		V/ $\mu s$
$V_{OH}$	High level output voltage	$R_L = 150\Omega$	3.7	3.9		V
$V_{OL}$	Low level output voltage	$R_L = 150\Omega$		40	60	mV
$I_{OUT}$	Output current	$V_{out} = 2Vp$ , $T_{amb}$	45	93		mA
		$-40^{\circ}C < T_{amb} < +85^{\circ}C$		83		
	Output short circuit current ( $I_{source}$ )			100		mA

Table 3.  $V_{CC} = +5V$  single supply,  $T_{amb} = 25^{\circ}C$  (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
<b>Noise and distortion</b>						
eN	Total input voltage noise	$F = 100kHz, R_{in} = 50\Omega$		8		nV/ $\sqrt{Hz}$
		$R_{in} = 50\Omega$ $Bw=30MHz$ $Bw=100MHz$		55 100		$\mu V_{rms}$
HD2	2nd harmonic distortion	$V_{out} = 2V_{p-p}, R_L = 150\Omega$ $F = 10MHz$ $F = 30MHz$		-57 -42		dBc
HD3	3rd harmonic distortion	$V_{out} = 2V_{p-p}, R_L = 150\Omega$ $F = 10MHz$ $F = 30MHz$		-72 -51		dBc

1. Output offset voltage is determined by the following expression:  $V_{OUT} = G.V_{IN} + V_{OS}$ .
2. See [Figure 28](#) and [Figure 29](#).
3. Non-tested value, guaranteed by design and evaluation. See [Figure 12](#).

Figure 1. Frequency response

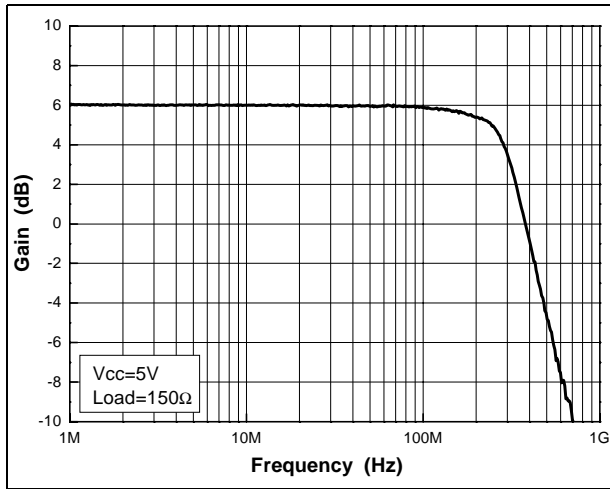


Figure 2. Gain flatness

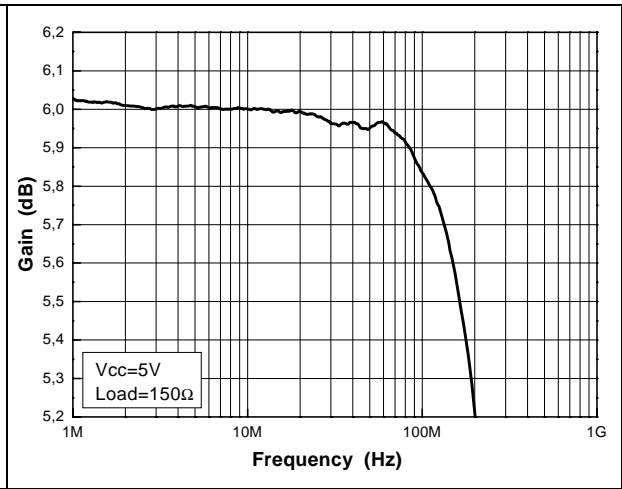


Figure 3. Cross-talk vs. frequency (amp1)

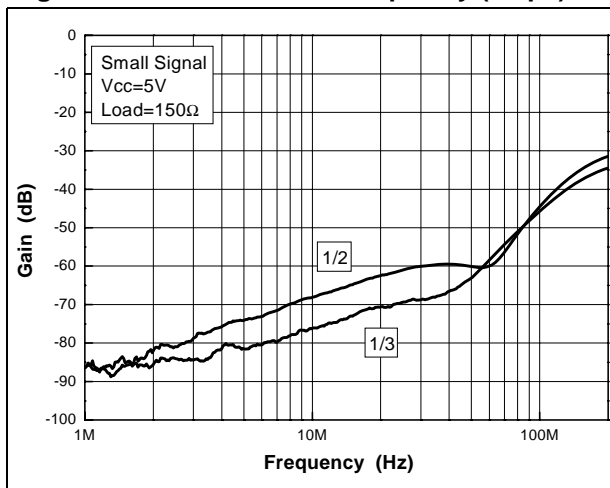


Figure 4. Cross-talk vs. frequency (amp2)

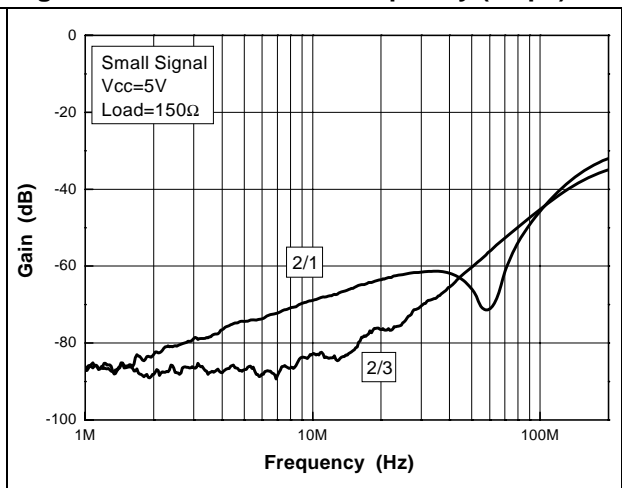


Figure 5. Cross-talk vs. frequency (amp3)

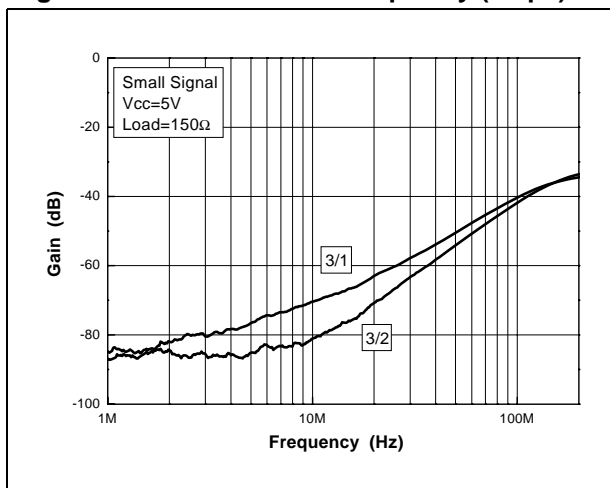


Figure 6. Input noise vs. frequency

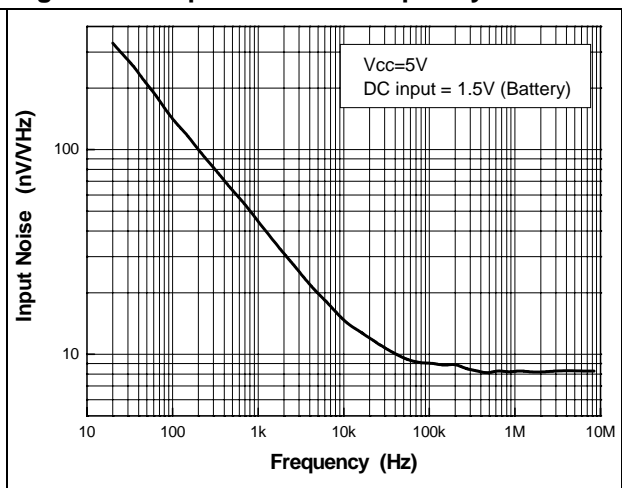


Figure 7. Distortion on 150Ω load - 10MHz

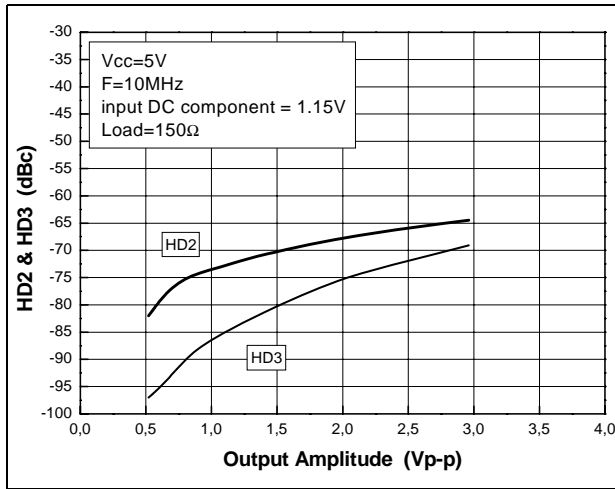


Figure 8. Distortion on 100Ω load - 10MHz

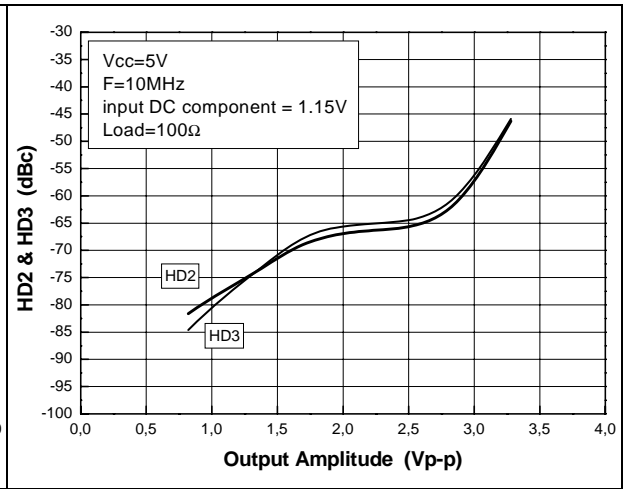


Figure 9. Distortion on 150Ω load - 30MHz

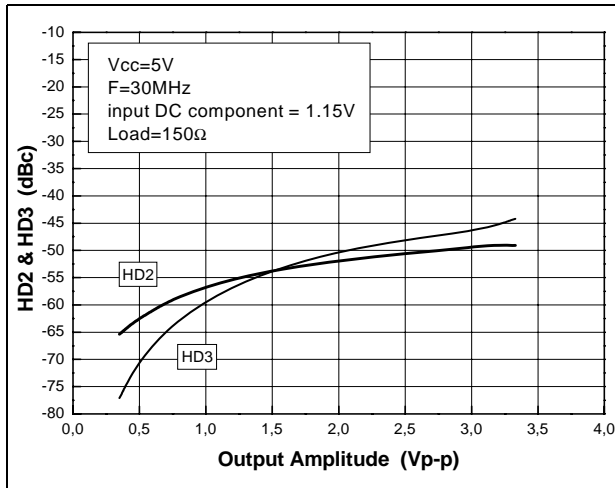


Figure 10. Distortion on 100Ω load - 30MHz

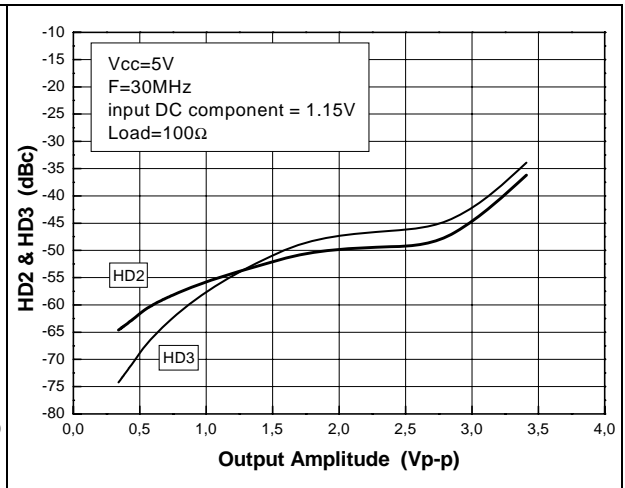


Figure 11. Output current

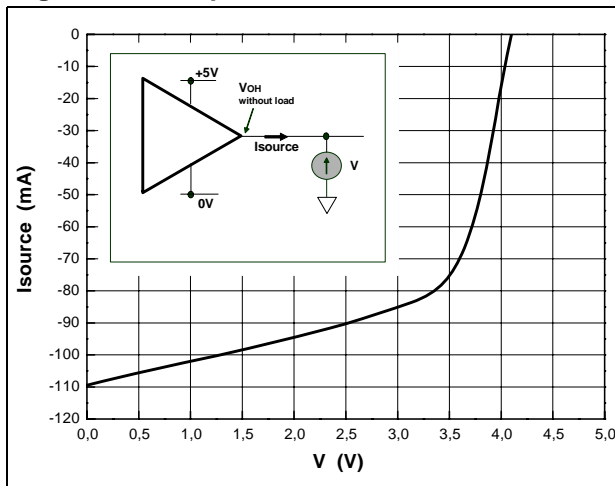


Figure 12. Slew rate

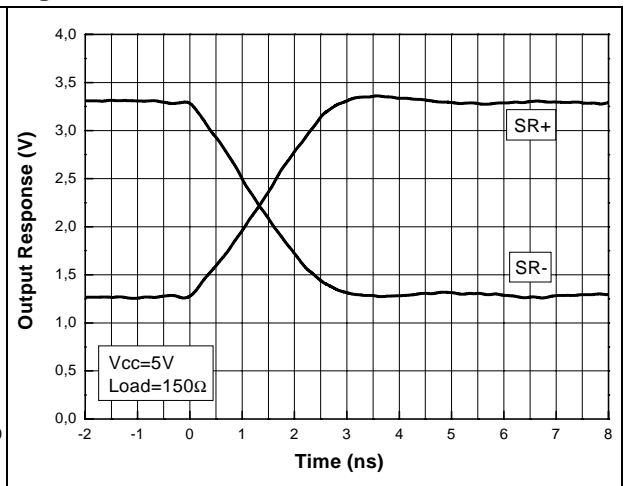


Figure 13. Reverse isolation vs. frequency

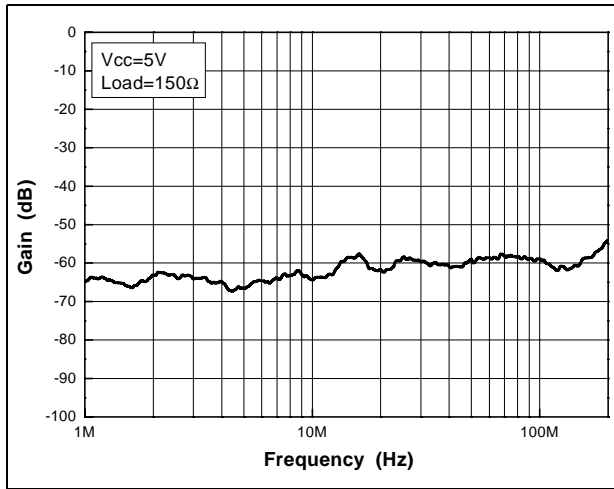


Figure 14. Output swing vs. frequency

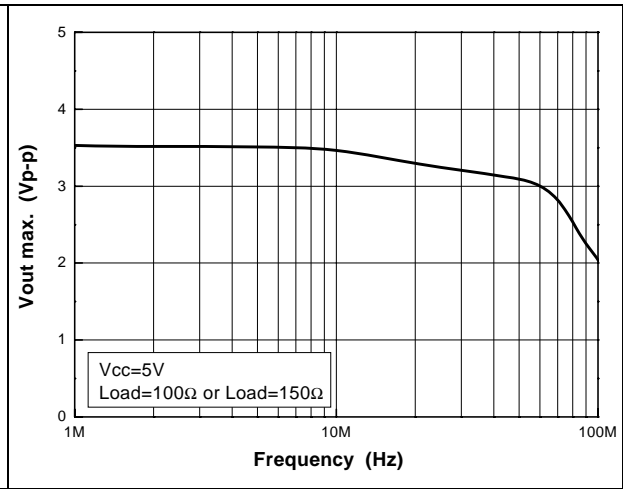


Figure 15. Quiescent current vs. supply

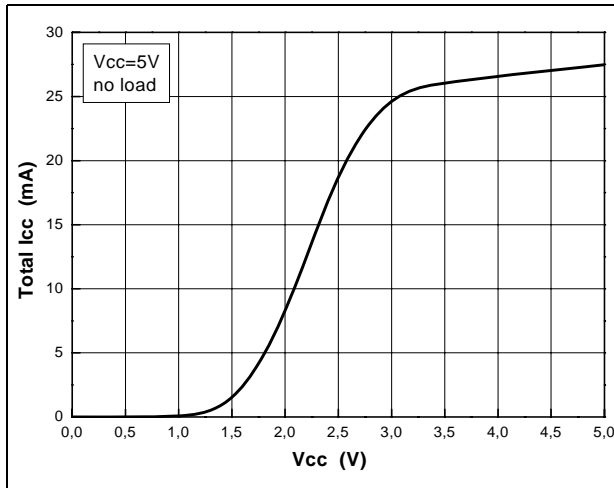


Figure 16. Output swing vs. supply

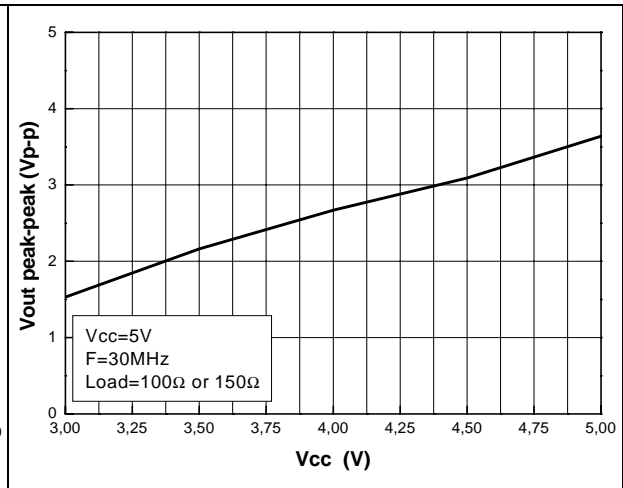


Figure 17. Bandwidth vs. temperature

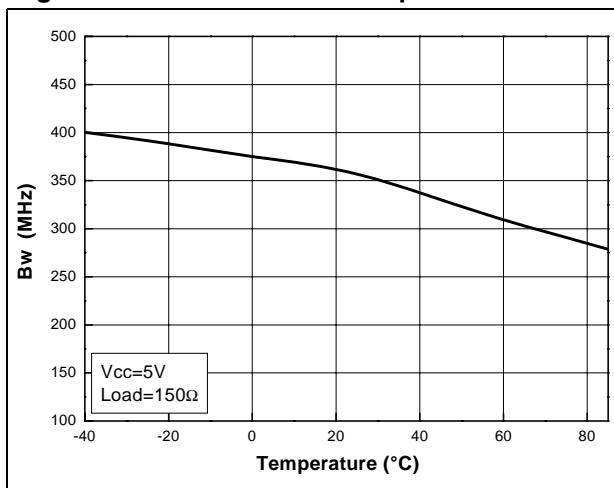


Figure 18. Voltage gain vs. temperature

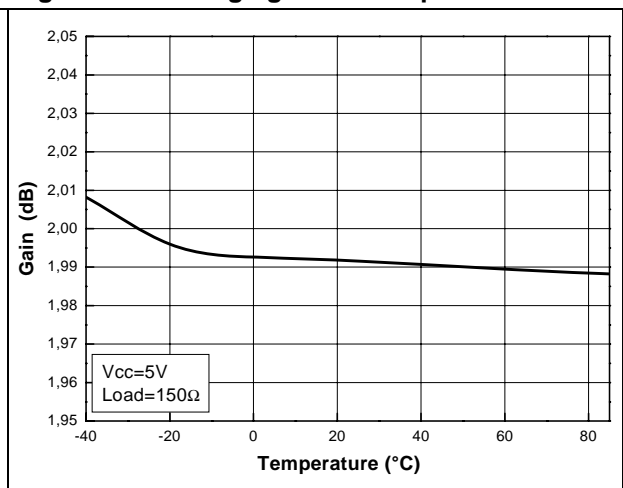


Figure 19.  $I_{bias}$  vs. temperature

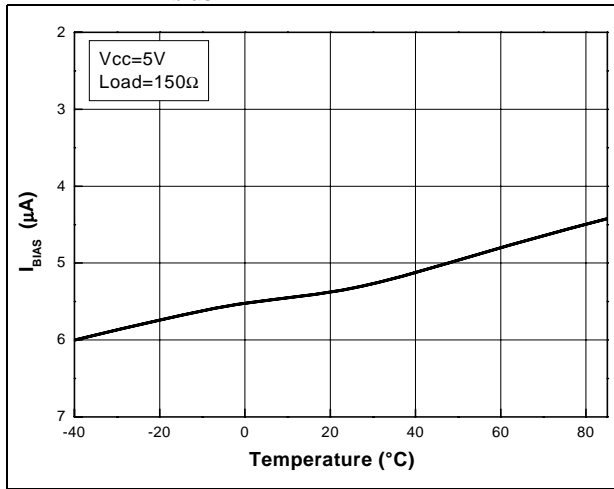


Figure 20. Gain matching vs. temperature

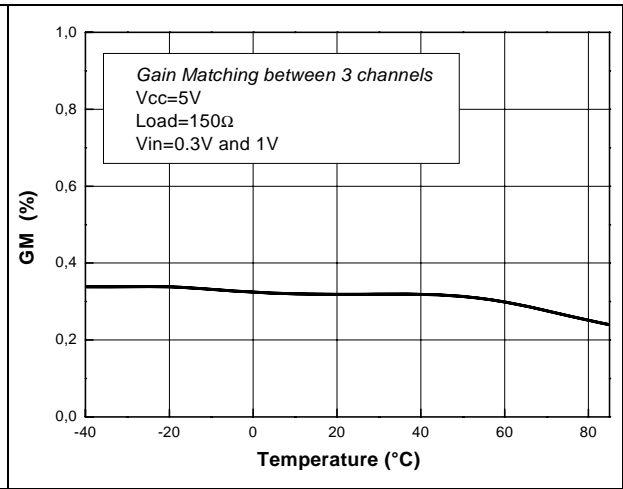


Figure 21. Supply current vs. temperature

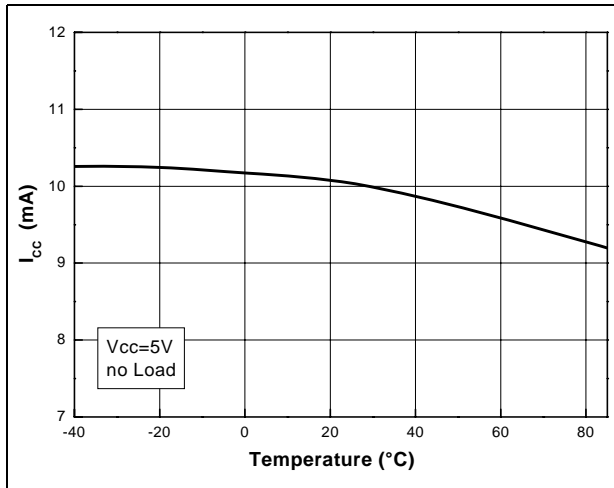


Figure 22. Output current vs. temperature

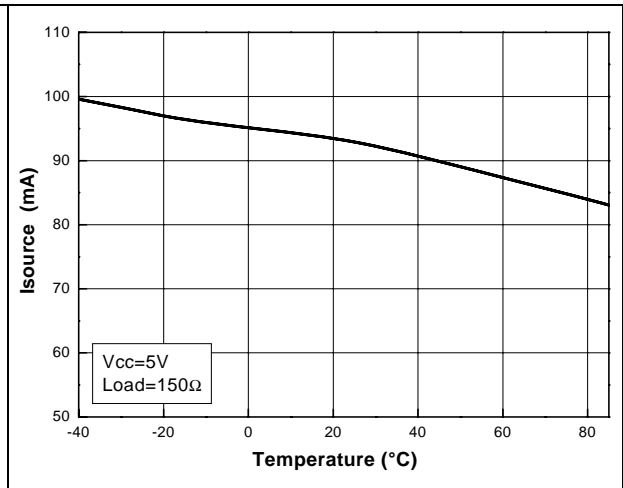


Figure 23. Output higher rail vs. temperature

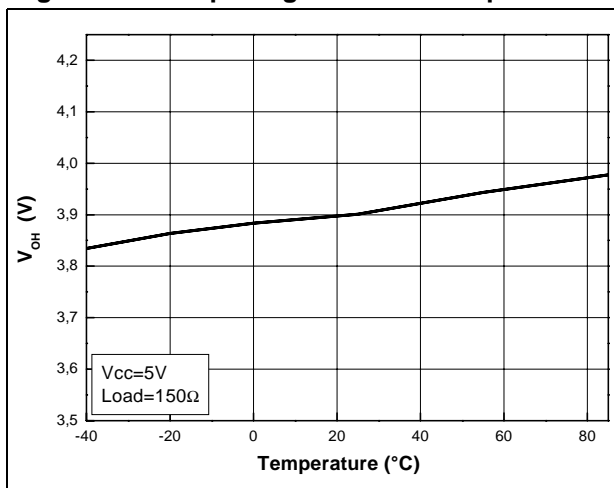
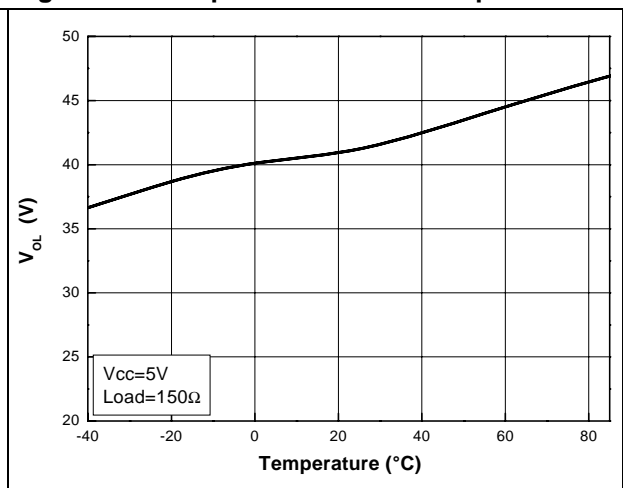


Figure 24. Output lower rail vs. temperature



### 3 Application information

#### 3.1 Using the TSH344 to drive R-G-B video components

Figure 25. Shapes of video signals coming from DACs

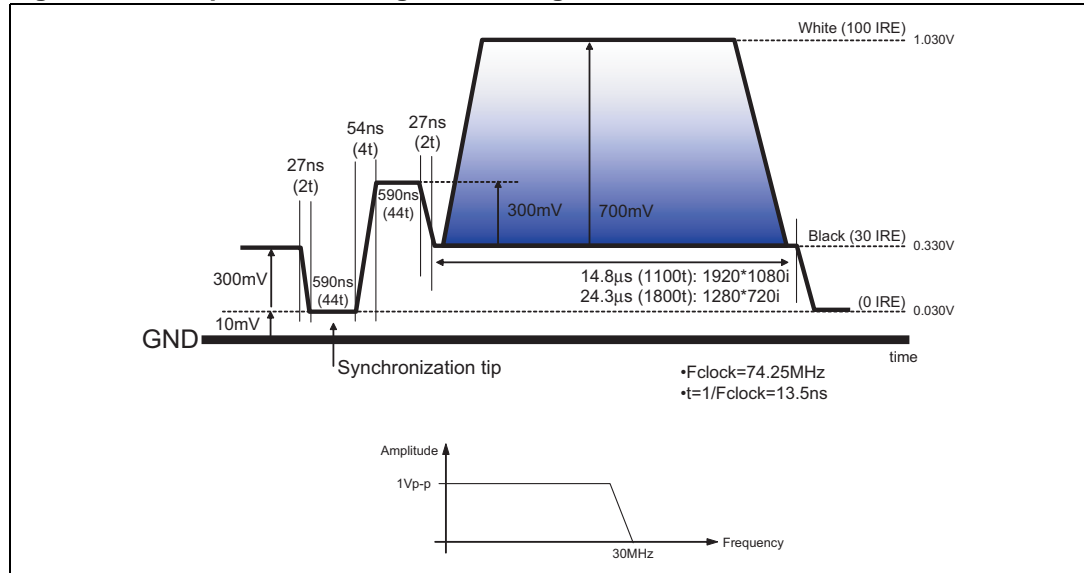
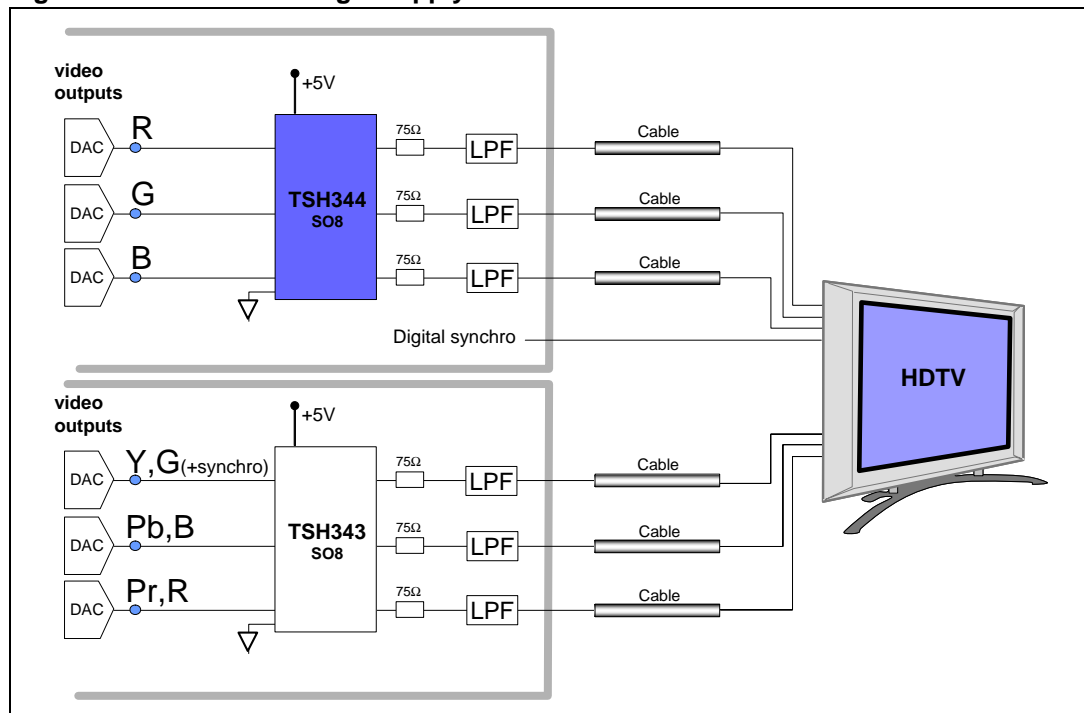
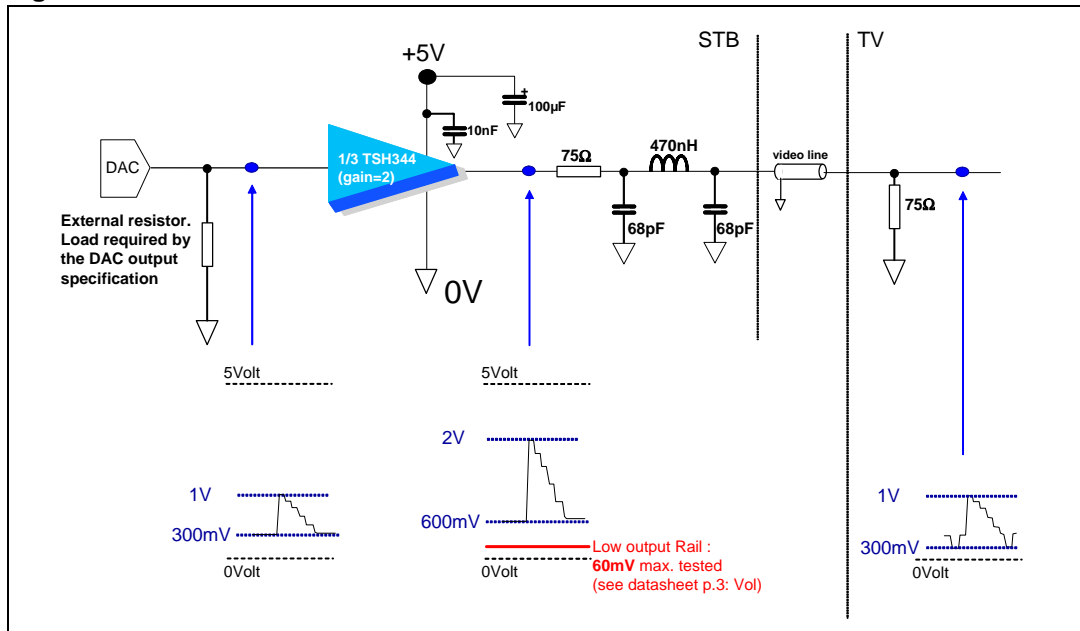


Figure 26. TSH344 in single supply for HD



Note: See the TSH343 datasheet on st.com for more information (the TSH343 is used to drive a video signal including a synchronization tip).

Figure 27. Details on one channel of the TSH344



Because of the shape of the signal described in [Figure 25](#), we use a very low output rail triple high-speed buffer. The TSH344 supplied in 5V single power supply features a low output rail of 60mV (guaranteed by test) on 150Ω load. It is dedicated for driving RGB signals without synchronisation (in the case where the synchronization is provided digitally on the digital bus).

The gain of the TSH344 (gain=2) is internal which makes it possible to remove two resistors on the BOM. To avoid any perturbation on matching from the DACs output impedance along a large band of 30MHz in HD, a discrete reconstruction filtering is implemented after the driver. This filter is matched on 75Ω. Note that the TSH344 uses a single supply architecture and it is not AC output coupled (it cannot sink an output current, therefore it is not possible to implement an output series capacitor).

### 3.2 Power supply considerations

Correct power supply bypassing is very important for optimizing performance in low and high-frequency ranges. Bypass capacitors should be placed as close as possible to the IC pin (pin 4) to improve high-frequency bypassing. A capacitor ( $C_{LF}$ ) greater than  $100\mu\text{F}$  is necessary to improve the PSRR in low frequencies. For better quality bypassing, a capacitor of  $470\text{nF}$  ( $C_{HF}$ ) is also added as close as possible to the IC pin to improve the PSRR in the higher frequencies.

**Figure 28. Circuit for power supply bypassing**

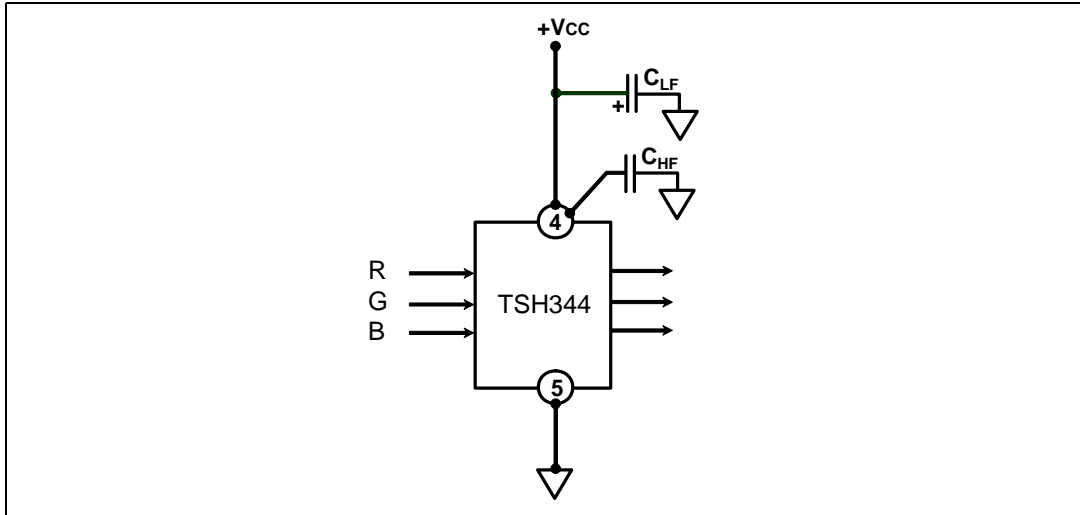
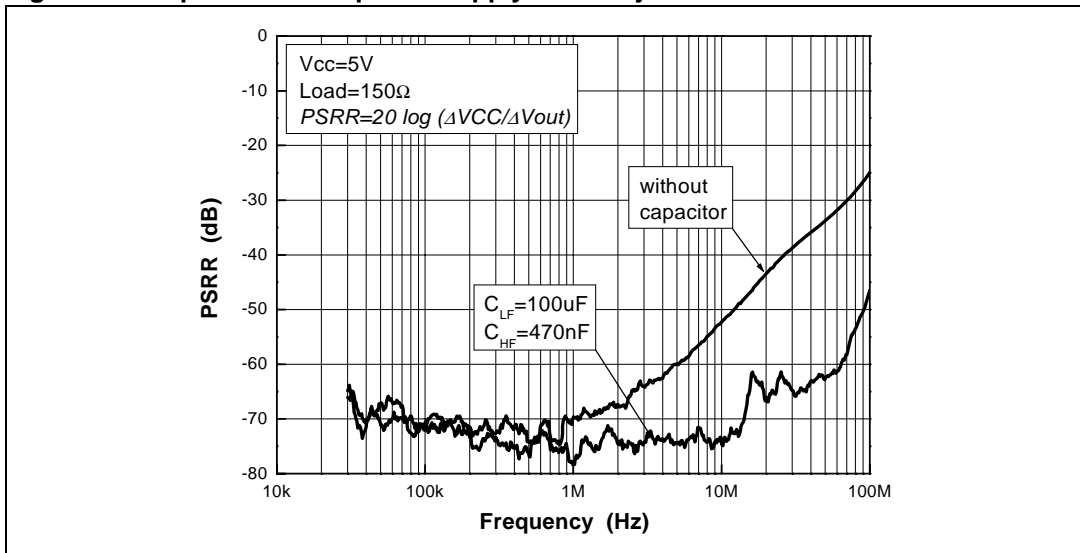


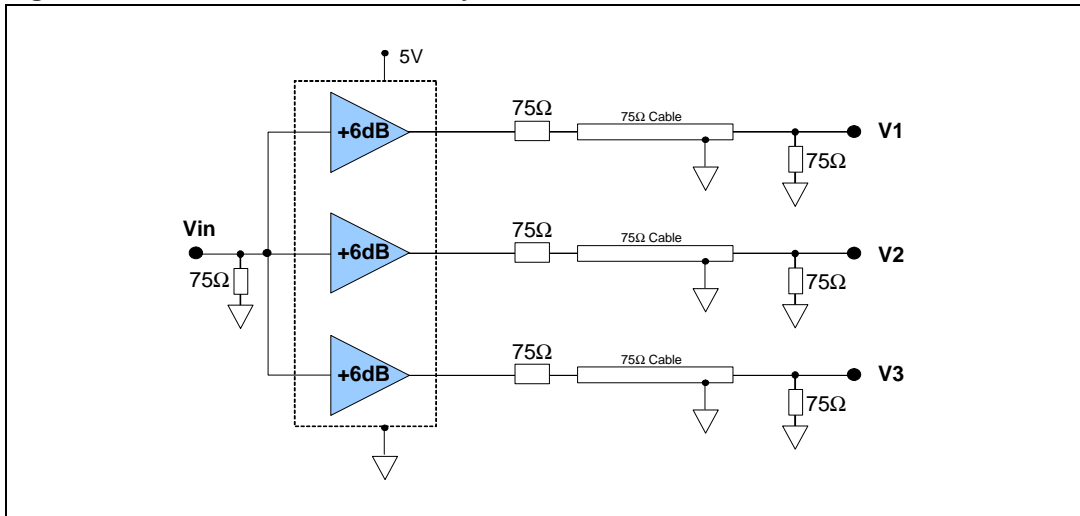
Figure 29 shows how the power supply noise rejection evolves versus frequency depending on how carefully the power supply decoupling is achieved.

**Figure 29. Improvement of power supply noise rejection**



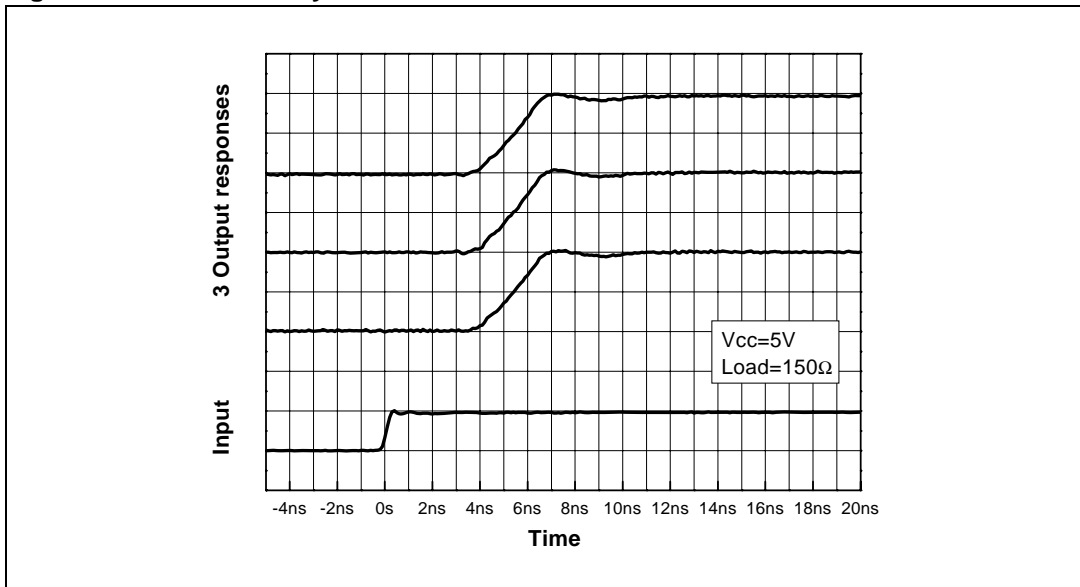
### 3.3 Delay between channels

Figure 30. Measurement of the delay between each channel



The delay between each video component is an important aspect in high definition video systems. To properly drive the three video components without any relative delay, the layout of the TSH344 dice has a very symmetrical geometry. This has a direct effect on the synchronization of each channel, as shown in [Figure 31](#). There is no delay detected between channels when the same  $V_{in}$  signal is applied on the three inputs. Note that the delay between the inputs and the outputs is equal to 4ns.

Figure 31. Relative delay between each channel



## 4 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK<sup>®</sup> packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

Figure 32. SO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	1°		8°	1°		8°
ccc			0.10			0.004

## 5 Ordering information

Table 4. Order codes

Part number	Temperature range	Package	Packing	Marking
TSH344ID	-40°C to +85°C	SO-8	Tube	TSH344I
TSH344IDT			Tape & reel	TSH344I

## 6 Revision history

Date	Revision	Changes
Dec-2005	1	First release of datasheet.
Jan-2006	2	Capa-load option paragraph deleted on page 11.
Jul-2006	3	Application information.
14-Mar-2007	4	Updated <a href="#">Section 3.2: Power supply considerations on page 12.</a>

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