



**THE DATASHEET OF  
TS5A23166DCUR**



## TS5A23166 0.9-Ω Dual-SPST Analog Switch 5-V and 3.3-V 2-Channel Analog Switch

### 1 Features

- Isolation in Powered-Down Mode,  $V_+ = 0$
- Low ON-state resistance (0.9 Ω)
- Control inputs are 5.5-V Tolerant
- Low charge injection
- Excellent ON-state resistance matching
- Low total harmonic distortion (THD)
- 1.65-V to 5.5-V Single-supply operation
- Latch-up performance exceeds 100 mA per JESD 78, class II
- ESD Performance tested per JESD 22
  - 2000-V Human-body model (A114-B, Class II)
  - 1000-V Charged-device model (C101)

### 2 Applications

- [Cell phones](#)
- [Portable instrumentation](#)
- [Audio and video signal routing](#)
- [Low-voltage data-acquisition systems](#)
- [Communication circuits](#)
- [Modems](#)
- [Hard Drives](#)
- [Computer Peripherals](#)
- [Wireless Terminals and Peripherals](#)

### 3 Description

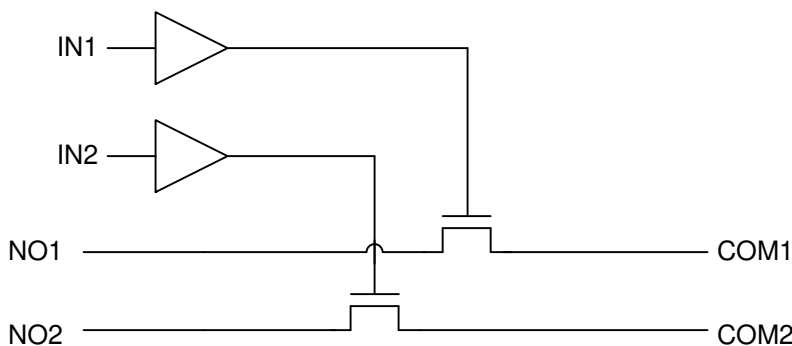
The TS5A23166 device is a dual single-pole single-throw (SPST) analog switch that is designed to operate from 1.65 V to 5.5 V. The TS5A23166 device offers a low ON-state resistance and an excellent channel-to-channel ON-state resistance matching. The TS5A23166 device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A23166	VSSOP (8)	2.30 mm × 2.00 mm
	DSBGA (8)	1.91 mm × 0.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Simplified Schematic



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision I (March 2018) to Revision J Page

- Changed the *Thermal Information* table .....

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### Changes from Revision H (May 2015) to Revision I Page

- Added Note: "Not tested in production" to leakage current at 25°C in the *Electrical Characteristics* tables .....

4

### Changes from Revision G (February 2013) to Revision H Page

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section .....
- Updated document to new TI data sheet format - no specification changes. ....
- Removed *Ordering Information* table. ....

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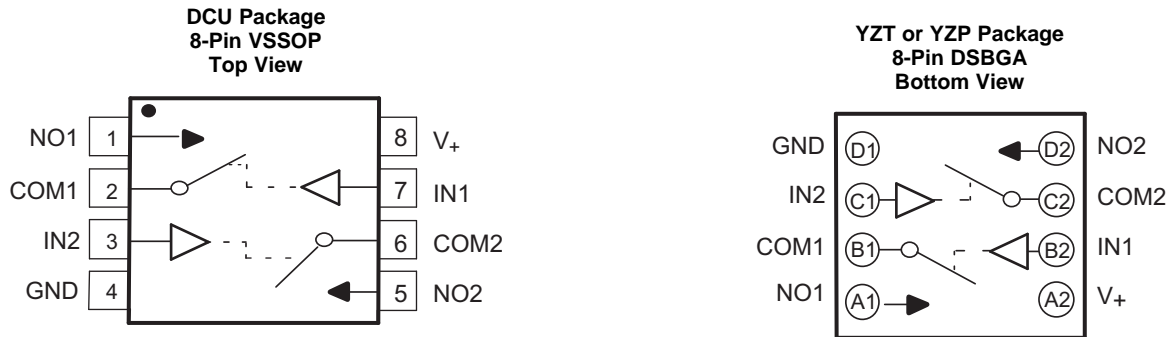
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### Changes from Revision F (September 2012) to Revision G Page

- Changed pin numbers for YZT or YZP package pinout. ....

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## 5 Pin Configuration and Functions



### Pin Functions

PIN			TYPE	DESCRIPTION
NAME	TSSOP NO.	DSBGA NO.		
COM1	2	B1	I/O	Common port for switch 1
COM2	6	C2	I/O	Common port for switch 2
GND	4	D1	GND	Ground
IN1	7	B2	I	Active-high control pin connecting NO1 to COM1.
IN2	3	C1	I	Active-high control pin connecting NO2 to COM2.
NO1	1	A1	I/O	Normally open switch path 1
NO2	5	D2	I/O	Normally open switch path 2
V+	8	A2	PWR	Power supply pin

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

		MIN	MAX	UNIT
V <sub>+</sub>	Supply voltage <sup>(3)</sup>	-0.5	6.5	V
V <sub>NO</sub> V <sub>COM</sub>	Analog voltage <sup>(3)(4)(5)</sup>	-0.5	V <sub>+</sub> + 0.5	V
I <sub>K</sub>	Analog port diode current	V <sub>NO</sub> , V <sub>COM</sub> < 0		mA
I <sub>NO</sub>	ON-state switch current	V <sub>NO</sub> , V <sub>COM</sub> = 0 to V <sub>+</sub>		mA
I <sub>COM</sub>	ON-state peak switch current <sup>(6)</sup>	V <sub>NO</sub> , V <sub>COM</sub> = 0 to V <sub>+</sub>		mA
V <sub>I</sub>	Digital input voltage <sup>(3)(4)</sup>	-0.5	6.5	V
I <sub>IK</sub>	Digital input clamp current	V <sub>I</sub> < 0		mA
I <sub>+</sub>	Continuous current through V <sub>+</sub>		100	mA
I <sub>GND</sub>	Continuous current through GND	-100	100	mA

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (5) This value is limited to 5.5 V maximum.
- (6) Pulse at 1-ms duration < 10% duty cycle.

## 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	+2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	+1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage	0	$V_+$	V
$V_+$	Supply voltage	1.65	5.5	V
$V_I$	Control Input Voltage	0	5.5	V
$T_A$	Operating free-air temperature	-40	85	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	TS5A23166			UNIT
	DCU (VSSOP)	YZP (DSBGA)	YZT (DSBGA)	
	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	212.2	99.9	99.7	°C/W
$R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance	77.6	1.0	1.4	°C/W
$R_{\theta JB}$ Junction-to-board thermal resistance	91.7	27.8	27.8	°C/W
$\phi_{JT}$ Junction-to-top characterization parameter	7.1	0.4	0.5	°C/W
$\phi_{JB}$ Junction-to-board characterization parameter	91.1	27.8	27.7	°C/W

(1) For more information about traditional and new thermal metrics, see the [IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics: 5-V Supply

$V_+ = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>									
$V_{COM}, V_{NO}$	Analog signal					0		$V_+$	V
$r_{peak}$	Peak ON resistance	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, see <a href="#">Figure 11</a>	25°C	4.5 V	0.9	1.1	1.2	$\Omega$
				Full					
$r_{on}$	ON-state resistance	$V_{NO} = 2.5\text{ V}$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, see <a href="#">Figure 11</a>	25°C	4.5 V	0.75	0.9	1	$\Omega$
				Full					
$\Delta r_{on}$	ON-state resistance match between channels	$V_{NO} = 2.5\text{ V}$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, see <a href="#">Figure 11</a>	25°C	4.5 V	0.04	0.1	0.1	$\Omega$
				Full					
$r_{on(flat)}$	ON-state resistance flatness	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -100\text{ mA}$ ,	Switch ON, see <a href="#">Figure 11</a>	25°C	4.5 V	0.2		$\Omega$	
				Full		25°C	0.15		0.25
						Full	0.25		
$I_{NO(OFF)}$	NO OFF leakage current	$V_{NO} = 1\text{ V}$ , $V_{COM} = 4.5\text{ V}$ , or $V_{NO} = 4.5\text{ V}$ , $V_{COM} = 1\text{ V}$ ,	Switch OFF, see <a href="#">Figure 12</a>	25°C	5.5 V	0 V	4	20 <sup>(2)</sup>	nA
				Full		-150	150		
$I_{NO(PWROFF)}$		$V_{NO} = 0\text{ to }5.5\text{ V}$ , $V_{COM} = 5.5\text{ V to }0$ ,	Switch OFF, see <a href="#">Figure 12</a>	25°C	0 V	-10	0.2	10 <sup>(2)</sup>	$\mu\text{A}$
				Full		-50	50		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

(2) Not tested in production.

**Electrical Characteristics: 5-V Supply (continued)**
 $V_+ = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		T <sub>A</sub>	V <sub>+</sub>	MIN	TYP	MAX	UNIT
I <sub>COM(OFF)</sub>	COM OFF leakage current	V <sub>COM</sub> = 1 V, V <sub>NO</sub> = 4.5 V, or V <sub>COM</sub> = 4.5 V, V <sub>NO</sub> = 1 V,	Switch OFF, see <a href="#">Figure 12</a>	25°C	5.5 V	0 V	4	20 <sup>(2)</sup>	nA
				Full		-150	150		
I <sub>COM(PWROFF)</sub>		V <sub>COM</sub> = 0 to 5.5 V, V <sub>NO</sub> = 5.5 V to 0,	Switch OFF, see <a href="#">Figure 12</a>	25°C	0 V	-10	0.2	10 <sup>(2)</sup>	μA
				Full		-50	50		
I <sub>NO(ON)</sub>	NO ON leakage current	V <sub>NO</sub> = 1 V, V <sub>COM</sub> = Open, or V <sub>NO</sub> = 4.5 V, V <sub>COM</sub> = Open,	Switch ON, see <a href="#">Figure 13</a>	25°C	5.5 V	-5	0.4	5 <sup>(2)</sup>	nA
				Full		-50	50		
I <sub>COM(ON)</sub>	COM ON leakage current	V <sub>COM</sub> = 1 V, V <sub>NO</sub> = Open, or V <sub>COM</sub> = 4.5 V, V <sub>NO</sub> = Open,	Switch ON, see <a href="#">Figure 13</a>	25°C	5.5 V	-5	0.4	5 <sup>(2)</sup>	nA
				Full		-50	50		
<b>Digital Control Inputs (IN1, IN2)<sup>(3)</sup></b>									
V <sub>IH</sub>	Input logic high			Full		2.4		5.5	V
V <sub>IL</sub>	Input logic low			Full		0		0.8	V
I <sub>IH</sub> , I <sub>IL</sub>	Input leakage current	V <sub>I</sub> = 5.5 V or 0		25°C	5.5 V	-2	0.3	2	nA
				Full		-20	20		
<b>Dynamic</b>									
Q <sub>C</sub>	Charge injection	V <sub>GEN</sub> = 0, R <sub>GEN</sub> = 0,	C <sub>L</sub> = 1 nF, see <a href="#">Figure 19</a>	25°C	5 V		6		pC
C <sub>NO(OFF)</sub>	NO OFF capacitance	V <sub>NO</sub> = V <sub>+</sub> or GND, Switch OFF,	See <a href="#">Figure 14</a>	25°C	5 V		19		pF
C <sub>COM(OFF)</sub>	COM OFF capacitance	V <sub>COM</sub> = V <sub>+</sub> or GND, Switch OFF,	See <a href="#">Figure 14</a>	25°C	5 V		18		pF
C <sub>NO(ON)</sub>	NO ON capacitance	V <sub>NO</sub> = V <sub>+</sub> or GND, Switch ON,	See <a href="#">Figure 14</a>	25°C	5 V		35.5		pF
C <sub>COM(ON)</sub>	COM ON capacitance	V <sub>COM</sub> = V <sub>+</sub> or GND, Switch ON,	See <a href="#">Figure 14</a>	25°C	5 V		35.5		pF
C <sub>I</sub>	Digital input capacitance	V <sub>I</sub> = V <sub>+</sub> or GND,	See <a href="#">Figure 14</a>	25°C	5 V		2		pF
BW	Bandwidth	R <sub>L</sub> = 50 Ω, Switch ON,	See <a href="#">Figure 16</a>	25°C	5 V		150		MHz
O <sub>ISO</sub>	OFF isolation	R <sub>L</sub> = 50 Ω, f = 1 MHz,	Switch OFF, see <a href="#">Figure 17</a>	25°C	5 V		-62		dB
X <sub>TALK</sub>	Crosstalk	R <sub>L</sub> = 50 Ω, f = 1 MHz,	Switch ON, see <a href="#">Figure 18</a>	25°C	5 V		-85		dB
THD	Total harmonic distortion	R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF,	f = 20 Hz to 20 kHz, see <a href="#">Figure 20</a>	25°C	5 V		0.005%		
<b>Supply</b>									
I <sub>+</sub>	Positive supply current	V <sub>I</sub> = V <sub>+</sub> or GND,	Switch ON or OFF	25°C	5.5 V		0.01	0.1	μA
				Full			1		

(3) All unused digital inputs of the device must be held at V<sub>+</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

## 6.6 Electrical Characteristics: 3.3-V Supply

 $V_+ = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>									
$V_{\text{COM}}, V_{\text{NO}}$	Analog signal range					0		$V_+$	V
$r_{\text{peak}}$	Peak ON resistance	$0 \leq V_{\text{NO}} \leq V_+$ , $I_{\text{COM}} = -100\text{ mA}$ ,	Switch ON, see <a href="#">Figure 11</a>	25°C	3 V	1.3		1.6	$\Omega$
				Full		1.8			
$r_{\text{on}}$	ON-state resistance	$V_{\text{NO}} = 2\text{ V}$ , $I_{\text{COM}} = -100\text{ mA}$ ,	Switch ON, see <a href="#">Figure 11</a>	25°C	3 V	1.1		1.5	$\Omega$
				Full		1.7			
$\Delta r_{\text{on}}$	ON-state resistance match between channels	$V_{\text{NO}} = 2\text{ V}$ , 0.8 V, $I_{\text{COM}} = -100\text{ mA}$ ,	Switch ON, see <a href="#">Figure 11</a>	25°C	3 V	0.04		0.1	$\Omega$
				Full		0.1			
$r_{\text{on(flat)}}$	ON-state resistance flatness	$0 \leq V_{\text{NO}} \leq V_+$ , $I_{\text{COM}} = -100\text{ mA}$	Switch ON, see <a href="#">Figure 11</a>	25°C	3 V	0.3		$\Omega$	
				Full		0.15			0.25
						0.25			
$I_{\text{NO(OFF)}}$	NO OFF leakage current	$V_{\text{NO}} = 1\text{ V}$ , $V_{\text{COM}} = 3\text{ V}$ , or $V_{\text{NO}} = 3\text{ V}$ , $V_{\text{COM}} = 1\text{ V}$ ,	Switch OFF, see <a href="#">Figure 12</a>	25°C	3.6 V	-5	0.5	5 <sup>(2)</sup>	nA
Full				-50		50			
$I_{\text{NO(PWROFF)}}$	COM OFF leakage current	$V_{\text{NO}} = 0\text{ to }3.6\text{ V}$ , $V_{\text{COM}} = 3.6\text{ V to }0$ ,	Switch OFF, see <a href="#">Figure 12</a>	25°C	0 V	-5	0.1	5 <sup>(2)</sup>	$\mu\text{A}$
Full				-25		25			
$I_{\text{COM(OFF)}}$	COM OFF leakage current	$V_{\text{COM}} = 1\text{ V}$ , $V_{\text{NO}} = 3\text{ V}$ , or $V_{\text{COM}} = 3\text{ V}$ , $V_{\text{NO}} = 1\text{ V}$ ,	Switch OFF, see <a href="#">Figure 12</a>	25°C	3.6 V	-5	0.5	5 <sup>(2)</sup>	nA
Full				-50		50			
$I_{\text{COM(PWROFF)}}$	NO ON leakage current	$V_{\text{COM}} = 0\text{ to }3.6\text{ V}$ , $V_{\text{NO}} = 3.6\text{ V to }0$ ,	Switch OFF, see <a href="#">Figure 12</a>	25°C	0 V	-5	0.1	5 <sup>(2)</sup>	$\mu\text{A}$
Full				-25		25			
$I_{\text{NO(ON)}}$	COM ON leakage current	$V_{\text{NO}} = 1\text{ V}$ , $V_{\text{COM}} = \text{Open}$ , or $V_{\text{NO}} = 3\text{ V}$ , $V_{\text{COM}} = \text{Open}$ ,	Switch ON, see <a href="#">Figure 13</a>	25°C	3.6 V	-2	0.3	2 <sup>(2)</sup>	nA
				Full		-20	20		
$I_{\text{COM(ON)}}$	NO ON leakage current	$V_{\text{COM}} = 1\text{ V}$ , $V_{\text{NO}} = \text{Open}$ , or $V_{\text{COM}} = 3\text{ V}$ , $V_{\text{NO}} = \text{Open}$ ,	Switch ON, see <a href="#">Figure 13</a>	25°C	3.6 V	-2	0.3	2 <sup>(2)</sup>	nA
				Full		-20	20		
<b>Digital Control Inputs (IN1, IN2)<sup>(3)</sup></b>									
$V_{\text{IH}}$	Input logic high			Full		2		5.5	V
$V_{\text{IL}}$	Input logic low			Full		0		0.8	V
$I_{\text{IH}}, I_{\text{IL}}$	Input leakage current	$V_I = 5.5\text{ V or }0$		25°C	3.6 V	-2	0.3	2	nA
				Full		-20	20		

- (1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.  
 (2) Not tested in production.  
 (3) All unused digital inputs of the device must be held at  $V_+$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

## Electrical Characteristics: 3.3-V Supply (continued)

 $V_+ = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Dynamic</b>									
$Q_C$	Charge injection	$V_{GEN} = 0$ , $R_{GEN} = 0$ ,	$C_L = 1\text{ nF}$ , see Figure 19	25°C	5 V		6		pC
$C_{NO(OFF)}$	NO OFF capacitance	$V_{NO} = V_+$ or GND, Switch OFF,	See Figure 14	25°C	3.3 V		19.5		pF
$C_{COM(OFF)}$	COM OFF capacitance	$V_{COM} = V_+$ or GND, Switch OFF,	See Figure 14	25°C	3.3 V		18.5		pF
$C_{NO(ON)}$	NO ON capacitance	$V_{NO} = V_+$ or GND, Switch ON,	See Figure 14	25°C	3.3 V		36		pF
$C_{COM(ON)}$	COM ON capacitance	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 14	25°C	3.3 V		36		pF
$C_I$	Digital input capacitance	$V_I = V_+$ or GND,	See Figure 14	25°C	3.3 V		2		pF
BW	Bandwidth	$R_L = 50\ \Omega$ , Switch ON,	See Figure 16	25°C	3.3 V		150		MHz
$O_{ISO}$	OFF isolation	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	Switch OFF, see Figure 17	25°C	3.3 V		-62		dB
$X_{TALK}$	Crosstalk	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	Switch ON, see Figure 18	25°C	3.3 V		-85		dB
THD	Total harmonic distortion	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ ,	$f = 20\text{ Hz to }20\text{ kHz}$ , see Figure 20	25°C	3.3 V		0.01%		
<b>Supply</b>									
$I_+$	Positive supply current	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	3.6 V		0.001	0.05	$\mu\text{A}$
				Full				0.3	

## 6.7 Electrical Characteristics: 2.5-V Supply

 $V_+ = 2.3\text{ V to }2.7\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Analog Switch</b>										
$V_{COM}, V_{NO}$	Analog signal range					0		$V_+$	V	
$r_{peak}$	Peak ON resistance	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -8\text{ mA}$ ,	Switch ON, see Figure 11	25°C	2.3 V		1.8	2.4	$\Omega$	
				Full				2.6		
$r_{on}$	ON-state resistance	$V_{NO} = 1.8\text{ V}$ , $I_{COM} = -8\text{ mA}$ ,	Switch ON, see Figure 11	25°C	2.3 V		1.2	2.1	$\Omega$	
				Full				2.4		
$\Delta r_{on}$	ON-state resistance match between channels	$V_{NO} = 1.8\text{ V}, 0.8\text{ V}$ , $I_{COM} = -8\text{ mA}$ ,	Switch ON, see Figure 11	25°C	2.3 V		0.04	0.15	$\Omega$	
				Full				0.15		
$r_{on(flat)}$	ON-state resistance flatness	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -8\text{ mA}$ ,	Switch ON, see Figure 11	25°C	2.3 V		0.7		$\Omega$	
				25°C				0.4		0.6
				Full						0.6
$I_{NO(OFF)}$	NO OFF leakage current	$V_{NO} = 0.5\text{ V}$ , $V_{COM} = 2.3\text{ V}$ , or $V_{NO} = 2.3\text{ V}$ , $V_{COM} = 0.5\text{ V}$ ,	Switch OFF, see Figure 12	25°C	2.7 V		-5	0.3	5 <sup>(2)</sup>	
				Full				-50	50	
$I_{NO(PWROFF)}$		$V_{NO} = 0\text{ to }2.7\text{ V}$ , $V_{COM} = 2.7\text{ V to }0$ ,	Switch OFF, see Figure 12	25°C	0 V		-2	0.05	2 <sup>(2)</sup>	
				Full				-15	15	

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

(2) Not tested in production.

**Electrical Characteristics: 2.5-V Supply (continued)**
 $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		$T_A$	$V_+$	MIN	TYP	MAX	UNIT
$I_{\text{COM(OFF)}}$	COM OFF leakage current	$V_{\text{NO}} = 2.3 \text{ V}$ , $V_{\text{COM}} = 0.5 \text{ V}$ , or $V_{\text{NO}} = 0.5 \text{ V}$ , $V_{\text{COM}} = 2.3 \text{ V}$ ,	Switch OFF, see <a href="#">Figure 12</a>	25°C	2.7 V	-5	0.3	5 <sup>(2)</sup>	nA
				Full		-50		50	
$I_{\text{COM(PWROFF)}}$		$V_{\text{COM}} = 0 \text{ to } 2.7 \text{ V}$ , $V_{\text{NO}} = 2.7 \text{ V to } 0$ ,	Switch OFF, see <a href="#">Figure 12</a>	25°C	0 V	-2	0.05	2 <sup>(2)</sup>	μA
				Full		-15		15	
$I_{\text{NO(ON)}}$	NO ON leakage current	$V_{\text{NO}} = 0.5 \text{ V}$ , $V_{\text{COM}} = \text{Open}$ , or $V_{\text{NO}} = 2.3 \text{ V}$ , $V_{\text{COM}} = \text{Open}$ ,	Switch ON, see <a href="#">Figure 13</a>	25°C	2.7 V	-2	0.3	2 <sup>(2)</sup>	nA
				Full		-20		20	
$I_{\text{COM(ON)}}$	COM ON leakage current	$V_{\text{COM}} = 0.5 \text{ V}$ , $V_{\text{NO}} = \text{Open}$ , or $V_{\text{COM}} = 2.3 \text{ V}$ , $V_{\text{NO}} = \text{Open}$ ,	Switch ON, see <a href="#">Figure 13</a>	25°C	2.7 V	-2	0.3	2 <sup>(2)</sup>	nA
				Full		-20		20	
<b>Digital Control Inputs (IN1, IN2)</b>									
$V_{\text{IH}}$	Input logic high			Full		1.8		5.5	V
$V_{\text{IL}}$	Input logic low			Full		0		0.6	V
$I_{\text{IH}}, I_{\text{IL}}$	Input leakage current	$V_I = 5.5 \text{ V or } 0$		25°C	2.7 V	-2	0.3	2	nA
				Full		-20		20	
<b>Dynamic</b>									
$Q_C$	Charge injection	$V_{\text{GEN}} = 0$ , $R_{\text{GEN}} = 0$ ,	$C_L = 1 \text{ nF}$ , see <a href="#">Figure 19</a>	25°C	2.5 V		4		pC
$C_{\text{NO(OFF)}}$	NO OFF capacitance	$V_{\text{NO}} = V_+ \text{ or GND}$ , Switch OFF,	See <a href="#">Figure 14</a>	25°C	2.5 V		19.5		pF
$C_{\text{COM(OFF)}}$	COM OFF capacitance	$V_{\text{COM}} = V_+ \text{ or GND}$ , Switch OFF,	See <a href="#">Figure 14</a>	25°C	2.5 V		18.5		pF
$C_{\text{NO(ON)}}$	NO ON capacitance	$V_{\text{NO}} = V_+ \text{ or GND}$ , Switch ON,	See <a href="#">Figure 14</a>	25°C	2.5 V		36.5		pF
$C_{\text{COM(ON)}}$	COM ON capacitance	$V_{\text{COM}} = V_+ \text{ or GND}$ , Switch ON,	See <a href="#">Figure 14</a>	25°C	2.5 V		36.5		pF
$C_I$	Digital input capacitance	$V_I = V_+ \text{ or GND}$ ,	See <a href="#">Figure 14</a>	25°C	2.5 V		2		pF
BW	Bandwidth	$R_L = 50 \Omega$ , Switch ON,	See <a href="#">Figure 16</a>	25°C	2.5 V		150		MHz
$O_{\text{ISO}}$	OFF isolation	$R_L = 50 \Omega$ , $f = 1 \text{ MHz}$ ,	Switch OFF, see <a href="#">Figure 17</a>	25°C	2.5 V		-62		dB
$X_{\text{TALK}}$	Crosstalk	$R_L = 50 \Omega$ , $f = 1 \text{ MHz}$ ,	Switch ON, see <a href="#">Figure 18</a>	25°C	2.5 V		-85		dB
THD	Total harmonic distortion	$R_L = 600 \Omega$ , $C_L = 50 \text{ pF}$ ,	$f = 20 \text{ Hz to } 20 \text{ kHz}$ , see <a href="#">Figure 20</a>	25°C	2.5 V		0.02%		
<b>Supply</b>									
$I_+$	Positive supply current	$V_I = V_+ \text{ or GND}$ ,	Switch ON or OFF	25°C	2.7 V		0.001	0.02	μA
				Full				0.25	

## 6.8 Electrical Characteristics: 1.8-V Supply

 $V_+ = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Analog Switch</b>										
$V_{COM}, V_{NO}$	Analog signal range					0		$V_+$	V	
$r_{peak}$	Peak ON resistance	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -2\text{ mA}$ ,	Switch ON, see Figure 11	25°C	1.65 V		4.2	25	$\Omega$	
				Full			30			
$r_{on}$	ON-state resistance	$V_{NO} = 0.6\text{ V}, 1.5\text{ V}$ , $I_{COM} = -2\text{ mA}$ ,	Switch ON, see Figure 11	25°C	1.65 V		1.6	3.9	$\Omega$	
				Full			4			
$\Delta r_{on}$	ON-state resistance match between channels	$V_{NO} = 1.5\text{ V}$ , $I_{COM} = -2\text{ mA}$ ,	Switch ON, see Figure 11	25°C	1.65 V		0.04	0.2	$\Omega$	
				Full			0.2			
$r_{on(Flat)}$	ON-state resistance flatness	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -2\text{ mA}$ ,	Switch ON, see Figure 11	25°C	1.65 V		2.8		$\Omega$	
				25°C			4.1	22		
				Full				27		
$I_{NO(OFF)}$	NO OFF leakage current	$V_{NO} = 0.3\text{ V}$ , $V_{COM} = 1.65\text{ V}$ , or $V_{NO} = 1.65\text{ V}$ , $V_{COM} = 0.3\text{ V}$ ,	Switch OFF, see Figure 12	25°C	1.95 V		-5	0.3	5 <sup>(2)</sup>	nA
				Full			-50	50		
$I_{NO(PWROFF)}$		$V_{NO} = 0\text{ to }1.95\text{ V}$ , $V_{COM} = 1.95\text{ V to }0$ ,	Switch OFF, see Figure 12	25°C	0 V		-2	0.05	2 <sup>(2)</sup>	$\mu\text{A}$
				Full			-10	10		
$I_{COM(OFF)}$	COM OFF leakage current	$V_{NO} = 1.65\text{ V}$ , $V_{COM} = 0.3\text{ V}$ , or $V_{NO} = 0.3\text{ V}$ , $V_{COM} = 1.65\text{ V}$ ,	Switch OFF, see Figure 12	25°C	1.95 V		-5	0.3	5 <sup>(2)</sup>	nA
				Full			-50	50		
$I_{COM(PWROFF)}$		$V_{COM} = 0\text{ to }1.95\text{ V}$ , $V_{NO} = 1.95\text{ V to }0$ ,	Switch OFF, see Figure 12	25°C	0 V		-2	0.05	2 <sup>(2)</sup>	$\mu\text{A}$
				Full			-10	10		
$I_{NO(ON)}$	NO ON leakage current	$V_{NO} = 0.3\text{ V}$ , $V_{COM} = \text{Open}$ , or $V_{NO} = 1.65\text{ V}$ , $V_{COM} = \text{Open}$ ,	Switch ON, see Figure 13	25°C	1.95 V		-2	0.3	2 <sup>(2)</sup>	nA
				Full			-20	20		
$I_{COM(ON)}$	COM ON leakage current	$V_{NO} = \text{Open}$ , $V_{COM} = 0.3\text{ V}$ , or $V_{NO} = \text{Open}$ , $V_{COM} = 1.65\text{ V}$ ,	Switch ON, see Figure 13	25°C	1.95 V		-2	0.3	2	nA
				Full			-20	20		
<b>Digital Control Inputs (IN1, IN2)</b>										
$V_{IH}$	Input logic high			Full		1.5		5.5	V	
$V_{IL}$	Input logic low			Full		0		0.6	V	
$I_{IH}, I_{IL}$	Input leakage current	$V_I = 5.5\text{ V or }0$		25°C	1.95 V		-2	0.3	2	$\mu\text{A}$
				Full			-20	20		
<b>Dynamic</b>										
$Q_C$	Charge injection	$V_{GEN} = 0$ , $R_{GEN} = 0$ ,	$C_L = 1\text{ nF}$ , see Figure 19	25°C	1.8 V		2		pC	
$C_{NO(OFF)}$	NO OFF capacitance	$V_{NO} = V_+ \text{ or GND}$ , Switch OFF,	See Figure 14	25°C	1.8 V		19.5		pF	
$C_{COM(OFF)}$	COM OFF capacitance	$V_{COM} = V_+ \text{ or GND}$ , Switch OFF,	See Figure 14	25°C	1.8 V		18.5		pF	
$C_{NO(ON)}$	NO ON capacitance	$V_{NO} = V_+ \text{ or GND}$ , Switch ON,	See Figure 14	25°C	1.8 V		36.5		pF	

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

(2) Not tested in production.

## Electrical Characteristics: 1.8-V Supply (continued)

 $V_+ = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		$T_A$	$V_+$	MIN	TYP	MAX	UNIT
$C_{\text{COM(ON)}}$	COM ON capacitance	$V_{\text{COM}} = V_+$ or GND, Switch ON,	See <a href="#">Figure 14</a>	25°C	1.8 V		36.5		pF
$C_I$	Digital input capacitance	$V_I = V_+$ or GND,	See <a href="#">Figure 14</a>	25°C	1.8 V		2		pF
BW	Bandwidth	$R_L = 50\ \Omega$ , Switch ON,	See <a href="#">Figure 16</a>	25°C	1.8 V		150		MHz
$O_{\text{ISO}}$	OFF isolation	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	Switch OFF, see <a href="#">Figure 17</a>	25°C	1.8 V		-62		dB
THD	Total harmonic distortion	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ ,	$f = 20\text{ Hz to }20\text{ kHz}$ , see <a href="#">Figure 20</a>	25°C	1.8 V		0.055%		
<b>Supply</b>									
$I_+$	Positive supply current	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	1.95 V		0.001	0.01	$\mu\text{A}$
				Full				0.15	

## 6.9 Switching Characteristics: 5-V Supply

 $V_+ = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Dynamic</b>									
$t_{\text{ON}}$	Turnon time	$V_{\text{COM}} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , see <a href="#">Figure 15</a>	25°C	5 V	1	4.5	7.5	ns
				Full	4.5 V to 5.5 V	1		9	
$t_{\text{OFF}}$	Turnoff time	$V_{\text{COM}} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , see <a href="#">Figure 15</a>	25°C	5 V	4.5	8	11	ns
				Full	4.5 V to 5.5 V	3.5		13	

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

## 6.10 Switching Characteristics: 3.3-V Supply

 $V_+ = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Dynamic</b>									
$t_{\text{ON}}$	Turnon time	$V_{\text{COM}} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , see <a href="#">Figure 15</a>	25°C	3.3 V	1.5	5	9.5	ns
				Full	3 V to 3.6 V	1		10	
$t_{\text{OFF}}$	Turnoff time	$V_{\text{COM}} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , see <a href="#">Figure 15</a>	25°C	3.3 V	4.5	8.5	11	ns
				Full	3 V to 3.6 V	3		12.5	

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

## 6.11 Switching Characteristics: 2.5-V Supply

 $V_+ = 2.3\text{ V to }2.7\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Dynamic</b>									
$t_{\text{ON}}$	Turnon time	$V_{\text{COM}} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , see <a href="#">Figure 15</a>	25°C	2.5 V	2	6	10	ns
				Full	2.3 V to 2.7 V	1		12	
$t_{\text{OFF}}$	Turnoff time	$V_{\text{COM}} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , see <a href="#">Figure 15</a>	25°C	2.5 V	4.5	8	12.5	ns
				Full	2.3 V to 2.7 V	3		15	

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

## 6.12 Switching Characteristics: 1.8-V Supply

 $V_+ = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS		$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Dynamic</b>									
$t_{ON}$	Turnon time	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , see <a href="#">Figure 15</a>	25°C	1.8 V	3	9	18	ns
				Full	1.65 V to 1.95 V	1		20	
$t_{OFF}$	Turnoff time	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , see <a href="#">Figure 15</a>	25°C	1.8 V	5	10	15.5	ns
				Full	1.65 V to 1.95 V	4		18.5	

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

### 6.13 Typical Characteristics

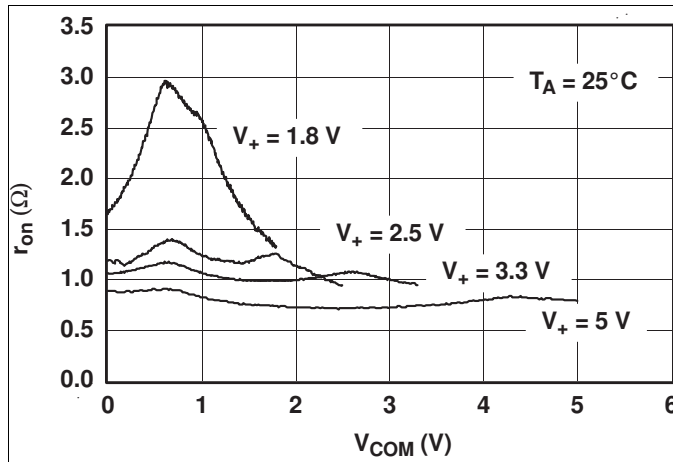


Figure 1.  $r_{on}$  vs  $V_{COM}$

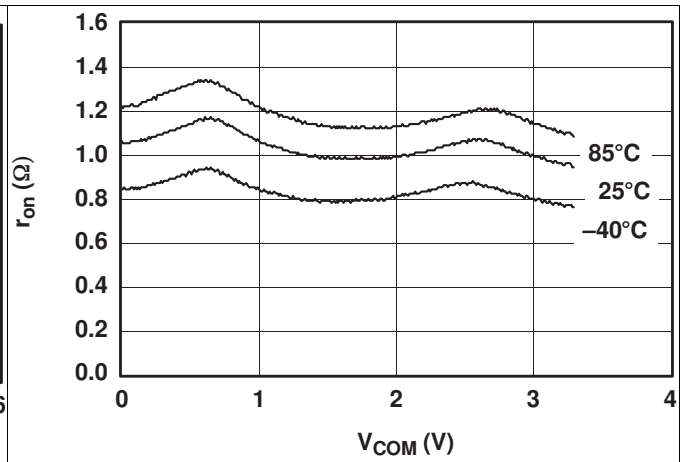


Figure 2.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 3.3$  V)

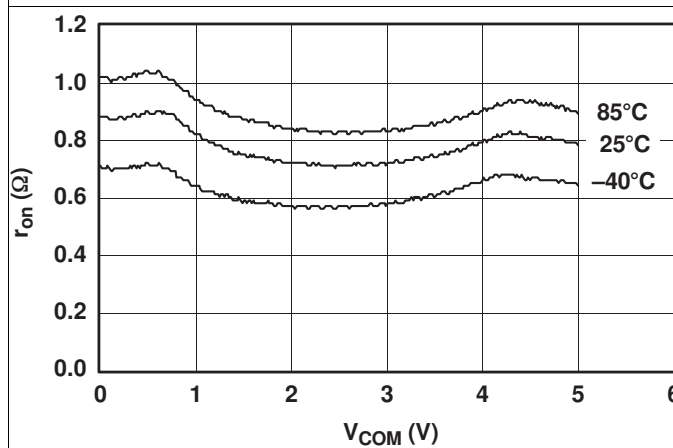


Figure 3.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 5$  V)

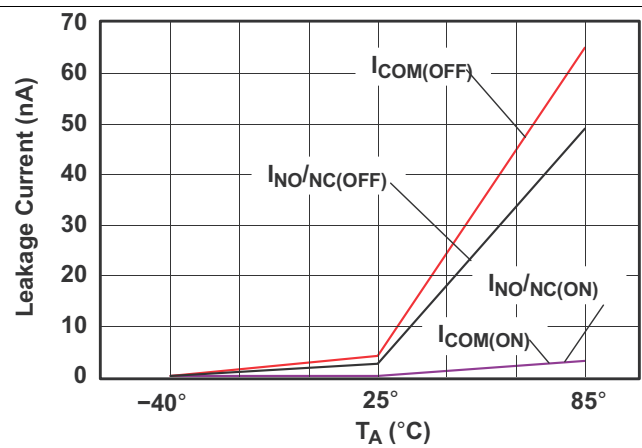


Figure 4. Leakage Current vs Temperature ( $V_+ = 5.5$  V)

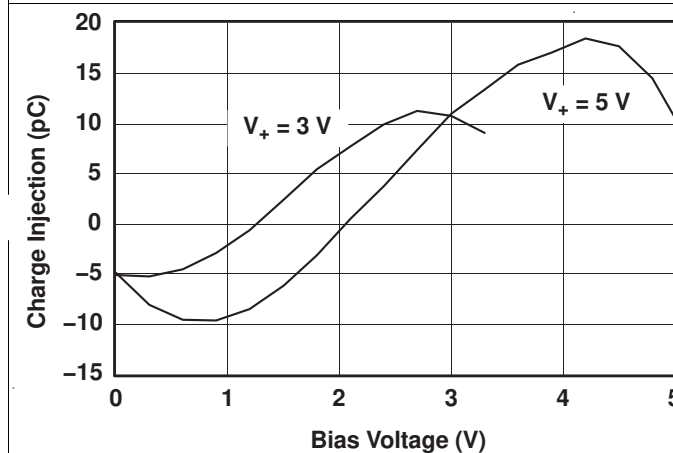


Figure 5. Charge Injection ( $Q_C$ ) vs  $V_{COM}$

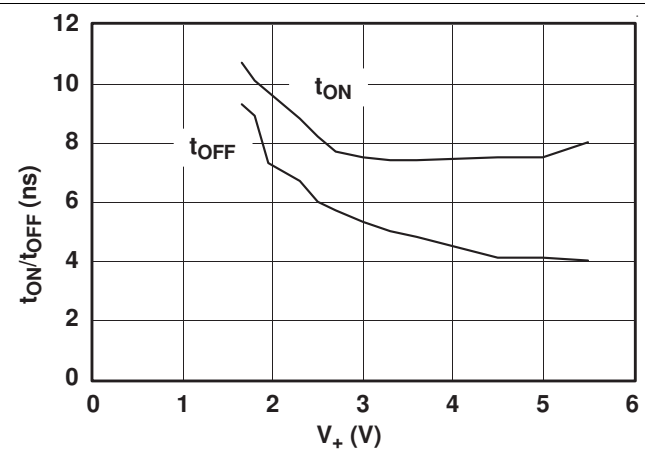


Figure 6.  $t_{ON}$  and  $t_{OFF}$  vs Supply Voltage

Typical Characteristics (continued)

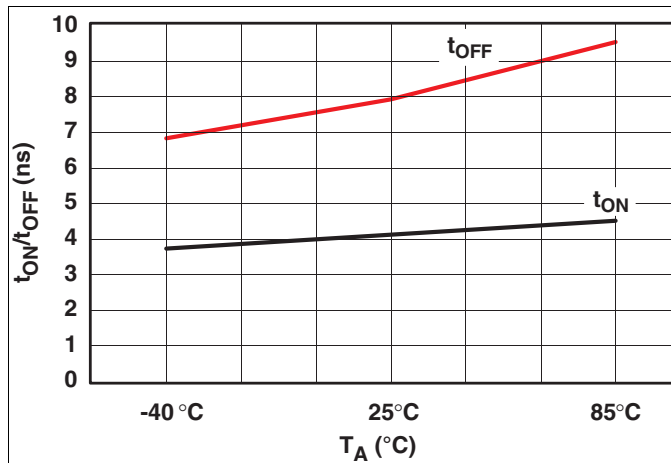


Figure 7. t<sub>ON</sub> and t<sub>OFF</sub> vs Temperature (V<sub>+</sub> = 5 V)

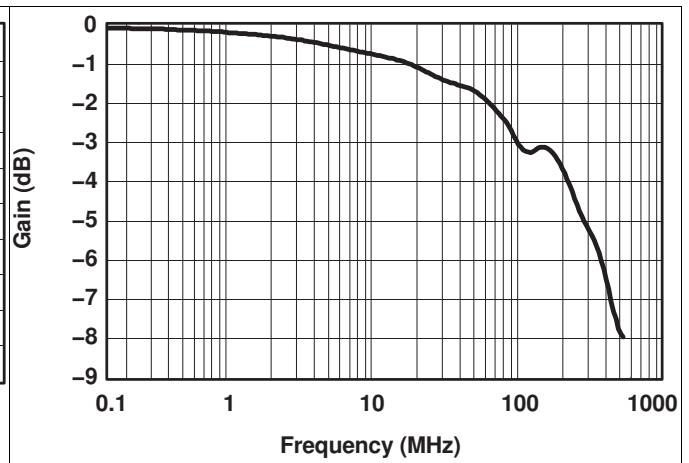


Figure 8. Bandwidth (V<sub>+</sub> = 5 V)

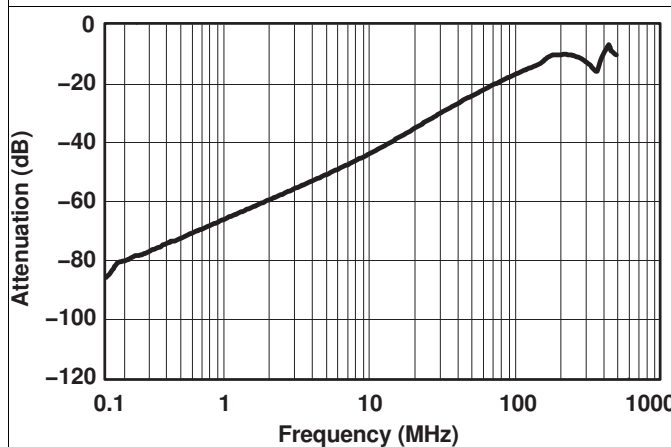


Figure 9. OFF Isolation and Crosstalk (V<sub>+</sub> = 5 V)

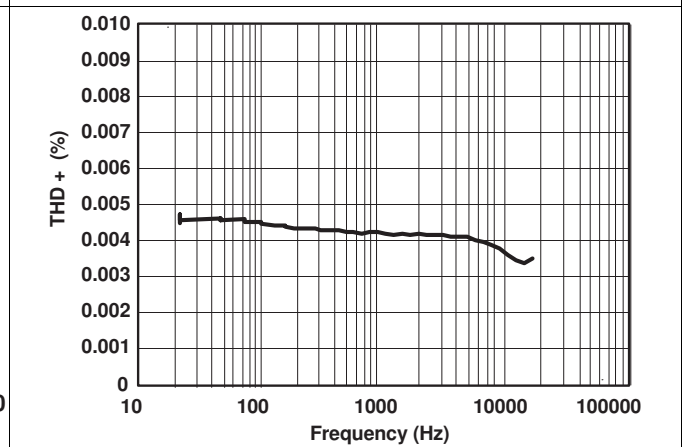


Figure 10. Total Harmonic Distortion vs Frequency

## 7 Parameter Measurement Information

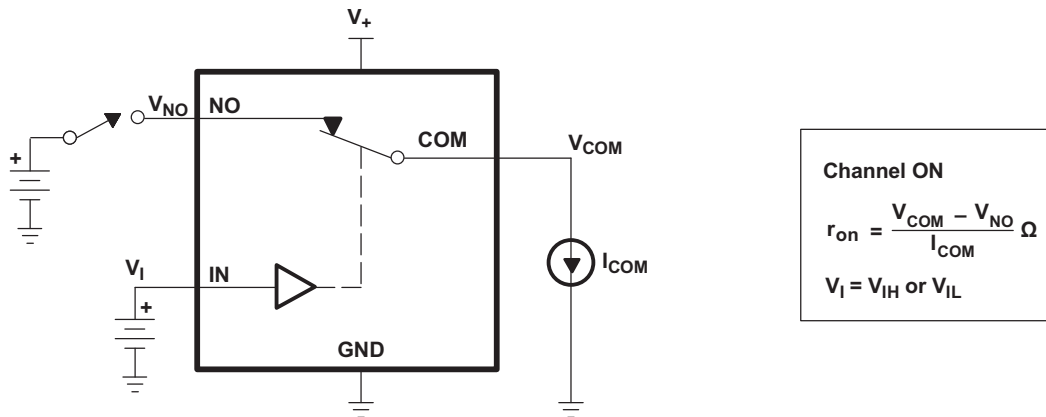


Figure 11. ON-State Resistance ( $r_{on}$ )

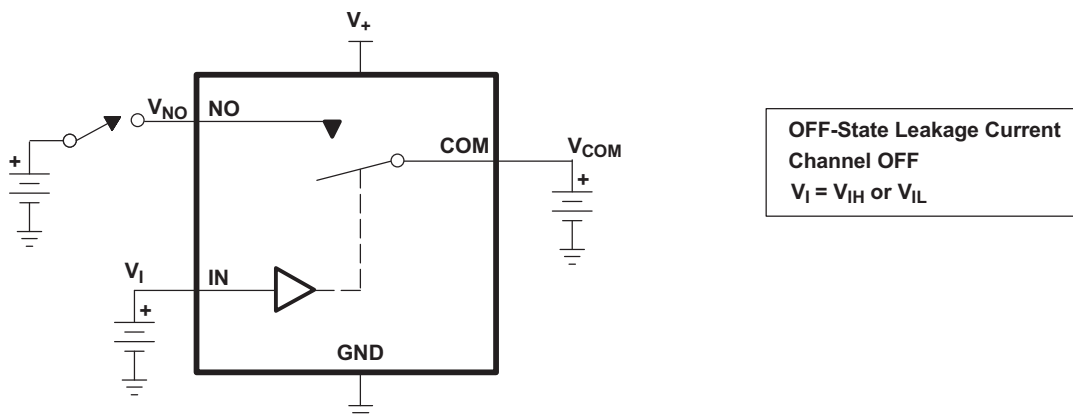


Figure 12. OFF-State Leakage Current ( $I_{COM(OFF)}$ ,  $I_{NC(OFF)}$ ,  $I_{COM(PWROFF)}$ ,  $I_{NC(PWR(F))}$ )

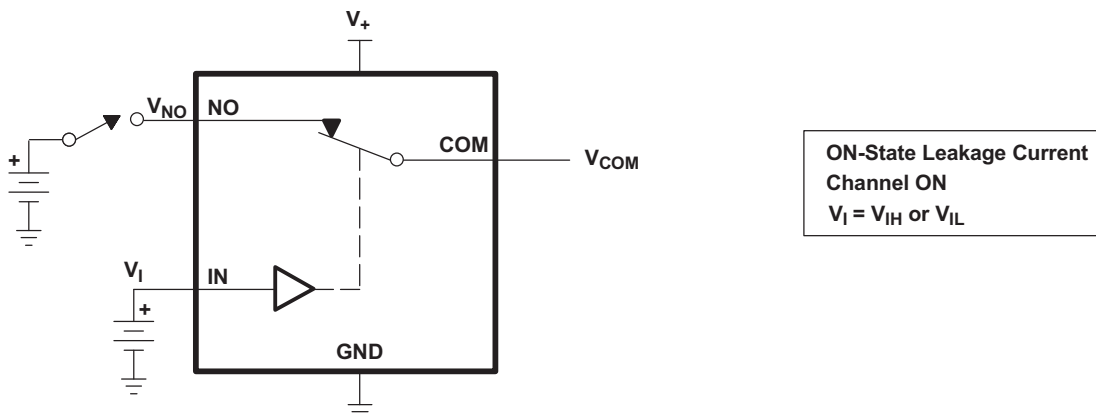


Figure 13. ON-State Leakage Current ( $I_{COM(ON)}$ ,  $I_{NC(ON)}$ )

Parameter Measurement Information (continued)

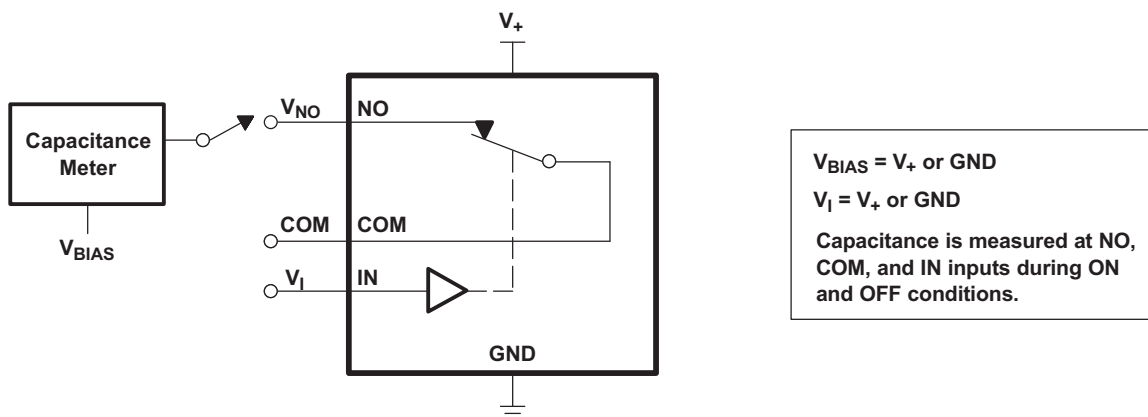
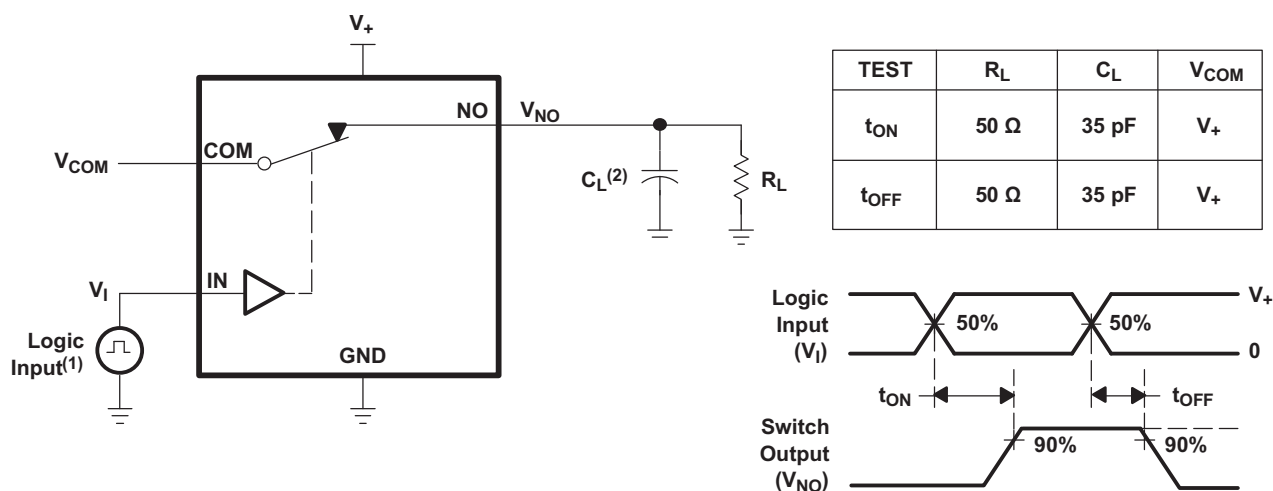


Figure 14. Capacitance ( $C_I$ ,  $C_{COM(OFF)}$ ,  $C_{COM(ON)}$ ,  $C_{NC(OFF)}$ ,  $C_{NC(ON)}$ )



- (1) All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.
- (2)  $C_L$  includes probe and jig capacitance.

Figure 15. Turnon ( $t_{ON}$ ) and Turnoff Time ( $t_{OFF}$ )

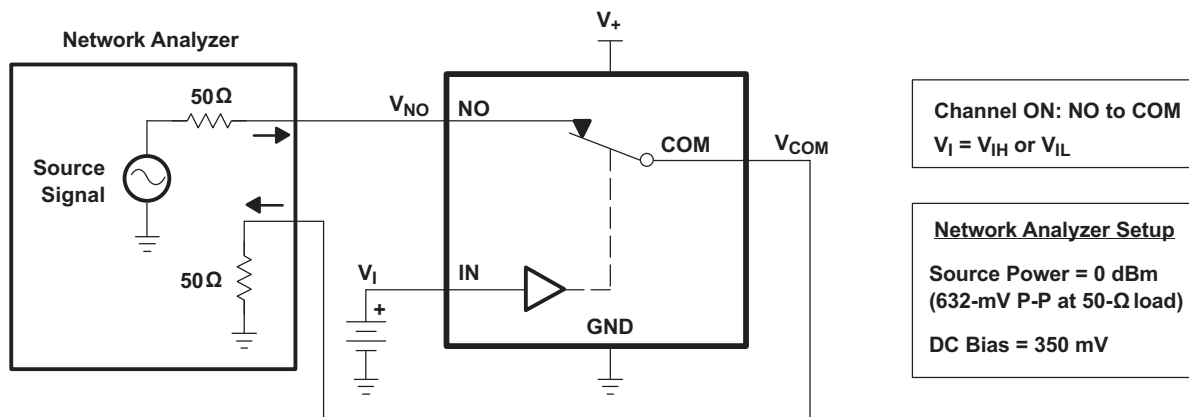


Figure 16. Bandwidth (BW)

Parameter Measurement Information (continued)

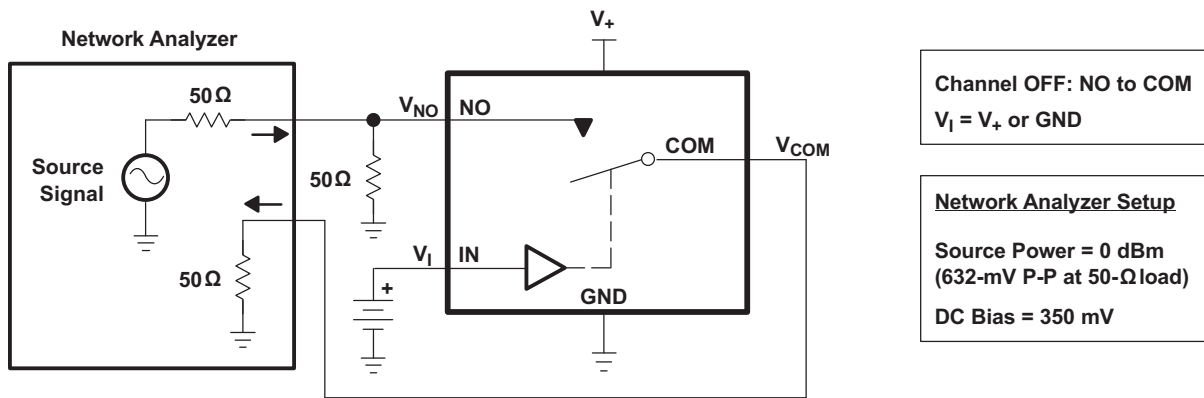


Figure 17. OFF Isolation ( $O_{ISO}$ )

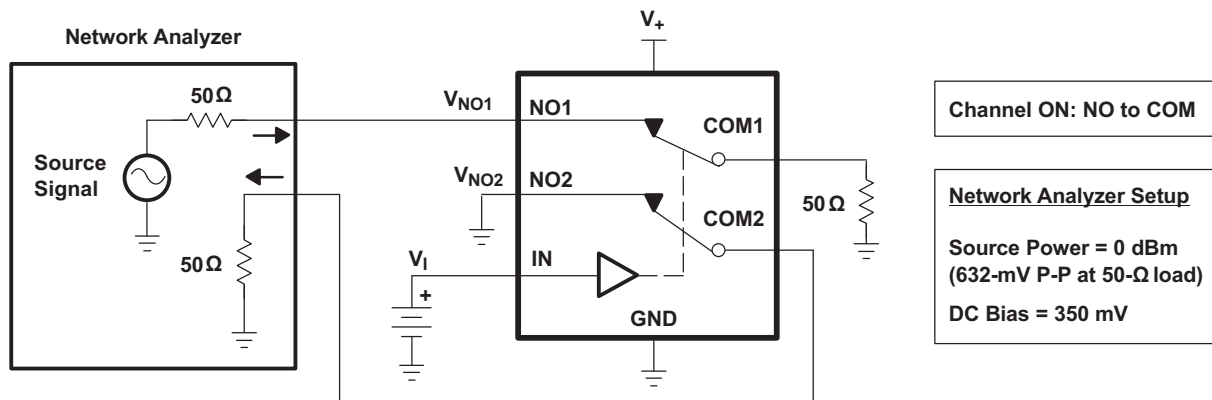
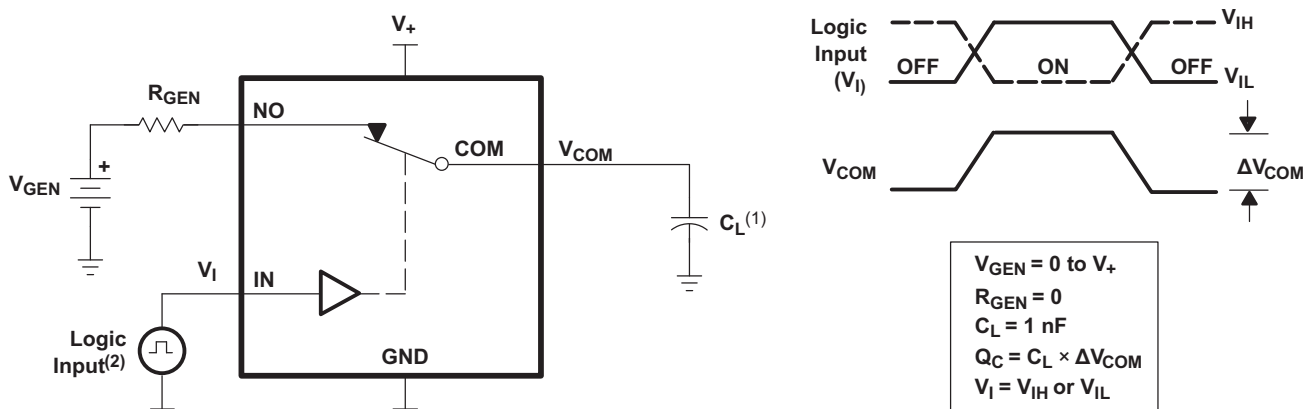


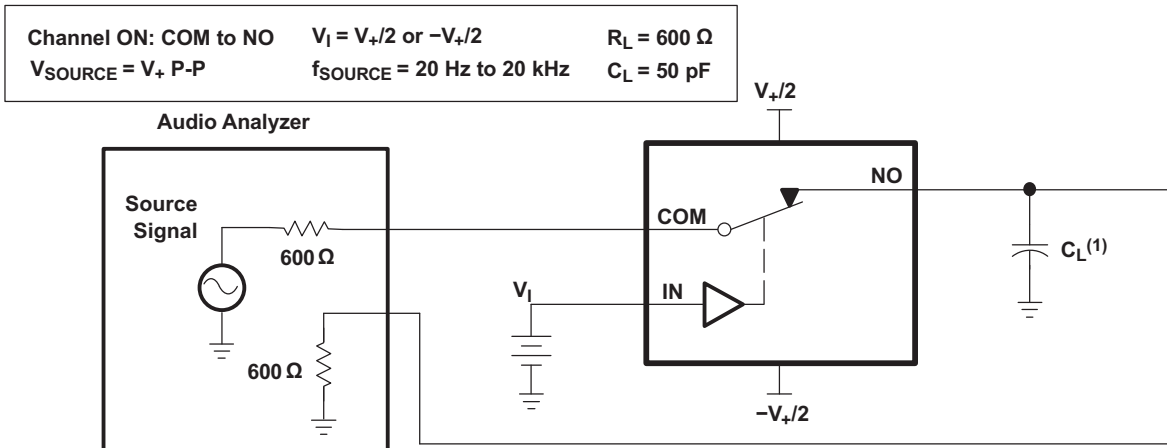
Figure 18. Crosstalk ( $X_{TALK}$ )



- (1)  $C_L$  includes probe and jig capacitance.
- (2) All input pulses are supplied by generators having the following characteristics:  
 $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r < 5 \text{ ns}$ ,  $t_f < 5 \text{ ns}$ .

Figure 19. Charge Injection ( $Q_C$ )

Parameter Measurement Information (continued)



(1)  $C_L$  includes probe and jig capacitance.

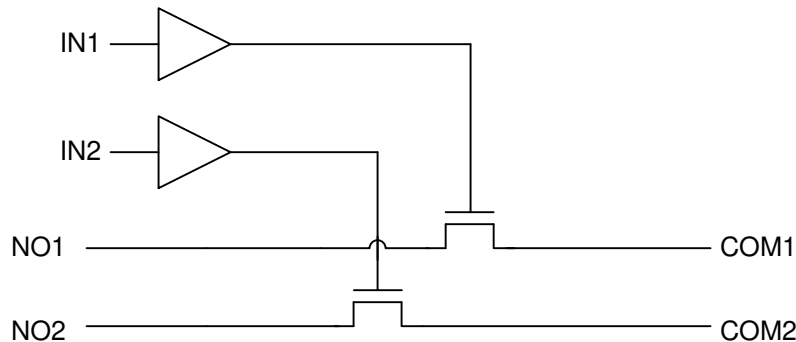
Figure 20. Total Harmonic Distortion (THD)

## 8 Detailed Description

### 8.1 Overview

The TS5A23166 is a dual single-pole single-throw (SPST) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications. [Table 2](#) shows the descriptions of each parameter specified in the datasheet.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

Tolerant control inputs allow 5-V logic levels to be present on the IN pin at any value of  $V_{CC}$ . Low ON-resistance allows minimal signal distortion through device.

### 8.4 Device Functional Modes

[Table 1](#) shows the functional modes for TS5A23166.

**Table 1. Function Table**

IN	NO TO COM, COM TO NO
L	OFF
H	ON

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TS5A23166 dual SPST analog switch is a basic component that could be used in any electrical system design. One example application is a gain selector, which is described in the *Typical Application* section.

### 9.2 Typical Application

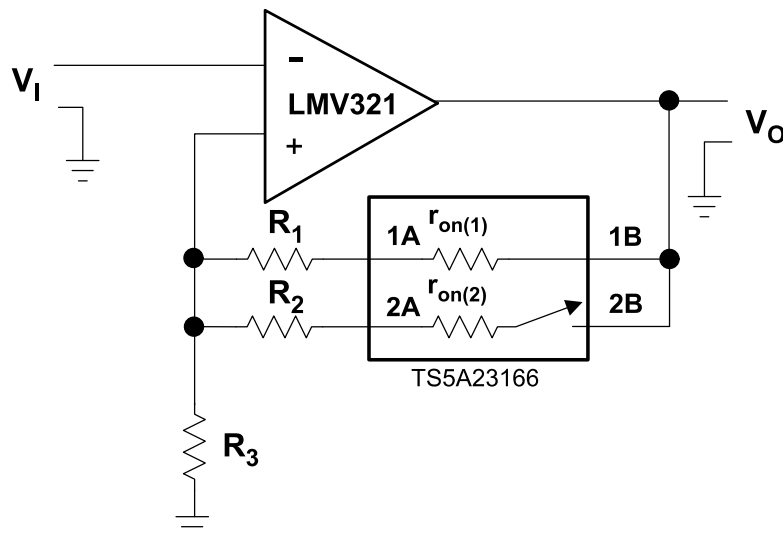


Figure 21. Gain-Control Circuit for OP Amplifier

#### 9.2.1 Design Requirements

By selecting values of  $R_1$  and  $R_2$ , such that  $R_x \gg r_{on(x)}$ ,  $r_{on}$  of TS5A23166 can be ignored. The gain of op amp can be calculated as follow:

$$V_o / V_i = 1 + R_{||} / R_3 \quad (1)$$

$$R_{||} = (R_1 + r_{on(1)}) || (R_2 + r_{on(2)}) \quad (2)$$

#### 9.2.2 Detailed Design Procedure

Place a switch in series with the input of the op amp. Because the op amp input impedance is very large, a switch on  $r_{on(1)}$  is irrelevant.

## Typical Application (continued)

### 9.2.3 Application Curve

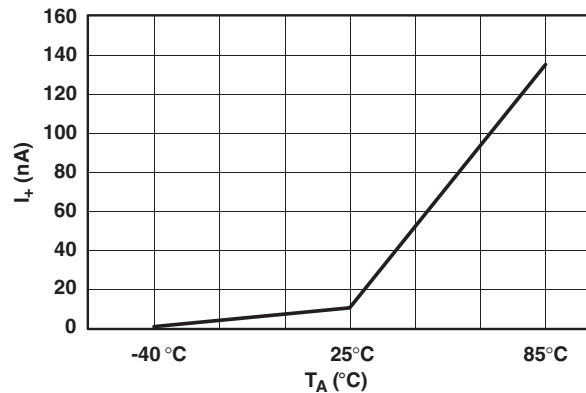


Figure 22. Power-Supply Current vs Temperature (V<sub>+</sub> = 5 V)

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#).

Each V<sub>CC</sub> terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF bypass capacitor is recommended. If there are multiple pins labeled V<sub>CC</sub>, then a 0.01-μF or 0.022-μF capacitor is recommended for each V<sub>CC</sub> because the VCC pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V<sub>CC</sub> and V<sub>DD</sub>, a 0.1-μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. [Figure 23](#) shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

### 11.2 Layout Example

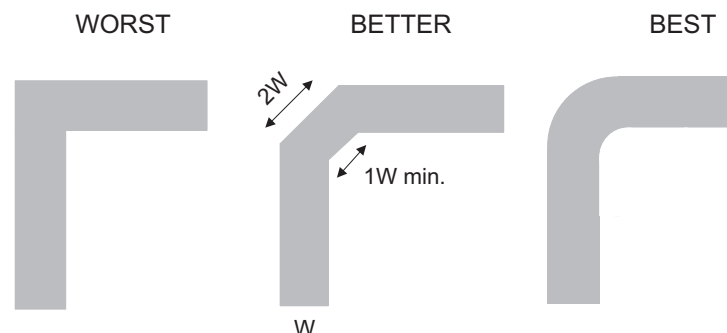


Figure 23. Trace Example

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Device Nomenclature

**Table 2. Parameter Description**

SYMBOL	DESCRIPTION
$V_{COM}$	Voltage at COM
$V_{NO}$	Voltage at NO
$r_{on}$	Resistance between COM and NO ports when the channel is ON
$r_{peak}$	Peak on-state resistance over a specified voltage range
$r_{on(Flat)}$	Difference between the maximum and minimum value of $r_{on}$ in a channel over the specified range of conditions
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF-state under worst-case input and output conditions
$I_{NO(PWROFF)}$	Leakage current measured at the NO port during the power-down condition, $V_+ = 0$
$I_{COM(OFF)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the OFF-state under worst-case input and output conditions
$I_{COM(PWROFF)}$	Leakage current measured at the COM port during the power-down condition, $V_+ = 0$
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON-state and the output (COM) open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the ON-state and the output (NO) open
$V_{IH}$	Minimum input voltage for logic high for the control input (IN)
$V_{IL}$	Maximum input voltage for logic low for the control input (IN)
$V_I$	Voltage at the control input (IN)
$I_{IH}, I_{IL}$	Leakage current measured at the control input (IN)
$t_{ON}$	Turnon time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON.
$t_{OFF}$	Turnoff time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF.
$Q_C$	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$ . $C_L$ is the load capacitance, and $\Delta V_{COM}$ is the change in analog output voltage.
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{COM(OFF)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is OFF
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is ON
$C_I$	Capacitance of control input (IN)
$O_{ISO}$	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NO to COM) in the OFF state.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
$I_+$	Static power-supply current with the control (IN) pin at $V_+$ or GND

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 12.4 Trademarks

E2E is a trademark of Texas Instruments.

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## 12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A23166DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	(AM, JAMQ, JAMR) JZ	<a href="#">Samples</a>
TS5A23166DCURG4	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAMR	<a href="#">Samples</a>
TS5A23166YZPR	ACTIVE	DSBGA	YZP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	JMN	<a href="#">Samples</a>
TS5A23166YZTR	ACTIVE	DSBGA	YZT	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	JMN	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

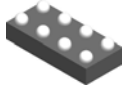
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A23166DCUR	VSSOP	DCU	8	3000	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
TS5A23166DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TS5A23166DCUR	VSSOP	DCU	8	3000	180.0	9.0	2.25	3.4	1.0	4.0	8.0	Q3
TS5A23166DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TS5A23166YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1
TS5A23166YZTR	DSBGA	YZT	8	3000	178.0	9.2	1.02	2.02	0.75	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A23166DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
TS5A23166DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
TS5A23166DCUR	VSSOP	DCU	8	3000	182.0	182.0	20.0
TS5A23166DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
TS5A23166YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0
TS5A23166YZTR	DSBGA	YZT	8	3000	220.0	220.0	35.0

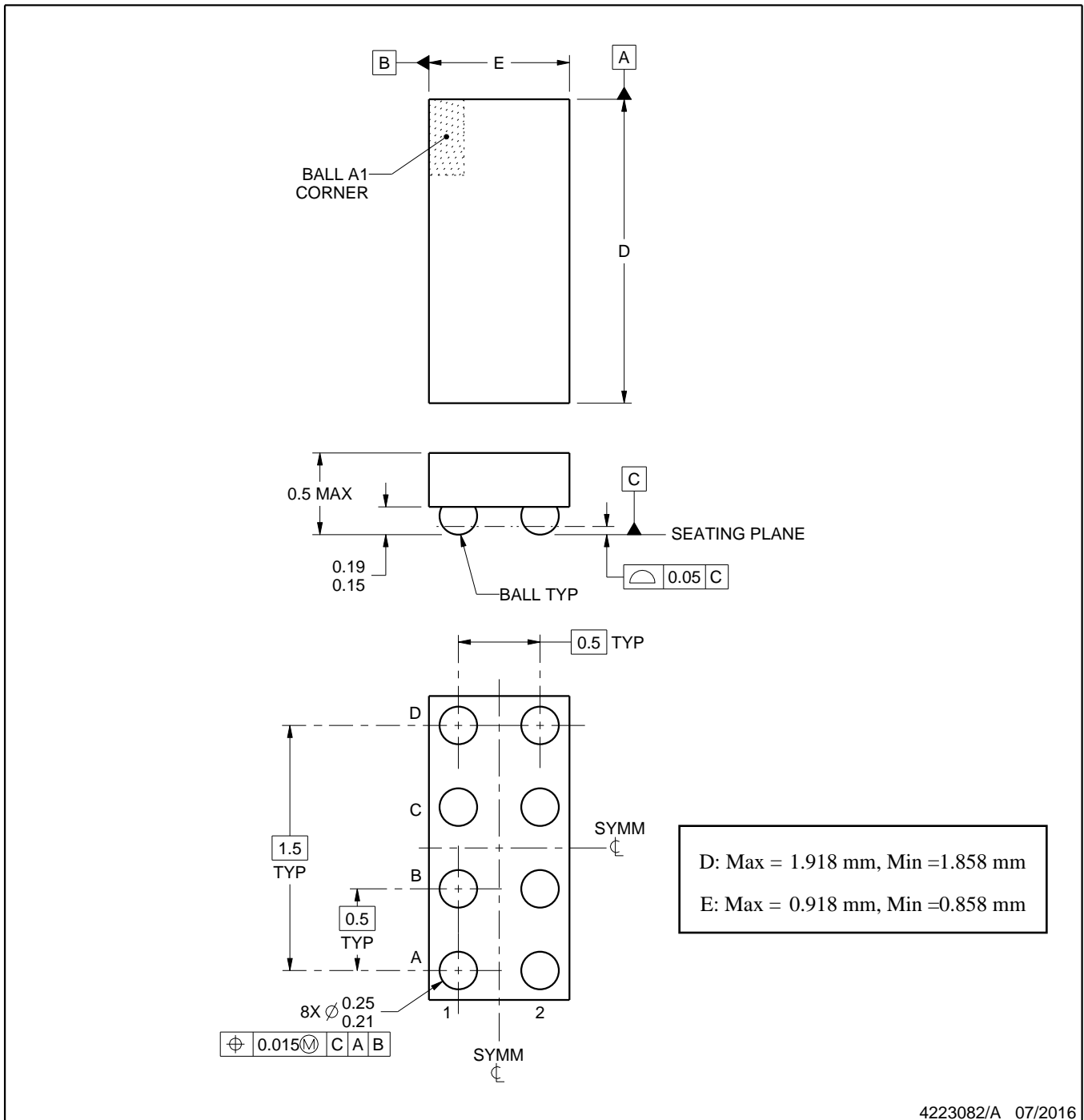
YZP0008



# PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

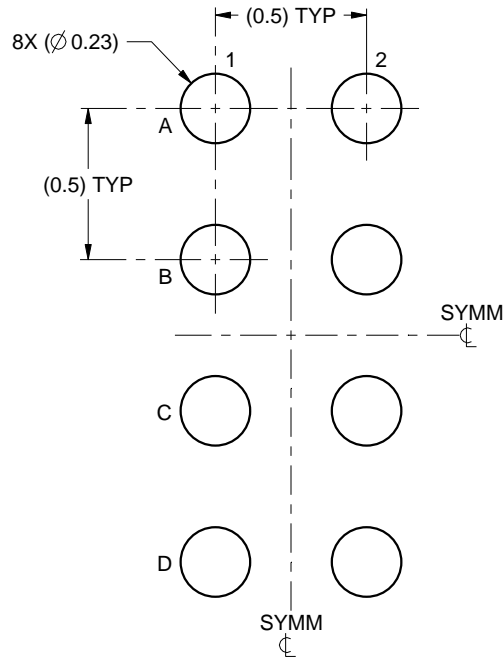
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

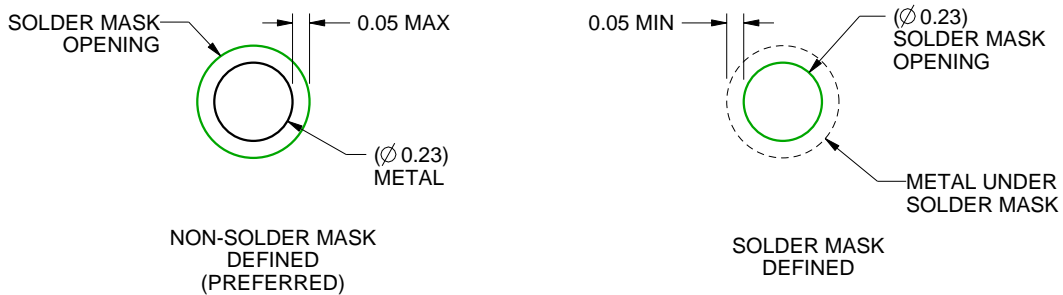
YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS  
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

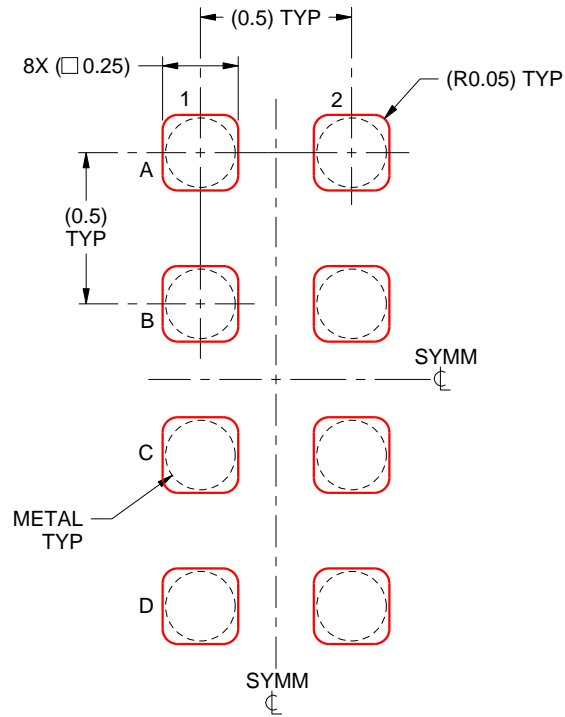
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

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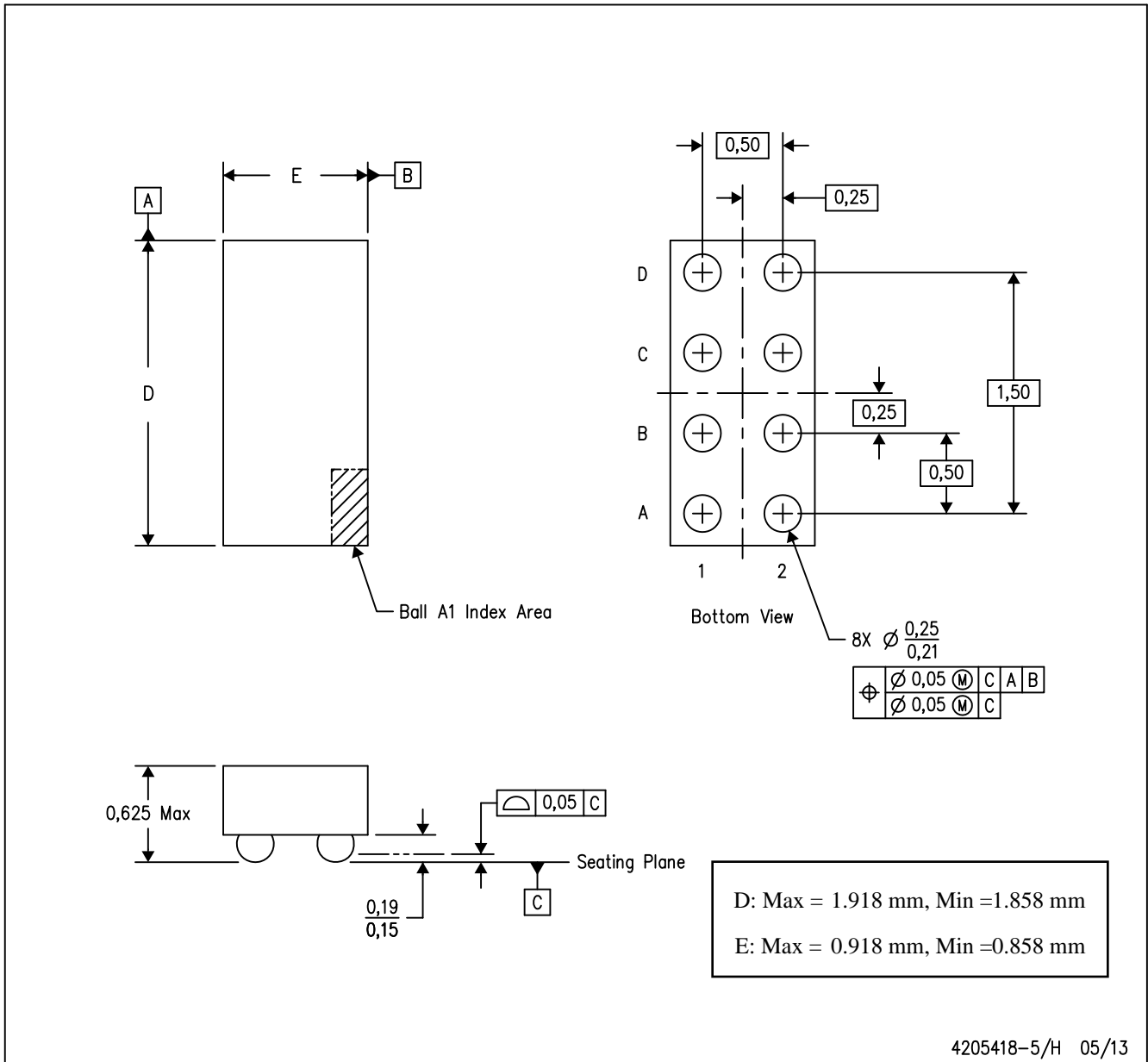
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

# MECHANICAL DATA

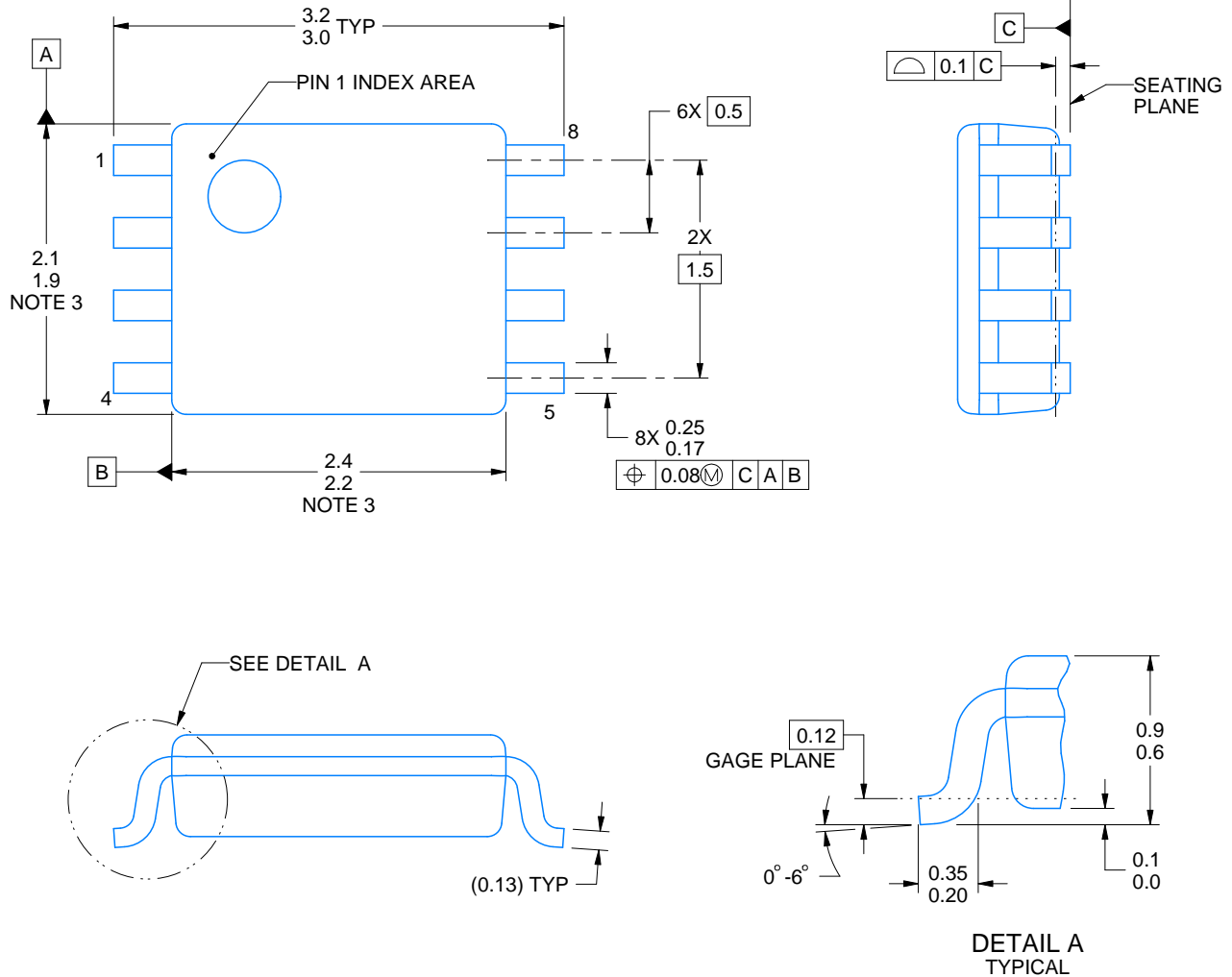
YZT (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.



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NOTES:

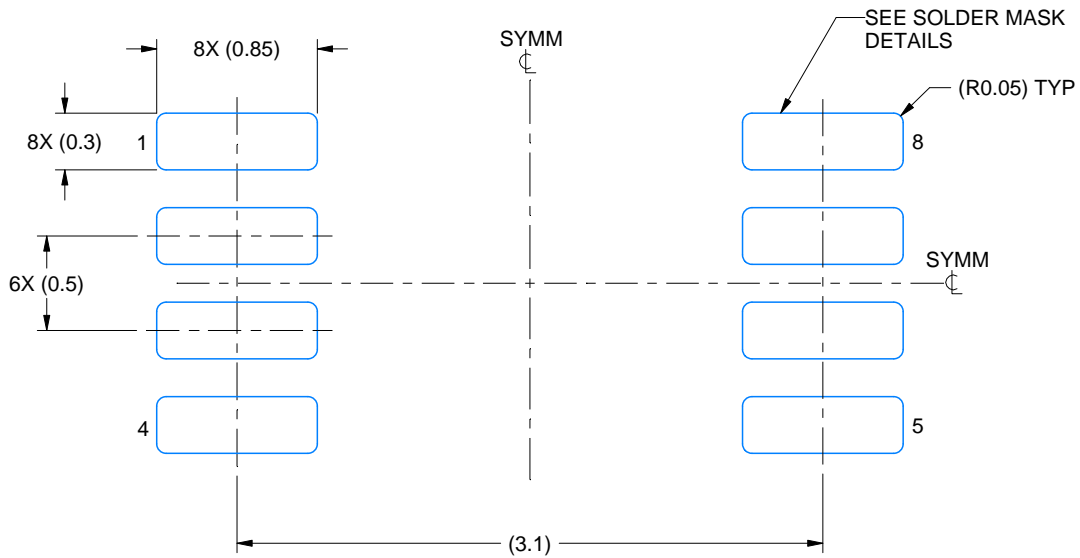
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

# EXAMPLE BOARD LAYOUT

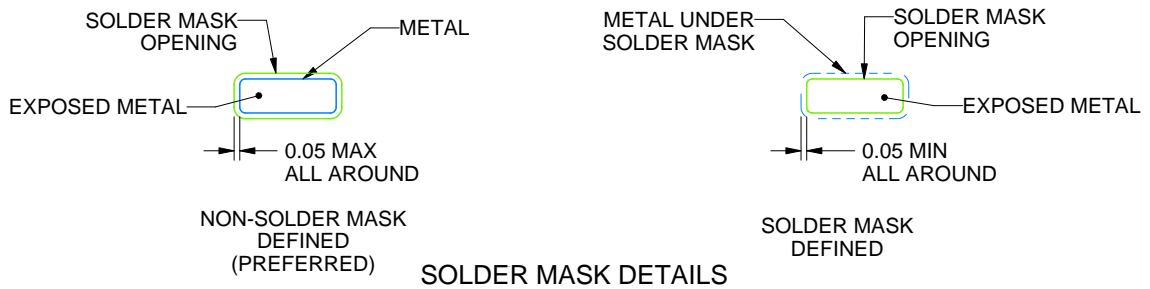
DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

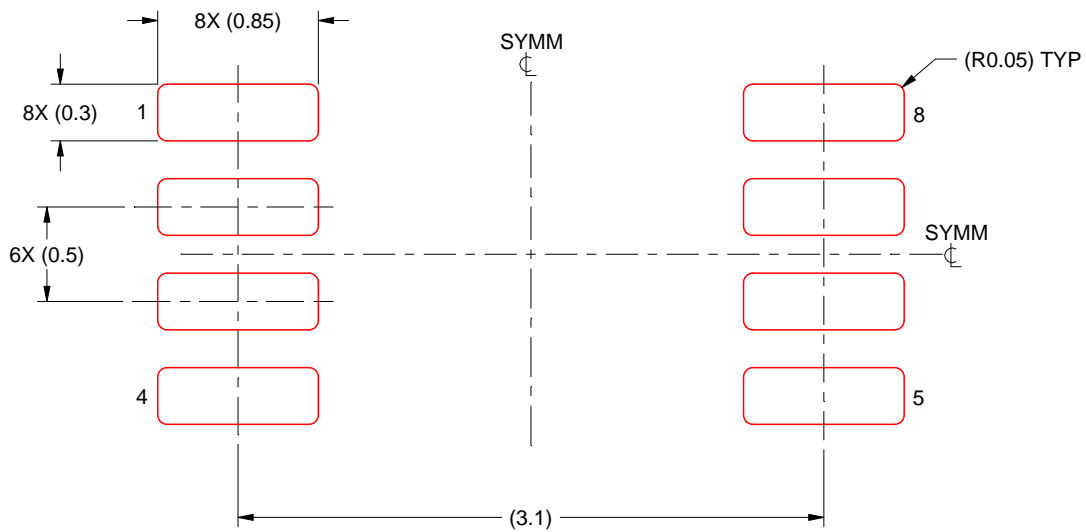
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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