



**THE DATASHEET OF
TS5A12301EYFPR**



TS5A12301E IEC Level 4 ESD-protected 0.75- Ω SPDT Analog Switch With 1.8-V Compatible Input Logic

1 Features

- Low ON-State Resistance (0.75 Ω)
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Isolation in Power-Down Mode, $V_{CC} = 0$
- Specified Break-Before-Make Switching
- 2.25-V to 5.5-V Power Supply (V_{CC})
- 6-M Ω Input Pulldown Allows Control Input (IN) to Be Unconnected
- 1.8-V Compatible Control Input Threshold Independent of V_{CC}
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 3000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- ESD Performance COM Port to GND
 - 8000-V Human-Body Model (A114-B, Class II)
 - ± 8 -kV Contact Discharge (IEC 61000-4-2)
 - ± 15 -kV Air-Gap Discharge (IEC 61000-4-2)

2 Applications

- Cell Phones
- PDAs
- Portable Instrumentation
- MP3 Players
- Portable Media Players

3 Description

The TS5A12301E device is a bidirectional, 1-channel, single-pole double-throw (SPDT) analog switch that is designed to operate from 2.25 V to 5.5 V. The device offers a low ON-state resistance with excellent channel-to-channel ON-state resistance matching and the break-before-make feature to prevent signal distortion during the transferring of a signal from one path to another.

The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications. The control input (IN) pin can be connected to low-voltage GPIOs, allowing it to be controlled by 1.8-V signals.

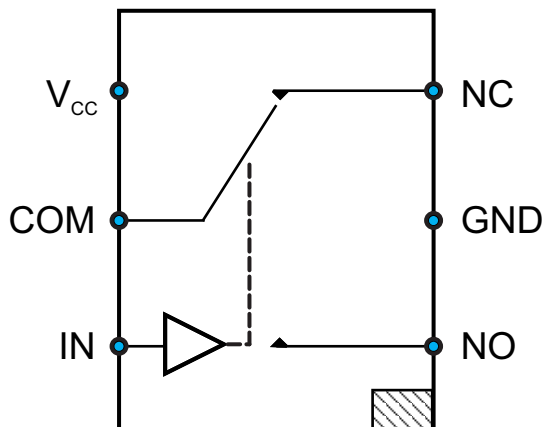
The TS5A12301E has ± 15 -kV air-gap discharge and ± 8 -kV contact discharge ESD protection for the COM port to GND, which makes it compliant with the IEC Level 4 ESD standard (IEC 61000-4-2).

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|-----------|--------------------------|
| TS5A12301E | DSBGA (6) | 1.16 mm \times 0.76 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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Table of Contents

| | | | |
|---|----|--|----|
| 1 Features | 1 | 8.2 Functional Block Diagram | 16 |
| 2 Applications | 1 | 8.3 Feature Description | 16 |
| 3 Description | 1 | 8.4 Device Functional Modes | 16 |
| 4 Revision History | 2 | 9 Application and Implementation | 17 |
| 5 Pin Configuration and Functions | 3 | 9.1 Application Information | 17 |
| 6 Specifications | 4 | 9.2 Typical Application | 17 |
| 6.1 Absolute Maximum Ratings | 4 | 10 Power Supply Recommendations | 18 |
| 6.2 ESD Ratings | 4 | 11 Layout | 18 |
| 6.3 Recommended Operating Conditions | 4 | 11.1 Layout Guidelines | 18 |
| 6.4 Thermal Information | 5 | 11.2 Layout Example | 18 |
| 6.5 Electrical Characteristics – 5-V Supply | 5 | 12 Device and Documentation Support | 19 |
| 6.6 Electrical Characteristics – 3.3-V Supply | 7 | 12.1 Receiving Notification of Documentation Updates | 19 |
| 6.7 Electrical Characteristics – 2.5-V Supply | 8 | 12.2 Community Resources | 19 |
| 6.8 Typical Characteristics | 10 | 12.3 Trademarks | 19 |
| 7 Parameter Measurement Information | 12 | 12.4 Electrostatic Discharge Caution | 19 |
| 8 Detailed Description | 16 | 12.5 Glossary | 19 |
| 8.1 Overview | 16 | 13 Mechanical, Packaging, and Orderable Information | 19 |

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2011) to Revision C

Page

| | |
|--|----|
| • Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. | 1 |
| • Changed all references of V+ pin to V _{CC} | 1 |
| • Deleted <i>Ordering Information</i> table; see POA at the end of the data sheet | 1 |
| • Deleted <i>Summary of Characteristics</i> table | 1 |
| • Changed continuous current parameter symbol from: I+ to: ICC | 4 |
| • Moved the on-state switch current and on-state peak switch current parameters to the <i>Recommended Operating Conditions</i> | 4 |
| • Changed R _{thetaJA} value for the YFP package from: 154.2°C/W to: 123.4°C/W | 5 |
| • Removed analog signal range parameters from the <i>Electrical Characteristics</i> tables | 5 |
| • Deleted Leakage Current vs Temperature (V _{CC} = 5 V) graph | 10 |
| • Deleted Control Input Thresholds graph | 10 |
| • Added ohm symbols to Figure 18 , Figure 19 , and Figure 22 | 14 |

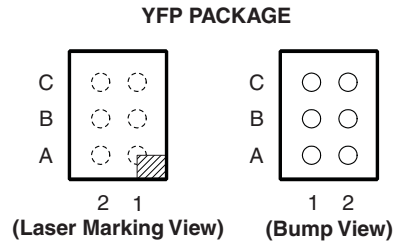
Changes from Revision A (December 2009) to Revision B

Page

| | |
|-----------------------------|---|
| • Added Logic Diagram | 1 |
|-----------------------------|---|

5 Pin Configuration and Functions

YFP Package
6-Pin DSBGA
Top View



Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----------------|-----|-----|---|
| NAME | NO. | | |
| COM | B2 | I/O | Common signal path |
| GND | B1 | — | Ground |
| IN | A2 | I | Digital control: High = COM connected to NO Low = COM connected to NC Floating = COM connected to NC |
| NC | C1 | I/O | Normally closed signal path |
| NO | A1 | I/O | Normally open signal path |
| V _{CC} | C2 | — | Power supply |

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

| | | MIN | MAX | UNIT |
|---------------------------------------|--|--|----------------|------|
| V_{CC} | Supply voltage ⁽³⁾ | -0.5 | 6.5 | V |
| V_{NC} , V_{NO} , V_{COM} | Analog voltage ⁽³⁾⁽⁴⁾ | -0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | Analog port diode current | $V_{CC} < V_{NC}, V_{NO}, V_{COM}$, or $V_{NC}, V_{NO}, V_{COM} < 0$ | | mA |
| V_{IN} | Digital input voltage ⁽³⁾⁽⁵⁾ | -0.5 | 6.5 | V |
| I_{IK} | Digital input clamp current | $V_I < 0$ | | mA |
| I_{CC} , I_{GND} | Continuous current through V_{CC} or GND | -100 | 100 | mA |
| T_{stg} | Storage temperature | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention (whereby the most negative value is a minimum and the most positive value is a maximum)
- (3) All voltages are with respect to ground (unless otherwise specified).
- (4) This value is limited to 5.5 V maximum.
- (5) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

6.2 ESD Ratings

| | | VALUE | UNIT |
|-------------|-------------------------|--|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | |
| | | Contact discharge (IEC 61000-4-2) | |
| | | Air-gap discharge (IEC 61000-4-2) | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------------------------------|---|---|----------|------|
| V_{CC} | Supply voltage | 2.25 | 5.5 | V |
| V_{NC} , V_{NO} , V_{COM} | Analog voltage | 0 | V_{CC} | V |
| V_{IN} | Digital input voltage | 0 | 5.5 | V |
| I_{NC} , I_{NO} , I_{COM} | On-state switch current | $V_{NC}, V_{NO}, V_{COM} = 0$ to V_{CC} | | mA |
| | On-state peak switch current ⁽¹⁾ | $V_{NC}, V_{NO}, V_{COM} = 0$ to V_{CC} | | |
| T_A | Operating temperature | -40 | 85 | °C |

- (1) Pulse at 1-ms duration < 10% duty cycle

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TS5A12301E | UNIT |
|-------------------------------|---|-------------|------|
| | | YFP (DSBGA) | |
| | | 6 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance ⁽²⁾ | 123.4 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 1.9 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 37.6 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 0.4 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 37.7 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

(2) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics – 5-V Supply

V_{CC} = 4.5 V to 5.5 V and T_A = –40°C to 85°C (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | | |
|--|--|---|--|-----------------------|-------|------|----|-----|
| ANALOG SWITCH | | | | | | | | |
| r _{on} | ON-state resistance | V _{NO} or V _{NC} = 2.5 V, I _{COM} = –100 mA, and V _{CC} = 4.5 V (see Figure 12) | T _A = 25°C | | 0.5 | 0.75 | Ω | |
| | | | T _A = –40°C to 85°C | | 0.8 | | | |
| Δr _{on} | ON-state resistance match between channels | V _{NO} or V _{NC} = 2.5 V, I _{COM} = –100 mA, and V _{CC} = 4.5 V (see Figure 12) | T _A = 25°C | | 0.05 | 0.1 | Ω | |
| | | | T _A = –40°C to 85°C | | 0.1 | | | |
| r _{on(flat)} | ON-state resistance flatness | 0 ≤ (V _{NO} or V _{NC}) ≤ V _{CC} , I _{COM} = –100 mA, V _{CC} = 4.5 V, and T _A = 25°C (see Figure 12) | | | 0.15 | | Ω | |
| | | | V _{NO} or V _{NC} = 1 V, 1.5 V, 2.5 V, I _{COM} = –100 mA, and V _{CC} = 4.5 V (see Figure 12) | T _A = 25°C | | 0.1 | | 0.2 |
| | | | T _A = –40°C to 85°C | | 0.25 | | | |
| I _{NO(OFF)} , I _{NC(OFF)} | NO and NC OFF leakage current | V _{NO} = 1 V, 4.5 V, V _{COM} = 4.5 V, 1 V, V _{NC} = open, or V _{NO} = 1 V, 4.5 V, V _{COM} = 4.5 V, 1 V, V _{NO} = open, and V _{CC} = 5.5 V (see Figure 13) | T _A = 25°C | | –20 | 2 | 20 | nA |
| | | | T _A = –40°C to 85°C | | –100 | 100 | | |
| I _{NO(PWROFF)} , I _{NC(PWROFF)} | NO and NC PWROFF leakage current | V _{NO} or V _{NC} = 0 V to 5.5 V, V _{COM} = 5.5 V to 0 V, and V _{CC} = 0 V (see Figure 13) | T _A = 25°C | | –10 | 10 | 10 | μA |
| | | | T _A = –40°C to 85°C | | –10 | 10 | | |
| I _{NO(ON)} | NC and NO ON leakage current | V _{NO} = 1 V, 4.5 V, V _{COM} : V _{NC} = open, or V _{NC} = 1 V, 4.5 V, V _{COM} : V _{NO} = open, and V _{CC} = 5.5 V (see Figure 14) | T _A = 25°C | | –20 | 2 | 20 | nA |
| | | | T _A = –40°C to 85°C | | –200 | 200 | | |
| I _{COM(ON)} | COM ON leakage current | V _{COM} = 1 V, 4.5 V, V _{NO} and V _{NC} = open, or V _{COM} = 1 V, 4.5 V, V _{NO} or V _{NC} = open, and V _{CC} = 5.5 V (see Figure 14) | T _A = 25°C | | –20 | 2 | 20 | nA |
| | | | T _A = –40°C to 85°C | | –200 | 200 | | |
| I _{COM(PWROFF)} | COM OFF leakage current | V _{NO} or V _{NC} = 0 V to 5.5 V, V _{COM} = 5.5 V to 0 V, and V _{CC} = 0 V (see Figure 13) | T _A = 25°C | | –10 | 10 | 10 | μA |
| | | | T _A = –40°C to 85°C | | –10 | 10 | | |
| DIGITAL CONTROL INPUT (IN) | | | | | | | | |
| V _{IH} | Input logic high | V _{CC} = 5.5 V and T _A = –40°C to 85°C | | | 1.05 | 5.5 | V | |
| V _{IL} | Input logic low | V _{CC} = 5.5 V and T _A = –40°C to 85°C | | | 0 | 0.65 | V | |
| I _{IH} , I _{IL} | Input leakage current | V _{IN} = 1.95 V or 0 V, V _{CC} = 5.5 V, and T _A = –40°C to 85°C | | | –0.05 | 0.5 | μA | |
| r _{IN} | Input resistance | V _{IN} = 1.95 V, V _{CC} = 5.5 V, and T _A = –40°C to 85°C | | | 6 | | MΩ | |

(1) The algebraic convention (whereby the most negative value is a minimum and the most positive value is a maximum)

Electrical Characteristics – 5-V Supply (continued)
 $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ and $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|--------------------------------|---------------------------|--|--|-------|-----|---------------|----|
| DYNAMIC | | | | | | | |
| t_{ON} | Turnon time | $V_{COM} = V_{CC}$, $R_L = 50 \Omega$, $C_L = 35 \text{ pF}$ (see Figure 16) | $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$ | 110 | 225 | ns | |
| | | | $V_{CC} = 4.5 \text{ V}$ and $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ | | 250 | | |
| t_{OFF} | Turnoff time | $V_{COM} = V_{CC}$, $R_L = 50 \Omega$, $C_L = 35 \text{ pF}$ (see Figure 16) | $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$ | 100 | 215 | ns | |
| | | | $V_{CC} = 4.5 \text{ V}$ and $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ | | 225 | | |
| t_{BBM} | Break-before-make time | $V_{COM} = V_{CC}$, $R_L = 50 \Omega$, $C_L = 35 \text{ pF}$ (see Figure 17) | $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$ | 1 | 10 | 15 | ns |
| | | | $V_{CC} = 4.5 \text{ V}$ and $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ | 1 | | 20 | |
| Q_C | Charge injection | $V_{GEN} = 0$, $R_{GEN} = 0$, $C_L = 1 \text{ nF}$, $V_{CC} = 5 \text{ V}$, and $T_A = 25^\circ\text{C}$ (see Figure 21) | | 97 | | pC | |
| $C_{NO(OFF)}$ | NO OFF capacitance | V_{NC} or $V_{NO} = V_{CC}$ or GND, switch OFF, $V_{CC} = 5 \text{ V}$, and $T_A = 25^\circ\text{C}$ (see Figure 15) | | 28 | | pF | |
| $C_{NC(ON)}$, $C_{NO(ON)}$ | NC and NO ON capacitance | V_{NC} or $V_{NO} = V_{CC}$ or GND, switch ON, $V_{CC} = 5 \text{ V}$, and $T_A = 25^\circ\text{C}$ (see Figure 15) | | 112 | | pF | |
| $C_{COM(ON)}$ | COM ON capacitance | $V_{COM} = V_{CC}$ or GND, switch ON, $V_{CC} = 5 \text{ V}$, and $T_A = 25^\circ\text{C}$ (see Figure 15) | | 112 | | pF | |
| C_I | Digital input capacitance | $V_{IN} = V_{CC}$ or GND, and $T_A = 25^\circ\text{C}$ (see Figure 15) | | 3 | | pF | |
| BW | Bandwidth | $R_L = 50 \Omega$, switch ON, $V_{CC} = 5 \text{ V}$, and $T_A = 25^\circ\text{C}$ (see Figure 18) | | 55 | | MHz | |
| O_{ISO} | OFF isolation | $R_L = 50 \Omega$, $f = 1 \text{ MHz}$, $V_{CC} = 5 \text{ V}$, and $T_A = 25^\circ\text{C}$ (see Figure 19) | | -63 | | dB | |
| X_{TALK} | Crosstalk | $R_L = 50 \Omega$, $f = 1 \text{ MHz}$, $V_{CC} = 5 \text{ V}$, and $T_A = 25^\circ\text{C}$ (see Figure 20) | | -63 | | dB | |
| THD | Total harmonic distortion | $R_L = 600 \Omega$, $C_L = 50 \text{ pF}$, $f = 20 \text{ Hz to } 20 \text{ kHz}$, $V_{CC} = 5 \text{ V}$, and $T_A = 25^\circ\text{C}$ (see Figure 22) | | 0.003 | | % | |
| SUPPLY | | | | | | | |
| ICC | Positive supply current | $V_{IN} = V_{CC}$ or GND, $V_{CC} = 5.5 \text{ V}$, and $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ | | | 10 | μA | |

6.6 Electrical Characteristics – 3.3-V Supply

 $V_{CC} = 3\text{ V to }3.6\text{ V}$ and $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|--|--|--|---|-------|------|----------|---------------|
| ANALOG SWITCH | | | | | | | |
| r_{on} | ON-state resistance | V_{NO} or $V_{NC} = 2\text{ V}$, $I_{COM} = -100\text{ mA}$, switch ON, and $V_{CC} = 3\text{ V}$ (see Figure 12) | $T_A = 25^\circ\text{C}$ | 0.75 | 0.9 | Ω | |
| | | | $T_A = -40^\circ\text{C to }85^\circ\text{C}$ | | 1.2 | | |
| Δr_{on} | ON-state resistance match between channels | V_{NO} or $V_{NC} = 2\text{ V}$, 0.8 V , $I_{COM} = -100\text{ mA}$, switch ON, and $V_{CC} = 3\text{ V}$ (see Figure 12) | $T_A = 25^\circ\text{C}$ | 0.1 | 0.15 | Ω | |
| | | | $T_A = -40^\circ\text{C to }85^\circ\text{C}$ | | 0.15 | | |
| $r_{on(flat)}$ | ON-state resistance flatness | $0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_{CC}$, $I_{COM} = -100\text{ mA}$, switch ON, $V_{CC} = 3\text{ V}$, and $T_A = 25^\circ\text{C}$ (see Figure 12) | | 0.2 | | Ω | |
| | | V_{NO} or $V_{NC} = 0.8\text{ V}$, 2 V , $I_{COM} = -100\text{ mA}$, switch ON, and $V_{CC} = 3\text{ V}$ (see Figure 12) | $T_A = 25^\circ\text{C}$ | 0.1 | 0.2 | | |
| | | | $T_A = -40^\circ\text{C to }85^\circ\text{C}$ | | 0.3 | | |
| $I_{NO(OFF)}$, $I_{NC(OFF)}$ | NO and NC OFF leakage current | $V_{NO} = 1\text{ V}$, 3 V , $V_{COM} = 3\text{ V}$, 1 V , $V_{NC} = \text{open}$, or $V_{NC} = 1\text{ V}$, 3 V , $V_{COM} = 3\text{ V}$, 1 V , $V_{NO} = \text{open}$, switch OFF, and $V_{CC} = 3.6\text{ V}$ (see Figure 13) | $T_A = 25^\circ\text{C}$ | -20 | 2 | 20 | nA |
| | | | $T_A = -40^\circ\text{C to }85^\circ\text{C}$ | -50 | | 50 | |
| $I_{NO(PWROFF)}$, $I_{NC(PWROFF)}$ | NO and NC PWROFF leakage current | V_{NO} or $V_{NC} = 0\text{ V to }3.6\text{ V}$, $V_{COM} = 3.6\text{ V to }0\text{ V}$, switch OFF, and $V_{CC} = 0\text{ V}$ (see Figure 13) | $T_A = 25^\circ\text{C}$ | -10 | | 10 | μA |
| | | | $T_A = -40^\circ\text{C to }85^\circ\text{C}$ | -10 | | 10 | |
| $I_{NO(ON)}$ | NC and NO ON leakage current | $V_{NO} = 1\text{ V}$, 3 V , V_{NC} and $V_{COM} = \text{open}$, or $V_{NC} = 1\text{ V}$, 3 V , V_{NO} and $V_{COM} = \text{open}$, switch ON, and $V_{CC} = 3.6\text{ V}$ (see Figure 14) | $T_A = 25^\circ\text{C}$ | -20 | 2 | 20 | nA |
| | | | $T_A = -40^\circ\text{C to }85^\circ\text{C}$ | -100 | | 100 | |
| $I_{COM(ON)}$ | COM ON leakage current | $V_{COM} = 1\text{ V}$, V_{NO} and $V_{NC} = \text{open}$, or $V_{COM} = 3\text{ V}$, V_{NO} and $V_{NC} = \text{open}$, and $V_{CC} = 3.6\text{ V}$ (see Figure 14) | $T_A = 25^\circ\text{C}$ | -20 | 2 | 20 | nA |
| | | | $T_A = -40^\circ\text{C to }85^\circ\text{C}$ | -100 | | 100 | |
| $I_{COM(PWROFF)}$ | COM OFF leakage current | V_{NO} or $V_{NC} = 0\text{ V to }3.6\text{ V}$, $V_{COM} = 3.6\text{ V to }0\text{ V}$, and $V_{CC} = 0\text{ V}$ (see Figure 13) | $T_A = 25^\circ\text{C}$ | -10 | | 10 | μA |
| | | | $T_A = -40^\circ\text{C to }85^\circ\text{C}$ | -10 | | 10 | |
| DIGITAL CONTROL INPUT (IN) | | | | | | | |
| V_{IH} | Input logic high | $V_{CC} = 3.6\text{ V}$ and $T_A = -40^\circ\text{C to }85^\circ\text{C}$ | | 1.05 | | 5.5 | V |
| V_{IL} | Input logic low | $V_{CC} = 3.6\text{ V}$ and $T_A = -40^\circ\text{C to }85^\circ\text{C}$ | | 0 | | 0.65 | V |
| I_{IH} , I_{IL} | Input leakage current | $V_I = 1.95\text{ V}$ or 0 V , $V_{CC} = 3.6\text{ V}$, and $T_A = -40^\circ\text{C to }85^\circ\text{C}$ | | -0.05 | | 0.5 | μA |
| r_{IN} | Input resistance | $V_I = 1.95\text{ V}$, $V_{CC} = 3.6\text{ V}$, and $T_A = -40^\circ\text{C to }85^\circ\text{C}$ | | | 6 | | M Ω |
| DYNAMIC | | | | | | | |
| t_{ON} | Turnon time | $V_{COM} = V_{CC}$, $R_L = 50\ \Omega$, $C_L = 35\text{ pF}$ (see Figure 16) | $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$ | 72 | 175 | ns | |
| | | | $V_{CC} = 3\text{ V}$ and $T_A = -40^\circ\text{C to }85^\circ\text{C}$ | | 185 | | |
| t_{OFF} | Turnoff time | $V_{COM} = V_{CC}$, $R_L = 50\ \Omega$, $C_L = 35\text{ pF}$ (see Figure 16) | $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$ | 105 | 165 | ns | |
| | | | $V_{CC} = 3\text{ V}$ and $T_A = -40^\circ\text{C to }85^\circ\text{C}$ | | 170 | | |
| t_{BBM} | Break-before-make time | $V_{COM} = V_{CC}$, $R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, (see Figure 17) | $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$ | 1 | 16 | 30 | ns |
| | | | $V_{CC} = 3\text{ V}$ and $T_A = -40^\circ\text{C to }85^\circ\text{C}$ | 1 | | 35 | |
| Q_C | Charge injection | $V_{GEN} = 0$, $R_{GEN} = 0$, $C_L = 1\text{ nF}$ (see Figure 21) | $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$ | | 97 | | pC |
| $C_{NO(OFF)}$ | NO OFF capacitance | $V_{NO} = V_{CC}$ or GND, switch OFF, $V_{CC} = 3.3\text{ V}$, and $T_A = 25^\circ\text{C}$ (see Figure 15) | | | 28 | | pF |
| $C_{NC(ON)}$, $C_{NO(ON)}$ | NC and NO ON capacitance | V_{NC} or $V_{NO} = V_{CC}$ or GND, switch ON, $V_{CC} = 3.3\text{ V}$, and $T_A = 25^\circ\text{C}$ (see Figure 15) | | | 115 | | pF |

(1) The algebraic convention (whereby the most negative value is a minimum and the most positive value is a maximum)

Electrical Characteristics – 3.3-V Supply (continued)

 $V_{CC} = 3\text{ V to }3.6\text{ V}$ and $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------|---------------------------|---|-----|--------|-----|---------------|
| $C_{COM(ON)}$ | COM ON capacitance | $V_{COM} = V_{CC}$ or GND, switch ON, $V_{CC} = 3.3\text{ V}$, and $T_A = 25^\circ\text{C}$ (see Figure 15) | | 115 | | pF |
| C_I | Digital input capacitance | $V_{IN} = V_{CC}$ or GND, $V_{CC} = 3.3\text{ V}$, and $T_A = 25^\circ\text{C}$ (see Figure 15) | | 3 | | pF |
| BW | Bandwidth | $R_L = 50\ \Omega$, switch ON, $V_{CC} = 3.3\text{ V}$, and $T_A = 25^\circ\text{C}$ (see Figure 18) | | 54 | | MHz |
| O_{ISO} | OFF isolation | $R_L = 50\ \Omega$, $f = 1\text{ MHz}$, $V_{CC} = 3.3\text{ V}$, and $T_A = 25^\circ\text{C}$ (see Figure 19) | | -63 | | dB |
| X_{TALK} | Crosstalk | $R_L = 50\ \Omega$, $f = 1\text{ MHz}$, $V_{CC} = 3.3\text{ V}$, and $T_A = 25^\circ\text{C}$ (see Figure 20) | | -63 | | dB |
| THD | Total harmonic distortion | $R_L = 600\ \Omega$, $C_L = 50\text{ pF}$, $f = 20\text{ Hz to }20\text{ kHz}$, $V_{CC} = 3.3\text{ V}$, and $T_A = 25^\circ\text{C}$ (see Figure 22) | | 0.004% | | |
| SUPPLY | | | | | | |
| ICC | Positive supply current | $V_{IN} = 1.95\text{ V or GND}$, $V_{CC} = 3.6\text{ V}$, and $T_A = 25^\circ\text{C}$ | | | 10 | μA |

6.7 Electrical Characteristics – 2.5-V Supply

 $V_{CC} = 2.25\text{ V to }2.75\text{ V}$ and $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|---|-----|------|-----|----------|
| ANALOG SWITCH | | | | | | |
| r_{on} | ON-state resistance | V_{NO} or $V_{NC} = 1.8\text{ V}$, $I_{COM} = -100\text{ mA}$, switch ON, and $V_{CC} = 2.25\text{ V}$ (see Figure 12) | | 1.1 | 1.3 | Ω |
| | | | | | 1.6 | |
| Δr_{on} | ON-state resistance match between channels | V_{NO} or $V_{NC} = 1.8\text{ V}$, 0.8 V , $I_{COM} = -100\text{ mA}$, switch ON, and $V_{CC} = 2.25\text{ V}$ (see Figure 12) | | 0.15 | 0.2 | Ω |
| | | | | | 0.2 | |
| $r_{on(Flat)}$ | ON-state resistance flatness | $0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_{CC}$, $I_{COM} = -100\text{ mA}$, switch ON, $V_{CC} = 2.25\text{ V}$, and $T_A = 25^\circ\text{C}$ (see Figure 12) | | 0.4 | | Ω |
| | | V_{NO} or $V_{NC} = 0.8\text{ V}$, 1 V , 1.8 V , $I_{COM} = -100\text{ mA}$, switch ON, and $V_{CC} = 2.25\text{ V}$ (see Figure 12) | | 0.25 | 0.5 | |
| $I_{NO(OFF)}$, $I_{NC(OFF)}$ | NO and NC OFF leakage current | $V_{NO} = 0.5\text{ V}$, 2.2 V , $V_{COM} = 2.2\text{ V}$, 0.5 V , $V_{NC} = \text{open}$, or $V_{NC} = 0.5\text{ V}$, 2.2 V , $V_{COM} = 2.2\text{ V}$, 0.5 V , $V_{NO} = \text{open}$, switch OFF, and $V_{CC} = 2.75\text{ V}$ (see Figure 13) | | -20 | 2 | 20 |
| $I_{NO(PWROFF)}$, $I_{NC(PWROFF)}$ | NO and NC PWROFF leakage current | V_{NO} or $V_{NC} = 0\text{ V to }2.75\text{ V}$, $V_{COM} = 2.75\text{ V to }0\text{ V}$, switch OFF, and $V_{CC} = 0\text{ V}$ (see Figure 13) | | -10 | | 10 |
| | | | | -10 | | 10 |
| $I_{NO(ON)}$ | NC and NO ON leakage current | $V_{NO} = 0.5\text{ V}$, 2.2 V , V_{NC} and $V_{COM} = \text{open}$, or $V_{NC} = 2.2\text{ V}$, 0.5 V , V_{NO} and $V_{COM} = \text{open}$, switch ON, and $V_{CC} = 2.75\text{ V}$ (see Figure 14) | | -20 | 2 | 20 |
| | | | | -100 | | 100 |
| $I_{COM(ON)}$ | COM ON leakage current | $V_{COM} = 0.5\text{ V}$, V_{NO} and $V_{NC} = \text{open}$, or $V_{COM} = 2.2\text{ V}$, V_{NO} and $V_{NC} = \text{open}$, switch ON, and $V_{CC} = 2.75\text{ V}$ (see Figure 14) | | -20 | 2 | 20 |
| | | | | -100 | | 100 |
| $I_{COM(PWROFF)}$ | COM OFF leakage current | V_{NO} or $V_{NC} = 0\text{ V to }2.75\text{ V}$, $V_{COM} = 2.75\text{ V to }0\text{ V}$, and $V_{CC} = 0\text{ V}$ (see Figure 13) | | -10 | | 10 |
| | | | | -10 | | 10 |

(1) The algebraic convention (whereby the most negative value is a minimum and the most positive value is a maximum)

Electrical Characteristics – 2.5-V Supply (continued)
 $V_{CC} = 2.25\text{ V to }2.75\text{ V}$ and $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------------|---------------------------|---|---|--------|------|------------------|
| DIGITAL CONTROL INPUT (IN) | | | | | | |
| V_{IH} | Input logic high | $V_{CC} = 2.75\text{ V}$ and $T_A = -40^\circ\text{C to }85^\circ\text{C}$ | 1.05 | | 5.5 | V |
| V_{IL} | Input logic low | $V_{CC} = 2.75\text{ V}$ and $T_A = -40^\circ\text{C to }85^\circ\text{C}$ | 0 | | 0.65 | V |
| I_{IH} , I_{IL} | Input leakage current | $V_{IN} = 1.95\text{ V or }0$, $V_{CC} = 2.75\text{ V}$, and $T_A = -40^\circ\text{C to }85^\circ\text{C}$ | -0.05 | | 0.5 | μA |
| r_{IN} | Input resistance | $V_{IN} = 1.95\text{ V}$, $V_{CC} = 2.75\text{ V}$, and $T_A = -40^\circ\text{C to }85^\circ\text{C}$ | | 6 | | $\text{M}\Omega$ |
| DYNAMIC | | | | | | |
| t_{ON} | Turnon time | $V_{COM} = V_{CC}$, $R_L = 50\ \Omega$, and $C_L = 35\text{ pF}$ (see Figure 16) | $V_{CC} = 2.5\text{ V}$ and $T_A = 25^\circ\text{C}$ | 97 | 170 | ns |
| | | | $V_{CC} = 2.25\text{ V}$ and $T_A = -40^\circ\text{C to }85^\circ\text{C}$ | | 175 | |
| t_{OFF} | Turnoff time | $V_{COM} = V_{CC}$, $R_L = 50\ \Omega$, and $C_L = 35\text{ pF}$ (see Figure 16) | $V_{CC} = 2.5\text{ V}$ and $T_A = 25^\circ\text{C}$ | 80 | 155 | ns |
| | | | $V_{CC} = 2.25\text{ V}$ and $T_A = -40^\circ\text{C to }85^\circ\text{C}$ | | 160 | |
| t_{BBM} | Break-before-make time | $V_{COM} = V_{CC}$, $R_L = 50\ \Omega$, and $C_L = 35\text{ pF}$ (see Figure 17) | $V_{CC} = 2.5\text{ V}$ and $T_A = 25^\circ\text{C}$ | 5 | 18 | ns |
| | | | $V_{CC} = 2.25\text{ V}$ and $T_A = -40^\circ\text{C to }85^\circ\text{C}$ | 5 | 40 | |
| Q_C | Charge injection | $V_{GEN} = 0$, $R_{GEN} = 0$, $C_L = 1\text{ nF}$, $V_{CC} = 2.5\text{ V}$, and $T_A = 25^\circ\text{C}$ (see Figure 21) | | 82 | | pC |
| $C_{NO(OFF)}$ | NO OFF capacitance | $V_{NO} = V_{CC}$ or GND, switch OFF, $V_{CC} = 2.5\text{ V}$, and $T_A = 25^\circ\text{C}$ (see Figure 15) | | 29 | | pF |
| $C_{NC(ON)}$, $C_{NO(ON)}$ | NC and NO ON capacitance | V_{NC} or $V_{NO} = V_{CC}$ or GND, switch ON, $V_{CC} = 2.5\text{ V}$, and $T_A = 25^\circ\text{C}$ (see Figure 15) | | 116 | | pF |
| $C_{COM(ON)}$ | COM ON capacitance | $V_{COM} = V_{CC}$ or GND, switch ON, $V_{CC} = 2.5\text{ V}$, and $T_A = 25^\circ\text{C}$ (see Figure 15) | | 116 | | pF |
| C_I | Digital input capacitance | $V_{IN} = V_{CC}$ or GND, $V_{CC} = 2.5\text{ V}$, and $T_A = 25^\circ\text{C}$ (see Figure 15) | | 3 | | pF |
| BW | Bandwidth | $R_L = 50\ \Omega$, switch ON, $V_{CC} = 2.5\text{ V}$, and $T_A = 25^\circ\text{C}$ (see Figure 18) | | 54 | | MHz |
| O_{ISO} | OFF isolation | $R_L = 50\ \Omega$, $f = 1\text{ MHz}$, $V_{CC} = 2.5\text{ V}$, and $T_A = 25^\circ\text{C}$ (see Figure 19) | | -63 | | dB |
| X_{TALK} | Crosstalk | $R_L = 50\ \Omega$, $f = 1\text{ MHz}$, $V_{CC} = 2.5\text{ V}$, and $T_A = 25^\circ\text{C}$ (see Figure 20) | | -63 | | dB |
| THD | Total harmonic distortion | $R_L = 600\ \Omega$, $C_L = 50\text{ pF}$, $V_{CC} = 2.5\text{ V}$, $f = 20\text{ Hz to }20\text{ kHz}$, and $T_A = 25^\circ\text{C}$ (see Figure 22) | | 0.008% | | |
| SUPPLY | | | | | | |
| ICC | Positive supply current | $V_{IN} = 1.95\text{ V or GND}$, $V_{CC} = 2.75\text{ V}$, and $T_A = -40^\circ\text{C to }85^\circ\text{C}$ | | | 10 | μA |

6.8 Typical Characteristics

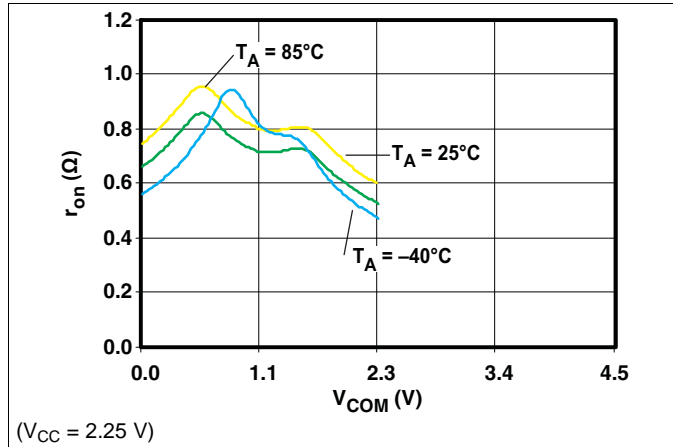


Figure 1. r_{on} vs V_{COM}

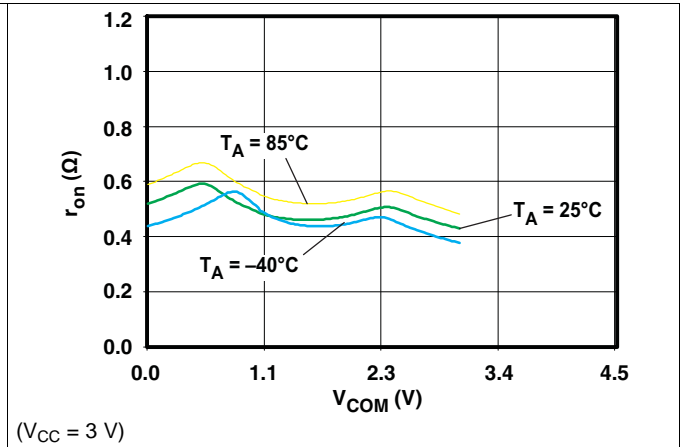


Figure 2. r_{on} vs V_{COM}

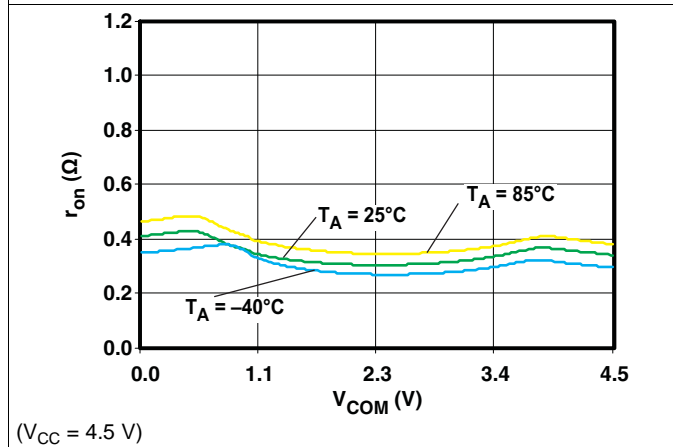


Figure 3. r_{on} vs V_{COM}

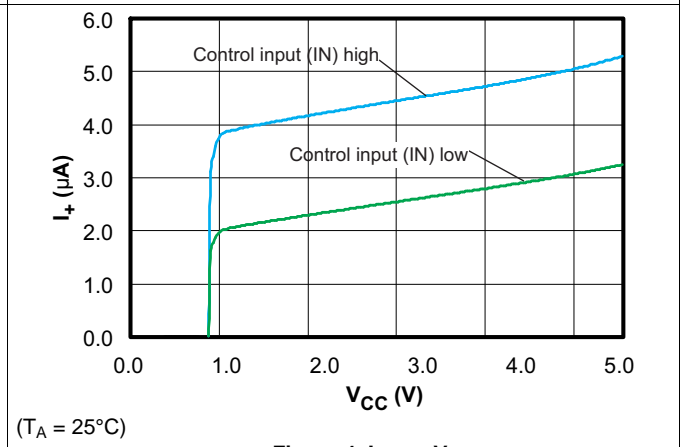


Figure 4. I_{CC} vs V_{CC}

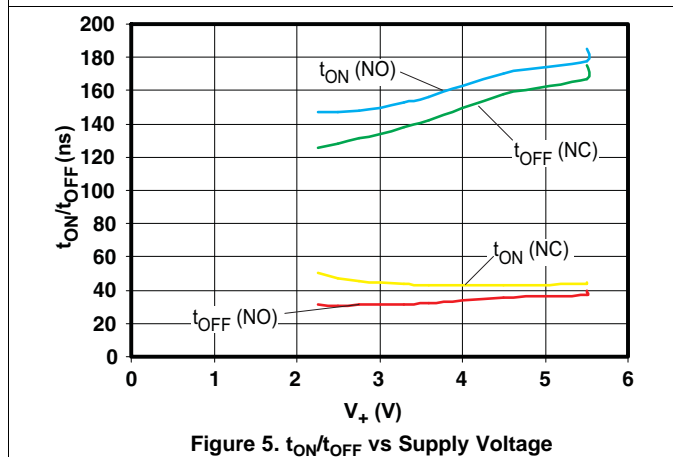


Figure 5. t_{ON}/t_{OFF} vs Supply Voltage

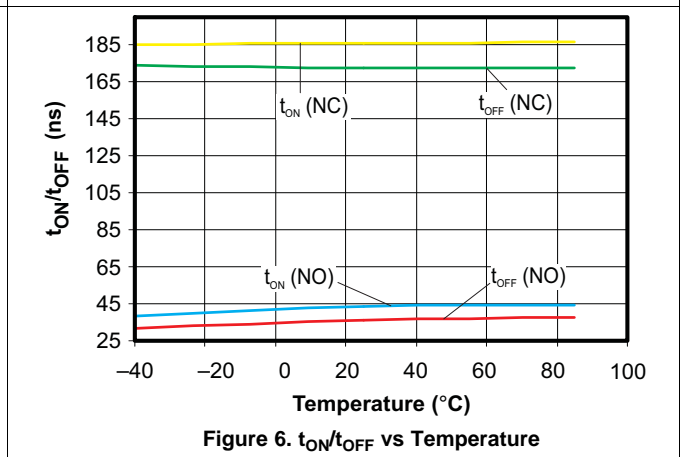


Figure 6. t_{ON}/t_{OFF} vs Temperature

Typical Characteristics (continued)

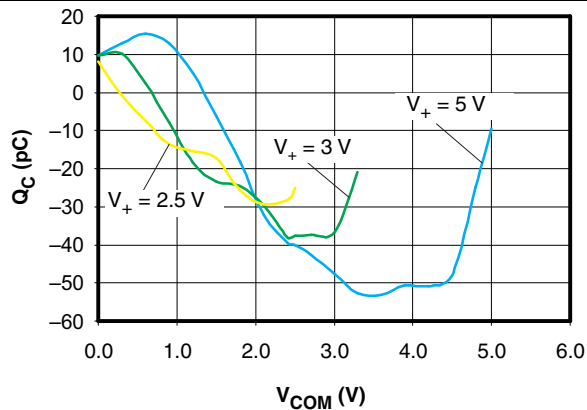


Figure 7. Charge Injection (Q_C) vs V_{COM}

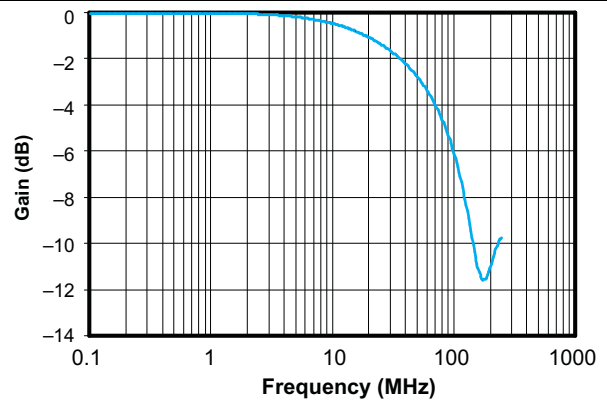


Figure 8. Gain vs Frequency

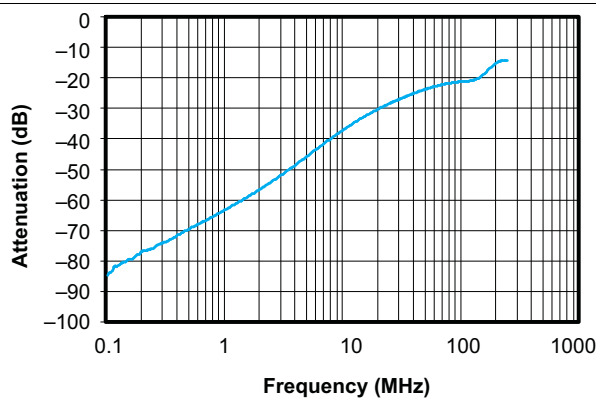


Figure 9. OFF Isolation vs Frequency

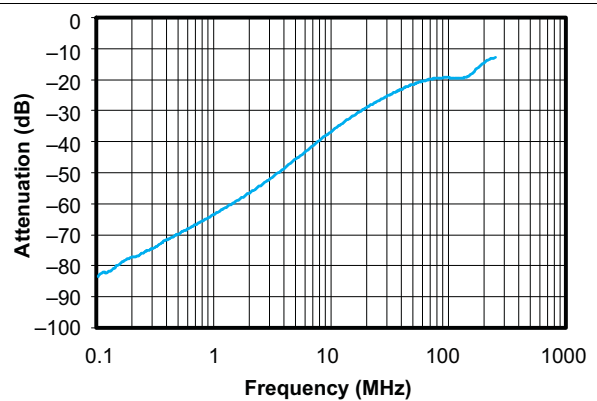


Figure 10. Crosstalk vs Frequency

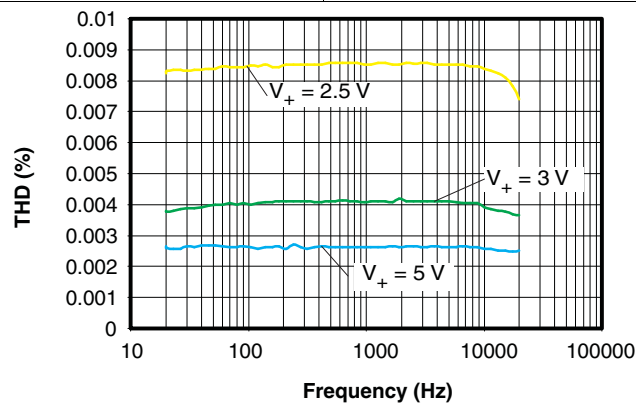


Figure 11. Total Harmonic Distortion (THD) vs Frequency

7 Parameter Measurement Information

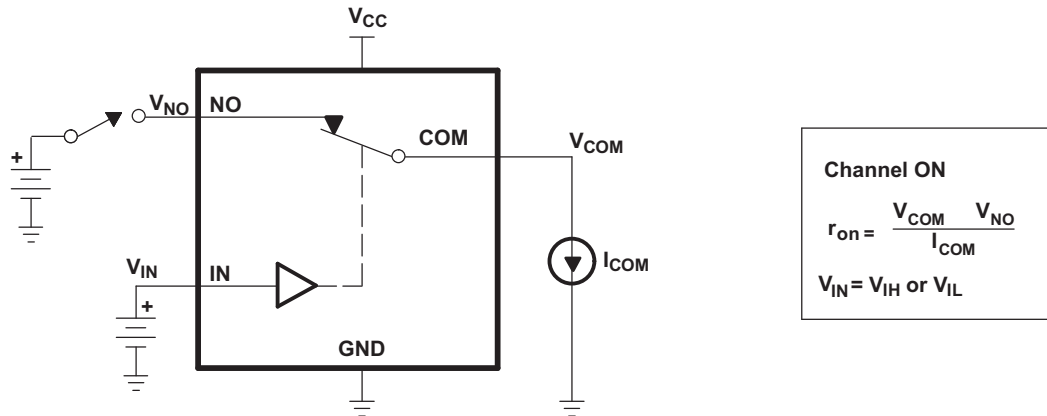


Figure 12. ON-State Resistance (r_{on})

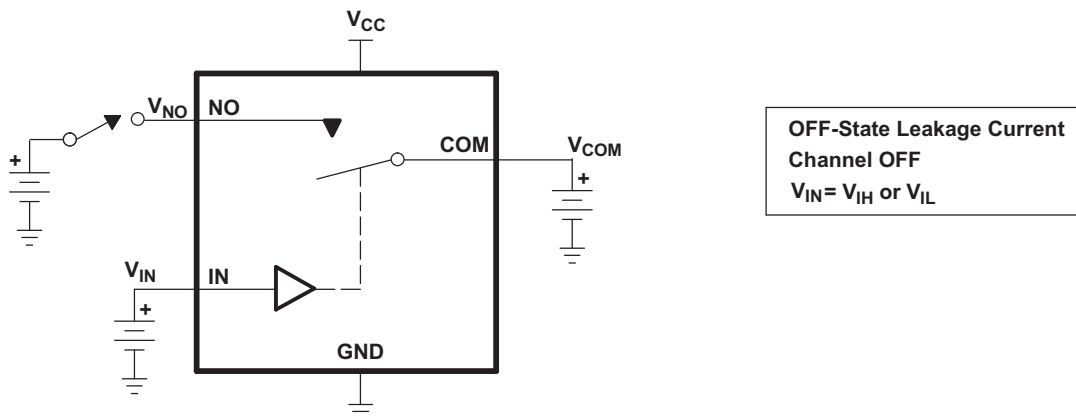


Figure 13. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NC(OFF)}$, $I_{COM(PWROFF)}$, $I_{NC(PWROFF)}$)

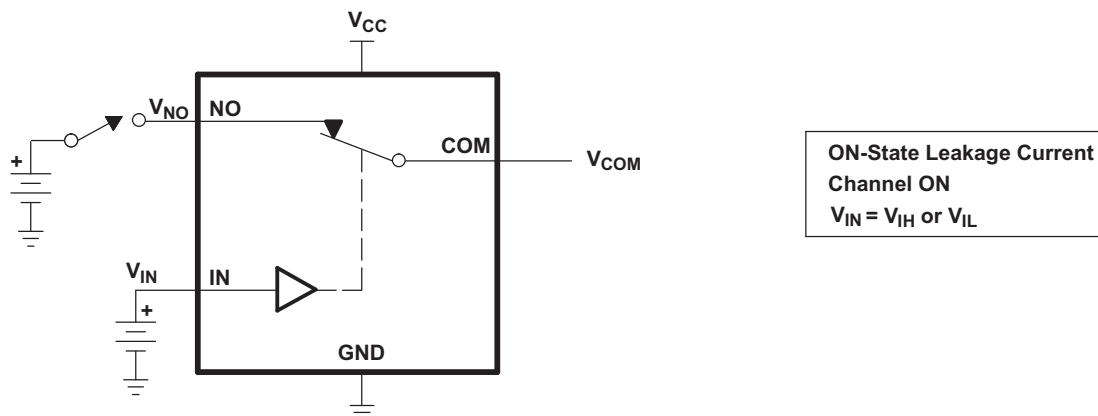


Figure 14. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$)

Parameter Measurement Information (continued)

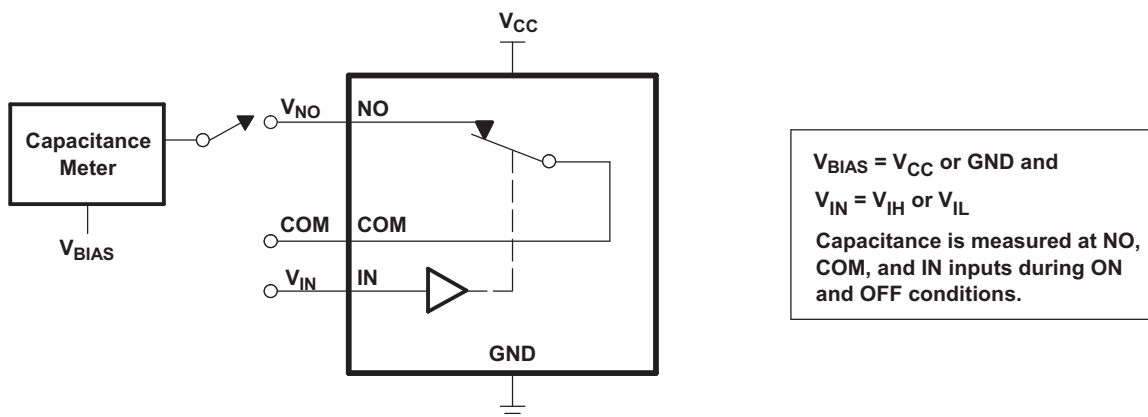
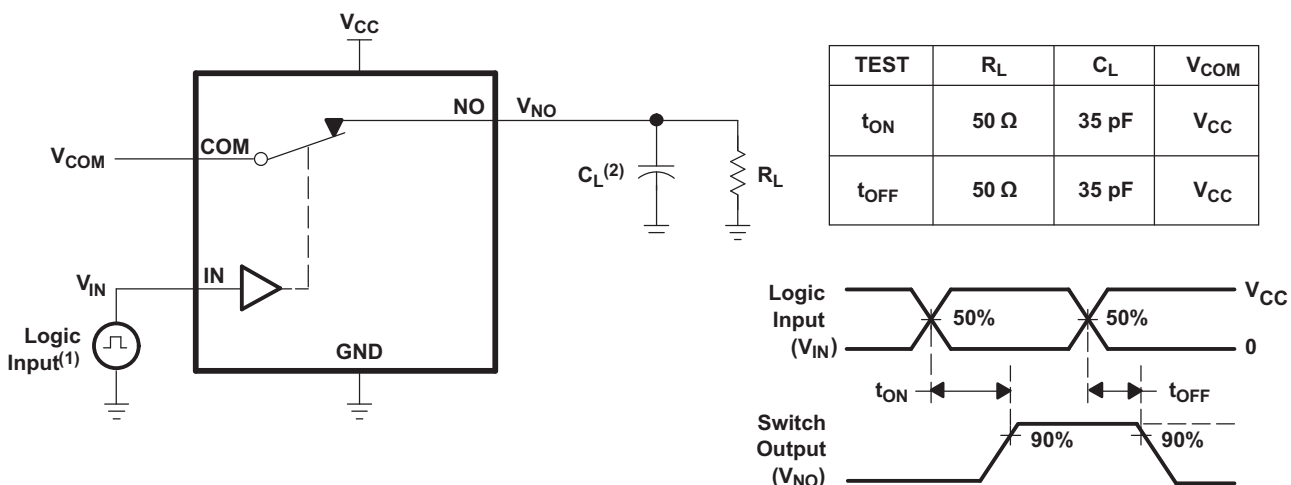


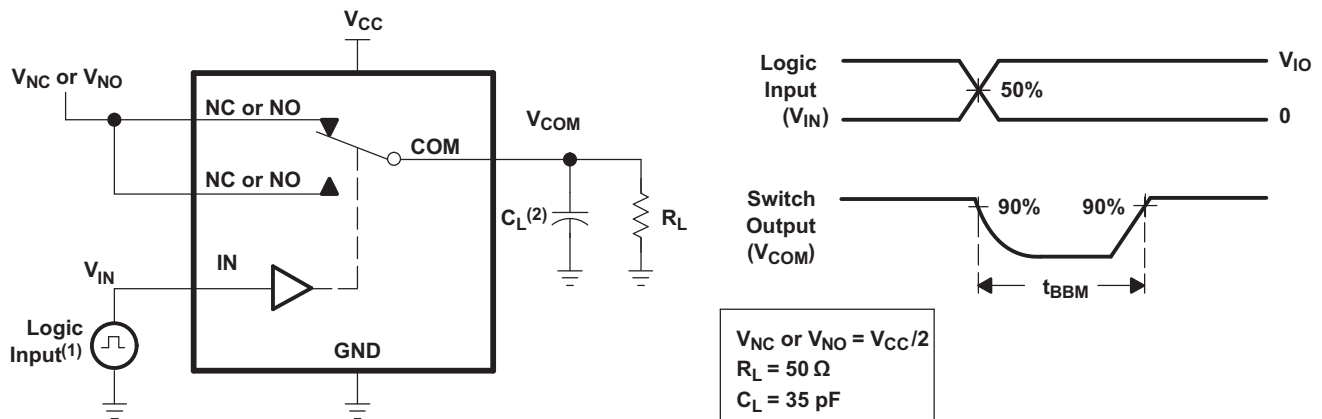
Figure 15. Capacitance (C_I , $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NC(ON)}$)



- A. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\ MHz$, $Z_O = 50\ \Omega$, $t_r < 5\ ns$, $t_f < 5\ ns$.
- B. C_L includes probe and jig capacitance.

Figure 16. Turnon (t_{ON}) and Turnoff Time (t_{OFF})

Parameter Measurement Information (continued)



- A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
- B. C_L includes probe and jig capacitance.

Figure 17. Break-Before-Make Time (t_{BBM})

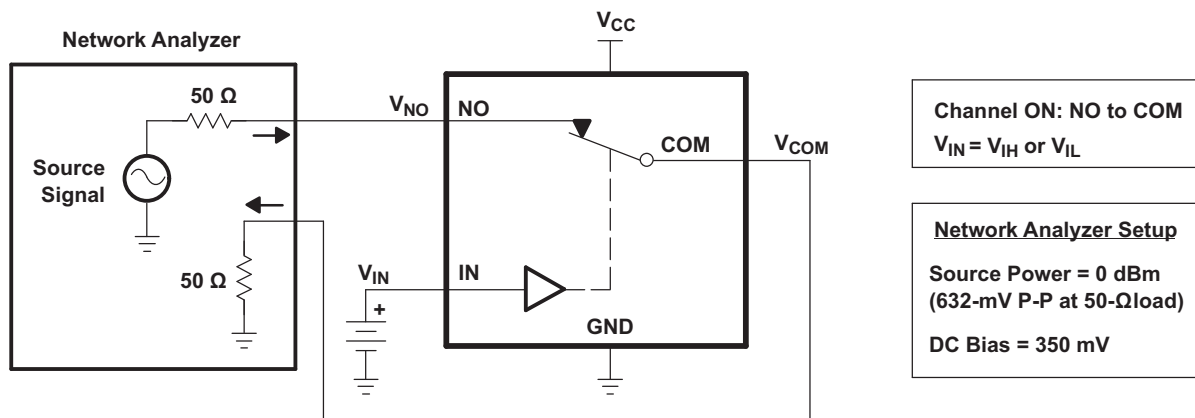


Figure 18. Bandwidth (BW)

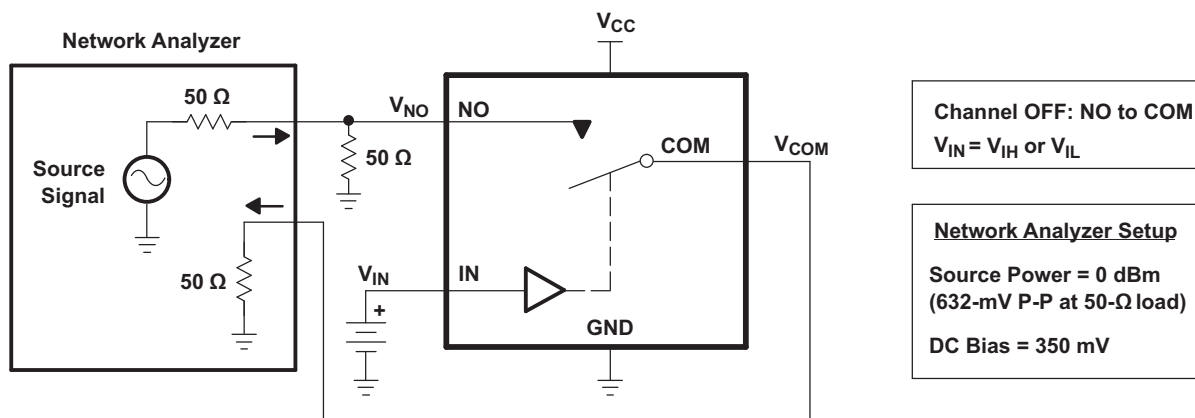


Figure 19. OFF Isolation (O_{ISO})

Parameter Measurement Information (continued)

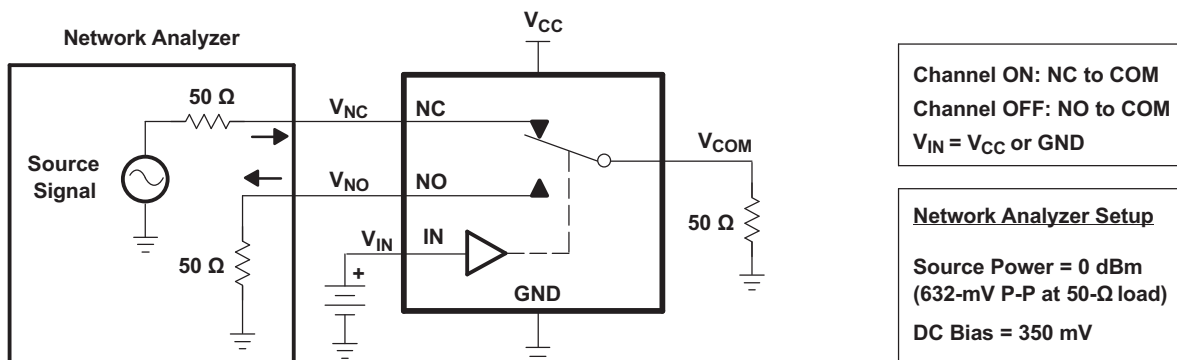
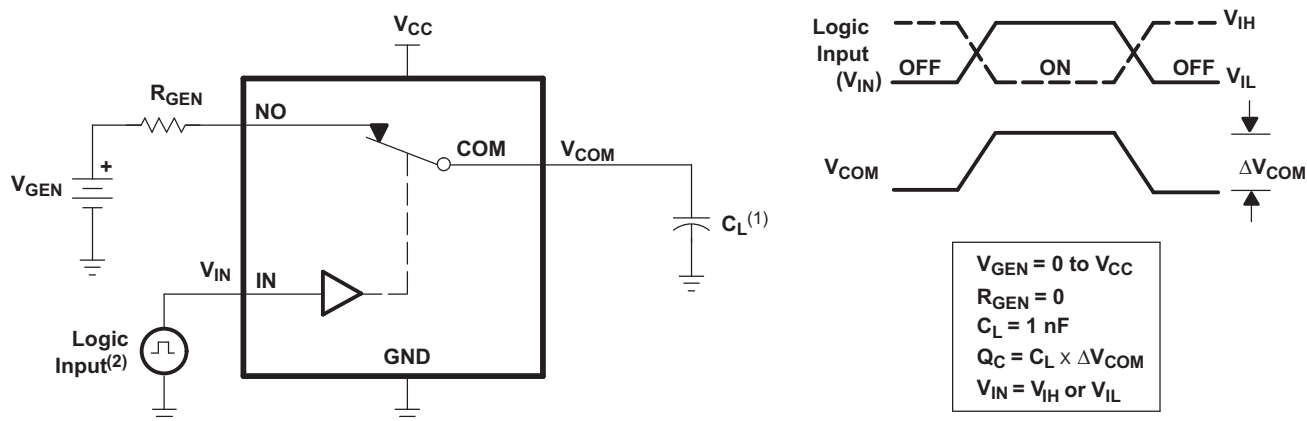
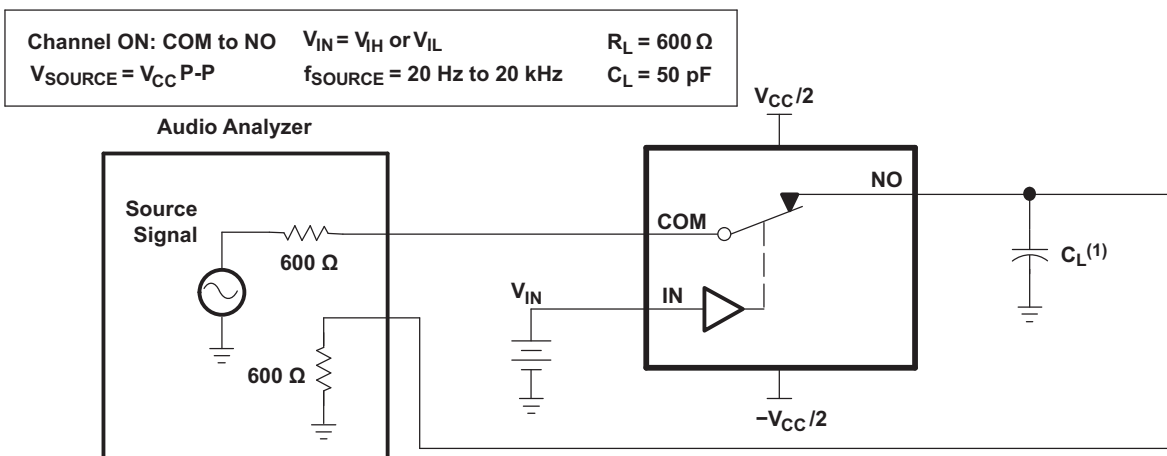


Figure 20. Crosstalk (X_{TALK})



- A. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.
- B. C_L includes probe and jig capacitance.

Figure 21. Charge Injection (Q_C)



- A. C_L includes probe and jig capacitance.

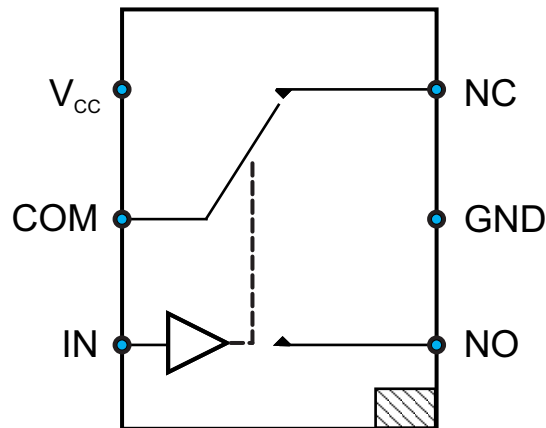
Figure 22. Total Harmonic Distortion (THD)

8 Detailed Description

8.1 Overview

The TS5A12301E device is a bidirectional, 1-channel, 1:2 mux, or single-pole double-throw (SPDT) analog switch. This switch offers low ON-state resistance and excellent THD performance, which makes it great for interfacing with an ADC.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Isolation

Isolation in power-down mode prevents current leakage through the device's signal path when $V_{CC} = 0$ V. This allows signals to be present on the COM, NO, or NC pins before the device is powered up without damaging the device.

8.3.2 1.8-V Compatible Logic

The TS5A12301E supports 1.8-V logic irrespective to the supply voltage applied to the IC.

8.3.3 Integrated Control Input Pulldown

There is an integrated 6-M Ω pulldown resistor on the digital control input pin (IN) to keep the device in a known logic state during power up without needing an external component.

8.4 Device Functional Modes

Table 1 lists the functional modes of the TS5A12301E.

Table 1. Function Table

| IN | NC TO COM, COM TO NC | NO TO COM, COM TO NO |
|-----------|-------------------------|-------------------------|
| L or Open | ON | OFF |
| H | OFF | ON |

9 Application and Implementation

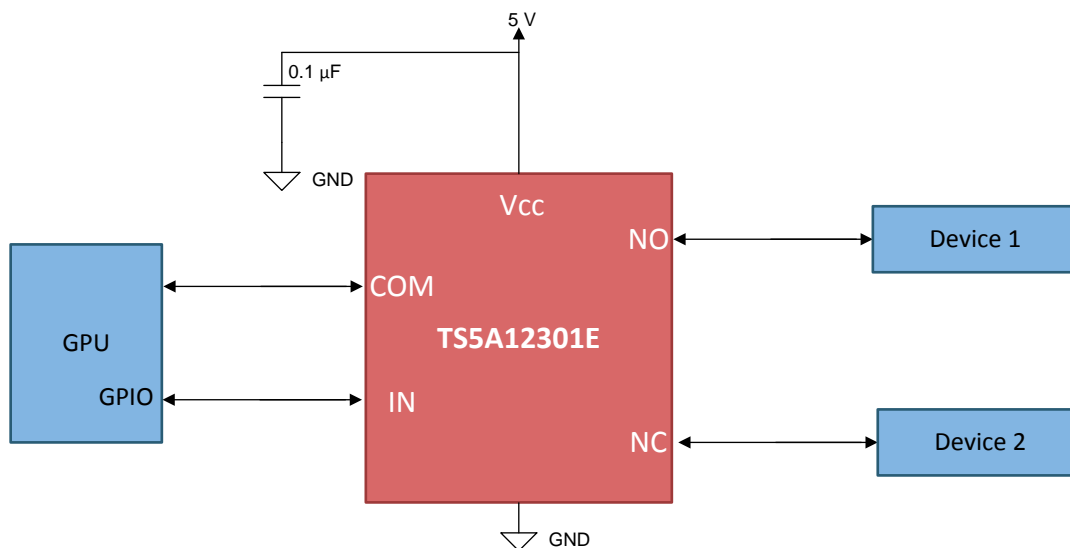
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The switch is bidirectional, so the NO, NC, and COM pins may be used as either inputs or outputs.

9.2 Typical Application



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Figure 23. Application Schematic

9.2.1 Design Requirements

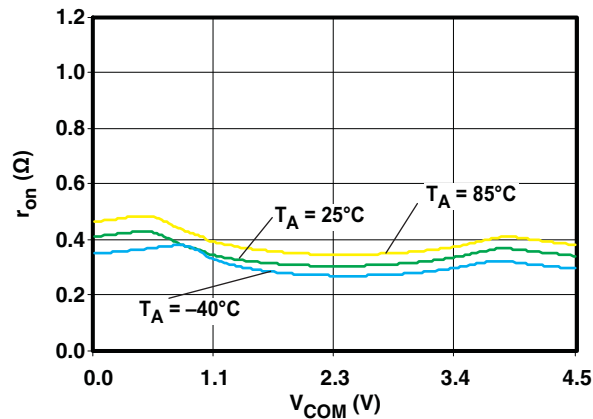
This TS5A12301E application may be properly operated without any external components. Unused pins (for example, COM, NC, and NO) may be left floating. Digital control pin (IN) has an integrated 6-M Ω pulldown resistor, so no external component is required to keep the logic pin in a known state.

9.2.2 Detailed Design Procedure

To ensure proper performance, keep all signals passing through the switch within the ranges specified in [Recommended Operating Conditions](#).

Typical Application (continued)

9.2.3 Application Curve



$$V_{CC} = 4.5 \text{ V}$$

Figure 24. r_{on} vs V_{COM}

10 Power Supply Recommendations

The TS5A12301E does not have power sequencing requirements. If there is a voltage present on the COM, NC, and NO pins before power is supplied to the VCC pin, the isolation feature in power-down mode ($V_{CC} = 0$) protects the device and signal path.

Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the VCC supply to other components. A 0.1- μF capacitor, connected from VCC to GND, is adequate for most applications.

11 Layout

11.1 Layout Guidelines

High-speed switches require proper layout and design procedures for optimum performance. Reduce stray inductance and capacitance by keeping traces short and wide. Ensure that bypass capacitors are placed as close to the device as possible. Use large ground planes where possible.

11.2 Layout Example

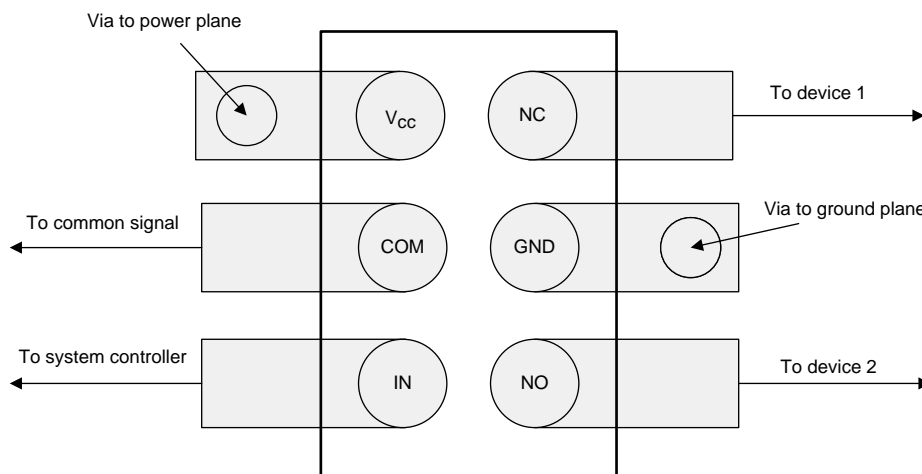


Figure 25. TS5A12301E Layout

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|---------|
| TS5A12301EYFPR | ACTIVE | DSBGA | YFP | 6 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | (3W2 ~ 3W7 ~ 3WN) | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

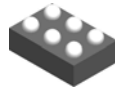
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TS5A12301EYFPR | DSBGA | YFP | 6 | 3000 | 178.0 | 9.2 | 0.89 | 1.29 | 0.62 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TS5A12301EYFPR | DSBGA | YFP | 6 | 3000 | 220.0 | 220.0 | 35.0 |

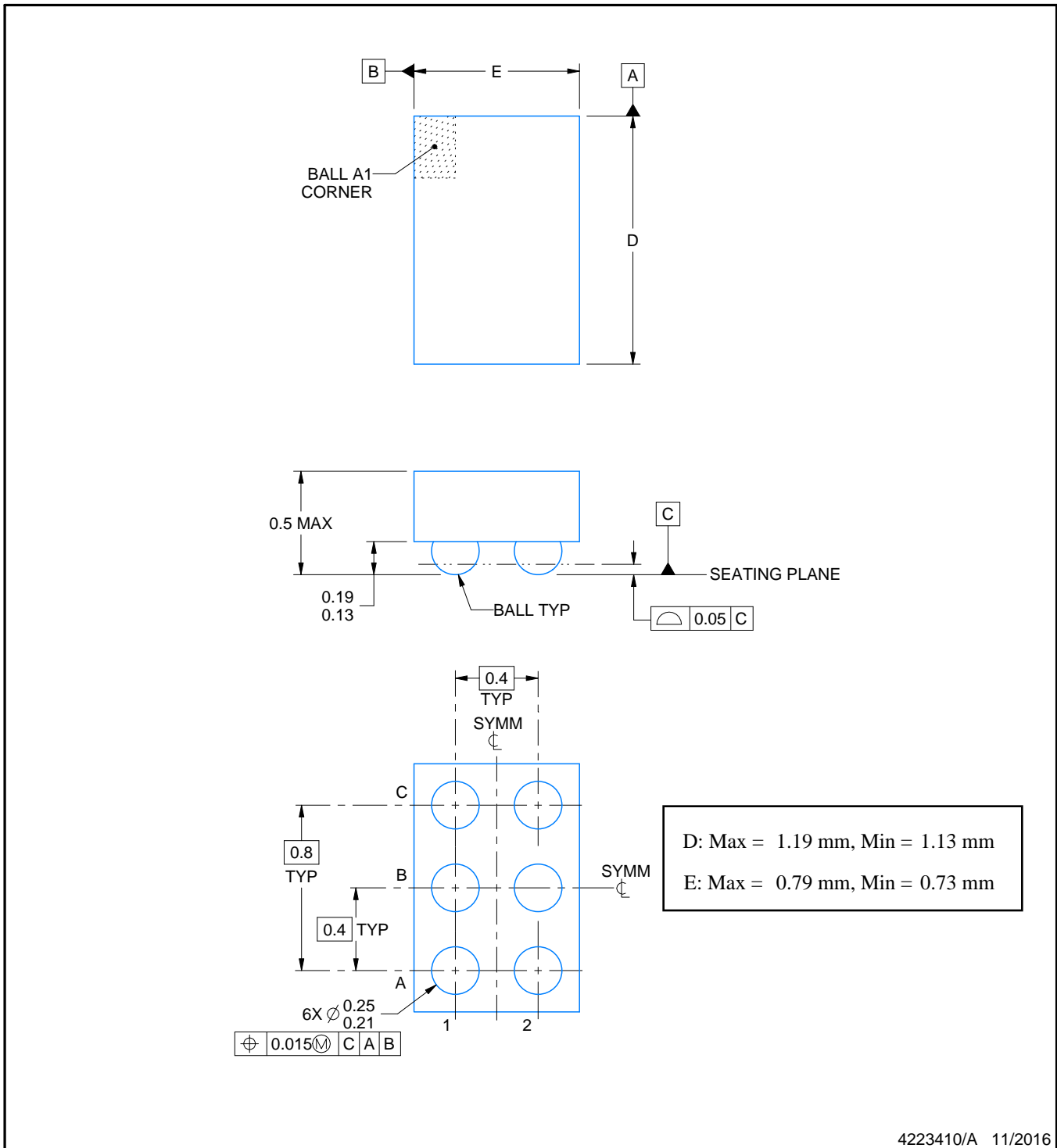
YFP0006



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4223410/A 11/2016

NOTES:

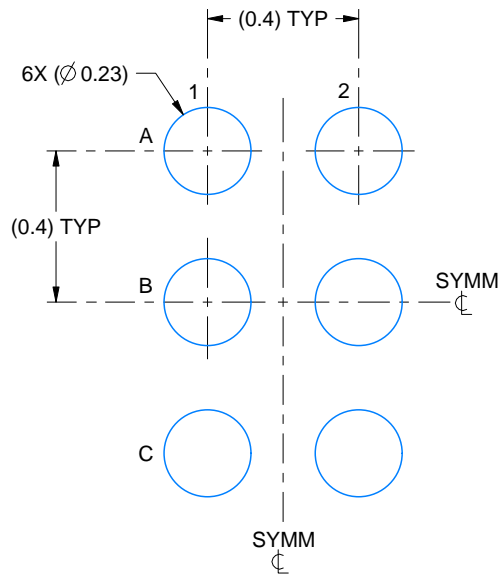
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

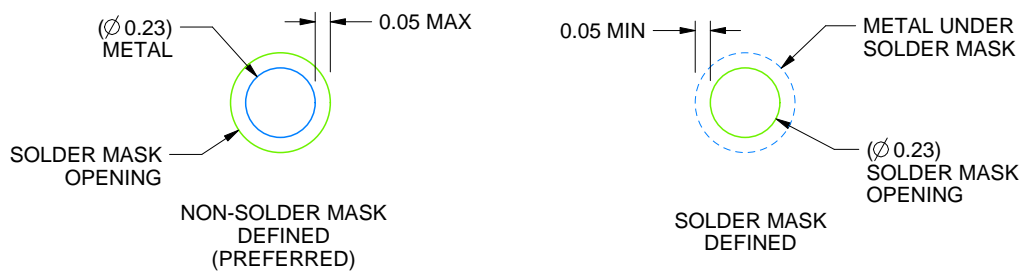
YFP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

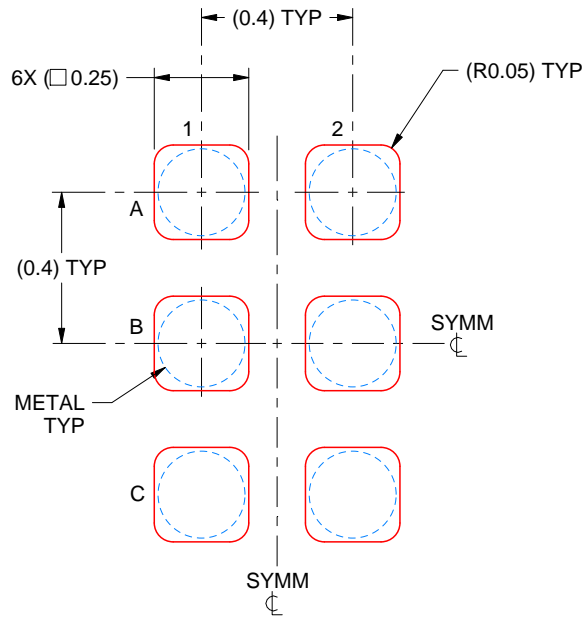
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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