



**THE DATASHEET OF  
TS3DV421RUAR**



# 4-CHANNEL DIFFERENTIAL 8:16 MULTIPLEXER SWITCH FOR DVI/HDMI APPLICATIONS

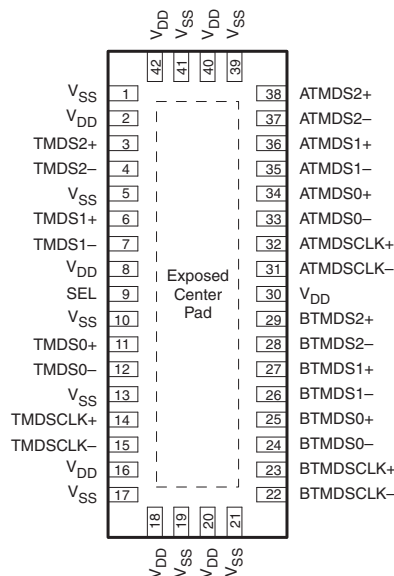
Check for Samples: [TS3DV421](#)

## FEATURES

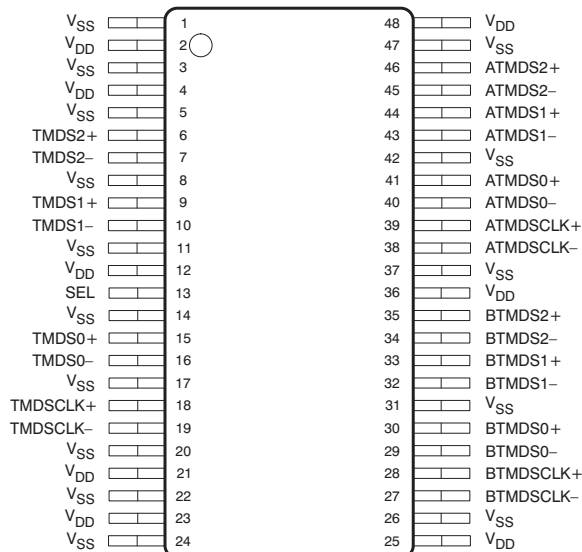
- **Compatible With HDMI v1.3 DVI 1.0 High-Speed Digital Interface**
  - Wide Bandwidth of Over 3.8 Gbps
  - Serial Data Stream at 10x Pixel Clock Rate
  - Supports All Video Formats up to 1080p and SXGA (1280 × 1024 at 75 Hz)
  - High Bandwidth of 4.95 Gbps (Single Link)
  - HDCP Compatible
- **Low Crosstalk** ( $X_{TALK} = -50$  dB Typ at 1.65 Gbps)
- **Off Isolation** ( $O_{IRR} = -50$  dB Typ at 1.65 Gbps)
- **Low Bit-to-Bit Skew** ( $t_{sk(o)} = 0.1$  ns Max)
- **Low and Flat ON-State Resistance** ( $r_{ON} = 12.5$   $\Omega$  Max,  $r_{ON(Flat)} = 0.5$   $\Omega$  Typ)
- **Low Input/Output Capacitance** ( $C_{ON} = 4.5$  pF Max)
- **Enables Application-Specific Operating Voltage Selection**
  - $V_{DD}$  Operating Range From 1.5 V to 2.1 V When  $V_{SS} = GND$
  - $V_{DD}$  Operating Range From 3.0 V to 3.6 V When  $V_{SS} = 1.5$  V
- **$I_{off}$  Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- **For DisplayPort Applications:**  
 $V_{DD} = 1.8$  V ,  $V_{SS} = GND$
- **For HDMI /DVI Applications:**  
 $V_{DD} = 3.3$  V ,  $V_{SS} = 1.5$  V

## APPLICATIONS

- **DVI/HDMI Signal Switching**
- **Differential DVI, HDMI Signal Multiplexing for Audio/Video Receivers and High-Definition Televisions (HDTVs)**

**RUA PACKAGE  
(TOP VIEW)**


For RUA, the exposed center pad must be connected to  $V_{SS}$  or electronically open. For this part to be used in HDMI/TMDS applications,  $V_{SS}$  can be elevated to 1.5 V. See [Figure 1](#).

**DGV PACKAGE  
(TOP VIEW)**


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

## DESCRIPTION/ORDERING INFORMATION

The TS3DV421 is a 4-channel differential 2:1 multiplexer/demultiplexer digital video switch controlled with one select input (SEL). SEL controls the data path of the multiplexer/demultiplexer and can be connected to any GPIO in the system, using an external voltage divider system. The device provides high bandwidth necessary for DVI and HDMI applications. This device expands the high-speed physical link interface from a single HDMI port to two HDMI ports (A or B port). The unselected channel is set to a high-impedance state.

The most common application for the TS3DV421 is in the sink application. In this case, there are two sources (i.e., DVD, set-top box, or game console) that must be routed to one HDMI receiver. The TS3DV421 can route the signals where one HDMI receiver (in a DLP, LCD TV, PDP, or other high-definition display) can be expanded to three ports.

The HDMI application calls for a 100-Ω differential impedance between the differential lines (TMDSn+ and TMDSn-). Additionally, because the TS3DV421 is a high-bandwidth, low-r<sub>ON</sub> pass transistor-type switch, a properly designed board retains a 100-Ω differential impedance through the switch. The unselected port is in the high-impedance mode, such that the receiver receives information from only one source. HDCP encryption is passed through the switch for the HDMI receiver to decode.

**Table 1. ORDERING INFORMATION**

T <sub>A</sub>	PACKAGE <sup>(1) (2)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RUA	Tape and reel	TS3DV421RUAR
	TVSOP – DGV	Tape and reel	TS3DV421DGVR

(1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

## TYPICAL APPLICATION

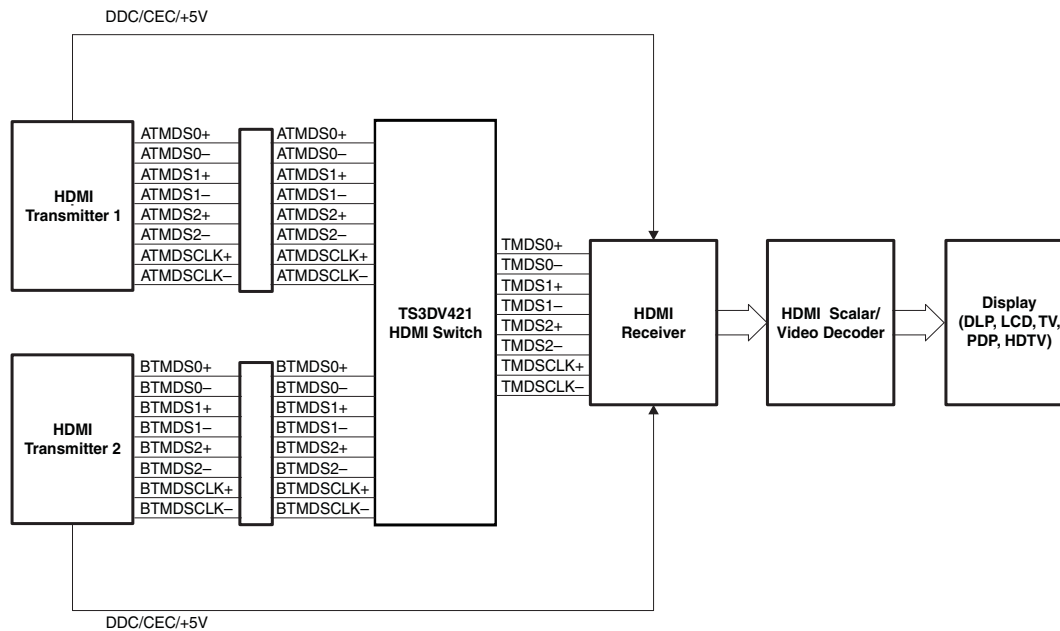
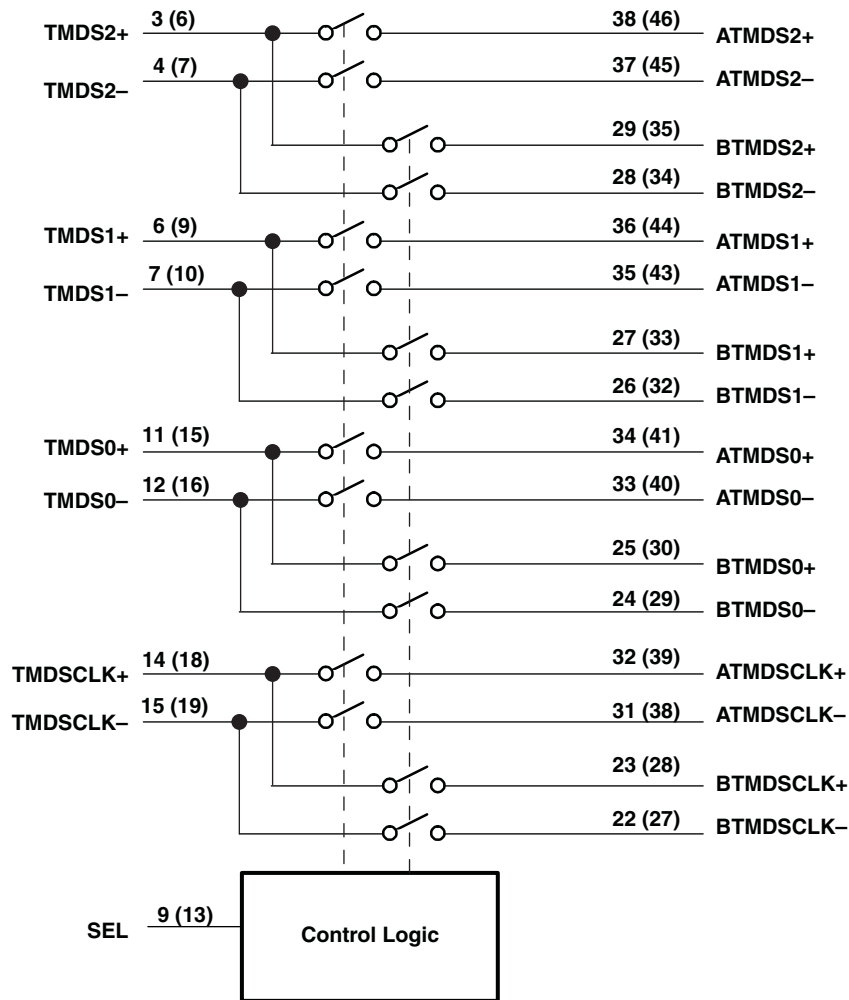


Table 2. FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSClk+ = ATMDSCLK+ TMDSClk- = ATMDSCLK- BTMDSn+ = High impedance BTMDSn- = High impedance BTMDSCLK+ = High impedance BTMDSCLK- = High impedance	TMDSn+ TMDSn- TMDSClk+ TMDSClk-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSClk+ = BTMDSCLK+ TMDSClk- = BTMDSCLK- ATMDSn+ = High impedance ATMDSn- = High impedance ATMDSCLK+ = High impedance ATMDSCLK- = High impedance	TMDSn+ TMDSn- TMDSClk+ TMDSClk-

FUNCTIONAL DIAGRAM



A. TVSOP package pin identification in parenthesis.

### TERMINAL FUNCTIONS

NAME	TERMINAL		TYPE	DESCRIPTION
	NO.			
	QFN (RUA)	TVSOP (DGV)		
ATMDS0–	33	40	I/O	Port A, channel 0, TMDS negative signal
ATMDS0+	34	41	I/O	Port A, channel 0, TMDS positive signal
ATMDS1–	35	43	I/O	Port A, channel 1, TMDS negative signal
ATMDS1+	36	44	I/O	Port A, channel 1, TMDS positive signal
ATMDS2–	37	45	I/O	Port A, channel 2, TMDS negative signal
ATMDS2+	38	46	I/O	Port A, channel 2, TMDS positive signal
ATMDSCLK–	31	38	I/O	Port A TMDS negative clock
ATMDSCLK+	32	39	I/O	Port A TMDS positive clock
BTMDS0–	24	29	I/O	Port B, channel 0, TMDS negative signal
BTMDS0+	25	30	I/O	Port B, channel 0, TMDS positive signal
BTMDS1–	26	32	I/O	Port B, channel 1, TMDS negative signal
BTMDS1+	27	33	I/O	Port B, channel 1, TMDS positive signal
BTMDS2–	28	34	I/O	Port B, channel 2, TMDS negative signal
BTMDS2+	29	35	I/O	Port B, channel 2, TMDS positive signal
BTMDSCLK–	22	27	I/O	Port B TMDS negative clock
BTMDSCLK+	23	28	I/O	Port B TMDS positive clock
SEL	9	13	I	Select pin to choose between port A or port B. Referenced to $V_{SS}$
TMDS0–	12	16	I/O	TMDS channel 0 negative signal
TMDS0+	11	15	I/O	TMDS channel 0 positive signal
TMDS1–	7	10	I/O	TMDS channel 1 negative signal
TMDS1+	6	9	I/O	TMDS channel 1 positive signal
TMDS2–	4	7	I/O	TMDS channel 2 negative signal
TMDS2+	3	6	I/O	TMDS channel 2 positive signal
TMDSCLK–	15	19	I/O	TMDS negative clock
TMDSCLK+	14	18	I/O	TMDS positive clock
$V_{DD}$	2, 8, 16, 18, 20, 30, 40, 42	2, 4, 12, 21, 23, 25, 36, 48	Power	Positive power supply voltage
$V_{SS}$	1, 5, 10, 13, 17, 19, 21, 39, 41	1, 3, 5, 8, 14, 17, 20, 22, 24, 26, 31, 37, 42, 47	Power	Negative power supply voltage

## ABSOLUTE MINIMUM AND MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted), - All voltages are with respect to  $V_{SS}$

			MIN	MAX	UNIT
$V_{DD}$	Supply voltage range		-0.5	2.5	V
$V_{IN}$	Control input voltage range <sup>(2)</sup>		-0.5	2.5	V
$V_{I/O}$	Switch I/O voltage range <sup>(2) (3)</sup>		-0.5	2.5	V
$I_{IK}$	Control input clamp current	$V_{IN} < V_{SS}$		50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < V_{SS}$		50	mA
$I_{I/O}$	ON-state switch current <sup>(4)</sup>			100	mA
$I_{DD}$	Continuous current through $V_{DD}$			100	mA
$I_{SS}$	Continuous current through $V_{SS}$			100	mA
$\theta_{JA}$	Package thermal impedance <sup>(5)</sup>	DGV package		58.0	°C/W
		RUA package		51.2	
$T_{stg}$	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3)  $V_I$  and  $V_O$  are used to denote specific conditions for  $V_{I/O}$ .
- (4)  $I_I$  and  $I_O$  are used to denote specific conditions for  $I_{I/O}$ .
- (5) The package thermal impedance is calculated in accordance with JESD 51-7.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
$V_{DD}$	Supply voltage	$V_{SS} = \text{GND}$	1.5	1.8	2.1	V
		$V_{SS} = 1.5 \text{ V}$	3	3.3	3.6	
$V_{IH}$	High-level input voltage	$3 \text{ V} < V_{DD} < 3.6 \text{ V}, V_{SS} = 1.5 \text{ V}$	$0.65(V_{DD} - V_{SS}) + V_{SS}$			V
$V_{IL}$	Low-level input voltage	$1.5 \text{ V} < V_{DD} < 2.1 \text{ V}, V_{SS} = 0 \text{ V}$	$0.35(V_{DD} - V_{SS}) + V_{SS}$			V
$V_{IO}$	Switch input/output voltage		0		$V_{DD}$	V
$T_A$	Operating free-air temperature		0		85	°C

## ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY<sup>(1)</sup>

$V_{DD} = 1.5 \text{ V to } 2.1 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{IK}$	SEL	$V_{DD} = 2.1 \text{ V}$ ,	$I_{IN} = -18 \text{ mA}$		-0.7	-1.2	V
$I_{IH}$	SEL	$V_{DD} = 2.1 \text{ V}$ ,	$V_{IN} = V_{DD}$			$\pm 1$	$\mu\text{A}$
$I_{IL}$	SEL	$V_{DD} = 2.1 \text{ V}$ ,	$V_{IN} = V_{SS}$			$\pm 1$	$\mu\text{A}$
$I_{off}$		$V_{DD} = 0$ ,	$V_O = 0 \text{ to } 2.1 \text{ V}$ ,			1	$\mu\text{A}$
$I_{CC}$		$V_{DD} = 2.1 \text{ V}$ ,	$I_{I/O} = 0$ ,		230	450	$\mu\text{A}$
			Switch ON or OFF				
$C_{IN}$	SEL	$f = 1 \text{ MHz}$ ,	$V_{IN} = 0$		0.7	1	pF
$C_{OFF}$	B port	$V_I = 0$ ,	$f = 1 \text{ MHz}$ ,		1	1.5	pF
			Outputs open,				
			Switch OFF				
$C_{ON}$		$V_I = 0$ ,	$f = 1 \text{ MHz}$ ,		4	4.5	pF
			Outputs open,				
			Switch ON				
$r_{on}$		$V_{DD} = 1.8 \text{ V}$ ,	$V_{SS} \leq V_I \leq V_{DD}$ ,		12.5	20	$\Omega$
			$I_O = -40 \text{ mA}$				
$r_{on(\text{flat})}$ <sup>(3)</sup>		$V_{DD} = 1.8 \text{ V}$ ,	$V_I = 1.65 \text{ V to } 1.8 \text{ V}$		0.5		$\Omega$
			$I_O = -40 \text{ mA}$				
$\Delta r_{on}$ <sup>(4)</sup>		$V_{DD} = 1.8 \text{ V}$ ,	$V_{SS} \leq V_I \leq V_{DD}$ ,		-0.1	0.2	$\Omega$
			$I_O = -40 \text{ mA}$				
<b>Dynamic</b>							
$X_{TALK}$		$R_L = 50 \Omega$ ,	$f = 825 \text{ MHz}$	See <a href="#">Figure 7</a>		-50	dB
$O_{IRR}$		$R_L = 50 \Omega$ ,	$f = 825 \text{ MHz}$	See <a href="#">Figure 8</a>		-50	dB
BW				See <a href="#">Figure 6</a>		1.9	GHz
Max data rate				See <a href="#">Figure 6</a>		3.8	Gbps

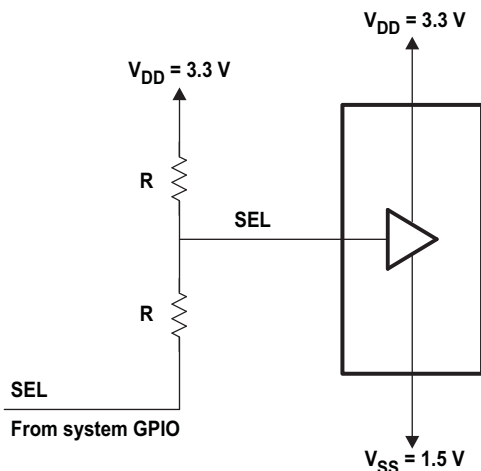
- (1)  $V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to I/O pins.  $V_{IN}$  refers to the control inputs.  
(2) All typical values are at  $V_{DD} = 1.8 \text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .  
(3)  $r_{on(\text{flat})}$  is the difference of  $r_{on}$  in a given channel at specified voltages.  
(4)  $\Delta r_{on}$  is the difference of  $r_{on}$  from centerports to any other port.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{DD} = 1.5 \text{ V to } 2.1 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ ,  $R_L = 200 \Omega$ ,  $C_L = 10 \text{ pF}$  (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{pd}$ <sup>(2)</sup>	TMDSn or xTMDSn	xTMDSn or TMDSn		0.25		ns
$t_{PZH}$ , $t_{PZL}$	SEL	TMDSn or xTMDSn	0.5		9	ns
$t_{PHZ}$ , $t_{PLZ}$	SEL	TMDSn or xTMDSn	0.5		5	ns
$t_{sk(o)}$ <sup>(3)</sup>	TMDSn or xTMDSn	xTMDSn or TMDSn		0.06		ns
$t_{sk(p)}$ <sup>(4)</sup>				0.06	0.1	ns

- (1) All typical values are at  $V_{DD} = 1.8 \text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .  
(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).  
(3) Output skew between center port to any other port  
(4) Skew between opposite transitions of the same output in a given device  $|t_{PHL} - t_{PLH}|$



This example circuit shows connecting control inputs to GPIOs of an application using  $V_{SS} = 1.5\text{ V}$ , which allows the device to pass TMDS signal levels

Figure 1. Example Voltage Divider Circuit

### TYPICAL CHARACTERISTICS

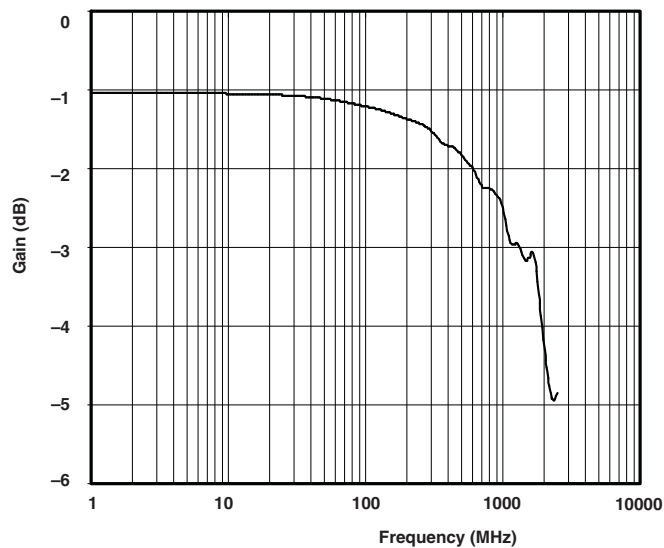


Figure 2. Insertion Loss

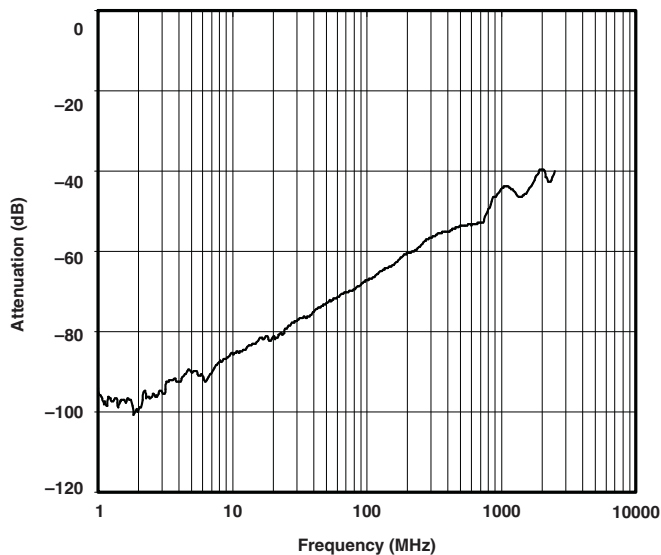
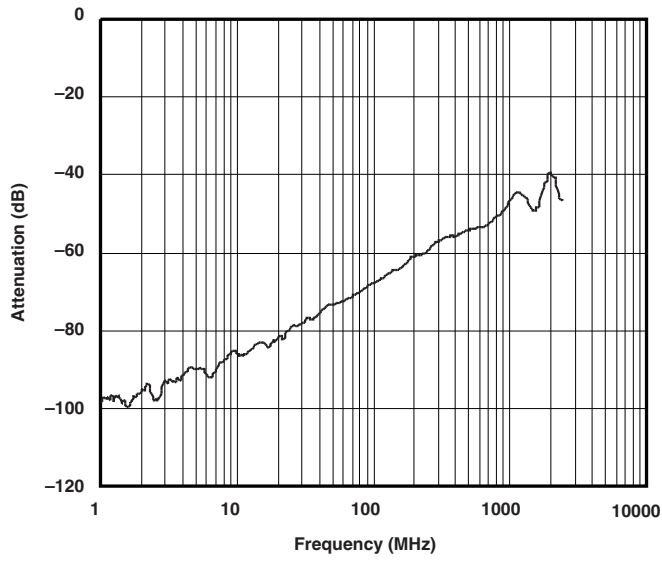
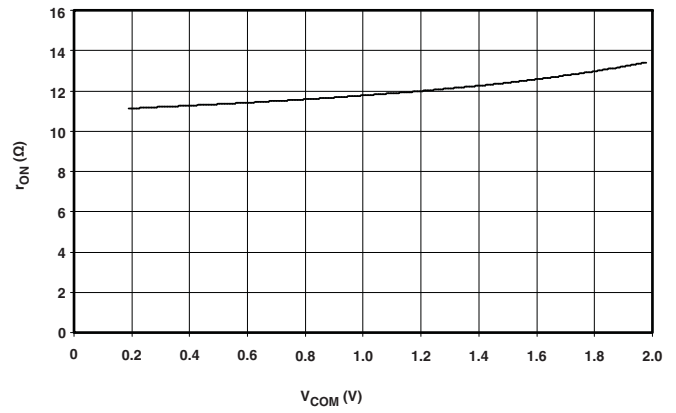


Figure 3. Crosstalk

**TYPICAL CHARACTERISTICS (continued)**

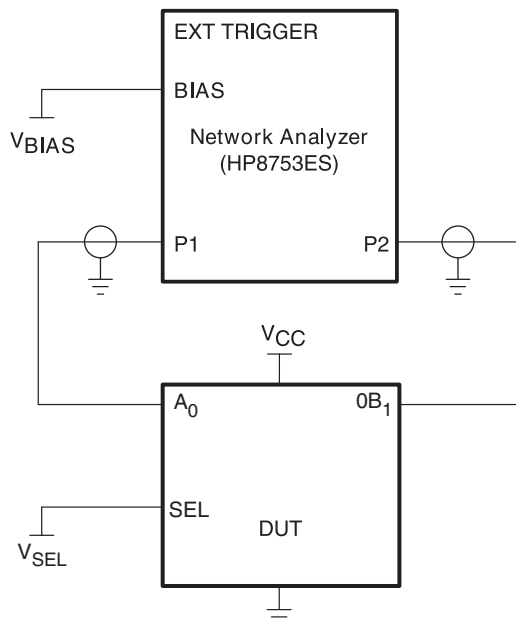


**Figure 4. Off Isolation vs Frequency**



**Figure 5. r<sub>ON</sub> vs V<sub>COM</sub>**

## PARAMETER MEASUREMENT INFORMATION



**Figure 6. Test Circuit for Frequency Response (BW)**

Frequency response is measured at the output of the ON channel. For example, when  $V_{SEL}$  is low and  $A_0$  is the input, the output is measured at  $0B_1$ . All unused analog I/O ports are left open.

### HP8753ES setup

Average = 4

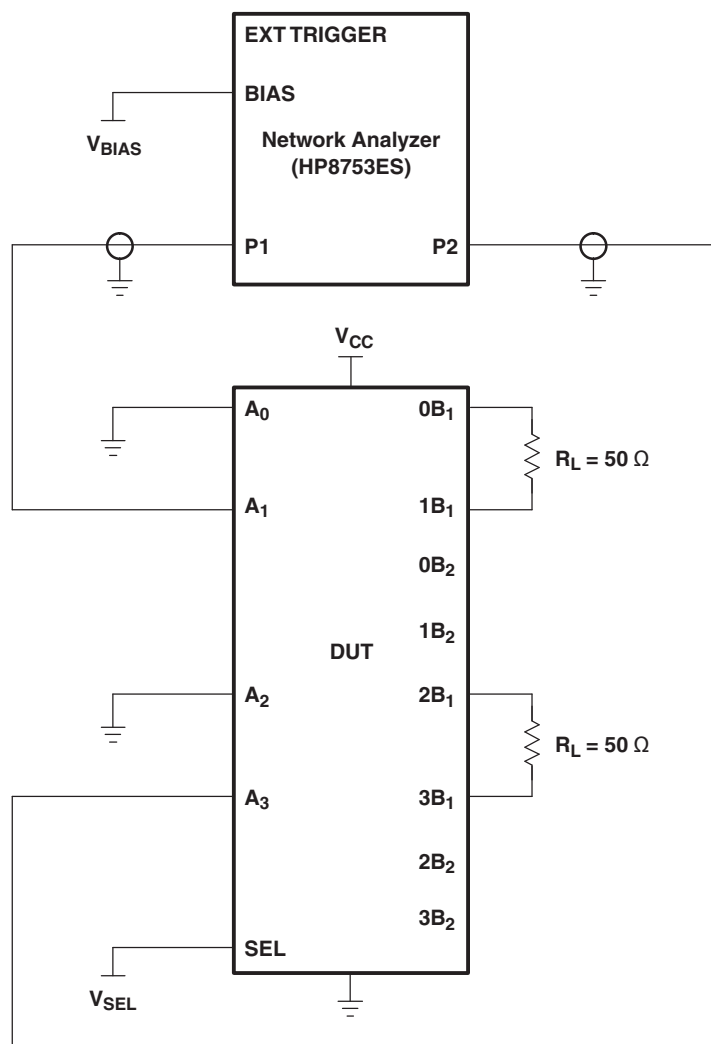
RBW = 3 kHz

$V_{BIAS} = 0.35$  V

ST = 2 s

P1 = 0 dBm

## PARAMETER MEASUREMENT INFORMATION (continued)



**Figure 7. Test Circuit for Crosstalk ( $X_{TALK}$ )**

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when  $V_{SEL}$  is low and  $A_0$  is the input, the output is measured at  $1B_1$ . All unused analog input (A) ports are connected to GND, and output (B) ports are connected to GND through 50- $\Omega$  pull-down resistors.

### HP8753ES setup

Average = 4

RBW = 3 kHz

$V_{BIAS}$  = 0.35 V

ST = 2 s

P1 = 0 dBm

PARAMETER MEASUREMENT INFORMATION (continued)

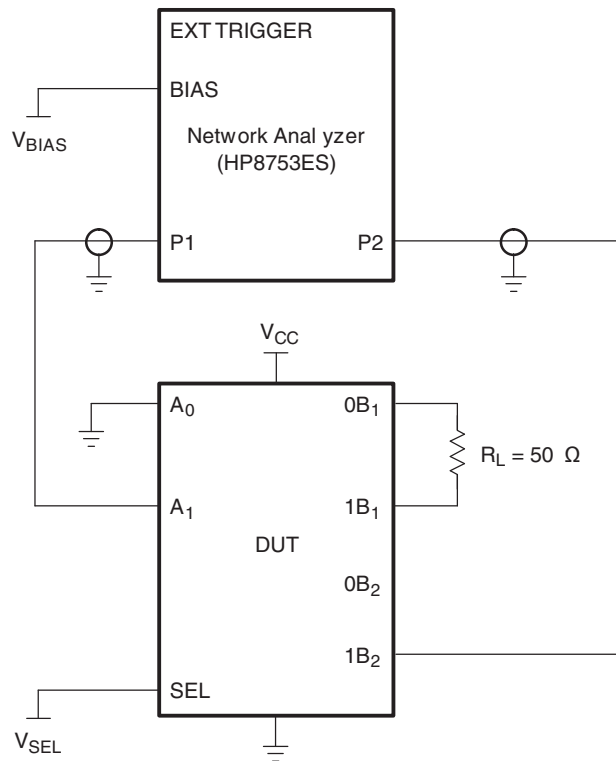


Figure 8. Test Circuit for OFF Isolation ( $O_{IRR}$ )

OFF isolation is measured at the output of the OFF channel. For example, when  $V_{SEL}$  is low and  $A_0$  is the input, the output is measured at  $0B_2$ . All unused analog input (A) ports are left open, and output (B) ports are connected to GND through 50- $\Omega$  pull-down resistors.

**HP8753ES setup**

Average = 4

RBW = 3 kHz

$V_{BIAS} = 0.35 \text{ V}$

ST = 2

P1 = 0 dBm

APPLICATION INFORMATION

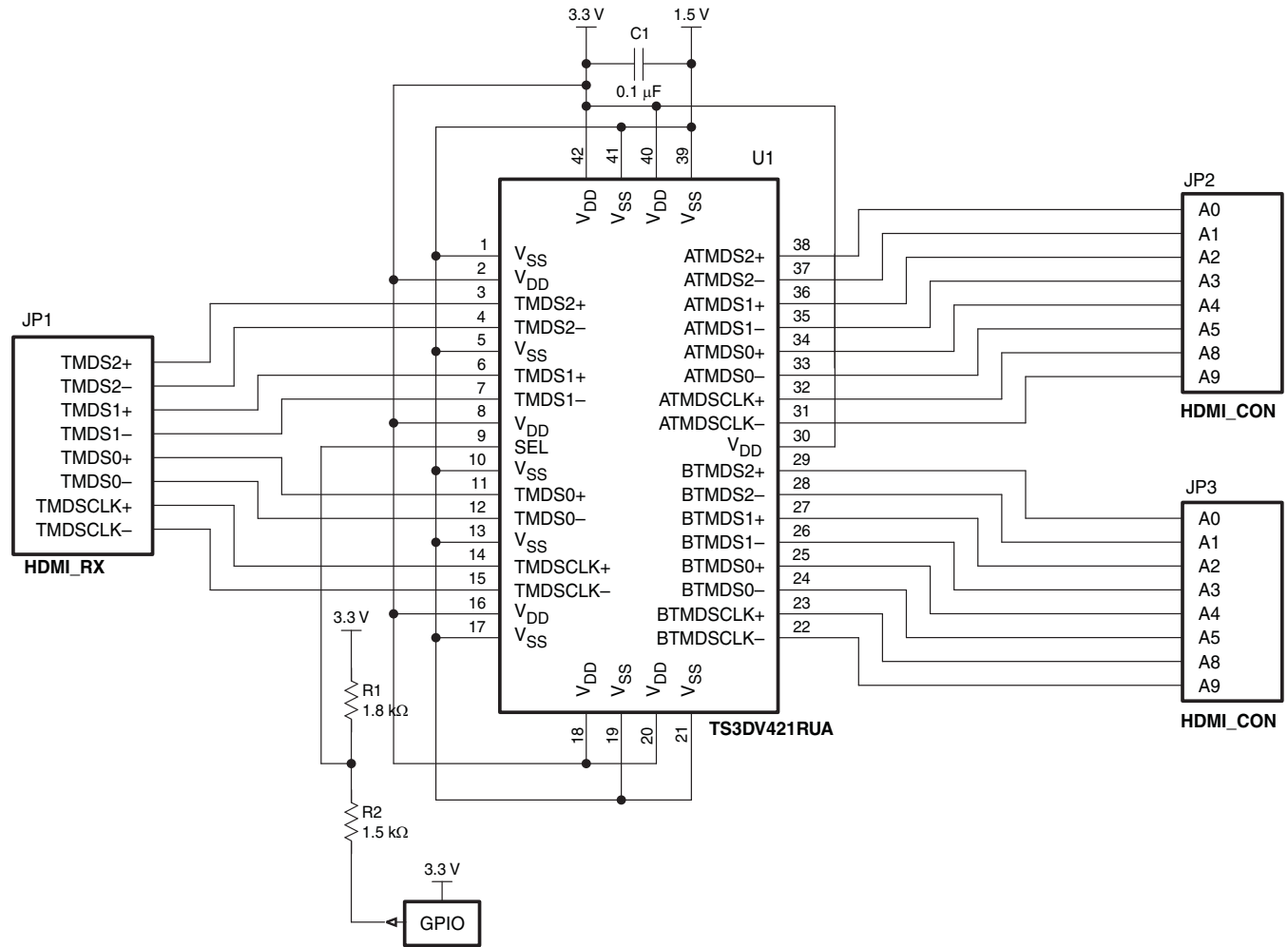


Figure 9. Reference Circuit for HDMI Application

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3DV421DGVR	ACTIVE	TVSOP	DGV	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SD421	<a href="#">Samples</a>
TS3DV421RUAR	ACTIVE	WQFN	RUA	42	3000	RoHS & Green	NIPDAU   NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	SD421	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3DV421DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
TS3DV421RUAR	WQFN	RUA	42	3000	330.0	24.4	3.9	9.4	1.0	8.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3DV421DGVR	TVSOP	DGV	48	2000	356.0	356.0	35.0
TS3DV421RUAR	WQFN	RUA	42	3000	346.0	346.0	35.0

## GENERIC PACKAGE VIEW

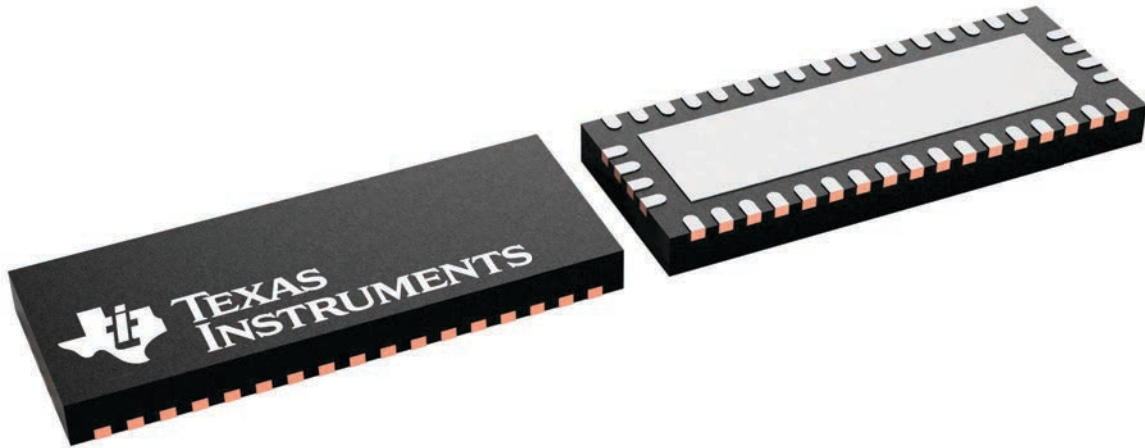
**RUA 42**

**WQFN - 0.8 mm max height**

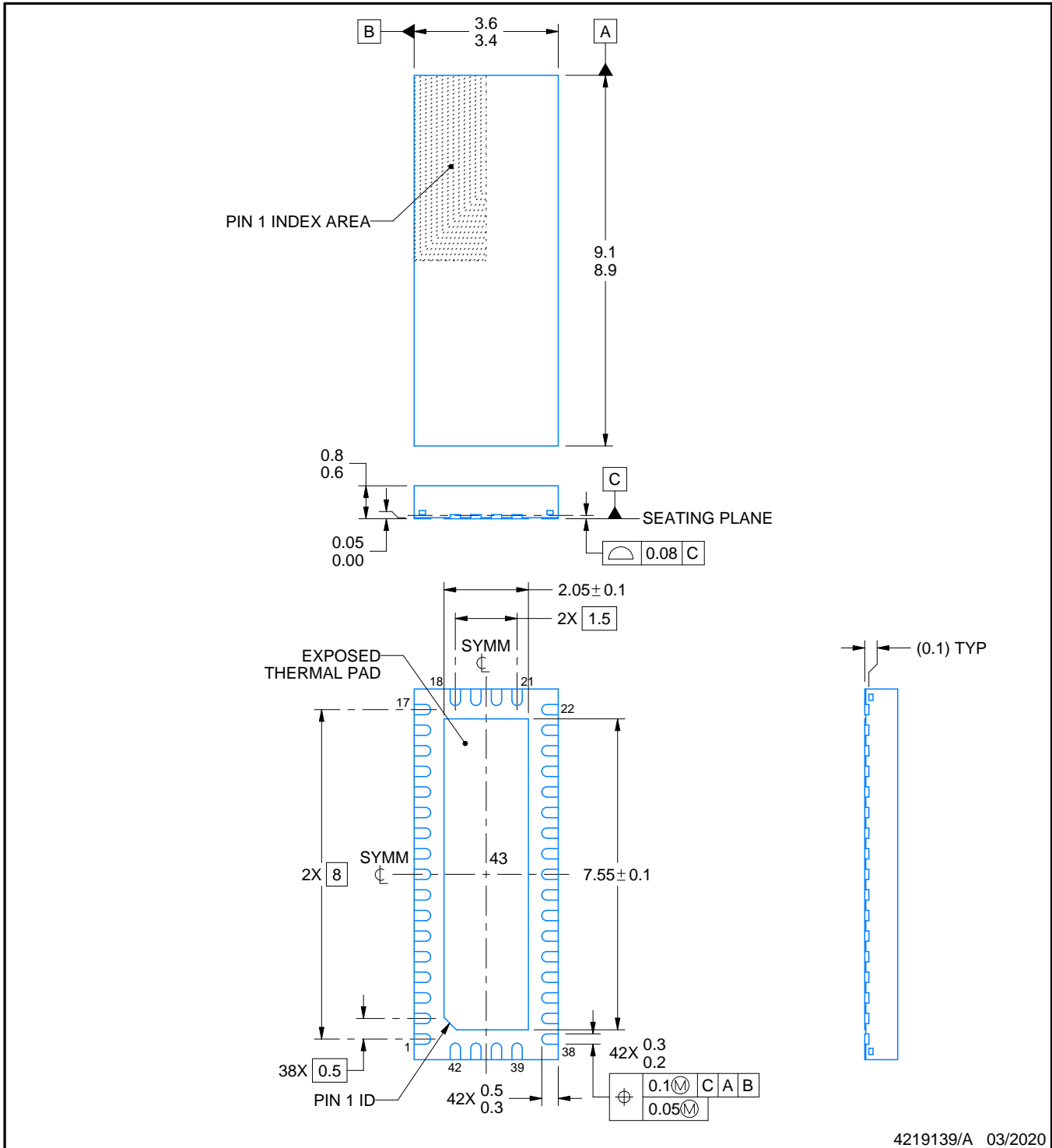
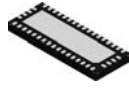
9 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4226504/A



4219139/A 03/2020

NOTES:

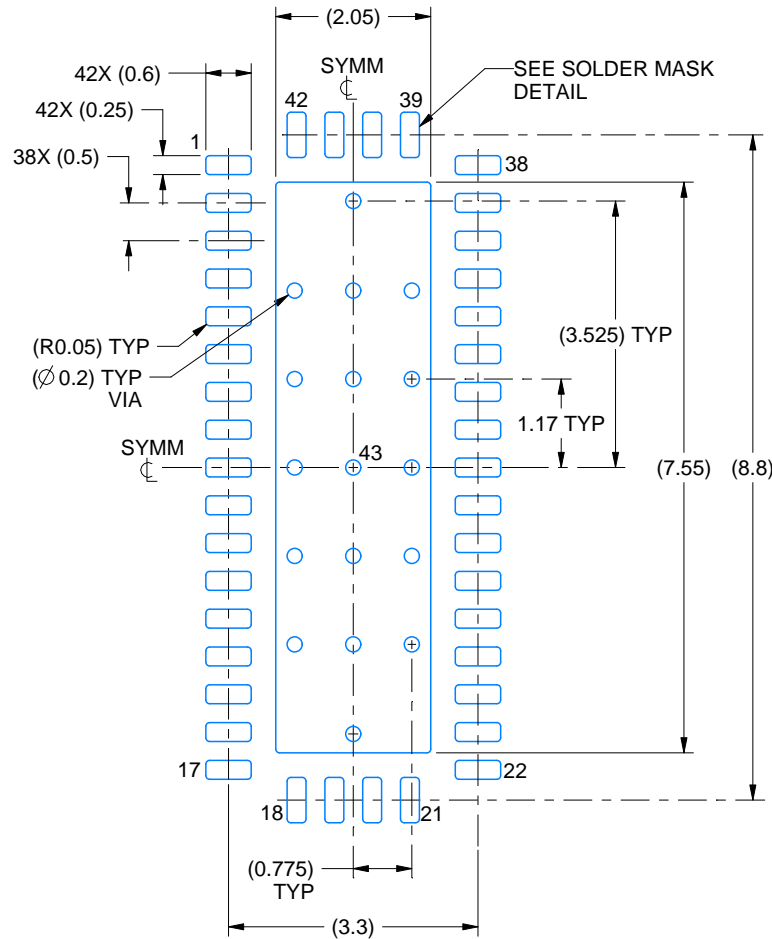
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

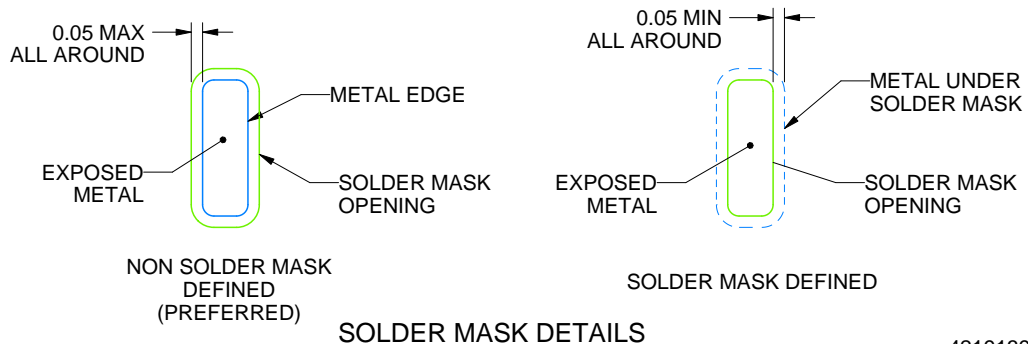
RUA0042A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4219139/A 03/2020

NOTES: (continued)

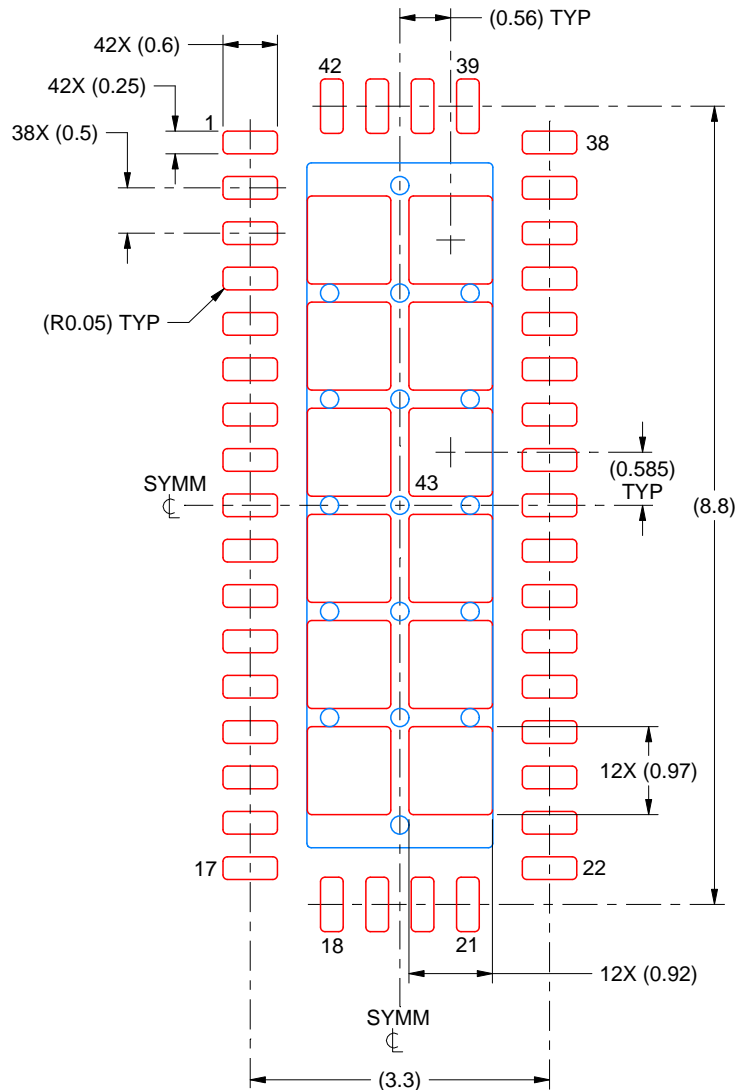
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RUA0042A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 12X

EXPOSED PAD 43  
69% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219139/A 03/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View TS3DV421RUAR on WIN SOURCE](#)

 [Texas Instruments](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management