THE DATASHEET OF

TPS51601ADRBR

Dual High Efficiency Synchronous MOSFET Driver

Check for Samples: TPS51601A

FEATURES

- **High Voltage Synchronous Buck Driver**
- **Integrated Boost Switch for Bootstrap Action**
- **Adaptive Dead Time Control and Shoot-through Protection**
- **0.4-Ω Sink Resistance for Low-side Drive**
- **1.0-Ω Source Resistance for High-side Drive**
- **$\overline{\text{SKIP}}$ Pin to Improve Light-Load Efficiency**
- **Adaptive Zero-Crossing Detection for Optimal Light-Load Efficiency**
- **8-Pin 3 mm × 3 mm SON (DRB) Package**

APPLICATIONS

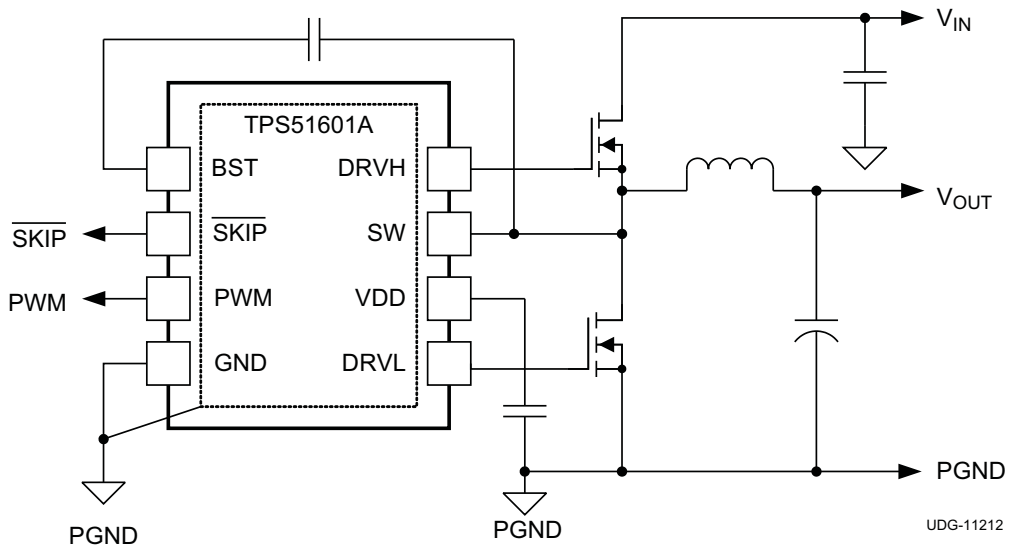
- **Mobile core regulator products**
- **High frequency DC-DC Converters**
- **High input voltage DC-DC converters**
- **Multiphase DC-DC converters**

DESCRIPTION

The TPS51601A is a synchronous buck MOSFET driver with integrated boost switch. This high-performance driver is capable of driving high-side and low-side side N-channel FETs with the highest speed and lowest switching loss. Adaptive dead-time control and shoot-through protection are included.

The TPS51601A is available in the space-saving 8-pin 3 mm × 3 mm SON package and operates between –40°C and 105°C.

SIMPLIFIED APPLICATION



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)(2)

T_A	PACKAGE	ORDERABLE NUMBER	PINS	TRANSPORT MEDIA	MINIMUM QUANTITY	ECO PLAN
–40°C to 105°C	Plastic Small Outline No-Lead (SON)	TPS51601ADRBT	8	Tape-and-reel (large)	250	Green (RoHS and no Sb/Br)
		TPS51601ADRBR		Tape-and-reel (small)	3000	

(1) For the most current package and ordering information see the *Package Option Addendum* at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

		MIN	MAX	UNIT
Input voltage	VDD	-0.3	6	V
	PWM, $\overline{SKIP}$	-0.3	6	
Output voltages	BST to SW	-0.3	6	V
	DRVH to SW	-0.3	6	
	DRVL	-0.3	6	
	SW	-1	32	
Ground	GND	-0.3	0.3	V
Operating junction temperature, T_J		-40	125	°C
Storage temperature, T_{stg}		-55	150	°C

(1) Stresses beyond those listed in this table may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the RECOMMENDED OPERATING CONDITIONS table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.
(3) Voltage values are with respect to the corresponding LL terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS51601 DRB 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	42.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	3.0	
θ_{JB}	Junction-to-board thermal resistance(4)	18.9	
ψ_{JT}	Junction-to-top characterization parameter(5)	62.1	
ψ_{JB}	Junction-to-board characterization parameter(6)	19.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	12.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
Input voltages	VDD	4.5		5.5	V
	PWM, $\overline{\text{SKIP}}$	-0.1		5.5	
Output voltages	BST to SW	-0.1		5.5	V
	DRVH to SW	-0.1		5.5	
	DRVL	-0.1		5.5	
	SW	-1		30	
Ground	GND	-0.1		0.1	V
Operating junction temperature, T_J		-40		105	°C

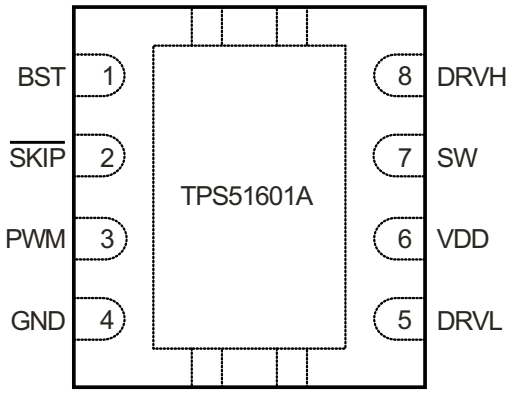
ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{VDD} = 5.0 V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY, UNDERVOLTAGE LOCKOUT						
I_{VDD}	VDD bias current	PWM = HI		160	220	µA
		PWM = LO		500		
		PWM = float		50		
$V_{UVLO(h)}$	VDD UVLO 'OK' threshold		3.5	3.7	3.9	V
$V_{UVLO(l)}$	VDD UVLO fault threshold		3.3	3.5	3.7	V
$V_{UVLO(hys)}$	VDD UVLO hysteresis			0.2		V
PWM INPUT						
$V_{IH(pwm)}$	HIGH-level PWM input		4.0			V
$V_{IL(pwm)}$	LOW-level PWM input				0.7	V
$R_{VDD-PWM}$	VDD-to-PWM resistance			30		kΩ
$R_{PWM-GND}$	PWM-to-GND resistance			20		kΩ
$V_{PWM(tri)}$	PWM tri-state voltage	PWM floating	1.5		2.5	V
$\overline{SKIP}$ INPUT						
$V_{IH(skip)}$	HIGH-level $\overline{SKIP}$ input logic		2.2			V
$V_{IL(\overline{skip})}$	LOW-level $\overline{SKIP}$ input logic				0.7	V
$IL_{\overline{SKIP}-GND}$	$\overline{SKIP}$-to-GND leakage	$V_{\overline{SKIP}}$ = 5 V			2	µA
GATE DRIVE OUTPUT						
R_{DRVH}	DRVH on resistance	Source resistance, (V_{BST} –V_{LL}) = 5 V, HIGH-state (V_{BST} – V_{DRVH}) = 0.1 V		1.0	2.5	Ω
		Sink resistance, (V_{BST} –V_{LL}) = 5 V, LOW-state (V_{DRVH} – V_{LL}) = 0.1 V		0.5	1.5	
R_{DRVL}	DRVL on resistance	Source resistance, (V_{VDD} – GND) = 5 V, HIGH-state, V_{VDD} – V_{DRVL}) = 0.1V		0.8	1.5	Ω
		Sink resistance, VDD – GND = 5 V LOW-state, VDRVL – GND = 0.1 V		0.4	1.0	
TIMING CHARACTERISTICS						
t_{DRVH}	DRVH transition time	DRVH rising, C_{DRVH} = 3.3 nF		15	35	ns
		DRVH falling, C_{DRVH} = 3.3 nF		10	35	
t_{DRVL}	DRVL transition time	DRVL rising, C_{DRVL} = 3.3 nF		15	35	ns
		DRVL, falling, C_{DRVL} = 3.3 nF		10	35	
$t_{NONOVLP}$	Driver non-overlap time	DRVH LOW to DRVL HIGH	5	20		ns
		DRVL LOW to DRVH HIGH	5	20		
$t_{DLY(rise)}$	PWM rising to drive output delay	DCM mode: PWM rising to DRVH rising		25		ns
		CCM mode: PWM rising to DRVL falling		25		
$t_{DLY(fall)}$	PWM falling to drive output delay	PWM falling to DRVH falling		25		ns
t_{DLY1}	3-state propagation delay to LOW	PWM floating to PWM LOW		40		ns
t_{DLY2}	3-state propagation delay to HIGH	PWM floating ti PWM HIGH		50		ns
$t_{TS(hold)}$	3-state hold-off time	PWM entering tri-state from HIGH or LOW		150		ns
$t_{\overline{SKIP}(pdh)}$	$\overline{SKIP}$ LOW-to-HIGH propagation delay			15		ns
$t_{\overline{SKIP}(pdl)}$	$\overline{SKIP}$ HIGH-to-LOW propagation delay			15		ns
$t_{DRVH(min)}$	Minimum DRVH width				80	ns
$t_{DRVL(min)}$	Minimum DRVL width	Minimum DRVL width before Zero-crossing can turn OFF DRVL		400	500	ns
BOOT-STRAP SWITCH (BST)						
R_{BST}	BST switch on-resistance	I_{BST} = 10 mA	4	10	20	Ω
$I_{BST(leak)}$	BST switch leakage current	V_{BST} = 34 V, V_{SW} = 28 V			2	µA

DEVICE INFORMATION

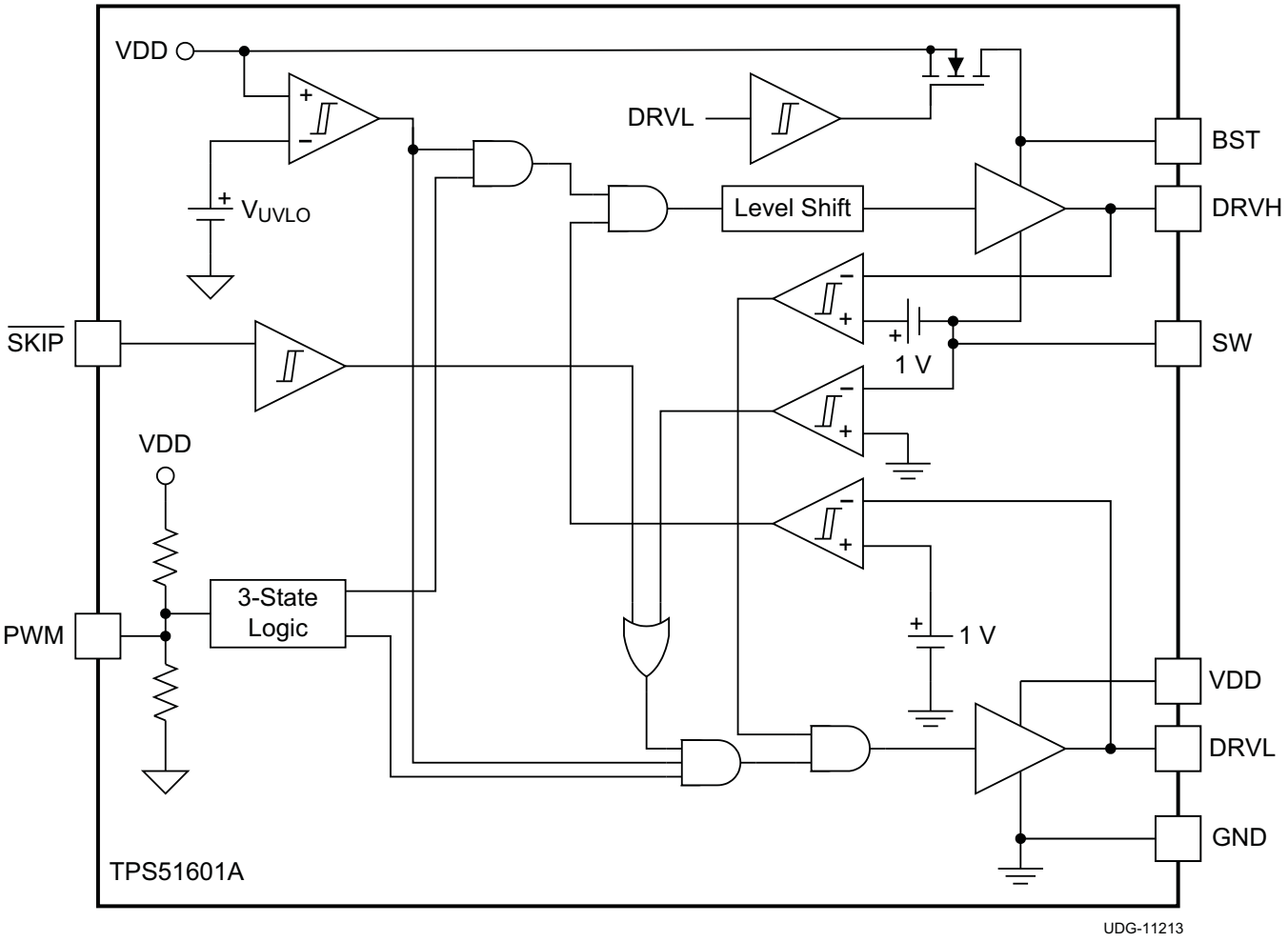
QFN (DRB) PACKAGE
8 PINS
(TOP VIEW)



PIN FUNCTIONS

PIN NAME	I/O	DESCRIPTION
BST	I	High-side, N-channel FET bootstrap voltage input, supply for high-side driver
DRVH	O	High-side, N-channel FET gate drive output.
DRVL	O	Low-side, synchronous N-channel FET gate drive output
GND	–	Low-side, synchronous N-channel FET gate drive return and device ground.
PWM	I	PWM input. This defines the on-time for the high-side FET of the converter. Input is coming from PWM controller. A 3-state voltage on this pin turns OFF both the high-side (DRVH) and low-side drivers (DRVL)
PwrPAD	–	Thermal pad. This is a non-electrical pad and is recommended to be connected to GND.
$\overline{\text{SKIP}}$	I	If $\overline{\text{SKIP}}$ is LOW, then the inductor current zero-crossing is active and DRVL turns off when inductor current goes to zero. (discontinuous conduction mode active) If $\overline{\text{SKIP}}$ is HIGH, then the DRVL stays HIGH as long as PWM stays LOW. (forced continuous conduction mode)
SW	I/O	High-side N-channel FET gate drive return. Also used as input for sensing inductor current for zero-crossing.
VDD	I	5-V power supply input for the device.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

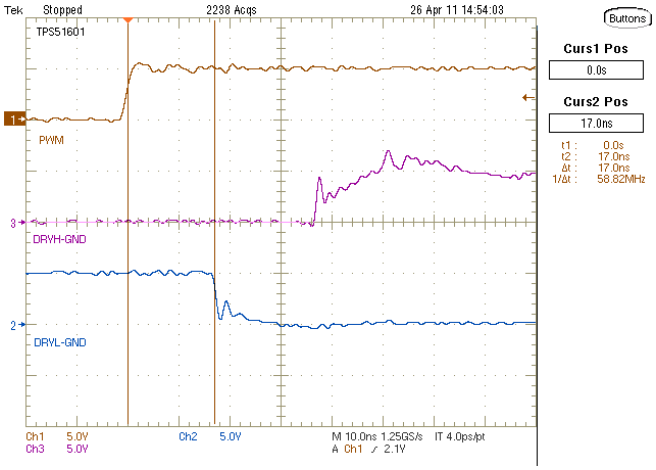


Figure 1. PWM Rising to DRVL Falling

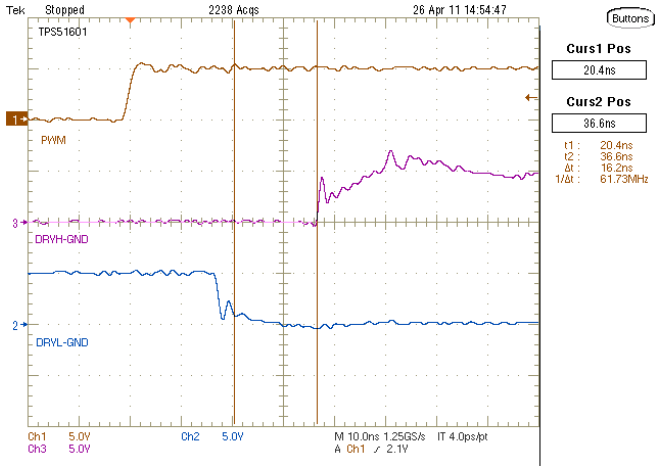


Figure 2. DRVL Falling to DRVH rising

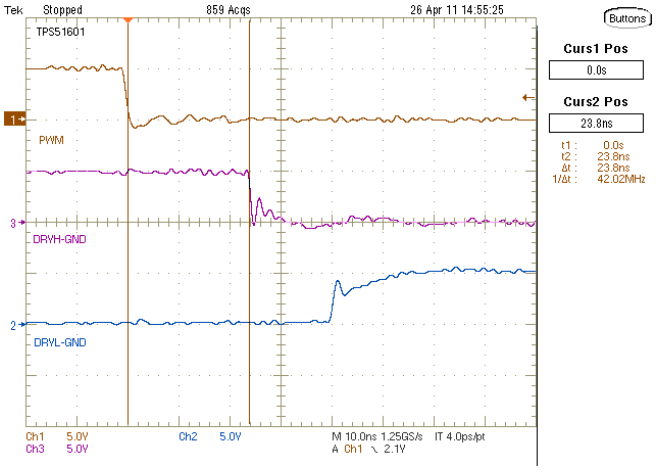


Figure 3. PWM Falling to DRVH Falling

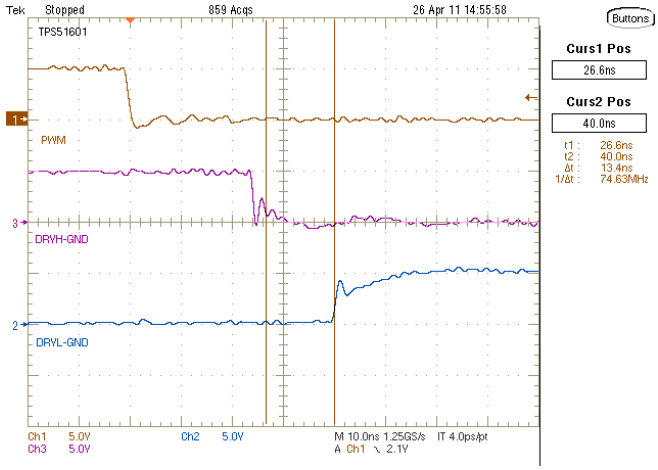


Figure 4. SW-Node Falling to DRVL Rising

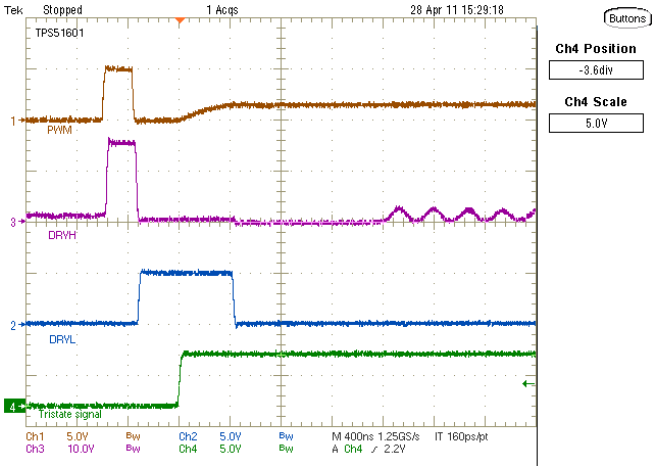


Figure 5. 3-State Entry on DRVL

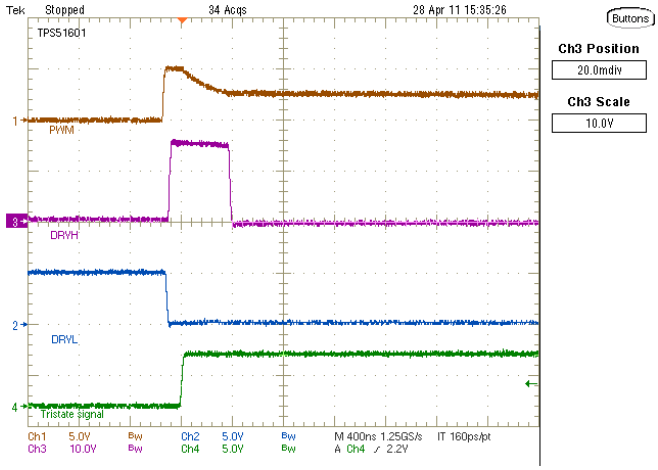


Figure 6. 3-State Entry on DRVH

TYPICAL CHARACTERISTICS (continued)

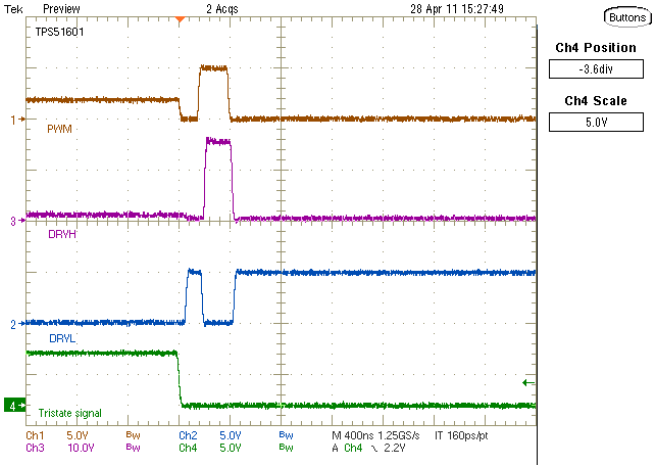


Figure 7. 3-State Exit on DRVL

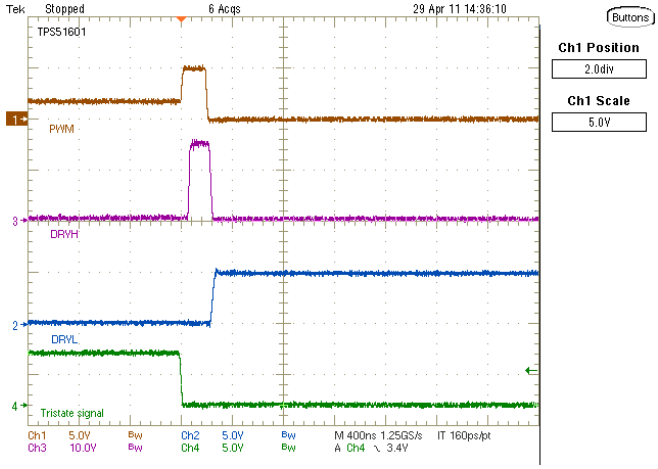


Figure 8. 3-State Exit on DRVH

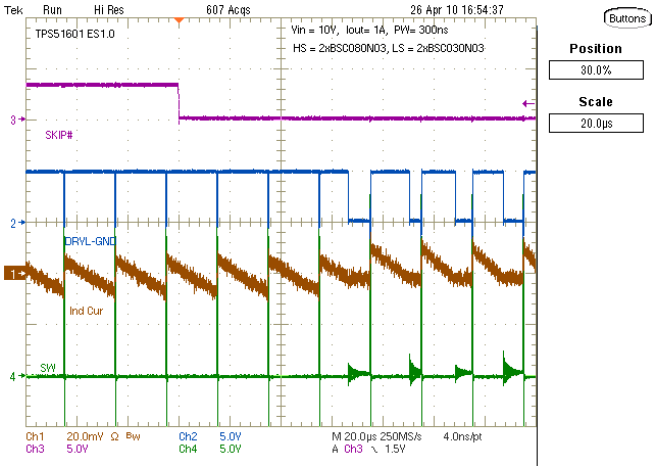


Figure 9. FCCM Exit and SKIP Mode Entry

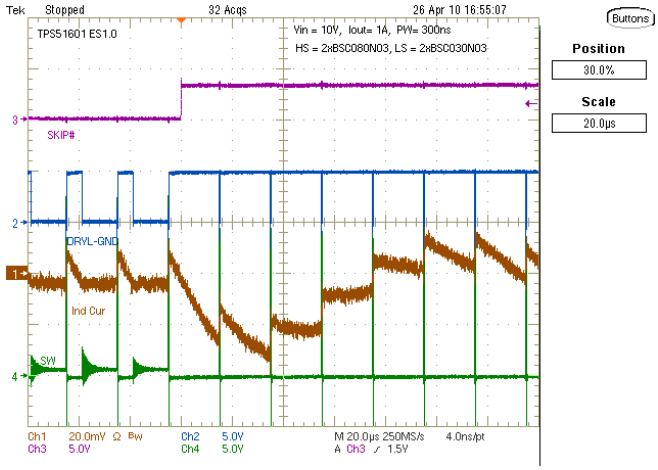


Figure 10. SKIP Mode Exit and FCCM Entry

TYPICAL CHARACTERISTICS

For Figure 11 through Figure 16 high-side FET used is CSD17302Q5A and low-side FET used is CSD17303Q5.

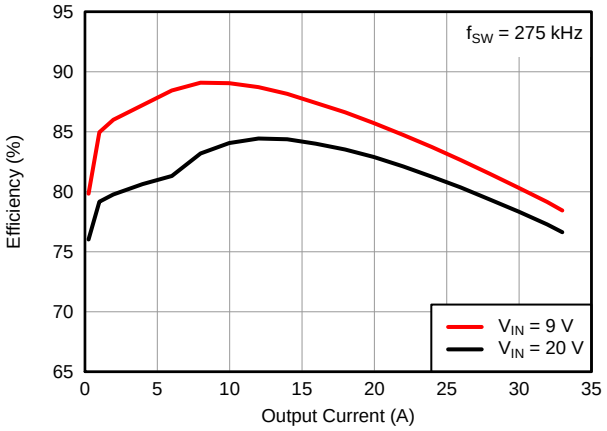


Figure 11. Efficiency vs. Output Current

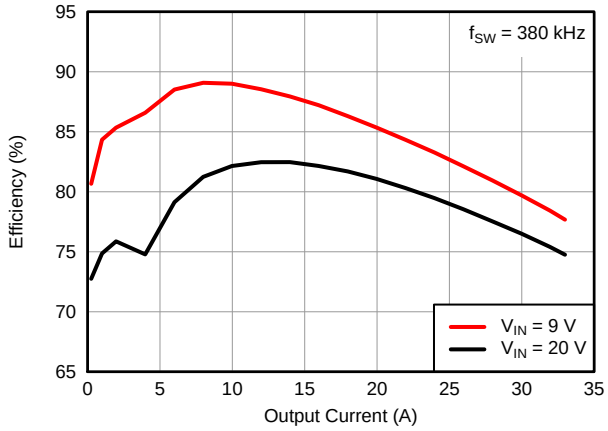


Figure 12. Efficiency vs. Output Current

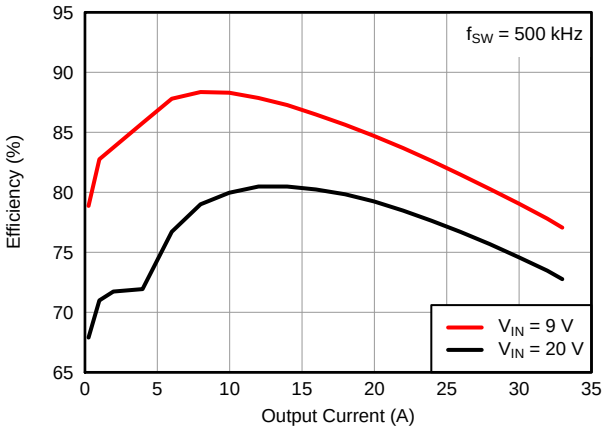


Figure 13. Efficiency vs. Output Current

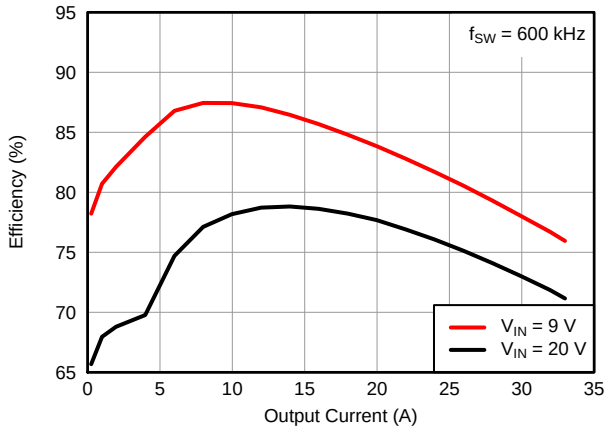


Figure 14. Efficiency vs. Output Current

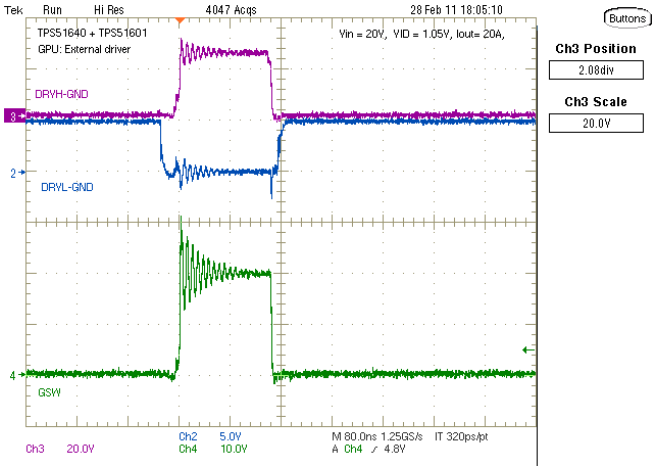


Figure 15. Gate Driver Waveforms Using TPS51640 Controller and TPS51601A Driver at V_{IN} = 9 V

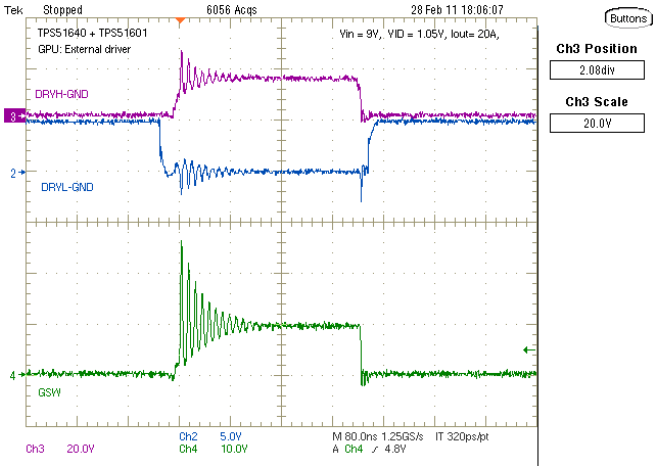


Figure 16. Gate Driver Waveforms Using TPS51640 Controller and TPS51601A Driver at V_{IN} = 20 V

DETAILED DESCRIPTION

UVLO

The TPS51601A includes an undervoltage lockout circuit that disables the driver and external power FETs in an OFF state when the input supply voltage, (V_{VDD}) is insufficient to drive external power FET reliably. During the power-up sequence, both gate drive outputs remain low until the VDD voltage reaches UVLO-H threshold, typically 3.7 V. Once the UVLO threshold is reached, the condition of the gate drive outputs is defined by the input PWM and SKIP signals. During the power-down sequence, the UVLO threshold is set lower, typically 3.5 V.

PWM Input

Once the input supply voltage is above the UVLO threshold, the gate drive outputs are defined by the PWM input and SKIP input. Prior to PWM going HIGH, both the gate drive outputs, (DRVH and DRVL) are held LOW. The DRVL is LOW until the first PWM HIGH pulse to support pre-biased start-up. Once PWM goes HIGH for the first time, DRVH goes HIGH. Then, when PWM goes LOW, DRVH goes LOW first. After the non-overlap time, DRVL goes HIGH.

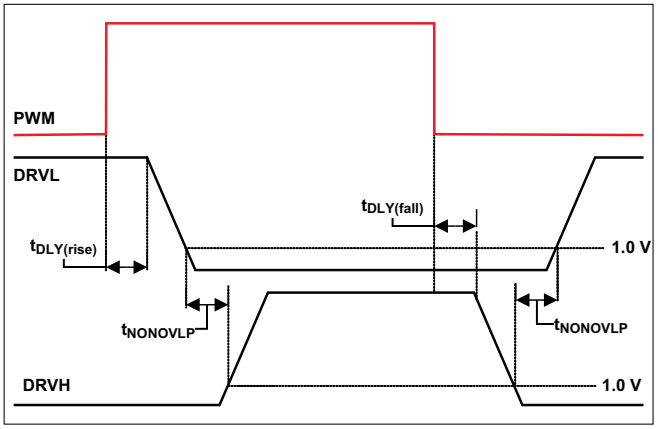


Figure 17. Continuous Conduction Mode Waveforms

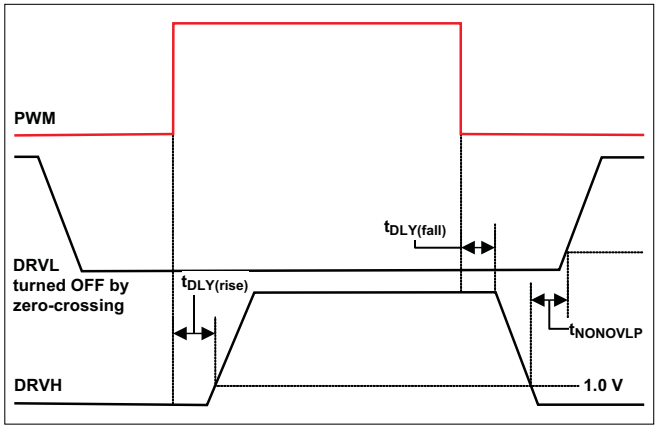


Figure 18. Discontinuous Conduction Mode Waveforms

SKIP/FCCM Mode Operation

The TPS51601A can be configured in two ways. When used as the external driver for Phase 1, this pin connects to the corresponding SKIP pin of the PWM controller. The SKIP pin is active low signal. This means when SKIP is low, then the zero crossing detection circuit of the driver is active. When SKIP is high, the zero-crossing detector is disabled and the converter operates in forced continuous conduction mode (FCCM).

Adaptive Zero-Crossing

The TPS51601A has an adaptive zero-crossing detector. Zero crossing accuracy is detected by checking the switch-node voltage at an appropriate time after the low-side FET is turned OFF by DRVL going low. Then the zero-crossing comparator offset is updated based on previous result. After several zero-crossing events, the comparator offset is optimized to give the best efficiency.

Adaptive Dead-Time Control (Anti-Cross Conduction)

The TPS51601A has an adaptive dead-time control logic to minimize the non-overlap time between DRVH and DRVL signals. The internal signal to the low-side driver goes HIGH only when the DRVH-SW voltage goes below approximately 1 V and DRVH goes below approximately 1 V to ensure the high-side MOSFET has turned OFF. Additional driver delays ensure that there is some non-overlap time between DRVH falling edge and DRVL rising edge. Similarly, the internal signal to the DRVH goes high only after DRVL-GND goes below 1 V.

Integrated Boost-Switch

To maintain a BST-SW voltage close to VDD (to get lower conduction losses on the high-side FET), the conventional diode from VDD to BST is replaced by a FET which is gated by DRVL signal.

APPLICATION INFORMATION

Figure 19 shows a typical application. Resistors R1 and R2 can be used if necessary to reduce the switch-node ringing.

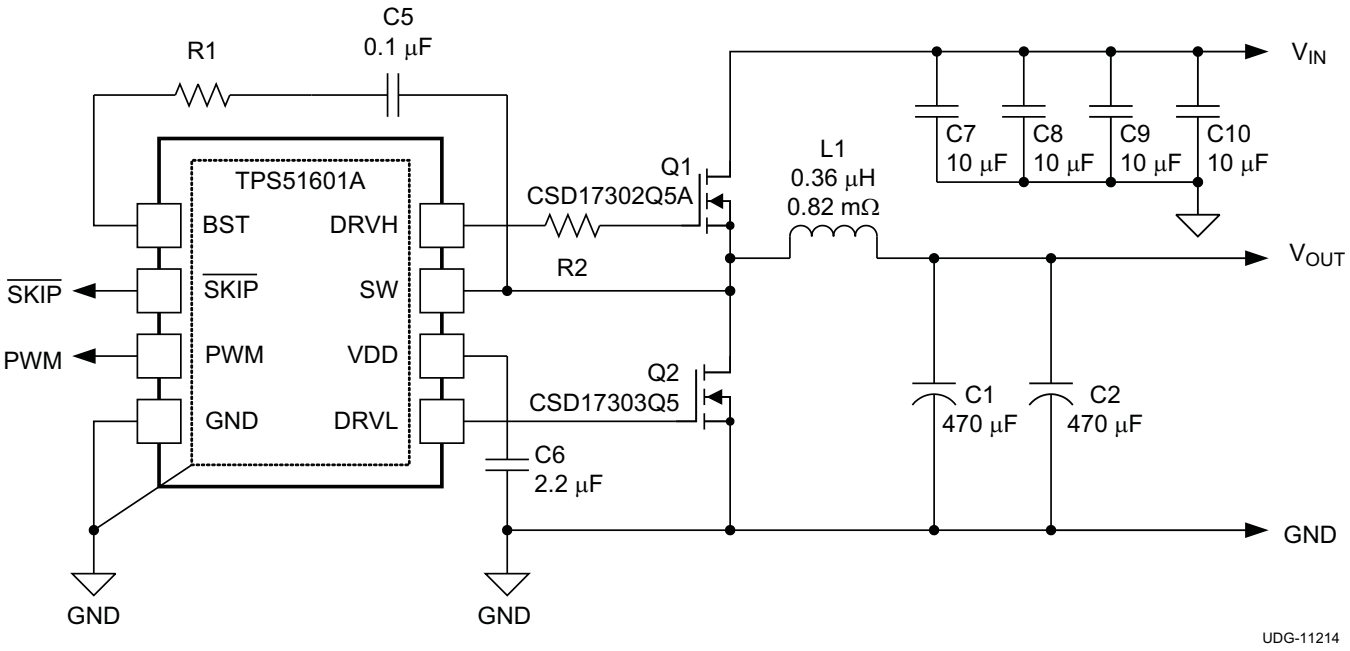


Figure 19. Typical Application

PCB Layout Guidelines

Figure 20 shows the primary current loops in each phase, numbered in order of importance. The most important loop to minimize the area of is Loop 1, the path from the input capacitor through the high-side and low-side FETs, and back to the capacitor through ground. Loop 2 is from the inductor through the output capacitor, ground and Q2. The layout of the low side gate drive (loops 3a and 3b) is important. The guidelines for gate drive layout are:

- Make the low-side gate drive as short as possible (1 inch or less preferred).
- Make the DRVL width to length ratio of 1:10, wider (1:5) if possible.
- If changing layers is necessary, use at least two vias.
- Decouple VDD to GND (C_D in Figure 20) with at ceramic capacitor with a value of least a 2.2-µF.

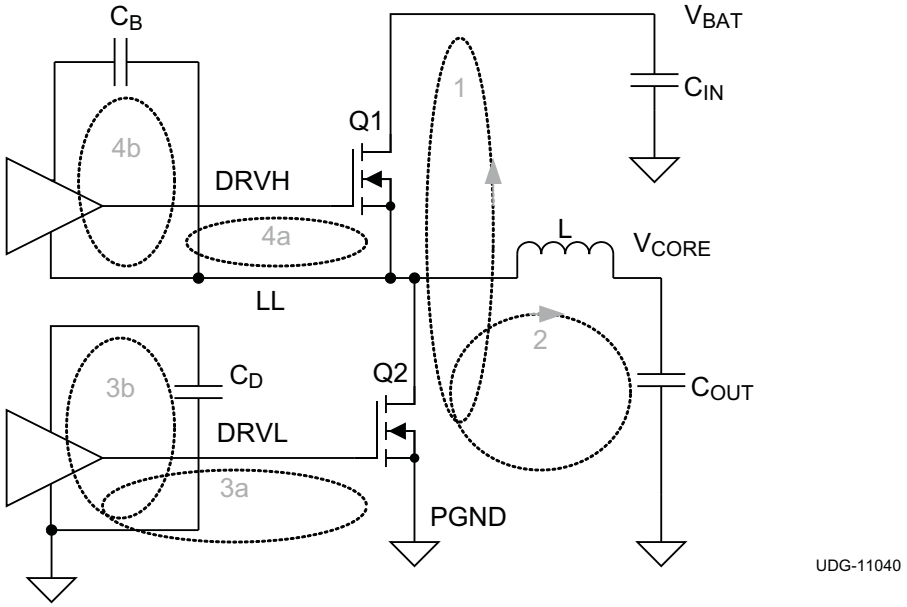


Figure 20. Minimizing Current Loops

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS51601ADRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	601A	Samples
TPS51601ADRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	601A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

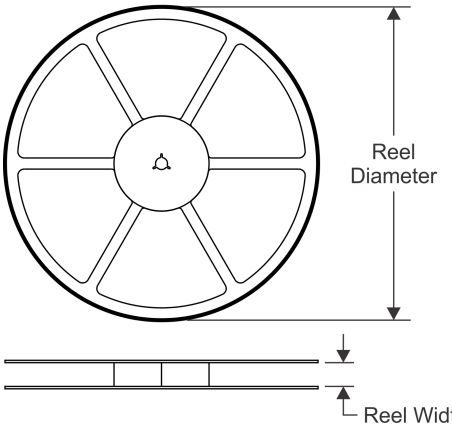
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

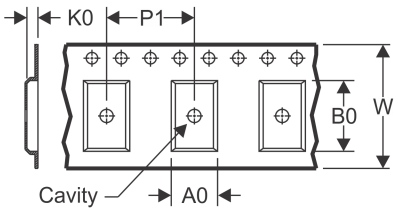
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

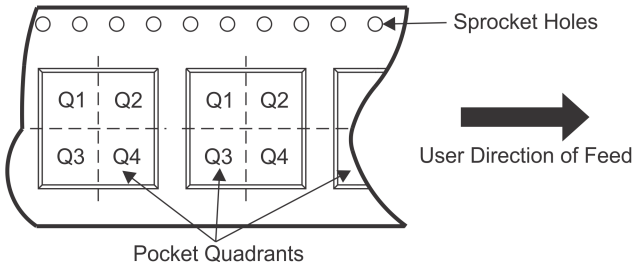


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

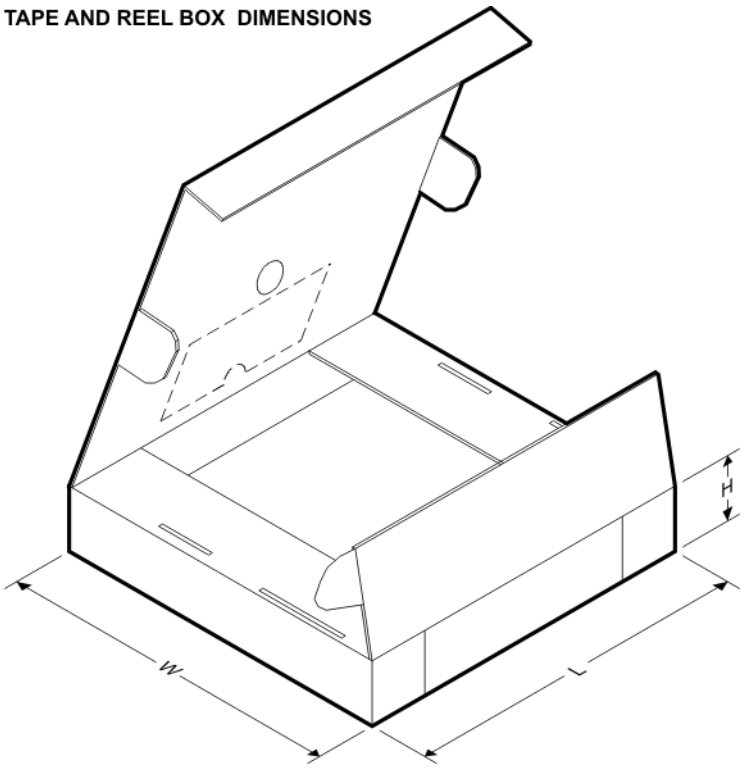
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51601ADRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS51601ADRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51601ADRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS51601ADRBT	SON	DRB	8	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DRB 8

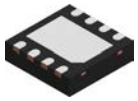
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

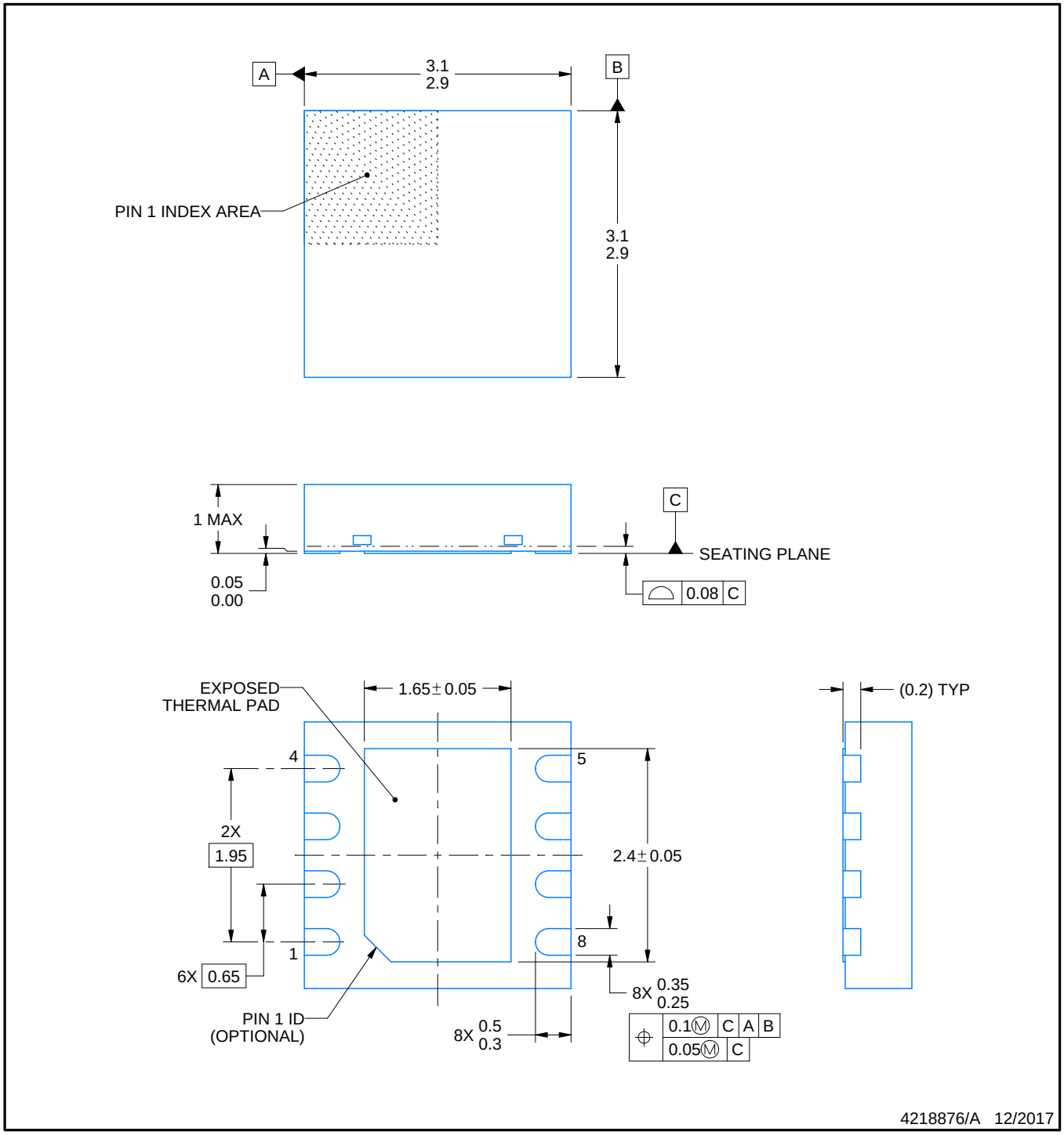
DRB0008B



PACKAGE OUTLINE

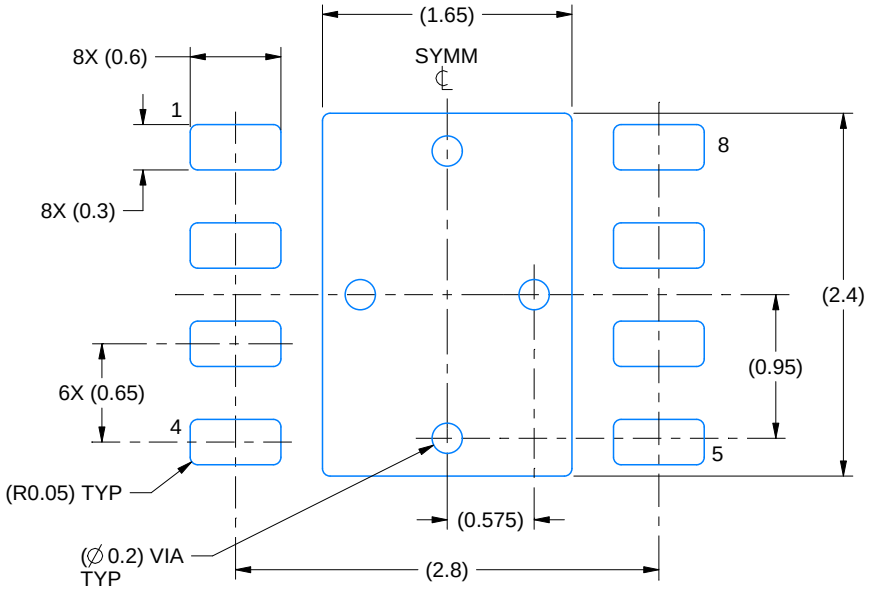
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

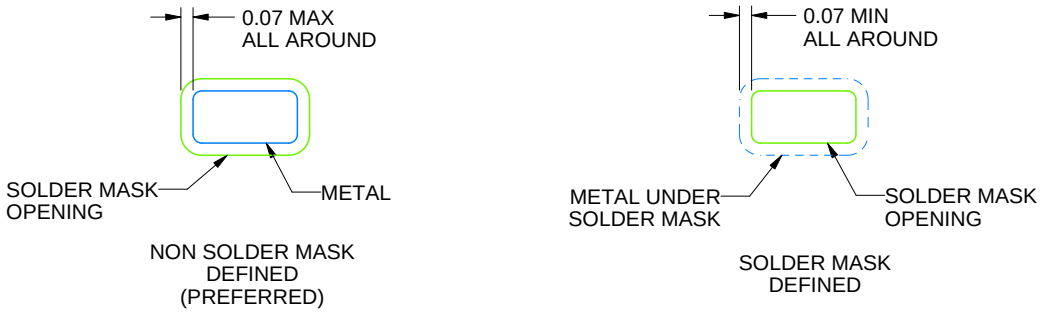


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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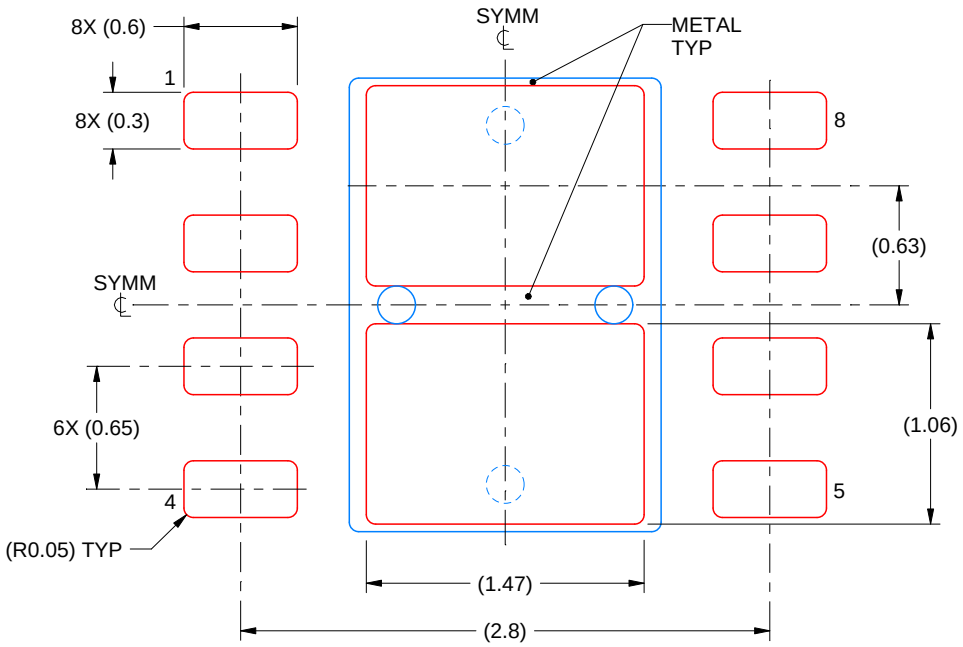
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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