# THE DATASHEET OF

# TPS3808G33MDBVREP

# TPS3808-EP Low Quiescent Current, Programmable Delay Supervisory Circuit

## 1 Features

- Controlled Baseline
  - One Assembly Site
  - One Test Site
  - One Fabrication Site
- Extended Temperature Performance of –55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree (1)
- Power-On Reset Generator With Adjustable Delay Time: 1.25 ms to 10 s
- Very Low Quiescent Current: 2.4 µA Typical
- High Threshold Accuracy: 0.5% Typical
- Fixed Threshold Voltages for Standard Voltage Rails From 0.9 V to 5 V and Adjustable Voltage Down to 0.4 V Are Available
- Manual Reset ($\overline{MR}$) Input
- Open-Drain $\overline{RESET}$ Output
- Temperature Range: –55°C to 125°C
- Small SOT-23 Package

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

## 2 Applications

- DSP or Microcontroller Applications
- Notebook/Desktop Computers
- PDAs and Hand-Held Products
- Portable and Battery Powered Products
- FPGA and ASIC Applications

## 3 Description

The TPS3808xxx family of microprocessor supervisory circuits monitors system voltages from 0.4 V to 5.0 V, asserting an open-drain $\overline{RESET}$ signal when the SENSE voltage drops below a preset threshold or when the manual reset ($\overline{MR}$) pin drops to a logic low. The $\overline{RESET}$ output remains low for the user-adjustable delay time after the SENSE voltage and manual reset ($\overline{MR}$) return above the respective thresholds.

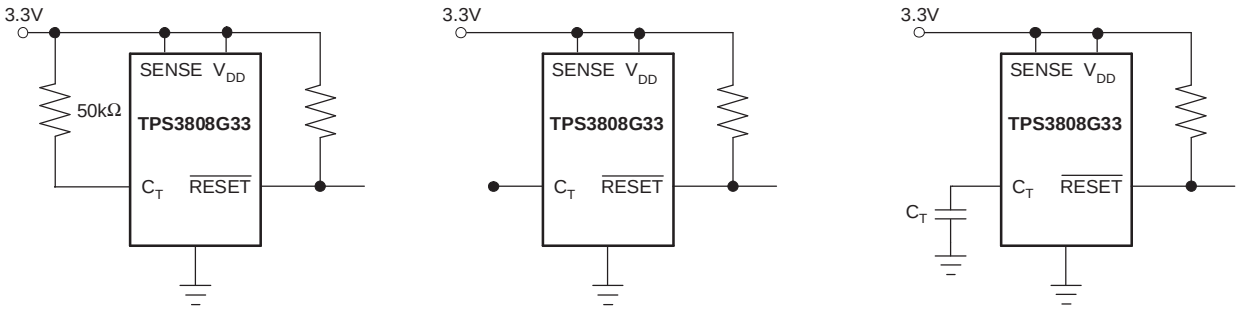
The TPS3808 uses a precision reference to achieve 0.5% threshold accuracy for $V_{IT} \leq 3.3$ V. The reset delay time can be set to 20 ms by disconnecting the $C_T$ pin, 300 ms by connecting the $C_T$ pin to $V_{DD}$ using a resistor, or can be user-adjusted between 1.25 ms and 10 s by connecting the $C_T$ pin to an external capacitor. The TPS3808 has a very low typical quiescent current of 2.4 µA, so it is well-suited to battery-powered applications. It is available in a small SOT-23 package, and is fully specified over a temperature range of –55°C to +125°C ($T_J$).

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS3808-EP | SOT (6) | 2.90 mm x 1.60 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Typical Application Circuit**



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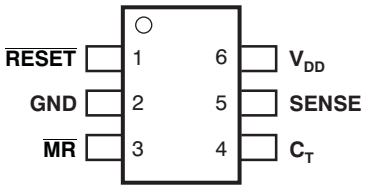
## 4 Revision History

**Changes from Revision C (September 2008) to Revision D** **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 4

# 5 Pin Configuration and Functions

**DBV PACKAGE**
**SOT-23**
**(TOP VIEW)**




**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| $\overline{\text{RESET}}$ | 1 | O | $\overline{\text{RESET}}$ is an open-drain output that is driven to a low impedance state when $\overline{\text{RESET}}$ is asserted (either the SENSE input is lower than the threshold voltage ($V_{IT}$) or the $\overline{\text{MR}}$ pin is set to a logic low). $\overline{\text{RESET}}$ remains low (asserted) for the reset period after both SENSE is above $V_{IT}$ and $\overline{\text{MR}}$ is set to a logic high. A pullup resistor from 10 kΩ to 1 MΩ should be used on this pin, and allows the reset pin to attain voltages higher than $V_{DD}$. |
| GND | 2 | — | Ground |
| $\overline{\text{MR}}$ | 3 | I | Driving the manual reset pin ($\overline{\text{MR}}$) low asserts $\overline{\text{RESET}}$. $\overline{\text{MR}}$ is internally tied to $V_{DD}$ by a 90kΩ pullup resistor. |
| $C_T$ | 4 | I | Reset period programming pin. Connecting this pin to $V_{DD}$ through a 40-kΩ to 200-kΩ resistor or leaving it open results in fixed delay times (see *Switching Characteristics*). Connecting this pin to a ground referenced capacitor ≥ 100 pF gives a user-programmable delay time. See the *Selecting the Reset Delay Time* section for more information. |
| SENSE | 5 | I | This pin is connected to the voltage to be monitored. If the voltage at this terminal drops below the threshold voltage $V_{IT}$, then $\overline{\text{RESET}}$ is asserted. |
| $V_{DD}$ | 6 | I | Supply voltage. It is good analog design practice to place a 0.1-µF ceramic capacitor close to this pin. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

Over operating junction temperature range, unless otherwise noted.(1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Input voltage, $V_{DD}$ | –0.3 | 7.0 | V |
| $C_T$ voltage, $V_{CT}$ | –0.3 | $V_{DD}$ + 0.3 | |
| Other voltage: $V_{RESET}$, $V_{MR}$, $V_{SENSE}$ | –0.3 | 7 | |
| $\overline{RESET}$ pin current | | 5 | mA |
| Operating junction temperature, $T_J$ (2) | –55 | 150 | °C |
| Storage temperature, $T_{stg}$ | –65 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

## 6.2 ESD Ratings

| | | VALUE | UNIT |
|---|---|---|---|
| $V_{(ESD)}$ Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±3000 | V |
| | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Input supply range | 1.7 | | 6.5 | V |
| Power-up reset voltage | $V_{OL}$ (max) = 0.2 V, I $\overline{RESET}$ = 15 µA | | | 0.8 | V |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | TPS3808-EP DBV 6 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 180.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 117.8 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 27.8 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1.12 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 27.3 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

1.7 V ≤ $V_{DD}$ ≤ 6.5 V, $R_{LRESET}$ = 100 kΩ, $C_{LRESET}$ = 50 pF, over operating temperature range ($T_J$ = –55°C to +125°C), unless otherwise noted. Typical values are at $T_J$ = +25°C.

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{DD}$ | Input supply range | | | 1.7 | | 6.5 | V |
| $I_{DD}$ | Supply current (current into $V_{DD}$ pin) | | $V_{DD}$ = 3.3 V, $\overline{RESET}$ not asserted $\overline{MR}$, $\overline{RESET}$, $C_T$ open | | 2.4 | 5.0 | µA |
| | | | $V_{DD}$ = 6.5 V, $\overline{RESET}$ not asserted $\overline{MR}$, $\overline{RESET}$, $C_T$ open | | 2.7 | 6.0 | |
| $V_{OL}$ | Low-level output voltage | | 1.3 V ≤ $V_{DD}$ < 1.8 V, $I_{OL}$ = 0.4 mA | | | 0.3 | V |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 6.5 V, $I_{OL}$ = 1.0 mA | | | 0.4 | |
| | Power-up reset voltage(1) | | $V_{OL}$ (max) = 0.2 V, I $\overline{RESET}$ = 15 µA | | | 0.8 | |
| $V_{IT}$ | Negative-going input threshold accuracy | TPS3808G01 | | –2.0% | ±1.0% | +2.0% | |
| | | $V_{IT}$ ≤ 3.3 V | | –1.7% | ±0.5% | +1.7% | |
| | | 3.3 V < $V_{IT}$ ≤ 5.0 V | | –2.0% | ±1.0% | +2.0% | |
| $V_{HYS}$ | Hysteresis on $V_{IT}$ pin | TPS3808G01 | | | 1.5% | 3.0% | $V_{IT}$ |
| | | Fixed versions | | | 1.0% | 2.5% | |
| R $\overline{MR}$ | $\overline{MR}$ Internal pullup resistance | | | 70 | 90 | | kΩ |
| $I_{SENSE}$ | Input current at SENSE pin | TPS3808G01 | $V_{SENSE}$ = $V_{IT}$ | –25 | | 25 | nA |
| | | Fixed versions | $V_{SENSE}$ = 6.5 V | | 1.7 | | µA |
| $I_{OH}$ | $\overline{RESET}$ leakage current | | V $\overline{RESET}$ = 6.5 V, $\overline{RESET}$ not asserted | | | 300 | nA |
| $C_{IN}$ | Input capacitance, any pin | $C_T$ pin | $V_{IN}$ = 0 V to $V_{DD}$ | | 5 | | pF |
| | | Other pins | $V_{IN}$ = 0 V to 6.5 V | | 5 | | |
| $V_{IL}$ | $\overline{MR}$ logic low input | | | 0 | | 0.3 $V_{DD}$ | V |
| $V_{IH}$ | $\overline{MR}$ logic high input | | | 0.7 $V_{DD}$ | | $V_{DD}$ | |
| $\theta_{JA}$ | Thermal resistance, junction-to-ambient | | | | 290 | | °C/W |

(1) The lowest supply voltage ($V_{DD}$) at which $\overline{RESET}$ becomes active. $T_{rise(VDD)}$ ≥ 15 µs/V.

## 6.6 Switching Characteristics

1.7 V ≤ $V_{DD}$ ≤ 6.5 V, $R_{LRESET}$ = 100 kΩ, $C_{LRESET}$ = 50 pF, over operating temperature range ($T_J$ = –55°C to +125°C), unless otherwise noted. Typical values are at $T_J$ = +25°C.

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_w$ | Input pulse width to $\overline{RESET}$ | SENSE | $V_{IH}$ = 1.05 $V_{IT}$, $V_{IL}$ = 0.95 $V_{IT}$ | | 20 | | µs |
| | | $\overline{MR}$ | $V_{IH}$ = 0.7 $V_{DD}$, $V_{IL}$ = 0.3 $V_{DD}$ | | 0.001 | | |
| $t_d$ | $\overline{RESET}$ delay time | $C_T$ = Open | See *Timing Diagram* | 12 | 20 | 29 | ms |
| | | $C_T$ = $V_{DD}$ | | 180 | 300 | 440 | |
| | | $C_T$ = 100 pF | | 0.75 | 1.25 | 1.8 | |
| | | $C_T$ = 180 nF | | 0.7 | 1.2 | 1.8 | s |
| $t_{pHL}$ | Propagation delay | $\overline{MR}$ to $\overline{RESET}$ | $V_{IH}$ = 0.7 $V_{DD}$, $V_{IL}$ = 0.3 $V_{DD}$ | | 150 | | ns |
| | High-to-low level $\overline{RESET}$ delay | SENSE to $\overline{RESET}$ | $V_{IH}$ = 1.05 $V_{IT}$, $V_{IL}$ = 0.95 $V_{IT}$ | | 20 | | µs |

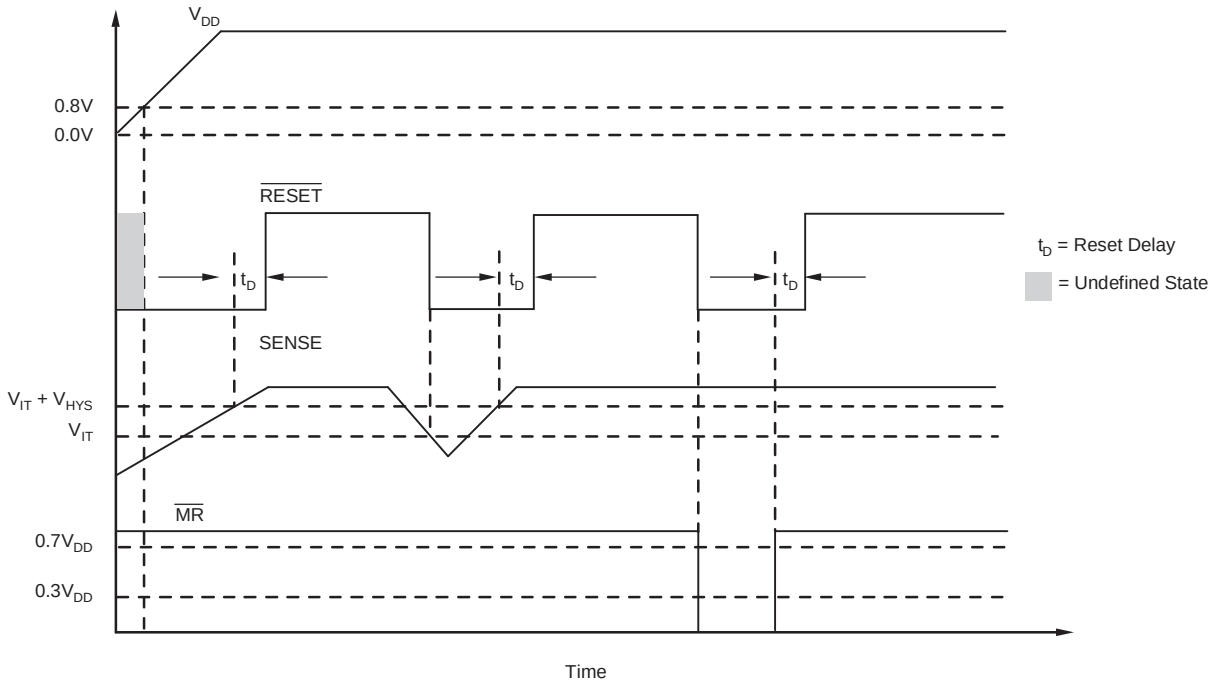



**Figure 1. TPS3808 Timing Diagram Showing $\overline{MR}$ and SENSE Reset Timing**

**Table 1. Truth Table**

| $\overline{MR}$ | SENSE > $V_{IT}$ | $\overline{RESET}$ |
|---|---|---|
| L | 0 | L |
| L | 1 | L |
| H | 0 | L |
| H | 1 | H |

## 6.7 Typical Characteristics

At $T_J$ = +25°C, $V_{DD}$ = 3.3 V, $R_{LRESET}$ = 100kΩ, and $C_{LRESET}$ = 50pF, unless otherwise noted.

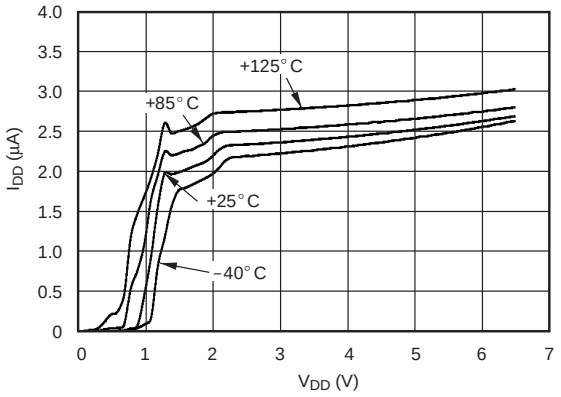



**Figure 2. Supply Current vs Supply Voltage**

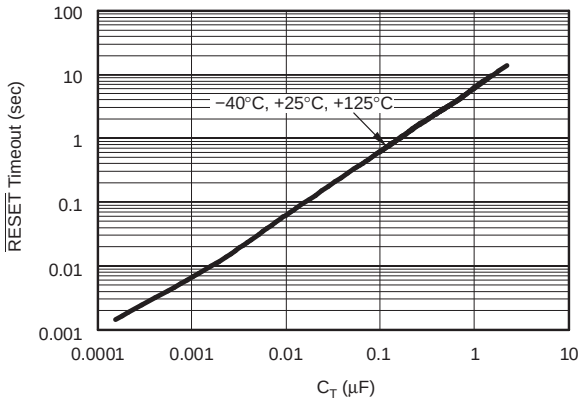
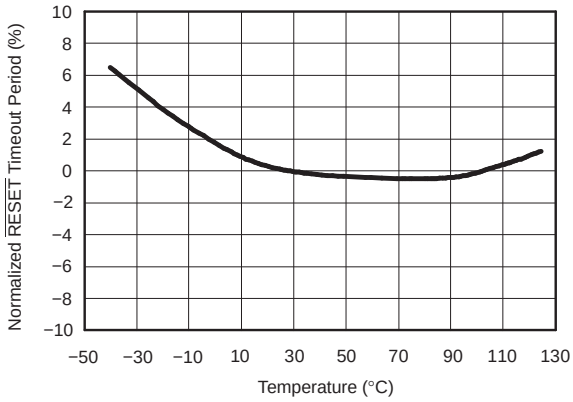



**Figure 3. $\overline{\text{RESET}}$ Timeout Period vs $C_T$**




$C_T$ = Open, $C_T$ = $V_{DD}$, $C_T$ = Any

**Figure 4. Normalized $\overline{\text{RESET}}$ Timeout Period vs Temperature**

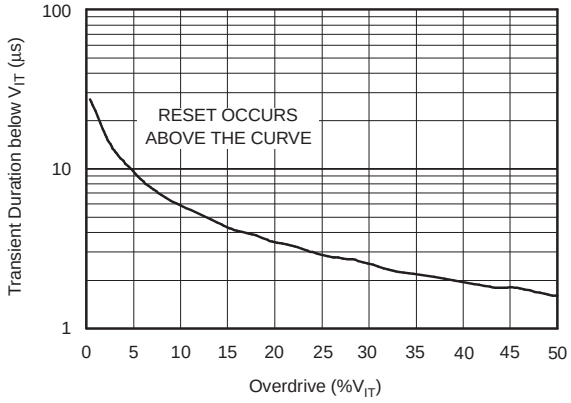



**Figure 5. Maximum Transient Duration at Sense vs Sense Threshold Overdrive Voltage**

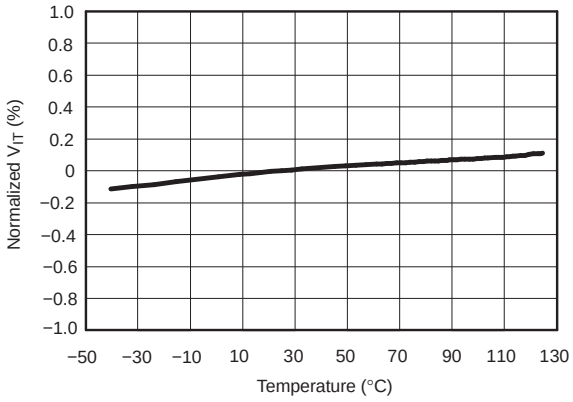



**Figure 6. Normalized Sense Threshold Voltage ($V_{IT}$) vs Temperature**

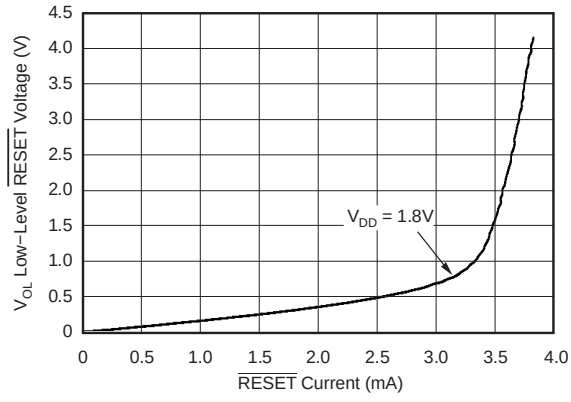



**Figure 7. Low-Level $\overline{\text{RESET}}$ Voltage vs $\overline{\text{RESET}}$ Current**

## Typical Characteristics (continued)

At $T_J$ = +25°C, $V_{DD}$ = 3.3 V, $R_{LRESET}$ = 100kΩ, and $C_{LRESET}$ = 50pF, unless otherwise noted.

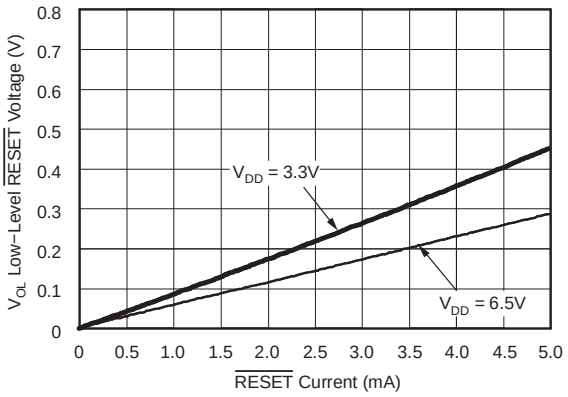


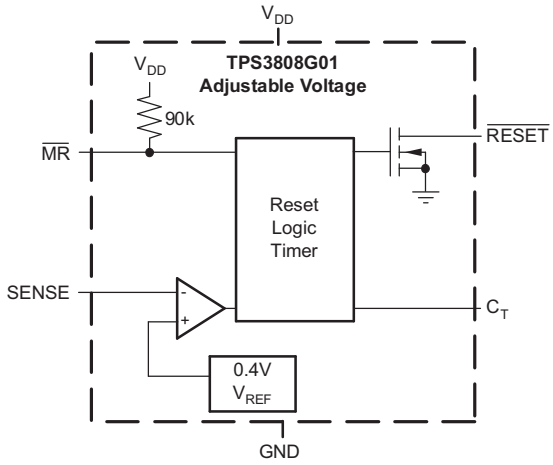

**Figure 8. Low-Level $\overline{\text{RESET}}$ Voltage vs $\overline{\text{RESET}}$ Current**

# 7 Detailed Description

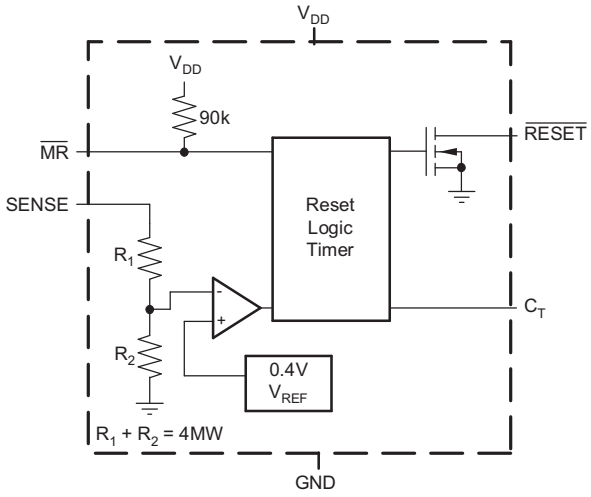
## 7.1 Overview

The TPS3808 microprocessor supervisory product family is designed to assert a $\overline{\text{RESET}}$ signal when either the SENSE pin voltage drops below $V_{IT}$ or the manual reset ($\overline{\text{MR}}$) is driven low. The $\overline{\text{RESET}}$ output remains asserted for a user-adjustable time after both the manual reset ($\overline{\text{MR}}$) and SENSE voltages return above the respective thresholds.

## 7.2 Functional Block Diagrams




Adjustable Voltage Version




Fixed Voltage Version

## 7.3 Feature Description

A broad range of voltage threshold and reset delay time adjustments are available for the TPS3808 device, allowing these devices to be used in a wide array of applications. Reset threshold voltages can be factory-set from 0.82 V to 3.3 V or from 4.4 V to 5.0 V, while the TPS3808G01 can be set to any voltage above 0.405 V using an external resistor divider. Two preset delay times are also user-selectable: connecting the $C_T$ pin to $V_{DD}$ results in a 300 ms reset delay, while leaving the $C_T$ pin open yields a 20-ms reset delay. In addition, connecting a capacitor between $C_T$ and GND allows the designer to select any reset delay period from 1.25 ms to 10 s.

## 7.4 Device Functional Modes

The TPS3808 has two functional modes:

- $\overline{\text{MR}}$ high: in this mode, $\overline{\text{RESET}}$ is high or low depending on the value of the SENSE pin relative to $V_{IT}$.
- $\overline{\text{MR}}$ low: in this mode, $\overline{\text{RESET}}$ is held low regarldess of the value of the SENSE pin.

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The following sections describe in detail how to properly use this device depending on the requirements of the final application.

### 8.1.1 SENSE Input

The SENSE input provides a terminal at which any system voltage can be monitored. If the voltage on this pin drops below $V_{IT}$, then $\overline{\text{RESET}}$ is asserted. The comparator has a built-in hysteresis to ensure smooth $\overline{\text{RESET}}$ assertions and de-assertions. It is good analog design practice to put a 1-nF to 10-nF bypass capacitor on the SENSE input to reduce sensitivity to transients and layout parasitics.

The TPS3808 device is relatively immune to short negative transients on the SENSE pin. Sensitivity to transients is dependent on threshold overdrive, as shown in the *Maximum Transient Duration at Sense vs Sense Threshold Overdrive Voltage* graph (Figure 5) in *Typical Characteristics*.

The TPS3808G01 can be used to monitor any voltage rail down to 0.405 V using the circuit shown in Figure 9.

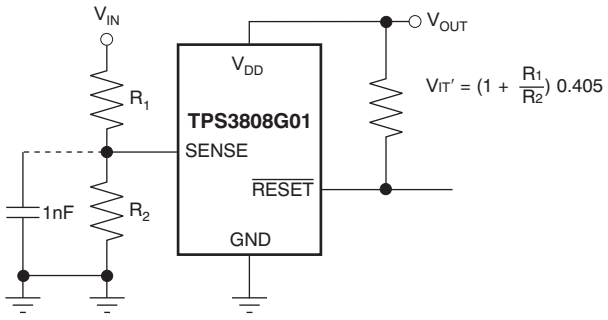



**Figure 9. Using the TPS3808G01 to Monitor a User-Defined Threshold Voltage**

### 8.1.2 Selecting the RESET Delay Time

The TPS3808 has three options for setting the $\overline{\text{RESET}}$ delay time as shown in Figure 10. Figure 10a shows the configuration for a fixed 300-ms typical delay time by tying $C_T$ to $V_{DD}$; a resistor from 40 kΩ to 200 kΩ must be used. Supply current is not affected by the choice of resistor. Figure 10b shows a fixed 20-ms delay time by leaving the $C_T$ pin open. Figure 10c shows a ground referenced capacitor connected to $C_T$ for a user-defined program time between 1.25 ms and 10 s.

## Application Information (continued)

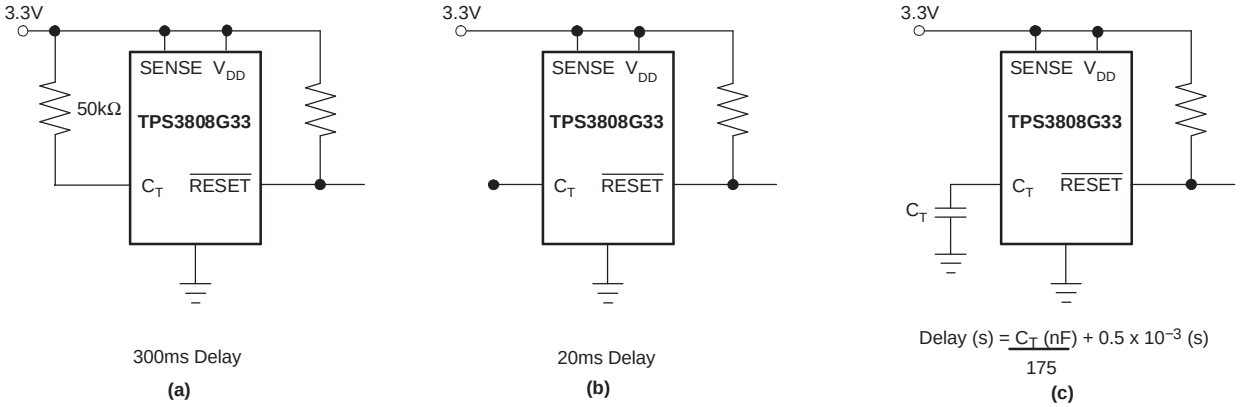



**Figure 10. Configuration Used to Set the $\overline{\text{RESET}}$ Delay Time**

The capacitor $C_T$ should be ≥ 100 pF nominal value in order for the TPS3808xxx to recognize that the capacitor is present. The capacitor value for a given delay time can be calculated using Equation 1.

$$C_T\,(\text{nF}) = \left[t_D\,(\text{s}) - 0.5 \times 10^{-3}\,(\text{s})\right] \times 175 \quad (1)$$

The reset delay time is determined by the time it takes an on-chip precision 220-nA current source to charge the external capacitor to 1.23 V. When a $\overline{\text{RESET}}$ is asserted the capacitor is discharged. When the $\overline{\text{RESET}}$ conditions are cleared, the internal current source is enabled and begins to charge the external capacitor. When the voltage on this capacitor reaches 1.23 V, $\overline{\text{RESET}}$ is deasserted. Note that a low-leakage type capacitor such as a ceramic should be used, and that stray capacitance around this pin may cause errors in the reset delay time.

### 8.1.3 Manual RESET($\overline{\text{MR}}$) Input

The manual reset ($\overline{\text{MR}}$) input allows a processor or other logic circuits to initiate a reset. A logic low (0.3 $V_{DD}$) on $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to assert. After $\overline{\text{MR}}$ returns to a logic high and SENSE is above its reset threshold, $\overline{\text{RESET}}$ is de-asserted after the user defined reset delay expires. Note that $\overline{\text{MR}}$ is internally tied to $V_{DD}$ using a 90-kΩ resistor so this pin can be left unconnected if $\overline{\text{MR}}$ will not be used.

See Figure 11 for how $\overline{\text{MR}}$ can be used to monitor multiple system voltages. Note that if the logic signal driving $\overline{\text{MR}}$ does not go fully to $V_{DD}$, there will be some additional current draw into $V_{DD}$ as a result of the internal pullup resistor on $\overline{\text{MR}}$. To minimize current draw, a logic-level FET can be used as illustrated in Figure 12.

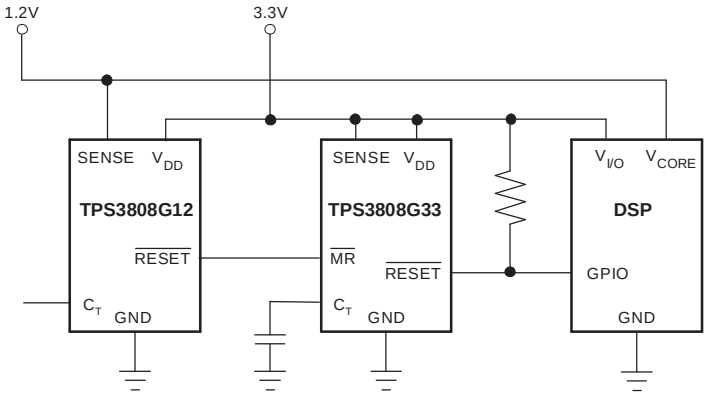



**Figure 11. Using $\overline{\text{MR}}$ to Monitor Multiple System Voltages**

## Application Information (continued)

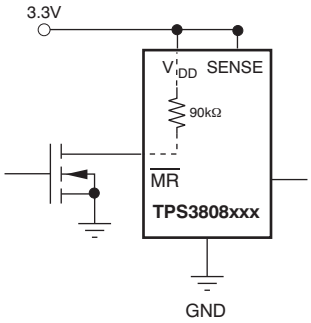



**Figure 12. Using an External MOSFET to Minimize $I_{DD}$ When $\overline{MR}$ Signal Does Not Go to $V_{DD}$**

### 8.1.4 RESET Output

$\overline{RESET}$ remains high (unasserted) as long as SENSE is above its threshold ($V_{IT}$) and the manual reset ($\overline{MR}$) is logic high. If either SENSE falls below $V_{IT}$ or $\overline{MR}$ is driven low, $\overline{RESET}$ is asserted, driving the $\overline{RESET}$ pin to a low impedance.

Once $\overline{MR}$ is again logic high and SENSE is above $V_{IT} + V_{HYS}$ (the threshold hysteresis), a delay circuit is enabled which holds $\overline{RESET}$ low for a specified reset delay period. Once the reset delay has expired, the $\overline{RESET}$ pin goes to a high impedance state. The pullup resistor from the open-drain $\overline{RESET}$ to the supply line can be used to allow the reset signal for the microprocessor to have a voltage higher than $V_{DD}$ (up to 6.5 V). The pullup resistor should be no smaller than 10 kΩ as a result of the finite impedance of the $\overline{RESET}$ line.

## 8.2 Typical Application

A typical application of the TPS3808G33 used with a 3.3 V processor is shown in Figure 13. The open-drain RESET output is typically connected to the RESET input of a microprocessor. A pullup resistor must be used to hold this line high when RESET is not asserted. The RESET output is undefined for voltage below 0.8 V, but this is normally not a problem since most microprocessors do not function below this voltage.

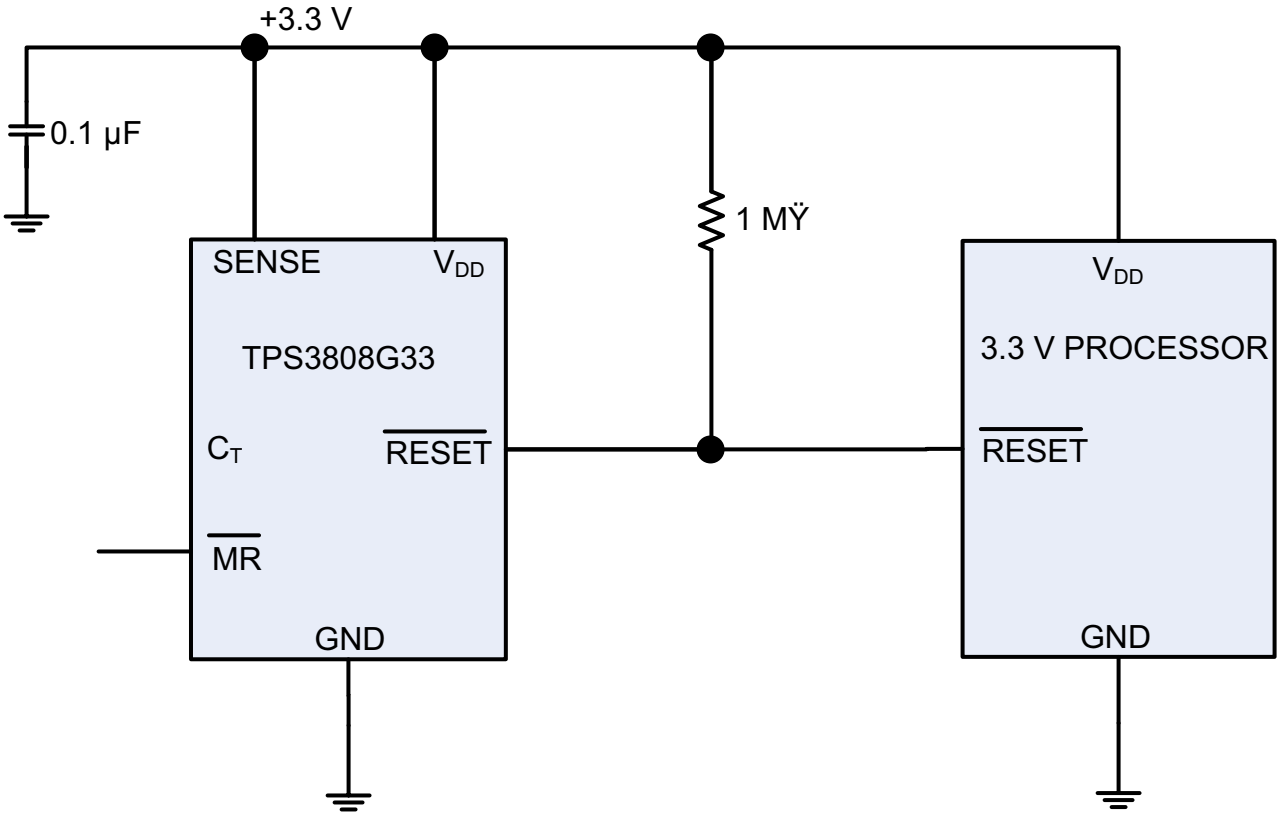



**Figure 13. Typical Application of the TPS3808 with a 3.3 V Processor**

### 8.2.1 Design Requirements

The TPS3808 is intended to drive the RESET input of a microprocessor. The RESET pin is pulled high with a 1 MΩ resistor and the reset delay time is controlled by $C_T$ depending on the reset requirement times of the microprocessor. In this case, $C_T$ is left open for a typical reset delay time of 20 ms.

### 8.2.2 Detailed Design Procedure

The main constraint for this application is the reset delay time. In this case, since $C_T$ is open, it is set to 20 ms. A 0.1 µF decoupling capacitor is connected to the $V_{DD}$pin and a 1 MΩ resistor is used to pull-up the RESET pin high. The MR pin can be connected to an external signal if desired.

## Typical Application (continued)

### 8.2.3 Application Curve

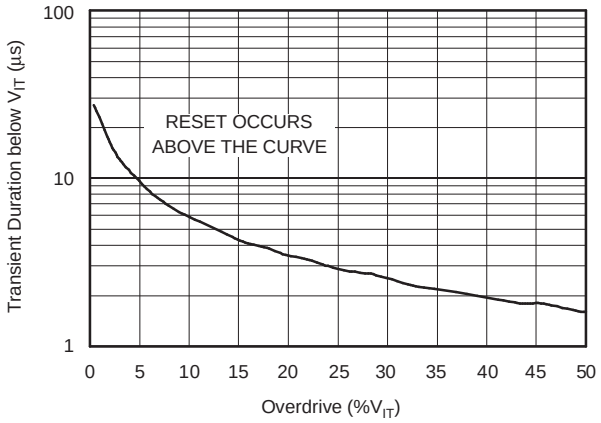



**Figure 14. Maximum Transient Duration at Sense vs Sense Threshold Overdrive Voltage**

# 9 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range between 1.7 and 6.5 V. Use a low-impedance power supply to eliminate inaccuracies caused by the current during the voltage reference refresh.

# 10 Layout

## 10.1 Layout Guidelines

Make sure the connection to the $V_{DD}$ pin is low impedance. Place a 0.1-µF ceramic capacitor near the $V_{DD}$ pin.

## 10.2 Layout Example

The layout example in Figure 15 shows how the TPS3808 is laid out on a PCB for a 20 ms delay.

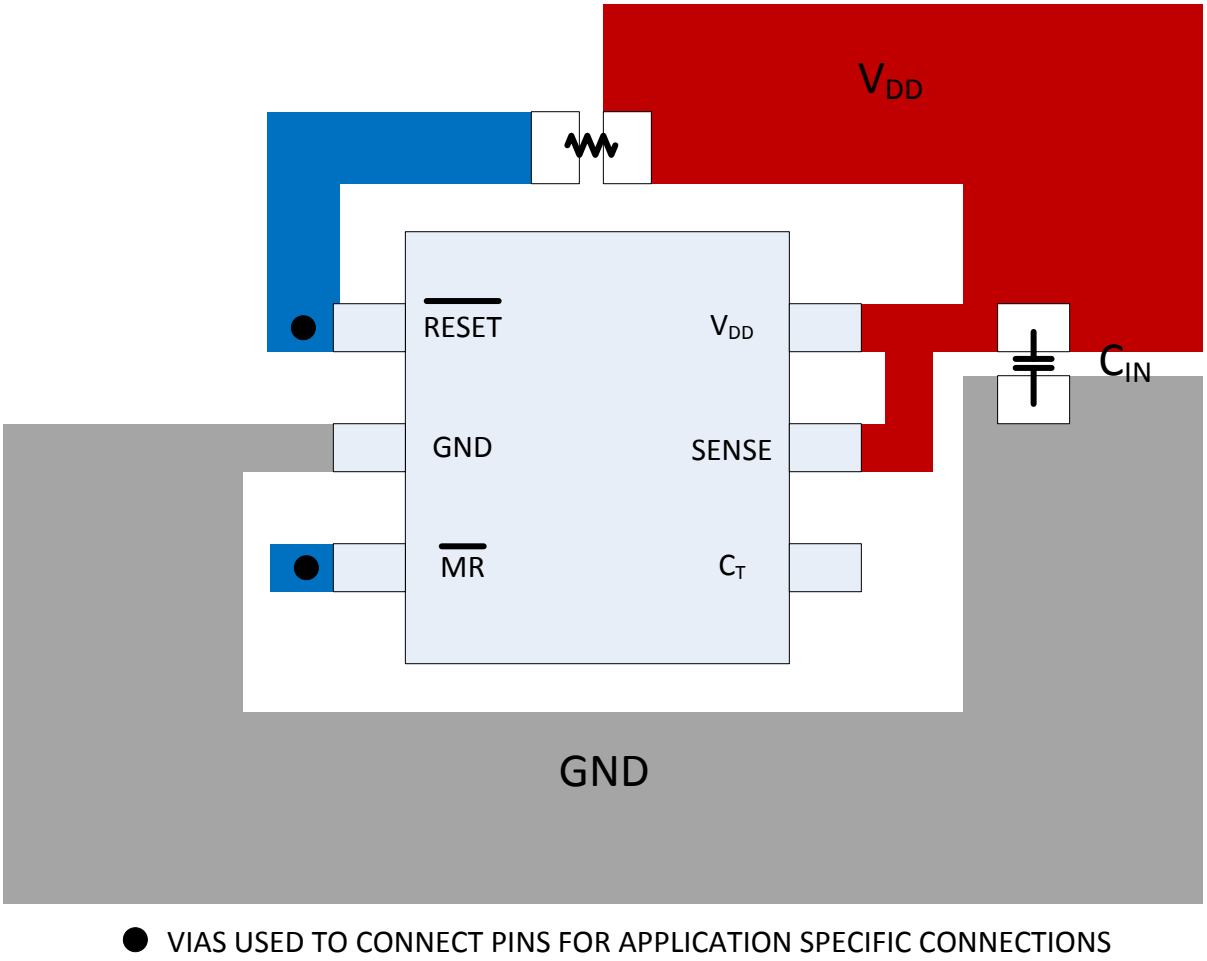



**Figure 15. Layout Example for a 20 ms Delay**

# 11 Device and Documentation Support

## 11.1 Trademarks

All trademarks are the property of their respective owners.

## 11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS3808G01MDBVTEP | ACTIVE | SOT-23 | DBV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | NXS | Samples |
| TPS3808G33MDBVREP | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CHK | Samples |
| V62/08607-01XE | ACTIVE | SOT-23 | DBV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | NXS | Samples |
| V62/08607-09XE | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CHK | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

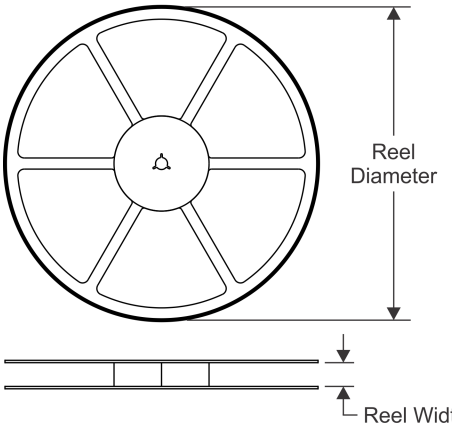
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

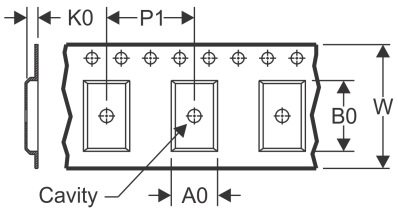
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

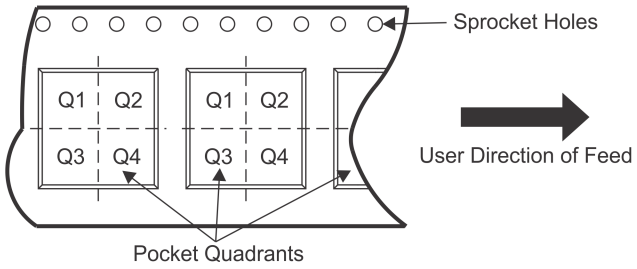



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

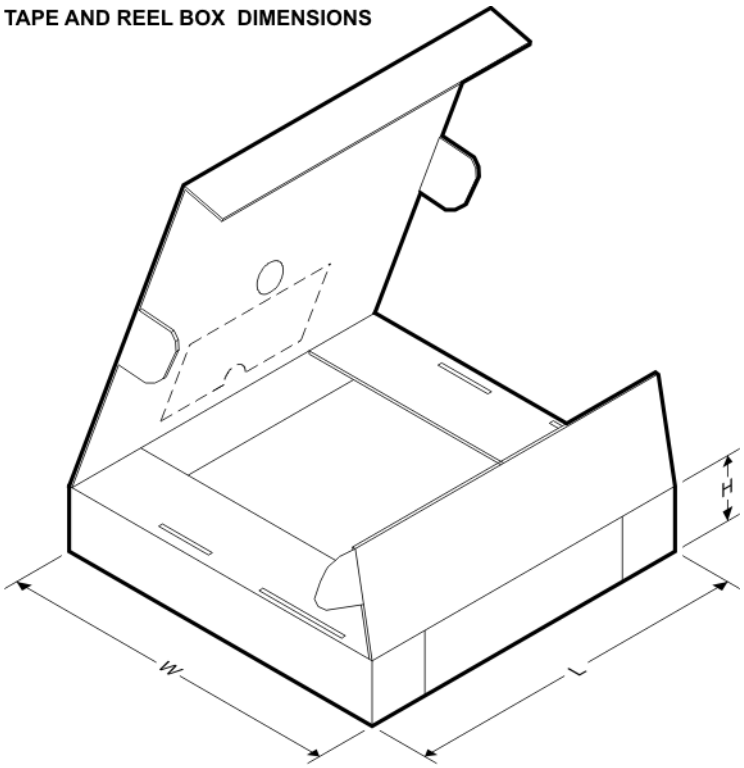
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS3808G01MDBVTEP | SOT-23 | DBV | 6 | 250 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS3808G33MDBVREP | SOT-23 | DBV | 6 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

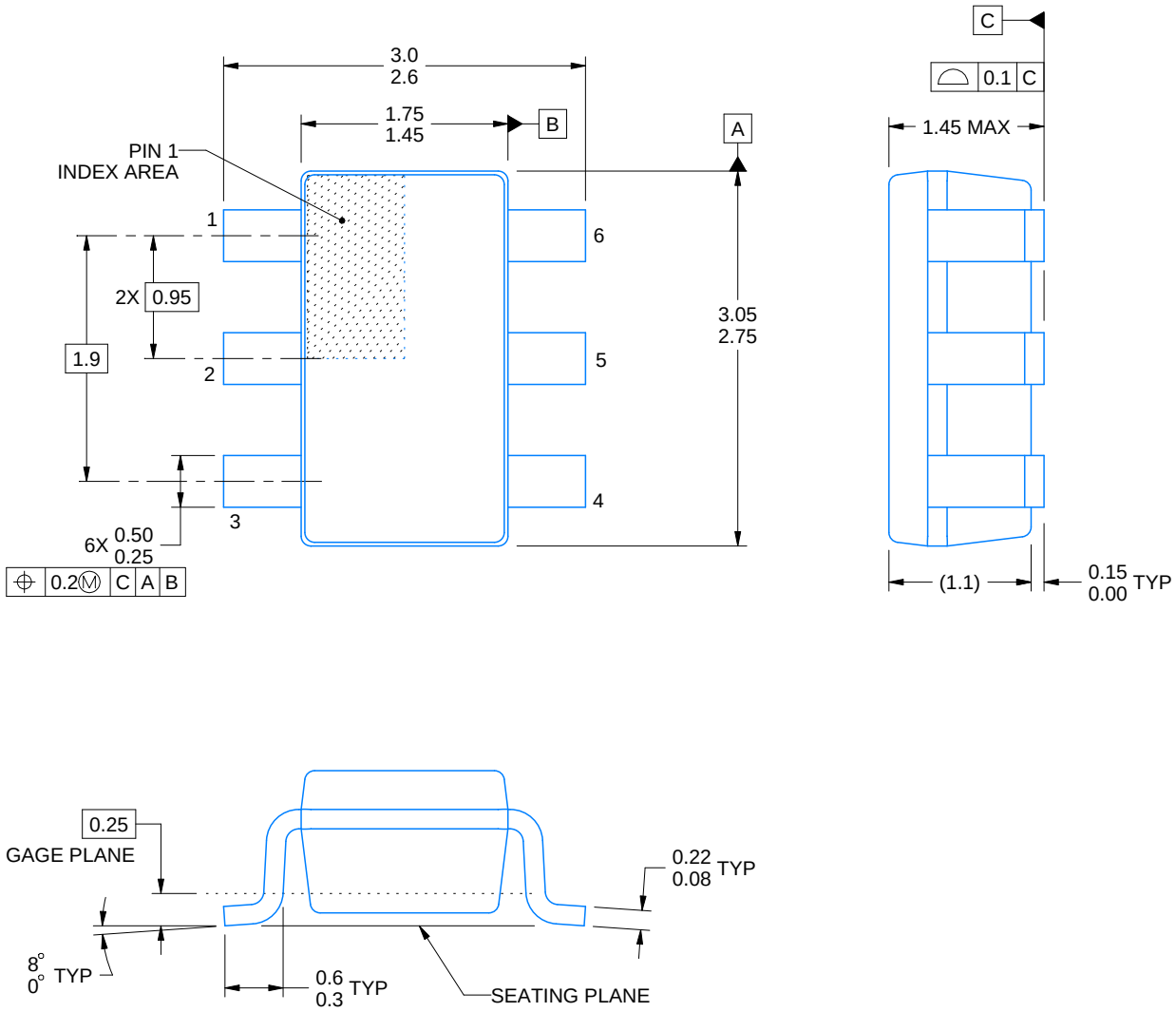
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS3808G01MDBVTEP | SOT-23 | DBV | 6 | 250 | 203.0 | 203.0 | 35.0 |
| TPS3808G33MDBVREP | SOT-23 | DBV | 6 | 3000 | 203.0 | 203.0 | 35.0 |

# PACKAGE OUTLINE

## DBV0006A

## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

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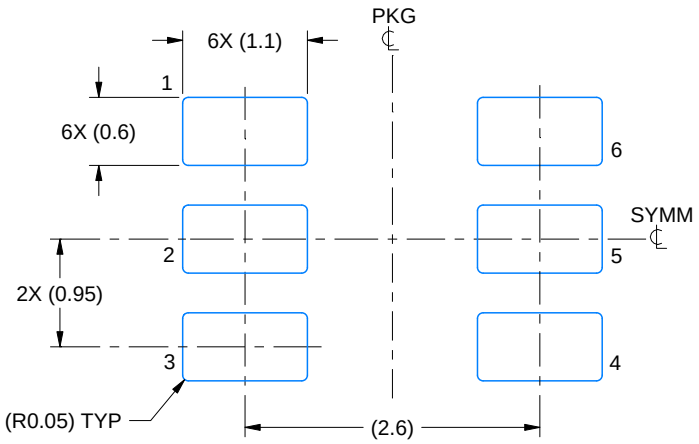
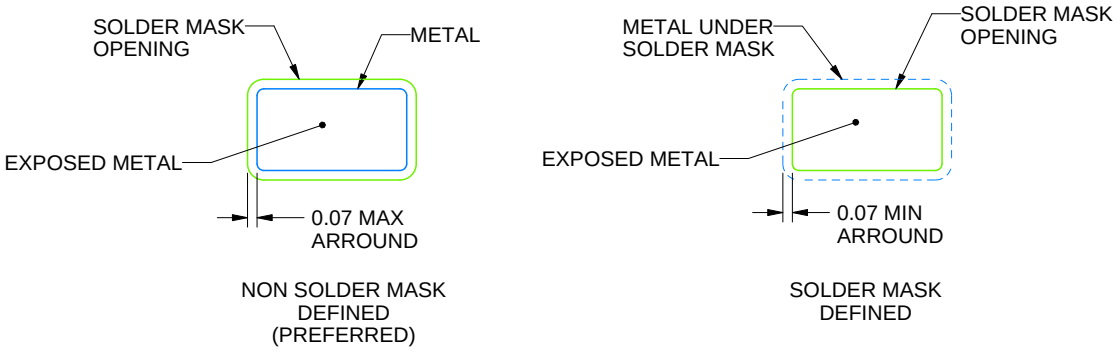
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X




SOLDER MASK DETAILS

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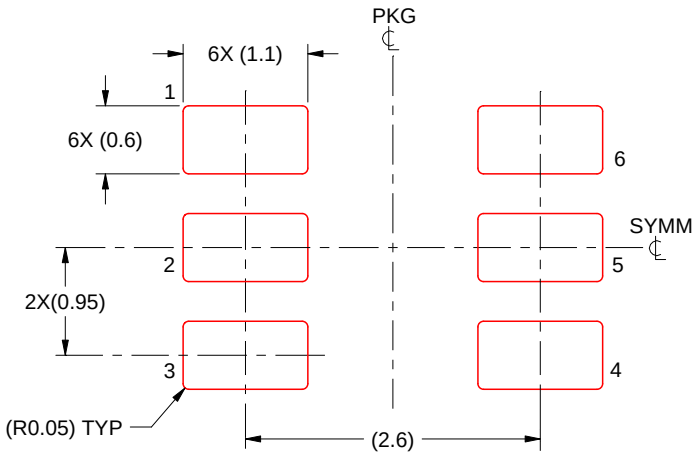
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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