THE DATASHEET OF

TPS2220BDBR

POWER-INTERFACE SWITCHES FOR SERIAL PCMCIA CONTROLLERS

FEATURES

- **Single-Slot Switch: TPS2220B**
- **Fast Current Limit Response Time**
- **Fully Integrated VCC and VPP Switching for 3.3 V, 5 V, and 12 V**
- **Meets Current PC Card™ Standards**
- **V_{pp} Output Selection Independent of V_{CC}**
- **12-V and 5-V Supplies Can Be Disabled**
- **TTL-Logic Compatible Inputs**
- **Short-Circuit and Thermal Protection**
- **24-Pin HTSSOP and 24-Pin SSOP**
- **140-µA (Typical) Quiescent Current from 3.3-V Input**
- **Break-Before-Make Switching**
- **Power-On Reset**
- **-40°C to 85°C Operating Ambient Temperature Range**

APPLICATIONS

- **Notebook and Desktop Computers**
- **Bar Code Scanners**
- **Digital Cameras**
- **Set-Top Boxes**
- **PDAs**

DESCRIPTION

The TPS2220B power-interface switch provides an integrated power-management solution for single Card sockets. The device allows the controlled distribution of 3.3 V, 5 V, and 12 V to one card slot. The current-limiting and thermal-protection features eliminate the need for fuses. Current-limit reporting helps the user isolate a system fault. The switch $r_{DS(on)}$ and current-limit values have been set for the peak and average current requirements stated in the PC Card specification, and optimized for cost.

Like the TPS2220A this device supports independent VPP/VCC switching. The TPS2220B is pin compatible with the TPA2220A execept for pin 20 of the TPS2220B which has no connection.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE	
	PLASTIC SMALL OUTLINE (DB-24)(1)	PowerPAD™ PLASTIC SMALL OUTLINE (PWP-24)(1)
-40°C to 85°C	TPS2220BDB	TPS2220BPWP

(1) The DB and PWP packages are also available taped and reeled. Add R suffix to device type (e.g., TPS2220BPWPR) for taped and reeled.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	SSOP(DB)(1)	STATUS	HTSSOP (PWP)(1)	STATUS
–40°C to 85°C	TPS2220BDB	Active	TPS2220BPWP	Active

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			TPA2220B
V_I	Input voltage range for card power	$V_{I(3.3V)}$	–0.3 V to 5.5 V
		$V_{I(5V)}$	–0.3 V to 5.5 V
		$V_{I(12V)}$	–0.3 V to 14 V
	Logic input/output voltage		–0.3 V to 6 V
V_O	Output voltage	$V_{O(AVCC)}$	–0.3 V to 6 V
		$V_{O(AVPP)}$	–0.3 V to 14 V
	Continuous total power dissipation		See Dissipation Rating Table
I_O	Output current	$I_{O(AVCC)}$	Internally Limited
		$I_{O(AVPP)}$	Internally Limited
T_J	Operating virtual junction temperature range		–40°C to 100°C
T_{stg}	Storage temperature range		–55°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds)		260°C
	$\overline{OC}$ sink current		10 mA

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE(1)		$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DB	24	890 mW	8.9 mW/°C	489 mW	356 mW
PWP	24	3322 mW	33.22 mW/°C	1827 mW	1329 mW

(1) These devices are mounted on aa JEDEC low-k board (2-oz. traces on surface).

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
	Input voltage, $V_{I(3.3V)}$ is required for all circuit operations. 5V and 12V are only required for their respective functions.	$V_{I(3.3V)}$ (1)	3	3.6	V
		$V_{I(5V)}$	3	5.5	
		$V_{I(12V)}$	7	13.5	
I_O	Output current	$I_{O(AVCC)}$ at T_J = 100°C		1	A
		$I_{O(AVPP)}$ at T_J = 100°C		100	mA
$f_{(clock)}$	Clock frequency			2.5	MHz
t_w	Pulse duration	Data	200		ns
		Latch	250		
		Clock	100		
		Reset	100		
t_h	Data-to-clock hold time (see Figure 2)		100		ns
t_{su}	Data-to-clock setup time (see Figure 2)		100		ns
$t_{d(latch)}$	Latch delay time (see Figure 2)		100		ns
$t_{d(clock)}$	Clock delay time (see Figure 2)		250		ns
T_J	Operating virtual junction temperature (maximum to be calculated at worst case P_D at 85°C ambient)		–40	100	°C

(1) It is understood that for $V_{I(3.3V)}$ < 3 V, voltages within the absolute maximum ratings applied to pin 5V or pin 12V do not damage the IC.

ELECTRICAL CHARACTERISTICS

T_J = 25°C, $V_{I(5V)}$ = 5 V, $V_{I(3.3V)}$ = 3.3 V, $V_{I(12V)}$ = 12 V, all outputs unloaded (unless otherwise noted)

PARAMETER				TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
POWER SWITCH									
$r_{DS(on)}$	Static drain-source on-state resistance	3.3V to AVCC		I_O = 750 mA each			85	110	mΩ
				I_O = 750 mA each, T_J = 100°C			110	140	
		5V to AVCC		I_O = 500 mA each			95	130	
				I_O = 500 mA each, T_J = 100°C			120	160	
		3.3V or 5V to AVPP		I_O = 50 mA each			0.8	1	Ω
				I_O = 50 mA each, T_J = 100°C			1	1.3	
		12V to AVPP		I_O = 50 mA each			2	2.5	
				I_O = 50 mA each, T_J = 100°C			2.5	3.4	
	Output discharge resistance	Discharge at AVCC		$I_{O(disc)}$ = 1 mA		0.5	0.7	1	kΩ
		Discharge at AVPP		$I_{O(disc)}$ = 1 mA		0.2	0.4	0.5	
I_{OS}	Short-circuit output current			Limit (steady-state value), output powered into a short circuit	$I_{OS(AVCC)}$	1	1.4	2	A
					$I_{OS(AVPP)}$	120	200	300	mA
				Limit (steady-state value), output powered into a short circuit, T_J = 100°C	$I_{OS(AVCC)}$	1	1.4	2	A
					$I_{OS(AVPP)}$	120	200	300	mA
T_J	Thermal shutdown temperature	Thermal trip point		Rising temperature			135		°C
		Hysteresis					10		
	Current-limit response time(2)(3)			5V to AVCC = 5 V, with 100-mΩ short to GND			10		µs
				5V to AVPP = 5 V, with 100-mΩ short to GND			3		
I_I	Input current, quiescent	Normal operation	$I_{I(3.3V)}$	V_O(AVCC) = V_O(AVPP) = 3.3 V and also for $\overline{RESET}$ = 0 V			140	200	µA
			$I_{I(5V)}$				8	12	
			$I_{I(12V)}$				100	180	
		Shutdown mode	$I_{I(3.3V)}$	V_O(AVCC) = V_O(AVPP) = Hi-Z			0.3	2	
			$I_{I(5V)}$				0.1	2	
			$I_{I(12V)}$				0.3	2	

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
(2) Specified by design; not tested in production.
(3) From application of short to 110% of final current limit.

ELECTRICAL CHARACTERISTICS (continued)

T_J = 25°C, $V_{I(5V)}$ = 5 V, $V_{I(3.3V)}$ = 3.3 V, $V_{I(12V)}$ = 12 V, all outputs unloaded (unless otherwise noted)

PARAMETER			TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
I_{lkg}	Leakage current, output off state	Shutdown mode	$V_{O(AVCC)}$ = 5 V, $V_{I(5V)}$ = $V_{I(12V)}$ = 0 V				10	µA
				T_J = 100°C			50	
			$V_{O(AVPP)}$ = 12 V, $V_{I(5V)}$ = $V_{I(12V)}$ = 0 V				10	
				T_J = 100°C			50	
LOGIC SECTION (CLOCK, DATA, LATCH, $\overline{\text{RESET}}$, $\overline{\text{SHDN}}$, $\overline{\text{OC}}$)								
I_I	Input current, logic	$I_{I(/RESET)}$ (4)	$\overline{\text{RESET}}$ = 5.5 V		–1		1	µA
			$\overline{\text{RESET}}$ = 0 V		–30	–20	–10	
		$I_{I(/SHDN)}$ (4)	$\overline{\text{SHDN}}$ = 5.5 V		–1		1	
			$\overline{\text{SHDN}}$ = 0 V		–50		-3	
		$I_{I(LATCH)}$ (4)	LATCH = 5.5 V				50	
			LATCH = 0 V		–1		1	
		$I_{I(CLOCK, DATA)}$	0 V to 5.5 V		–1		1	
V_{IH}	High-level input voltage, logic				2			V
V_{IL}	Low-level input voltage, logic						0.8	V
$V_{O(sat)}$	Output saturation voltage at $\overline{\text{OC}}$		I_O = 2 mA			0.14	0.4	V
I_{lkg}	Leakage current at $\overline{\text{OC}}$		$V_{O(/OC)}$ = 5.5 V			0	1	µA
UVLO AND POR (POWER-ON RESET)								
$V_{I(3.3V)}$	Input voltage at 3.3V pin, UVLO		3.3-V level below which all switches are Hi-Z		2.4	2.7	2.9	V
$V_{hys(3.3V)}$	UVLO hysteresis voltage at VA(5)					100		mV
$V_{I(5V)}$	Input voltage at 5V pin, UVLO		5-V level below which only 5V switches are Hi-Z		2.3	2.5	2.8	V
$V_{hys(5V)}$	UVLO hysteresis voltage at 5V(5)		Delay from voltage hit (step from 3 V to 2.3 V) to Hi-Z control (90% V_G to GND)			100		mV
t_{df}	Delay time for falling response, UVLO(5)					4		µs
$V_{I(POR)}$	Input voltage, power-on reset(5)		3.3-V voltage below which POR is asserted causing a RESET internally with all line switches open and all discharge switches closed.				1.7	V

(4) LATCH has low-current pulldown. $\overline{\text{RESET}}$ and $\overline{\text{SHDN}}$ have low-current pullup.
(5) Specified by design; not tested in production.

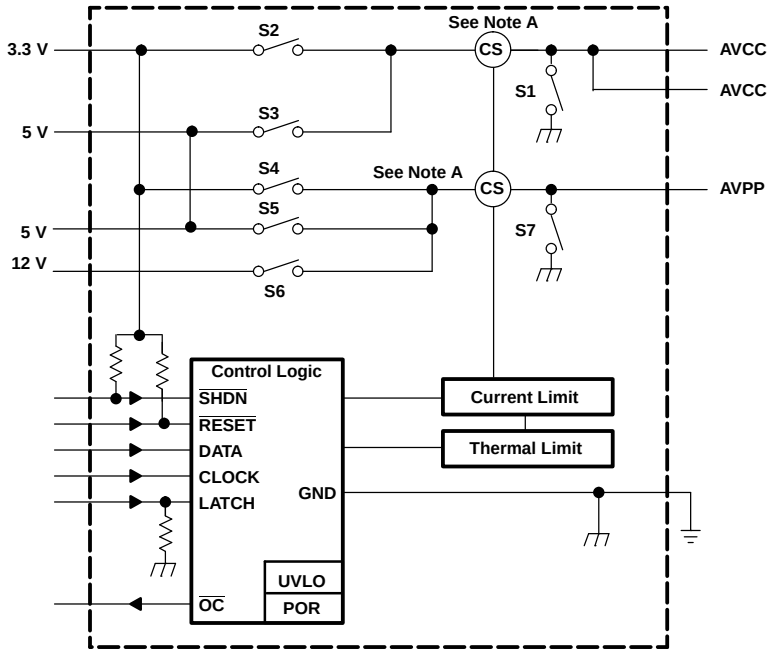
SWITCHING CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C, $V_{I(3.3V)}$ = 3.3 V, $V_{I(5V)}$ = 5 V, $V_{I(12)}$ = 12 V, all outputs unloaded (unless otherwise noted)

PARAMETER(1)		LOAD CONDITION	TEST CONDITIONS(2)		MIN	TYP	MAX	UNIT
t_r	Output rise times(3)	$C_{L(AVCC)}$ = 0.1 µF, $C_{L(AVPP)}$ = 0.1 µF, $I_{O(AVCC)}$ = 0 A, $I_{O(AVPP)}$ = 0 A	$V_{O(AVCC)}$ = 5 V			0.9		ms
			$V_{O(AVPP)}$ = 12 V			0.26		
		$C_{L(AVCC)}$ = 150 µF, $C_{L(AVPP)}$ = 10 µF, $I_{O(AVCC)}$ = 0.75 A, $I_{O(AVPP)}$ = 50 mA	$V_{O(AVCC)}$ = 5 V			1.1		
			$V_{O(AVPP)}$ = 12 V			0.6		
t_f	Output fall times (3)	$C_{L(AVCC)}$ = 0.1 µF, $C_{L(AVPP)}$ = 0.1 µF, $I_{O(AVCC)}$ = 0 A, $I_{O(AVPP)}$ = 0 A	$V_{O(AVCC)}$ = 5 V, Discharge switches ON			0.5		ms
			$V_{O(AVPP)}$ = 12 V, Discharge switches ON			0.2		
		$C_{L(AVCC)}$ = 150 µF, $C_{L(AVPP)}$ = 10 µF, $I_{O(AVCC)}$ = 0.75 A, $I_{O(AVPP)}$ = 50 mA	$V_{O(AVCC)}$ = 5 V			2.35		
			$V_{O(AVPP)}$ = 12 V			3.9		
t_{pd}	Propagation delay times(3)	$C_{L(AVCC)}$ = 0.1 µF, $C_{L(AVPP)}$ = 0.1 µF, $I_{O(AVCC)}$ = 0 A, $I_{O(AVPP)}$ = 0 A	Latch↑ to AVPP (12V)	t_{pdon}		2		ms
				t_{pdoff}		0.62		
			Latch↑ to AVPP (5V)	t_{pdon}		0.77		
				t_{pdoff}		0.51		
			Latch↑ to AVPP (3.3V)	t_{pdon}		0.75		
				t_{pdoff}		0.52		
			Latch↑ to AVCC (5V)	t_{pdon}		0.3		
				t_{pdoff}		2.5		
			Latch↑ to AVCC (3.3V)	t_{pdon}		0.3		
				t_{pdoff}		2.8		
		$C_{L(AVCC)}$ = 150 µF, $C_{L(AVPP)}$ = 10 µF, $I_{O(AVCC)}$ = 0.75 A, $I_{O(AVPP)}$ = 50 mA	Latch↑ to AVPP (12V)	t_{pdon}		2.2		ms
				t_{pdoff}		0.8		
			Latch↑ to AVPP (5V)	t_{pdon}		0.8		
				t_{pdoff}		0.6		
			Latch↑ to AVPP (3.3V)	t_{pdon}		0.8		
				t_{pdoff}		0.6		
			Latch↑ to AVCC (5V)	t_{pdon}		0.6		
				t_{pdoff}		2.5		
			Latch↑ to AVCC (3.3V)	t_{pdon}		0.5		
				t_{pdoff}		2.6		

(1) Refer to Parameter Measurement Information in Figure 1.
(2) No card inserted, assumes a 0.1-µF output capacitor (see Figure 1).
(3) Specified by design; not tested in production.

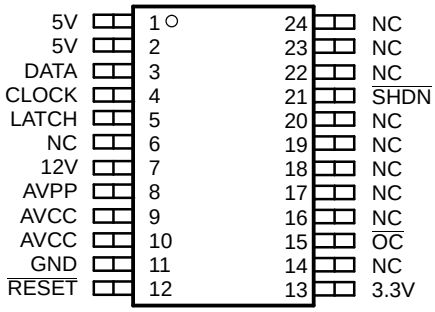
FUNCTIONAL BLOCK DIAGRAM



NOTES: A. Current sense

PIN ASSIGNMENTS

TPS2220B
DB OR PWP PACKAGE
(TOP VIEW)



NC − No internal connection

PIN ASSIGNMENTS (continued)

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
	TPS2220B		
3.3V	13	I	3.3-V input for card power and chip power
5V	1, 2	I	5-V input for card power
12V	7	I	12-V input for card power (AVPP).
AVCC	9, 10	O	Switched output that delivers 3.3 V, 5 V, ground or high impedance to card
AVPP	8	O	Switched output that delivers 3.3 V, 5 V, 12 V, ground or high impedance to card
GND	11		Ground
$\overline{OC}$	15	O	Open-drain overcurrent reporting output that goes low when an overcurrent condition exists. An external pullup is required.
$\overline{SHDN}$	21	I	Hi-Z (open) all switches. Identical function to serial D8. Asynchronous active-low command, internal pullup
$\overline{RESET}$	12	I	Logic-level RESET input active low. Asynchronous active-low command, internal pullup
CLOCK	4	I	Logic-level clock for serial data word
DATA	3	I	Logic-level serial data word
LATCH	5	I	Logic-level latch for serial data word, internal pulldown
NC	6, 14, 16, 17, 18, 19, 20, 22, 23, 24		No internal connection

PARAMETER MEASUREMENT INFORMATION

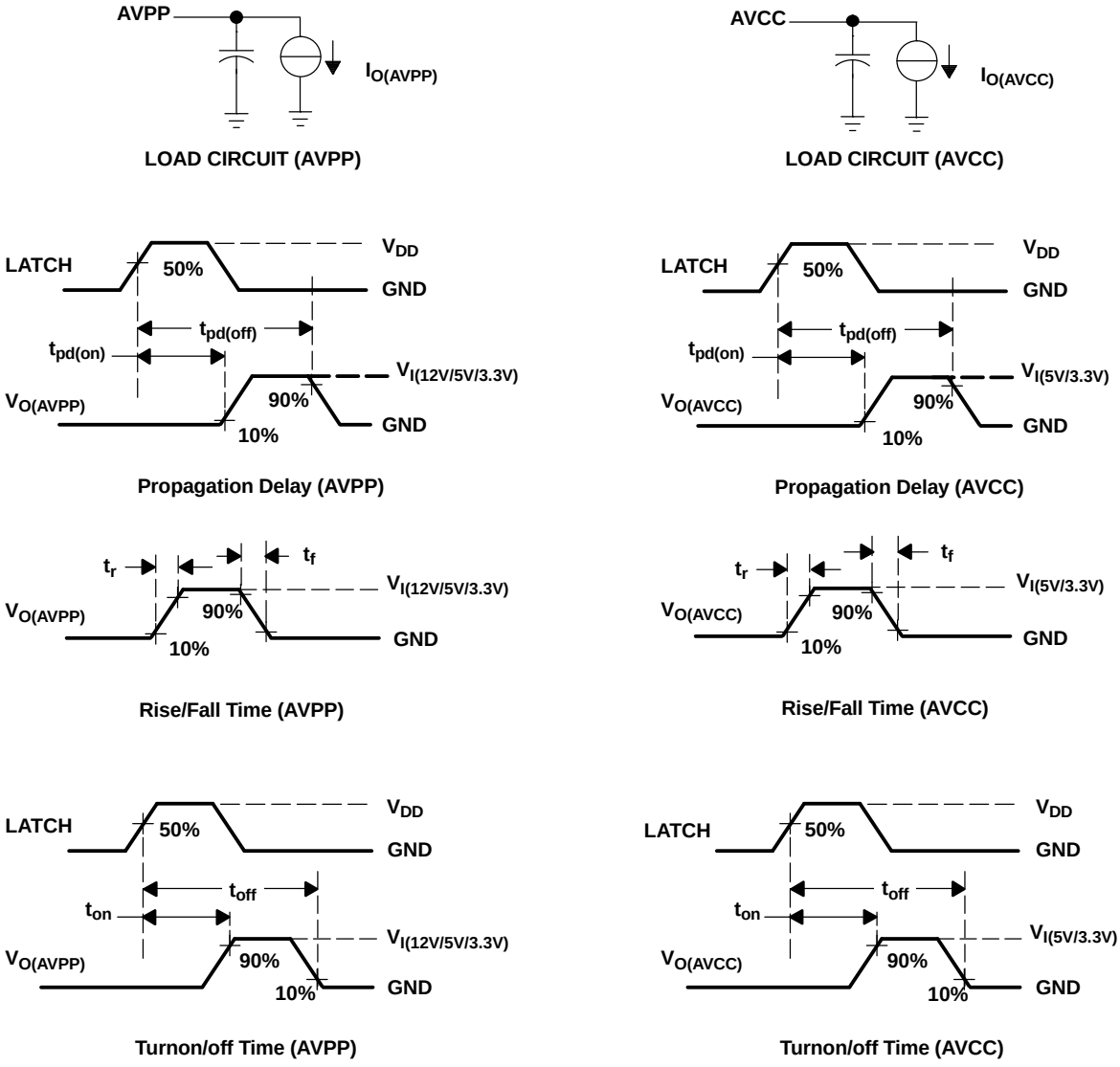
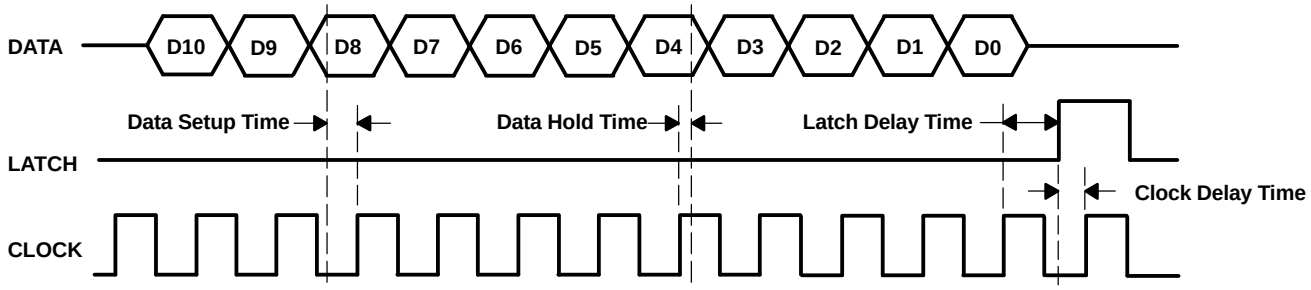


Figure 1. Test Circuits and Voltage Waveforms



NOTE: Data is clocked in on the positive edge of the clock. The positive edge of the latch signal should occur before the next positive edge of the clock. For definition of D0 to D10, see the control logic table.

Figure 2. Serial-Interface Timing for TPS2220B

Table of Graphs

		FIGURE
Short-circuit response, short applied to powered-on 5-V AVCC-switch output	vs Time	3
Short-circuit response, short applied to powered-on 12-V AVPP-switch output	vs Time	4
$\overline{OC}$ response with ramped overcurrent-limit load on 5-V AVCC-switch output	vs Time	5
$\overline{OC}$ response with ramped overcurrent-limit load on 12-V AVPP-switch output	vs Time	6
AVCC Turnon propagation delay time (C_L = 150 µF)	vs Junction temperature	7
AVCC Turnoff propagation delay time (C_L = 150 µF)	vs Junction temperature	8
AVPP Turnon propagation delay time (C_L = 10 µF)	vs Junction temperature	9
AVPP Turnoff propagation delay time (C_L = 10 µF)	vs Junction temperature	10
AVCC Turnon propagation delay time (T_J = 25°C)	vs Load capacitance	11
AVCC Turnoff propagation delay time (T_J = 25°C)	vs Load capacitance	12
AVPP Turnon propagation delay time (T_J = 25°C)	vs Load capacitance	13
AVPP Turnoff propagation delay time (T_J = 25°C)	vs Load capacitance	14
AVCC Rise time (C_L = 150 µF)	vs Junction temperature	15
AVCC Fall time (C_L = 150 µF)	vs Junction temperature	16
AVPP Rise time (C_L = 10 µF)	vs Junction temperature	17
AVPP Fall time (C_L = 10 µF)	vs Junction temperature	18
AVCC Rise time (T_J = 25°C)	vs Load capacitance	19
AVCC Fall time (T_J = 25°C)	vs Load capacitance	20
AVPP Rise time (T_J = 25°C)	vs Load capacitance	21
AVPP Fall time (T_J = 25°C)	vs Load capacitance	22

SHORT-CIRCIUT RESPONSE,
SHORT APPLIED TO POWERED-ON 5-V
AVCC-SWITCH OUTPUT

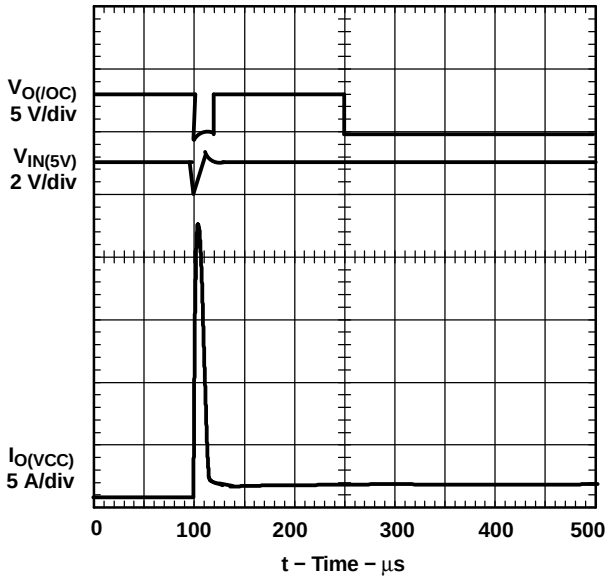


Figure 3.

SHORT-CIRCIUT RESPONSE,
SHORT APPLIED TO POWERED-ON 12-V
AVPP-SWITCH OUTPUT

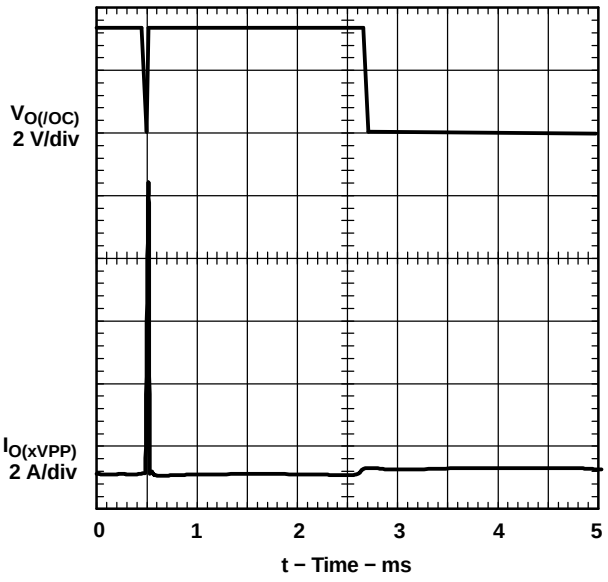


Figure 4.

$\overline{OC}$ RESPONSE WITH RAMPED
OVERCURRENT-LIMIT LOAD ON 5-V
AVCC-SWITCH OUTPUT

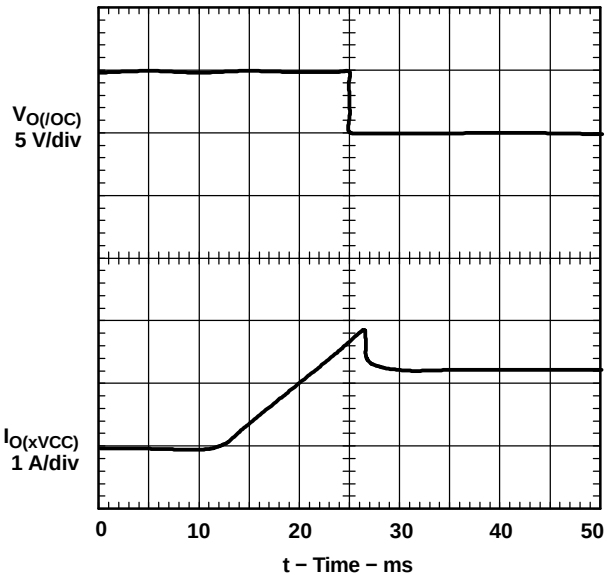


Figure 5.

$\overline{OC}$ RESPONSE WITH RAMPED
OVERCURRENT-LIMIT LOAD ON 12-V
AVPP-SWITCH OUTPUT

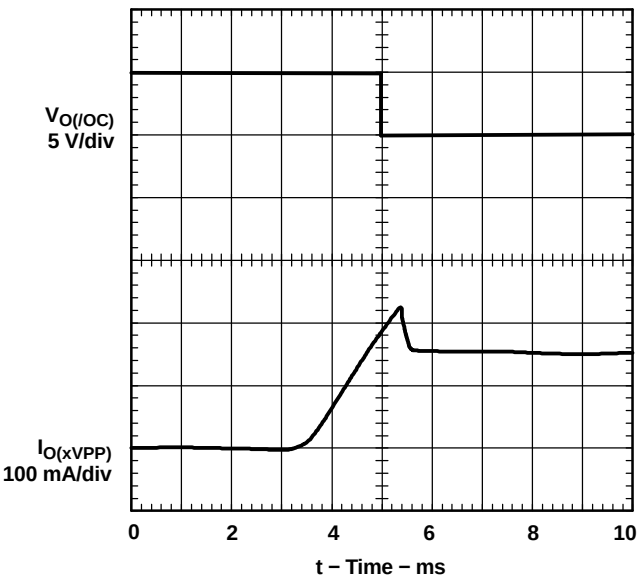


Figure 6.

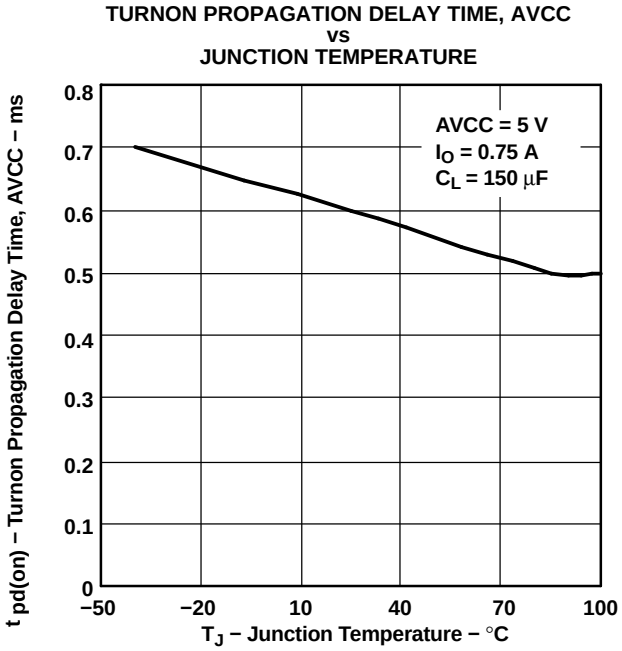


Figure 7.

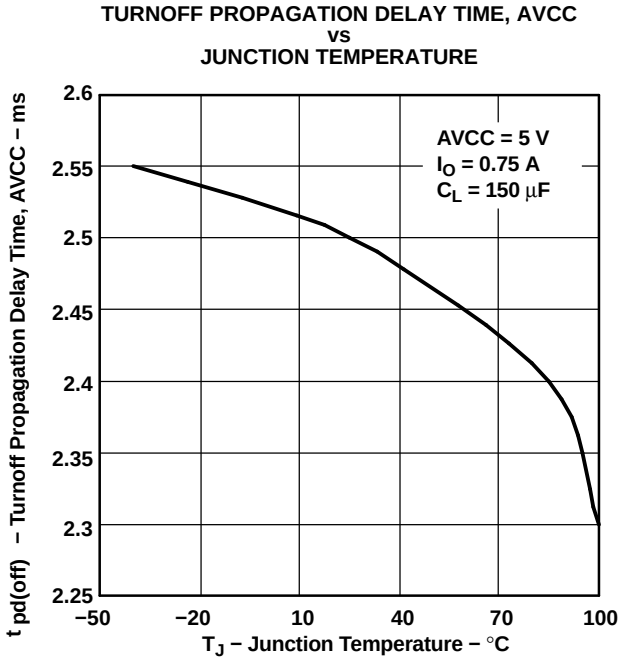


Figure 8.

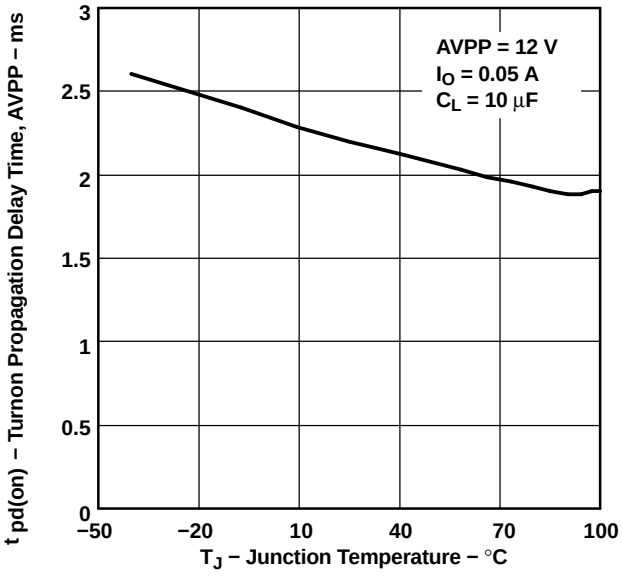


Figure 9.

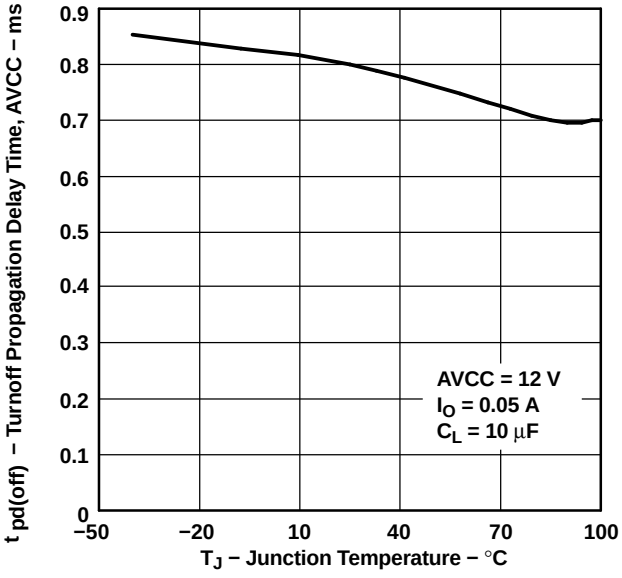


Figure 10.

TURNON PROPAGATION DELAY TIME, AVCC
vs
LOAD CAPACITANCE

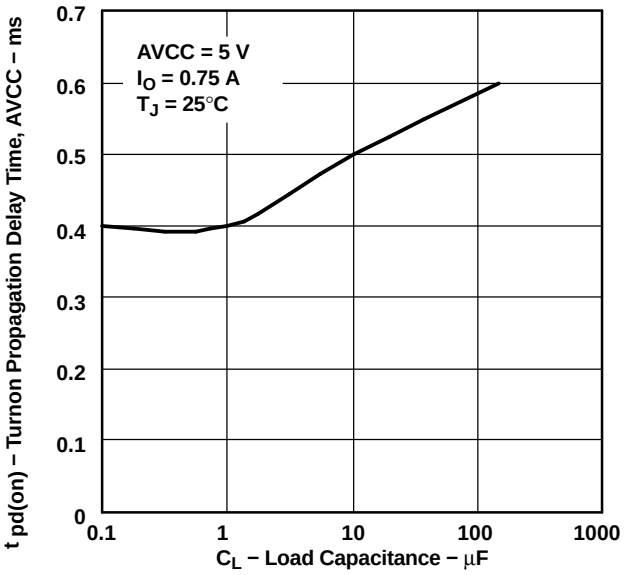


Figure 11.

TURNON PROPAGATION DELAY TIME, AVCC
vs
LOAD CAPACITANCE

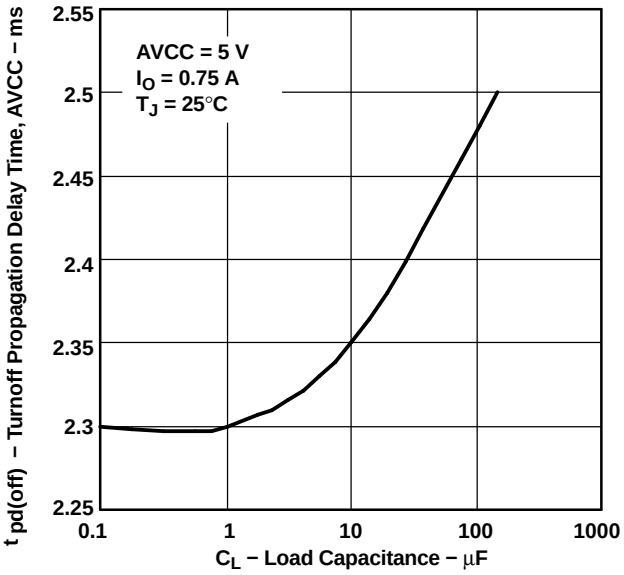


Figure 12.

TURNON PROPAGATION DELAY TIME, AVPP
vs
LOAD CAPACITANCE

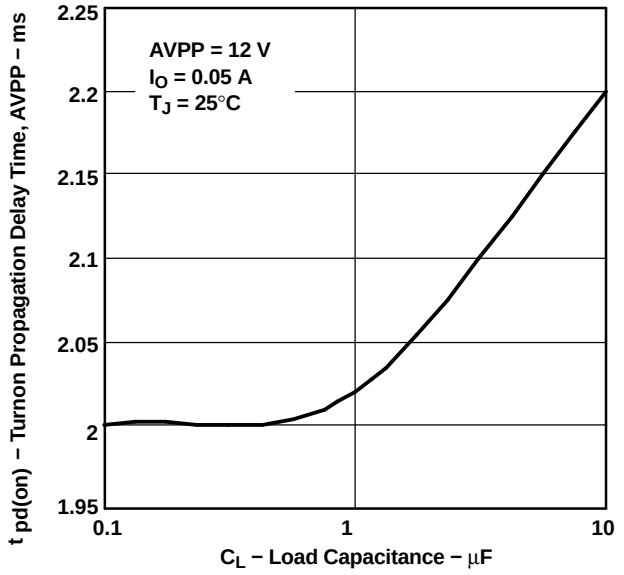


Figure 13.

TURNON PROPAGATION DELAY TIME, AVPP
vs
LOAD CAPACITANCE

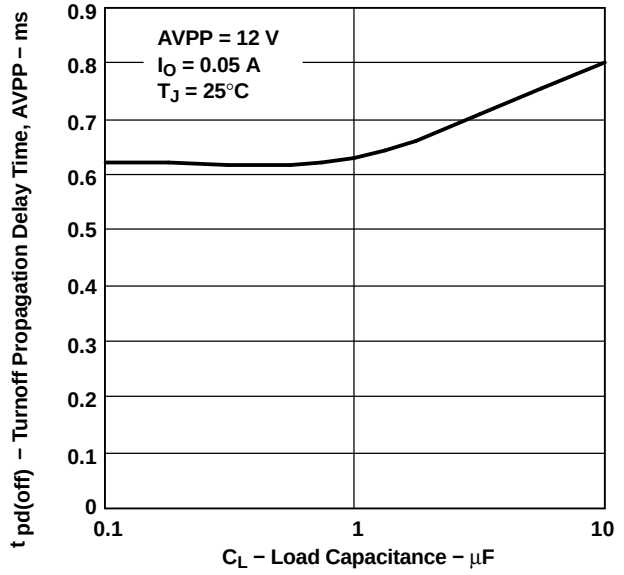


Figure 14.

RISE TIME, AVCC
vs
JUNCTION TEMPERATURE

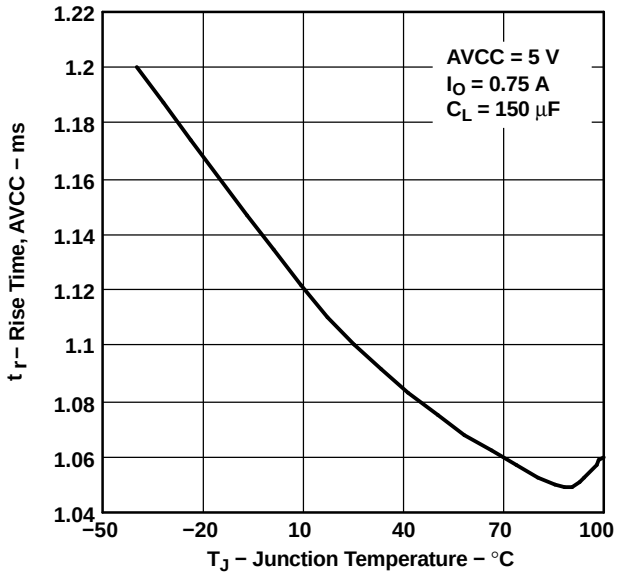


Figure 15.

FALL TIME, AVCC
vs
JUNCTION TEMPERATURE

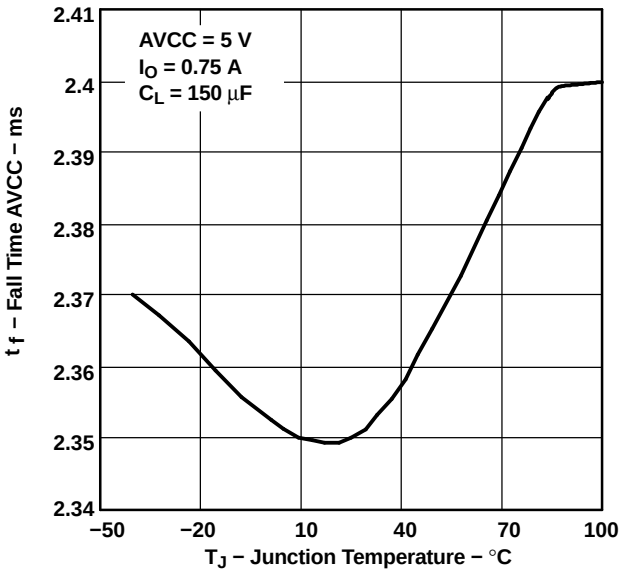


Figure 16.

RISE TIME, AVPP
vs
JUNCTION TEMPERATURE

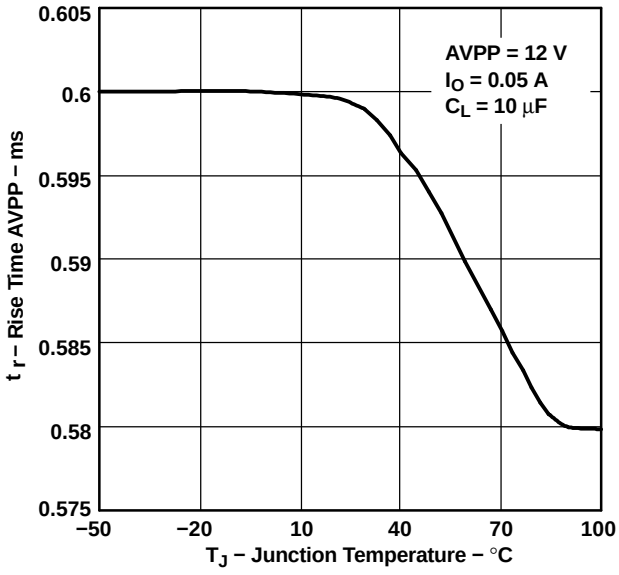


Figure 17.

FALL TIME, AVPP
vs
JUNCTION TEMPERATURE

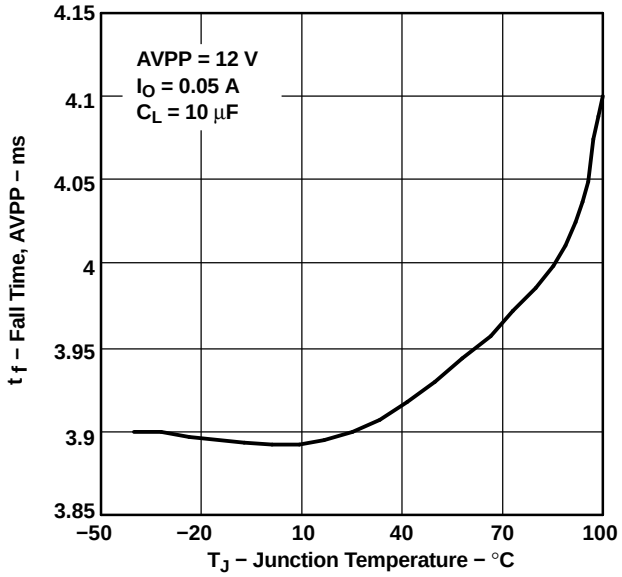


Figure 18.

RISE TIME, AVCC
vs
LOAD CAPACITANCE

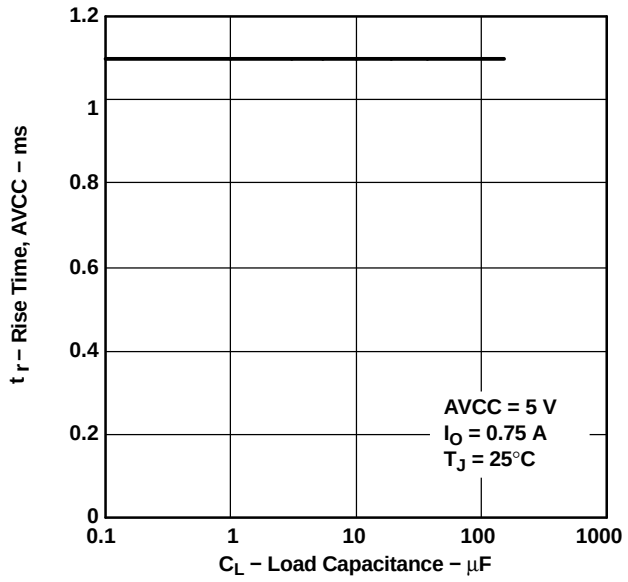


Figure 19.

FALL TIME, AVCC
vs
LOAD CAPACITANCE

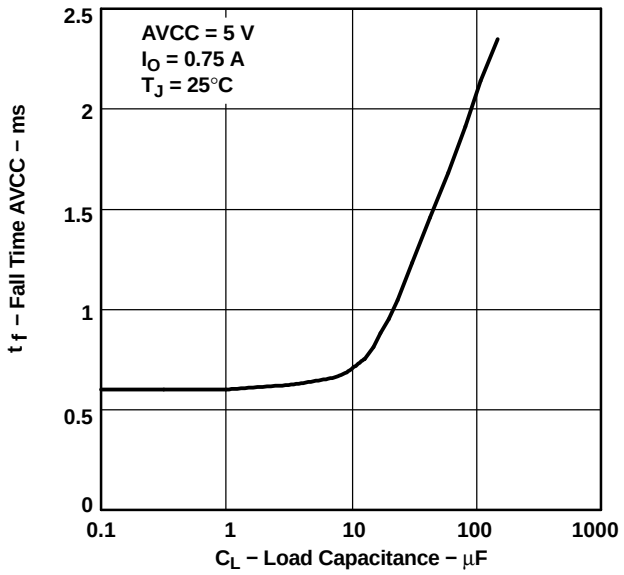


Figure 20.

RISE TIME, AVPP
vs
LOAD CAPACITANCE

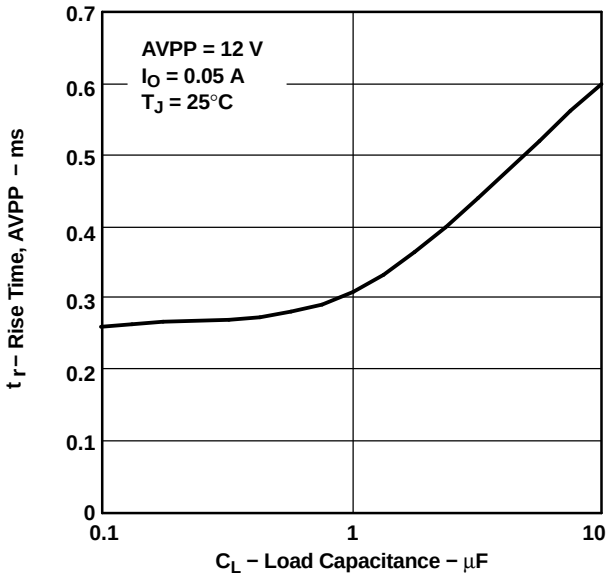


Figure 21.

FALL TIME, AVPP
vs
LOAD CAPACITANCE

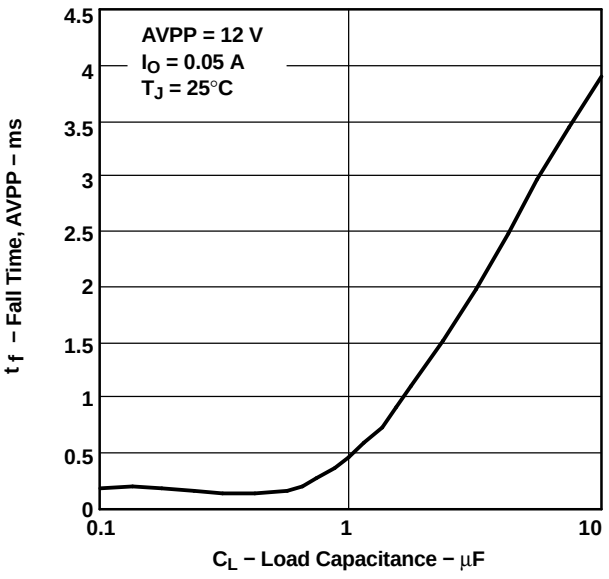


Figure 22.

TYPICAL CHARACTERISTICS

Table of Graphs

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V_O	AVCC switch voltage drop, 3.3-V input	vs Load current	29
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INPUT CURRENT, AVCC = 3.3 V
vs
JUNCTION TEMPERATURE

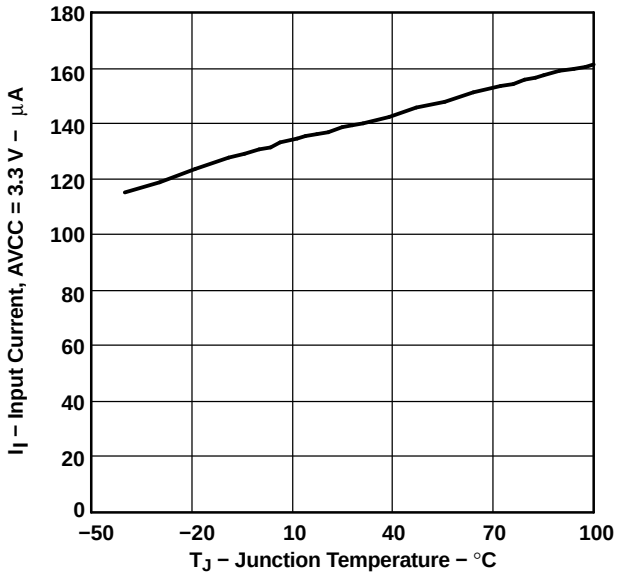


Figure 23.

INPUT CURRENT, AVCC = 5 V
vs
JUNCTION TEMPERATURE

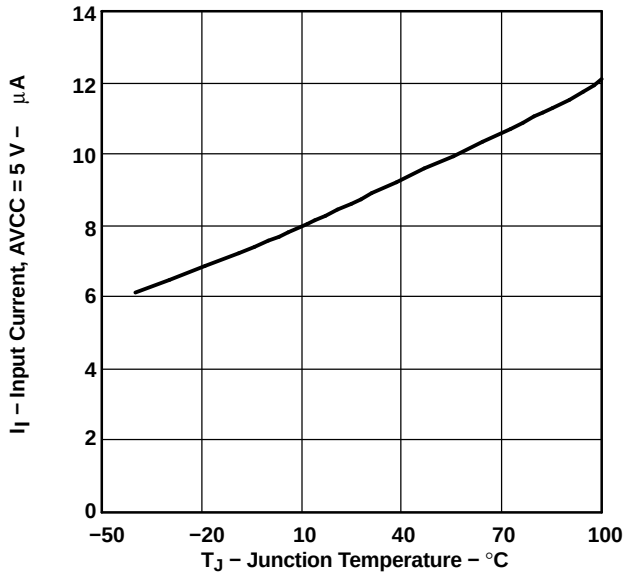


Figure 24.

INPUT CURRENT, AVPP = 12 V
vs
JUNCTION TEMPERATURE

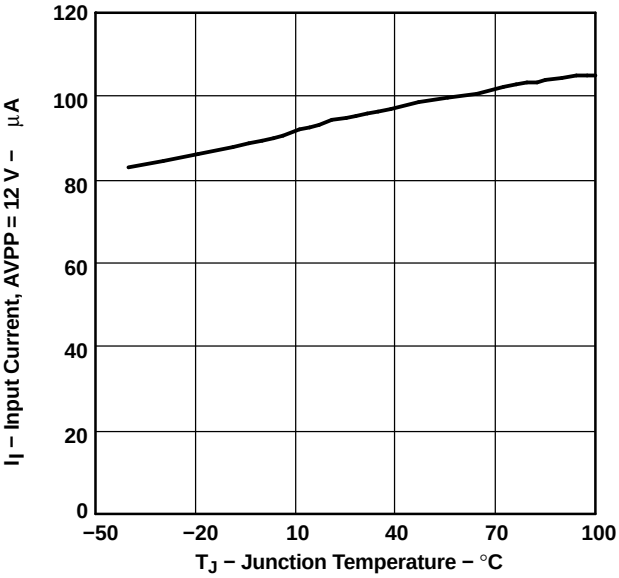


Figure 25.

STATIC DRAIN-SOURCE ON-STATE RESISTANCE,
3.3 V TO AVCC SWITCH
vs
JUNCTION TEMPERATURE

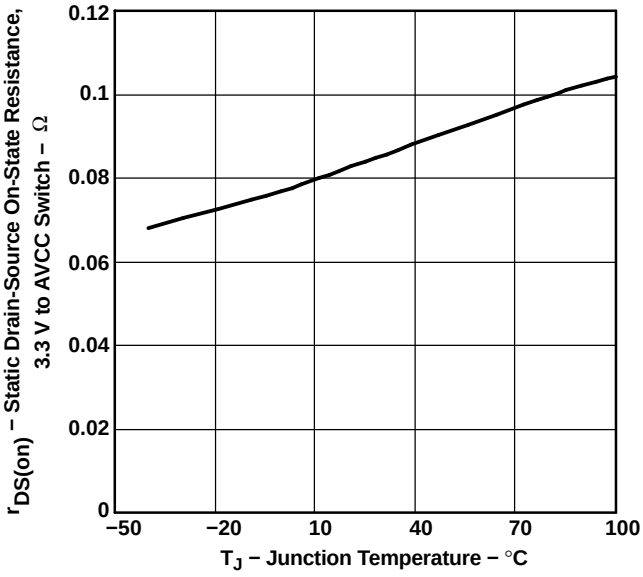


Figure 26.

STATIC DRAIN-SOURCE ON-STATE RESISTANCE,
5 V TO AVCC SWITCH
vs
JUNCTION TEMPERATURE

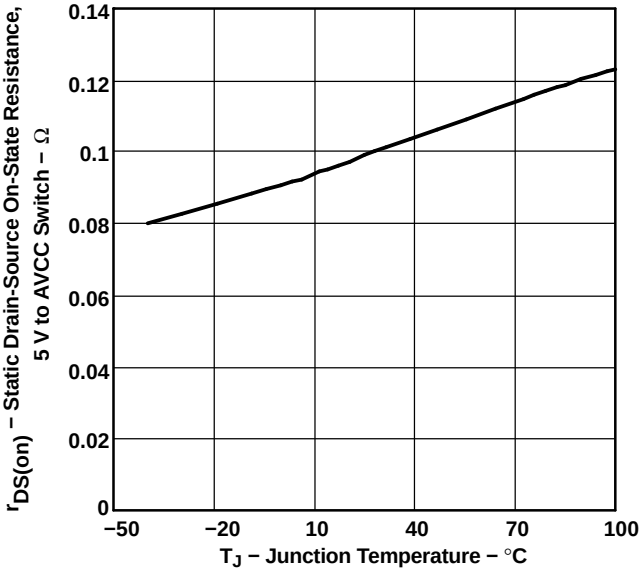


Figure 27.

STATIC DRAIN-SOURCE ON-STATE RESISTANCE,
12 V TO AVPP SWITCH
vs
JUNCTION TEMPERATURE

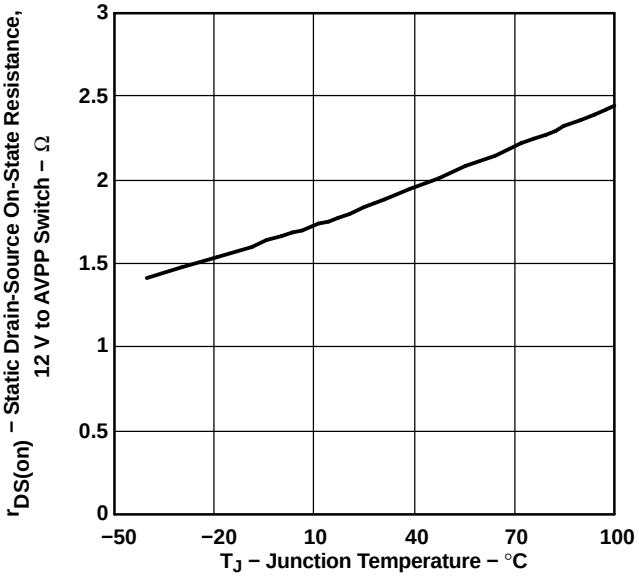


Figure 28.

AVCC SWITCH VOLTAGE DROP, 3.3-V INPUT
vs
LOAD CURRENT

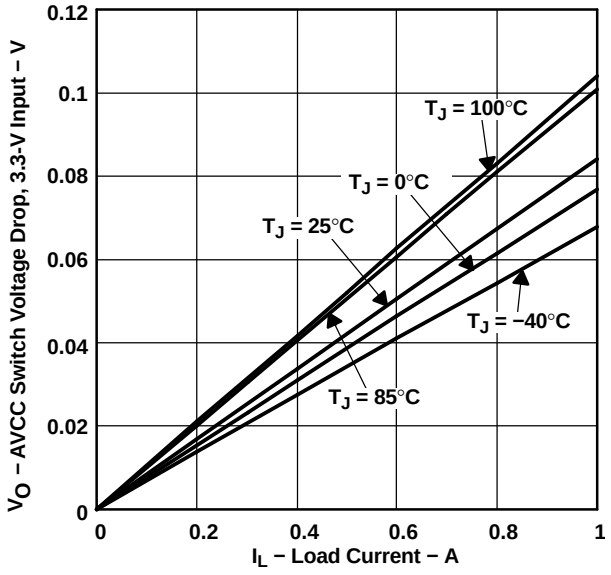


Figure 29.

AVCC SWITCH VOLTAGE DROP, 5-V INPUT
vs
LOAD CURRENT

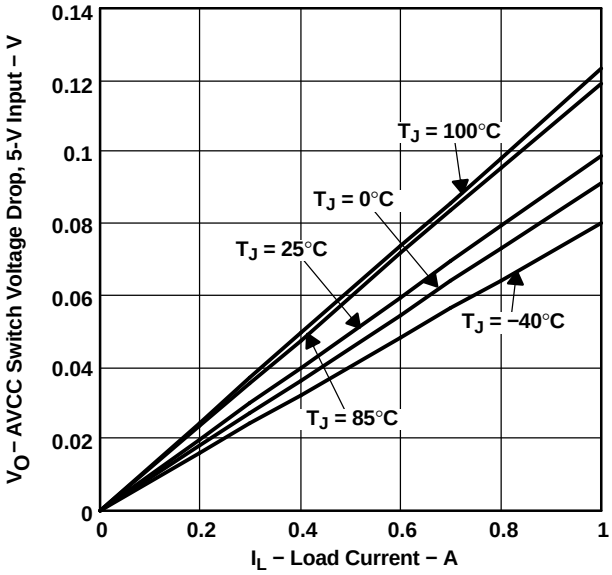


Figure 30.

AVPP SWITCH VOLTAGE DROP, 12-V INPUT
vs
LOAD CURRENT

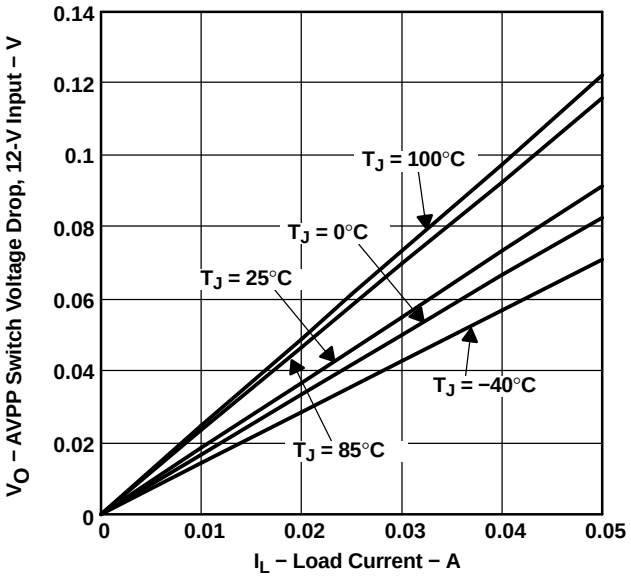


Figure 31.

SHORT-CIRCUIT CURRENT LIMIT, 3.3 V TO AVCC
vs
JUNCTION TEMPERATURE

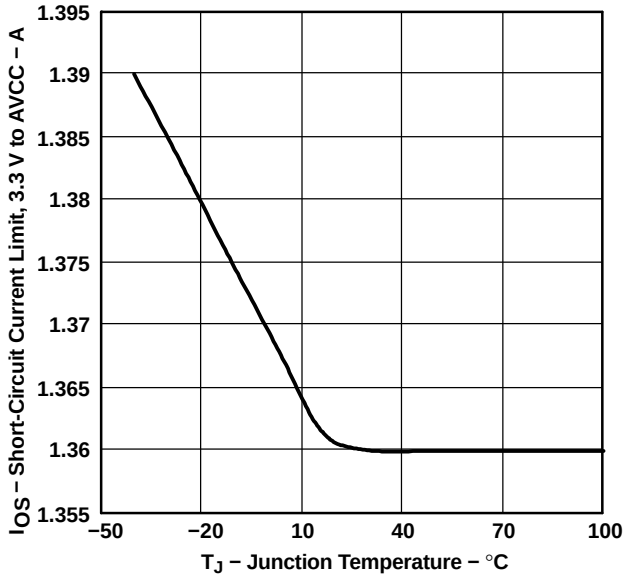


Figure 32.

SHORT-CIRCUIT CURRENT LIMIT, 5 V TO AVCC
vs
JUNCTION TEMPERATURE

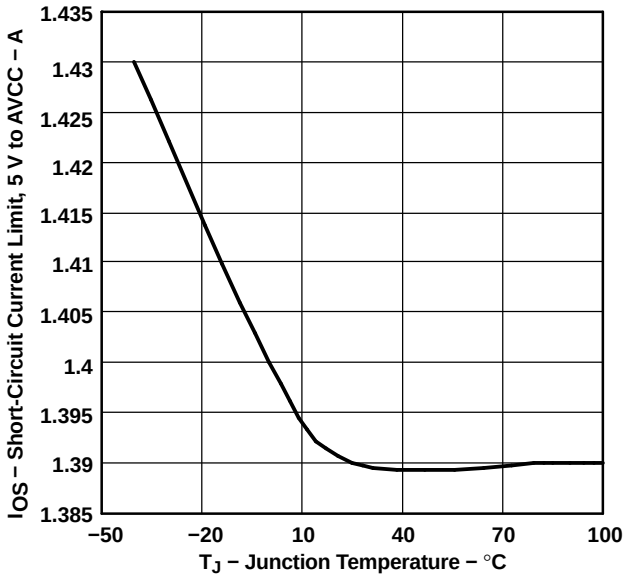


Figure 33.

SHORT-CIRCUIT CURRENT LIMIT, 12 V TO AVPP
vs
JUNCTION TEMPERATURE

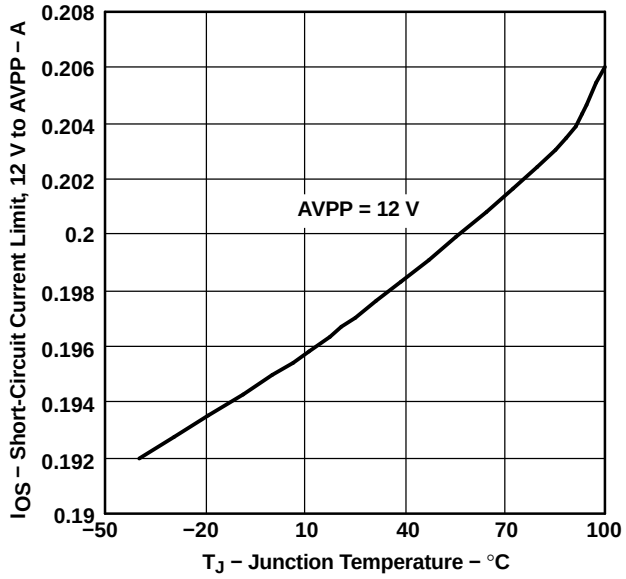


Figure 34.

APPLICATION INFORMATION

OVERVIEW

PC Cards were initially introduced as a means to add flash memory to portable computers. The idea of add-in cards quickly took hold, and modems, wireless LANs, global positioning satellite system (GPS), multimedia, and hard-disk versions were soon available. As the number of PC Card applications grew, the engineering community quickly recognized the need for a standard to ensure compatibility across platforms. Therefore, the PCMCIA (Personal Computer Memory Card International Association) was established, comprising members from leading computer, software, PC Card, and semiconductor manufacturers. One key goal was to realize the *plug-and-play* concept, so that cards and hosts from different vendors would be transparently compatible.

PC CARD POWER SPECIFICATION

System compatibility also means power compatibility. The most current set of specifications (PC Card Standard) set forth by the PCMCIA committee states that power is to be transferred between the host and the card through eight of the 68 terminals of the PC Card connector. This power interface consists of two V_{CC}, two V_{pp}, and four ground terminals. Multiple V_{CC} and ground terminals minimize connector-terminal and line resistance. The two V_{pp} terminals were originally specified as separate signals, but are normally tied together in the host to form a single node to minimize voltage losses. Card primary power is supplied through the V_{CC} terminals; flash-memory programming and erase voltage is supplied through the V_{pp} terminals. Cardbus cards of today typically do not use 12 V, which is now more of an optional requirement in the host.

DESIGNING FOR VOLTAGE REGULATION

The current PCMCIA specification for output voltage regulation, $V_{O(reg)}$, of the 5-V output is 5% (250 mV). In a typical PC power-system design, the power supply has an output-voltage regulation, $V_{PS(reg)}$, of 2% (100 mV). Also, a voltage drop from the power supply to the PC Card results from resistive losses, V_{PCB}, in the PCB traces and the PCMCIA connector. A typical design would limit the total of these resistive losses to less than 1% (50 mV) of the output voltage. Therefore, the allowable voltage drop, V_{DS}, for the TPS2220B would be the PCMCIA voltage regulation less the power supply regulation and less the PCB and connector resistive drops:

$$V_{DS} = V_{O(reg)} - V_{PS(reg)} - V_{PCB}$$

Typically, this would leave 100 mV for the allowable voltage drop across the 5-V switch. The specification for output voltage regulation of the 3.3-V output is 300 mV; therefore, using the same equation by deducting the voltage drop percentages (2%) for power-supply regulation and PCB resistive loss (1%), the allowable voltage drop for the 3.3-V switch is 200 mV. The voltage drop is the output current multiplied by the switch resistance of the device. Therefore, the maximum output current, I_O max, that can be delivered to the PC Card in regulation is the allowable voltage drop across the IC, divided by the output-switch resistance.

$$I_O max = \frac{V_{DS}}{r_{DS(on)}}$$

The AVCC outputs have been designed to deliver the peak and average currents defined by the PC Card specification within regulation over the operating temperature range. The AVPP outputs of the device have been designed to deliver 100 mA continuously.

OVERCURRENT AND OVERTEMPERATURE PROTECTION

PC Cards are inherently subject to damage that can result from mishandling. Host systems require protection against short-circuited cards that can lead to power-supply or PCB trace damage. Even extremely robust systems can undergo rapid battery discharge into a damaged PC Card, resulting in the sudden and unacceptable loss of system power. In comparison, the reliability of fused systems is poor because blown fuses require troubleshooting and repair, usually by the manufacturer.

The TPS2220B takes a two-pronged approach to overcurrent protection, which is designed to activate if an output is shorted or when an overcurrent condition is present when switches are powered up. First, instead of fuses, sense FETs monitor each of the AVCC and AVPP power outputs. Unlike sense resistors or polyfuses,

APPLICATION INFORMATION (continued)

these FETs do not add to the series resistance of the switch; therefore, voltage and power losses are reduced. Overcurrent sensing is applied to each output separately. Excessive current generates an error signal that limits the output current of only the affected output, preventing damage to the host. Each AVCC output overcurrent limits from 1 A to 2.0 A, typically around 1.6 A; the AVPP outputs limit from 100 mA to 250 mA, typically around 200 mA.

Second, when an overcurrent condition is detected, the TPS2220B asserts an active low $\overline{OC}$ signal that can be monitored by the microprocessor or controller to initiate diagnostics and/or send the user a warning message. If an overcurrent condition persists, causing the IC to exceed its maximum junction temperature, thermal-protection circuitry activates, shutting down all power outputs until the device cools to within a safe operating region, which is ensured by a thermal shutdown hysteresis. Thermal limiting prevents destruction of the IC from overheating beyond the package power-dissipation ratings.

During power up, the devices control the rise times of the AVCC and AVPP outputs and limit the inrush current into a large load capacitance, faulty card, or connector.

12-V SUPPLY NOT REQUIRED

Some PC Card switches use the externally supplied 12 V to power gate drive and other chip functions, which requires that power be present at all times. The TPS2220B offers considerable power savings by using an internal charge pump to generate the required higher gate drive voltages from the 3.3-V input. Therefore, the external 12-V supply can be disabled except when needed by the PC Card in the slot, thereby extending battery lifetime. A special feature in the 12-V circuitry actually helps to reduce the supply current demanded from the 3.3-V input. When 12 V is supplied and requested at the VPP output, a voltage selection circuit draws the charge-pump drive current for the 12-V FETs from the 12-V input. This selection is automatic and effectively reduces demand fluctuations on the normal 3.3-V VCC rail. For proper operation of this feature, a minimum 3.3-V input capacitance of 4.7 µF is recommended, and a minimum 12-V input ramp-up rate of 12 V/50 ms (240 V/s) is required. Additional power savings are realized during a software shutdown in which quiescent current drops to a maximum of 1 µA.

VOLTAGE-TRANSITIONING REQUIREMENT

PC Cards, like portables, are migrating from 5 V to 3.3 V to minimize power consumption, optimize board space, and increase logic speeds. The TPS2220B meets all combinations of power delivery as currently defined in the PCMCIA standard. The latest protocol accommodates mixed 3.3-V/5-V systems by first powering the card with 5 V, then polling it to determine its 3.3-V compatibility. The PCMCIA specification requires that the capacitors on 3.3-V-compatible cards be discharged to below 0.8 V before applying 3.3-V power. This action ensures that sensitive 3.3-V circuitry is not subjected to any residual 5-V charge and functions as a power reset. PC Card specification requires that V_{CC} be discharged within 100 ms. PC Card resistance cannot be relied on to provide a discharge path for voltages stored on PC Card capacitance because of possible high-impedance isolation by power-management schemes. The devices include discharge transistors on all AVCC and AVPP outputs to meet the specification requirement.

SHUTDOWN MODE

In the shutdown mode, which can be controlled by $\overline{SHDN}$ or bit D8 of the input serial DATA word, each of the AVCC and AVPP outputs is forced to a high-impedance state. In this mode, the chip quiescent current is reduced to 1 µA or less to conserve battery power.

POWER-SUPPLY CONSIDERATIONS

The devices has multiple pins for 5-V power input and for the switched AVCC output. Any individual pin can conduct the rated input or output current. Unless all pins are connected in parallel, the series resistance is higher than that specified, resulting in increased voltage drops and power loss. It is recommended that all input and output power pins be paralleled for optimum operation.

To increase the noise immunity of the TPS2220B the power-supply inputs should be bypassed with at least a 4.7-µF electrolytic or tantalum capacitor paralleled by a 0.047-µF to 0.1-µF ceramic capacitor. It is strongly

APPLICATION INFORMATION (continued)

recommended that the switched outputs be bypassed with a 0.1-µF (or larger) ceramic capacitor; doing so improves the immunity of the IC to electrostatic discharge (ESD). Care should be taken to minimize the inductance of PCB traces between the devices and the load. High switching currents can produce large negative voltage transients, which forward biases substrate diodes, resulting in unpredictable performance. Similarly, no pin should be taken below –0.3 V.

$\overline{\text{RESET}}$ INPUT

To ensure that cards are in a known state after power brownouts or system initialization, the PC Cards should be reset at the same time as the host by applying low-impedance paths from AVCC and AVPP terminals to ground. A low-impedance output state allows discharging of residual voltage remaining on PC Card filter capacitance, permitting the system (host and PC Cards) to be powered up concurrently. The active low $\overline{\text{RESET}}$ input closes internal ground switches S1, S4, S7, and S11 with all other switches left open. The TPS2220B remains in the low-impedance output state until the signal is deasserted and further data is clocked in and latched. The input serial data cannot be latched during reset mode. $\overline{\text{RESET}}$ is provided for direct compatibility with systems that use an active-low reset voltage supervisor. The $\overline{\text{RESET}}$ pin has an internal 150-kΩ pullup resistor.

CALCULATING JUNCTION TEMPERATURE

The switch resistance, $r_{DS(on)}$, is dependent on the junction temperature, T_J, of the die. The junction temperature is dependent on both $r_{DS(on)}$ and the current through the switch. To calculate T_J, first find $r_{DS(on)}$ from Figure 26 through Figure 28, using an initial temperature estimate about 30°C above ambient. Then, calculate the power dissipation for each switch, using the formula:

$$P_D = r_{DS(on)} \times I^2$$

Next, sum the power dissipation of all switches and calculate the junction temperature:

$$T_J = \left(\sum P_D \times R_{\theta JA}\right) + T_A$$

where:

$R_{\theta JA}$ is the inverse of the derating factor given in the dissipation rating table.

Compare the calculated junction temperature with the initial temperature estimate. If the temperatures are not within a few degrees of each other, recalculate using the calculated temperature as the initial estimate.

LOGIC INPUTS AND OUTPUTS

The serial interface consists of the DATA, CLOCK, and LATCH leads. The data is clocked in on the positive edge of the clock (see Figure 2). The 11-bit (D0-D10) serial data word is loaded during the positive edge of the latch signal. The positive edge of the latch signal should occur before the next positive edge of the clock occurs.

The serial interface of the device is compatible with serial-interface PCMCIA controllers.

An overcurrent output ($\overline{\text{OC}}$) is provided to indicate an overcurrent or overtemperature condition in any of the AVCC and AVPP outputs as previously discussed.

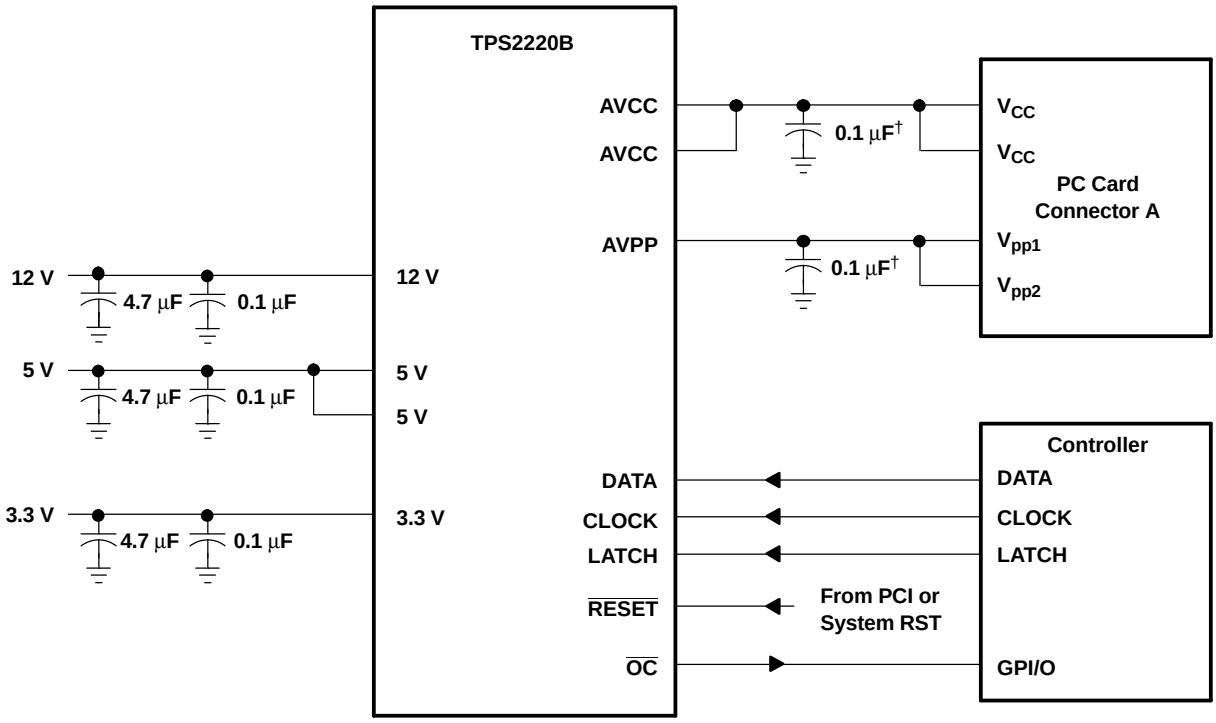
APPLICATION INFORMATION (continued)

TPS2220B CONTROL LOGIC

AVPP					AVCC			
AVPP CONTROL SIGNALS				OUTPUT V_AVPP	AVCC CONTROL SIGNALS			OUTPUT V_AVCC
D8 ($\overline{SHDN}$)	D0	D1	D9		D8 ($\overline{SHDN}$)	D3	D2	
1	0	0	X	0 V	1	0	0	0 V
1	0	1	0	3.3 V	1	0	1	3.3 V
1	0	1	1	5 V	1	1	0	5 V
1	1	0	X	12 V	1	1	1	0 V
1	1	1	X	Hi-Z	0	X	X	Hi-Z
0	X	X	X	Hi-Z				

ESD PROTECTIONS (see Figure 35)

All inputs and outputs of these devices incorporate ESD-protection circuitry designed to withstand a 2-kV human-body-model discharge as defined in MIL-STD-883C, Method 3015. The AVCC and AVPP outputs can be exposed to potentially higher discharges from the external environment through the PC Card connector. Bypassing the outputs with 0.1-µF capacitors protects the devices from discharges up to 10 kV.



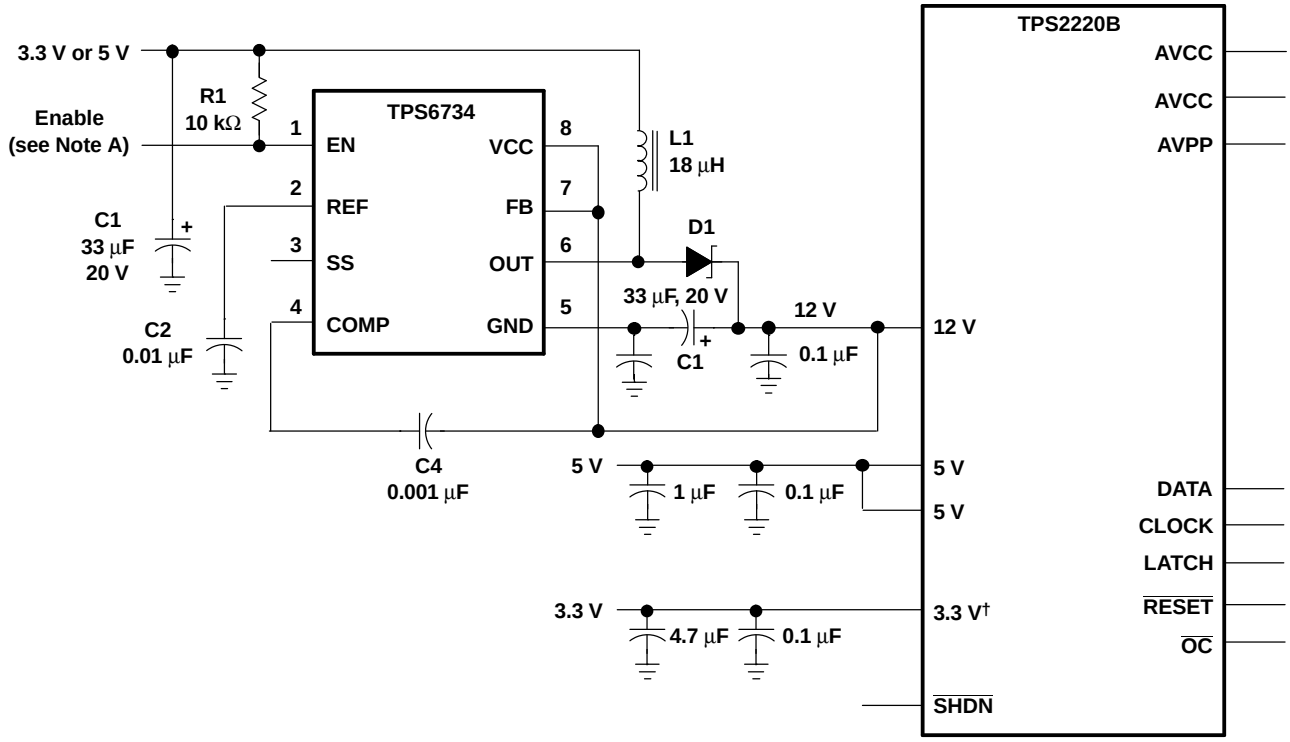
† Maximum recommended output capacitance for AVCC is 220 µF including card capacitance, and for AVPP is 10 µF, without $\overline{OC}$ glitch when switches are powered on.

Figure 35. Detailed Interconnections and Capacitor Recommendations

12-V FLASH MEMORY SUPPLY

The TPS6734 is a fixed 12-V output boost converter capable of delivering 120 mA from inputs as low as 2.7 V. The device is pin-for-pin compatible with the MAX734 regulator and offers the following advantages: lower supply current, wider operating input-voltage range, and higher output currents. As shown in Figure 36, the only external components required are: an inductor, a Schottky rectifier, an output filter capacitor, an input filter capacitor, and a small capacitor for loop compensation. The entire converter occupies less than 0.7 in^2 of PCB space when implemented with surface-mount components. An enable input is provided to shut the converter down and reduce the supply current to 3 µA when 12 V is not needed.

The TPS6734 is a 170-kHz current-mode PWM (pulse-width modulation) controller with an n-channel MOSFET power switch. Gate drive for the switch is derived from the 12-V output after start-up to minimize the die area needed to realize the 0.7-Ω MOSFET and improve efficiency at input voltages below 5 V. Soft start is accomplished with the addition of one small capacitor. A 1.22-V reference, pin 2 of TPS6734, is brought out for external use. For additional information, see the TPS6734 data sheet (SLVS127).



NOTE A: The enable terminal can be tied to a general-purpose I/O terminal on the PCMCIA controller or tied high.

Figure 36. TPS2220B With TPS6734 12-V, 120-mA Supply

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2220BDB	ACTIVE	SSOP	DB	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2220B	Samples
TPS2220BDBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2220B	Samples
TPS2220BPWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS2220B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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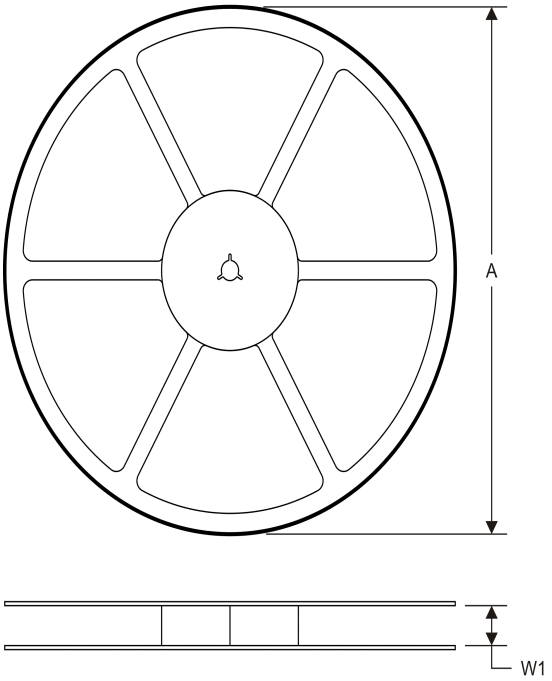
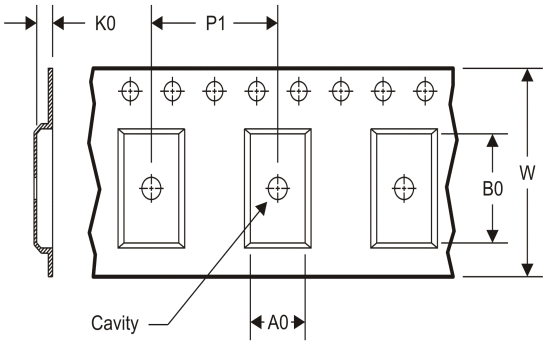
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



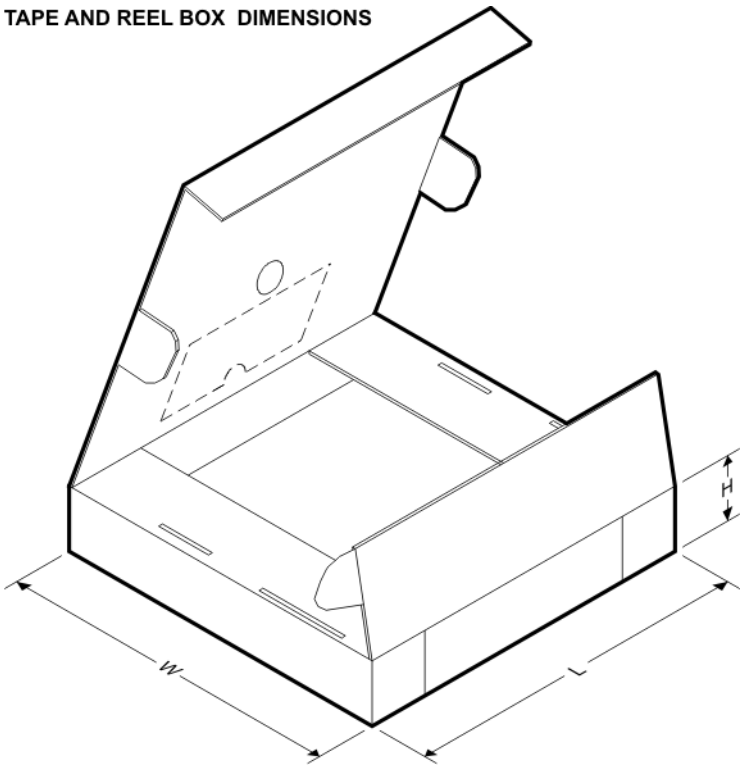
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2220BDBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
TPS2220BPWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

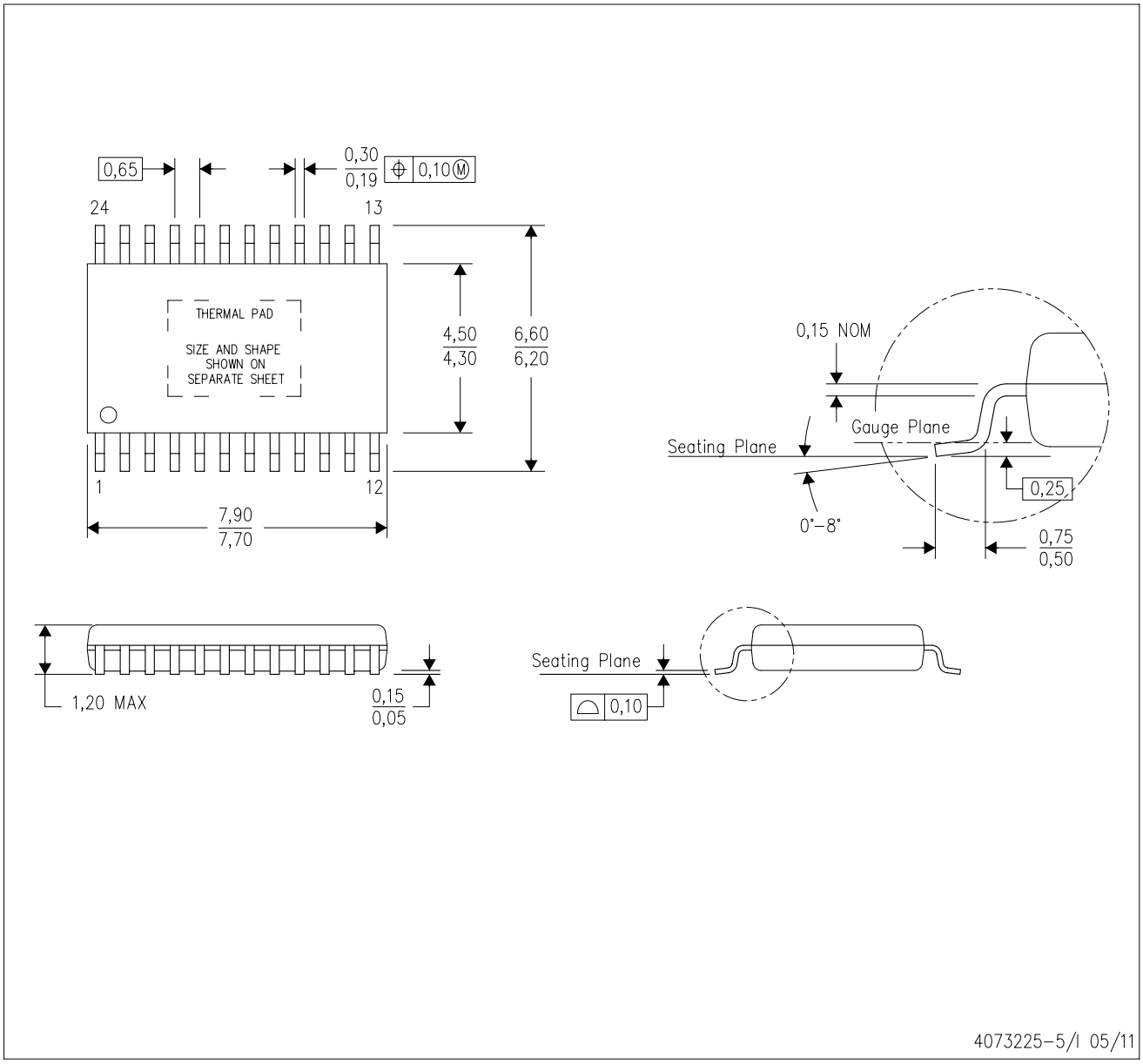
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2220BDBR	SSOP	DB	24	2000	367.0	367.0	38.0
TPS2220BPWPR	HTSSOP	PWP	24	2000	367.0	367.0	38.0

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

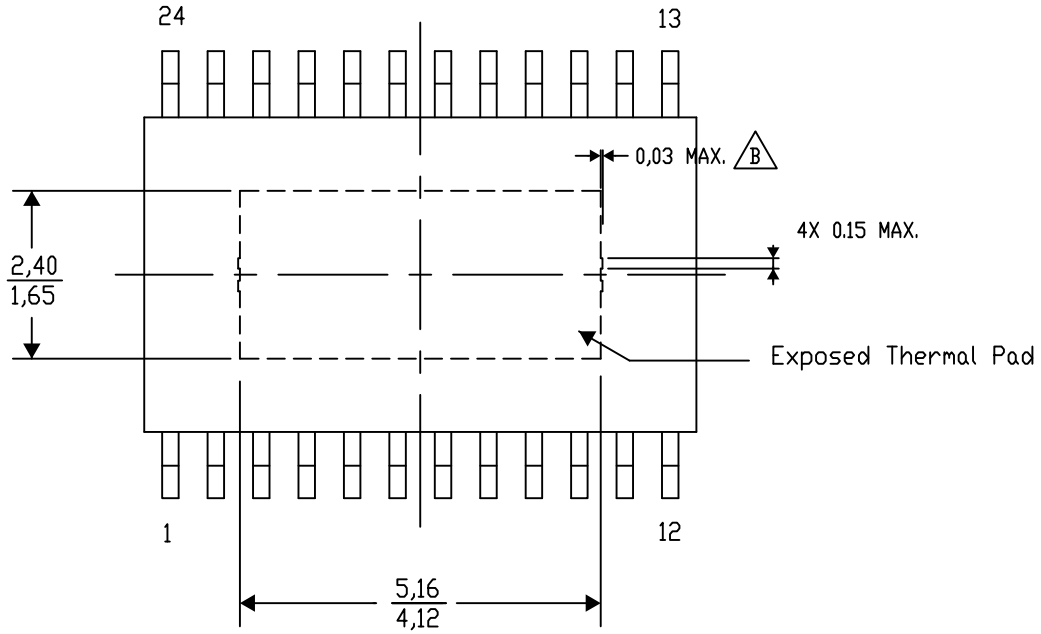
PWP (R–PDSO–G24) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

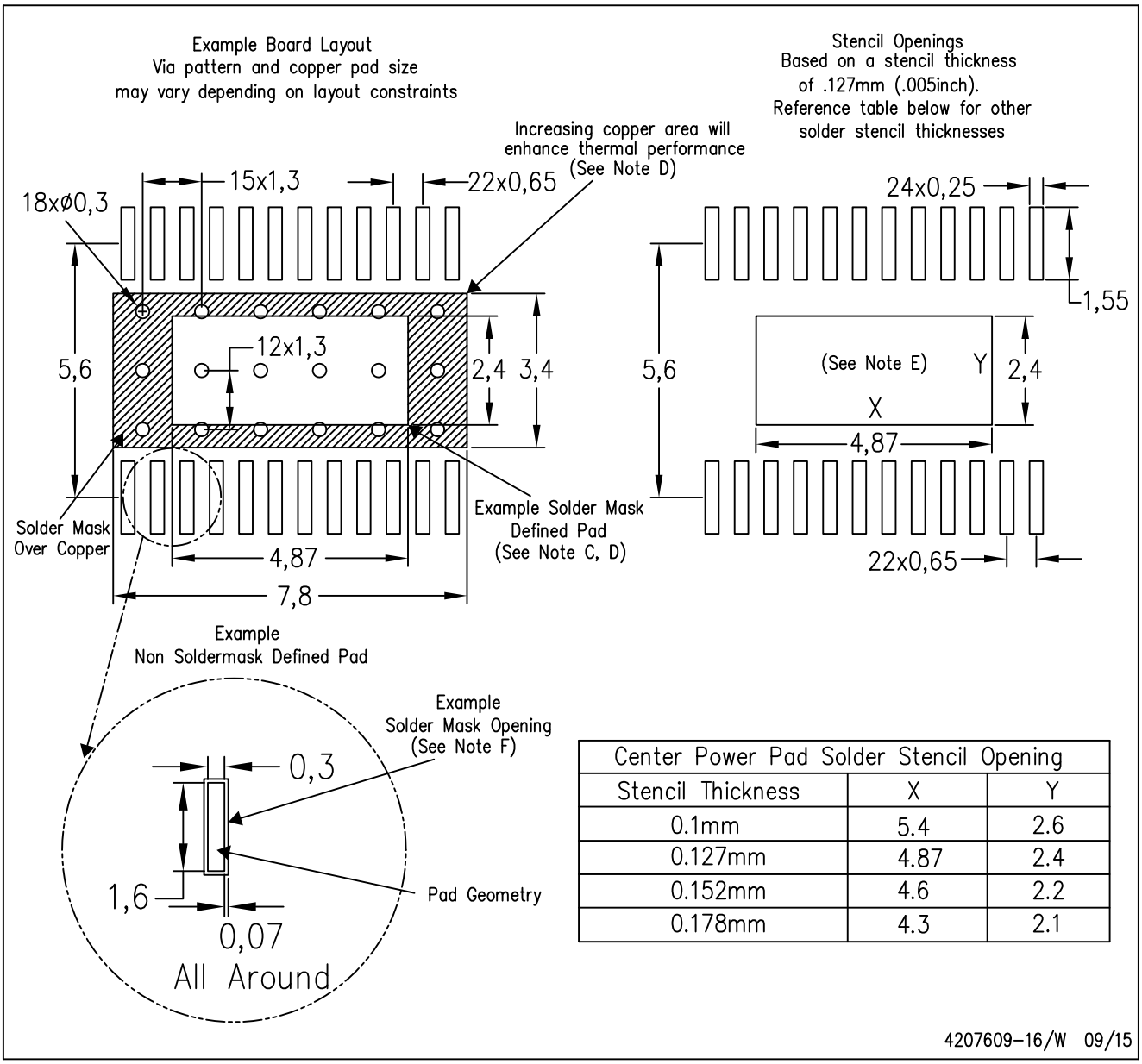
4206332–29/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.4	2.6
0.127mm	4.87	2.4
0.152mm	4.6	2.2
0.178mm	4.3	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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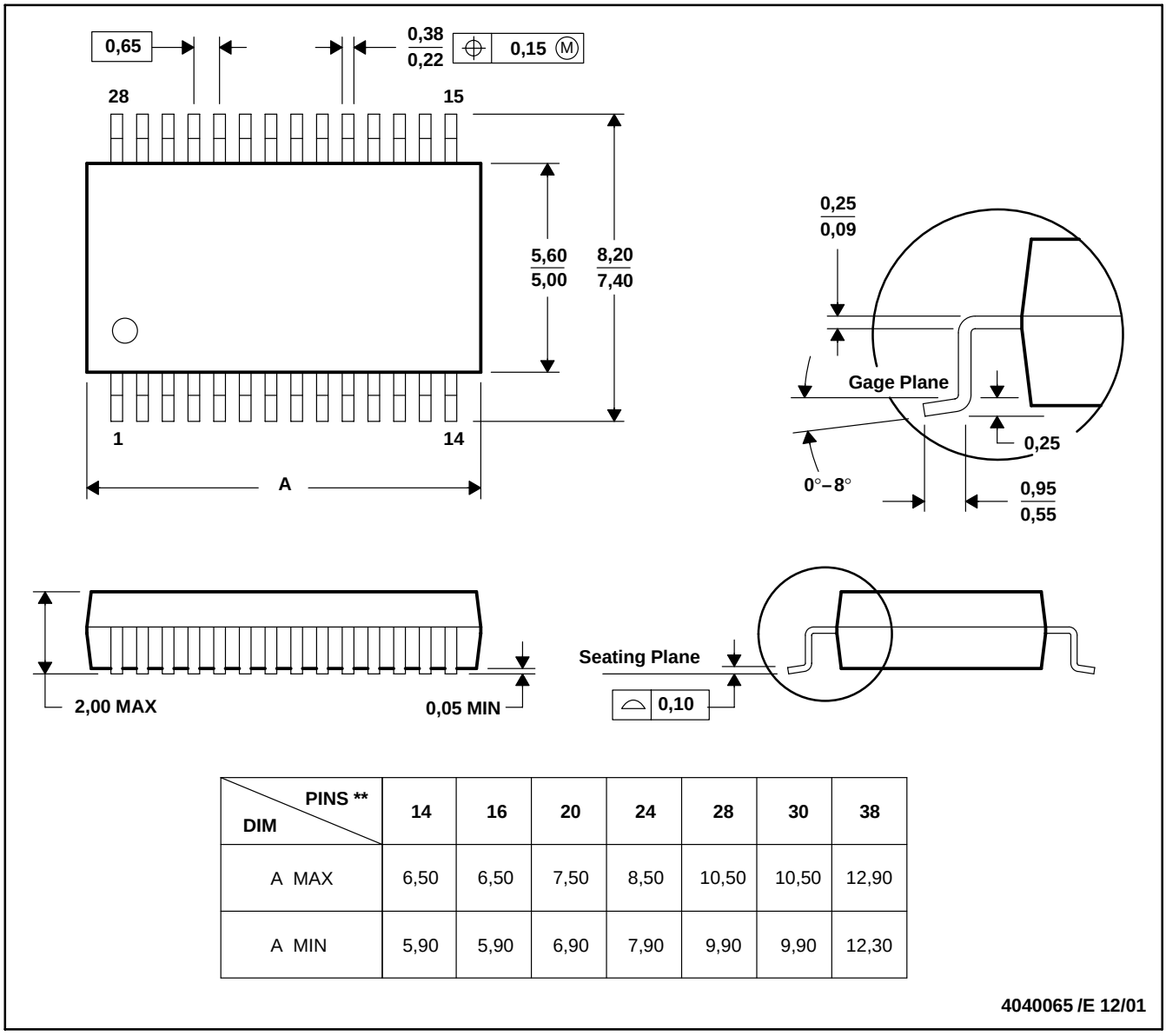
DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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