WINSOURCE
ELECTRONICS

THE DATASHEET OF

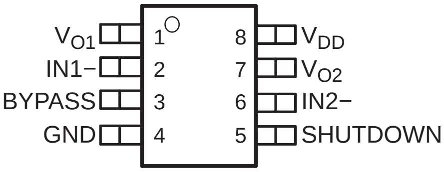
TPA6113A2DR

40-mW STEREO AUDIO POWER AMPLIFIER

FEATURES

- **40-mW Stereo Output**
- **PC Power Supply Compatible**
  - **Fully Specified for 3.3-V and 5-V Operation**
- **Pop Reduction Circuitry**
- **Internal Midrail Generation**
- **Thermal and Short-Circuit Protection**
- **Surface-Mount Packaging**
  - **SOIC**

D PACKAGE
(TOP VIEW)

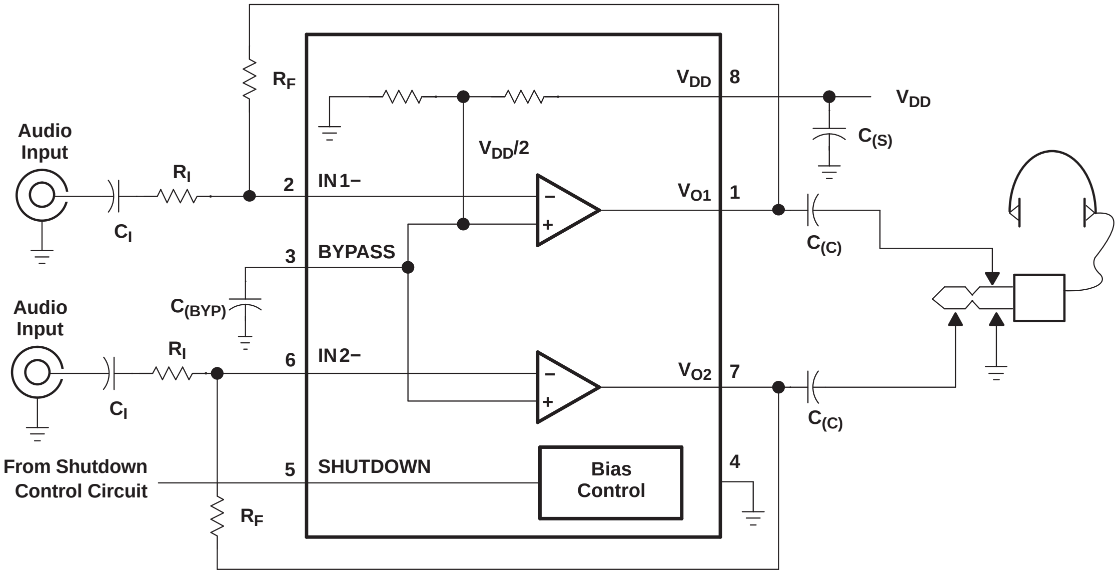


DESCRIPTION

The TPA6113A2 is a stereo audio power amplifier packaged in an 8-pin SOIC package capable of delivering 40 mW of continuous RMS power per channel into 16-Ω loads. Amplifier gain is externally configured by means of two resistors per input channel and does not require external compensation for settings of 0 to 20 dB.

THD+N, when driving a 16-Ω load from 5 V, is 0.03% at 1 kHz, and less than 1% across the audio band of 20 Hz to 20 kHz. For 32-Ω loads, the THD+N is reduced to less than 0.02% at 1 kHz, and is less than 1% across the audio band of 20 Hz to 20 kHz.

TYPICAL APPLICATION CIRCUIT



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	SMALL OUTLINE[1] (D)
–40°C to 85°C	TPA6113A2D

(1) The D package is available in left-ended tape and reel only (e.g., TPA6113A2DR).

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
BYPASS	3	I	Tap to voltage divider for internal mid-supply bias supply. Connect to a 0.1-µF to 1-µF low ESR capacitor for best performance.
GND	4	I	GND is the ground connection.
IN1–	2	I	IN1– is the inverting input for channel 1.
IN2–	6	I	IN2– is the inverting input for channel 2.
SHUTDOWN	5	I	Puts the device in a low quiescent current mode when held high
V_{DD}	8	I	V_{DD} is the supply voltage terminal.
V_{O1}	1	O	V_{O1} is the audio output for channel 1.
V_{O2}	7	O	V_{O2} is the audio output for channel 2.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		UNIT
V_{DD}	Supply voltage	6 V
V_I	Input voltage	–0.3 V to V_{DD} + 0.3 V
	Continuous total power dissipation	internally limited
T_J	Operating junction temperature range	–40°C to 150°C
T_{stg}	Storage temperature range	–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under "absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25 C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{DD}	Supply voltage	2.5	5.5	V
T_A	Operating free-air temperature	–40	85	°C
V_{IH}	High-level input voltage (SHUTDOWN)	60% x V_{DD}		V
V_{IL}	Low-level input voltage (SHUTDOWN)		25% x V_{DD}	V

DC ELECTRICAL CHARACTERISTICS

at V_{DD} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OO}	Output offset voltage				10	mV
PSRR	Power supply rejection ratio	V_{DD} = 3.2 V to 3.4 V		70		dB
I_{DD}	Supply current	SHUTDOWN (pin 5) = 0 V		1.5	3	mA
$I_{DD(SD)}$	Supply current in shutdown mode	SHUTDOWN (pin 5) = V_{DD}		1	10	μA
Z_i	Input impedance			> 1		MΩ

AC OPERATING CHARACTERISTICS

V_{DD} = 3.3 V, T_A = 25°C, R_L = 16 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%, f = 1 kHz		16		mW
THD+N	Total harmonic distortion + noise	P_O = 16 mW, 20 Hz – 20 kHz		0.4%		
B_{OM}	Maximum output power BW	G = 20 dB, THD < 5%		> 20		kHz
	Phase margin	Open loop		96°		
	Supply ripple rejection	f = 1 kHz, $C_{(BYP)}$ = 0.47 F		71		dB
	Channel/channel output separation	f = 1 kHz, P_O = 15 mW		89		dB
SNR	Signal-to-noise ratio	P_O = 15 mW, A_V = 1		93		dB
V_n	Noise output voltage	A_V = 1		11		μV(rms)

DC ELECTRICAL CHARACTERISTICS

at V_{DD} = 5.5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OO}	Output offset voltage				10	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V		70		dB
I_{DD}	Supply current	SHUTDOWN (pin 5) = 0 V		1.6	3.2	mA
$I_{DD(SD)}$	Supply current in shutdown mode	SHUTDOWN (pin 5) = V_{DD}		1	10	μA
$\lvert I_{IH} \rvert$	High-level input current (SHUTDOWN)	V_{DD} = 5.5 V, V_I = V_{DD}			1	μA
$\lvert I_{IL} \rvert$	Low-level input current (SHUTDOWN)	V_{DD} = 5.5 V, V_I = 0 V			1	μA
Z_i	Input impedance			> 1		MΩ

AC OPERATING CHARACTERISTICS

V_{DD} = 5 V, T_A = 25°C, R_L = 16 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%, f = 1 kHz		40		mW
THD+N	Total harmonic distortion + noise	P_O = 20 mW, 20 Hz – 20 kHz		0.4%		
B_{OM}	Maximum output power BW	G = 20 dB, THD < 5%		> 20		kHz
	Phase margin	Open loop		96°		
	Supply ripple rejection ratio	f = 1 kHz, $C_{(BYP)}$ = 0.47 μF		61		dB
	Channel/channel output separation	f = 1 kHz, P_O = 25 mW		90		dB
SNR	Signal-to-noise ratio	P_O = 25 mW, A_V = 1		94		dB
V_n	Noise output voltage	A_V = 1		11.7		μV(rms)

AC OPERATING CHARACTERISTICS

V_{DD} = 3.3 V, T_A = 25°C, R_L = 32 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%, f = 1 kHz		10		mW
THD+N	Total harmonic distortion + noise	P_O = 10 mW, 20 Hz – 20 kHz		0.4%		
B_{OM}	Maximum output power BW	G = 20 dB, THD < 2%		> 20		kHz
	Phase margin	Open loop		96°		
	Supply ripple rejection	f = 1 kHz, $C_{(BYP)}$ = 0.47 F		71		dB
	Channel/channel output separation	f = 1 kHz, P_O = 10 mW		95		dB
SNR	Signal-to-noise ratio	P_O = 10 mW, A_V = 1		94		dB
V_n	Noise output voltage	A_V = 1		11		μV(rms)

AC OPERATING CHARACTERISTICS

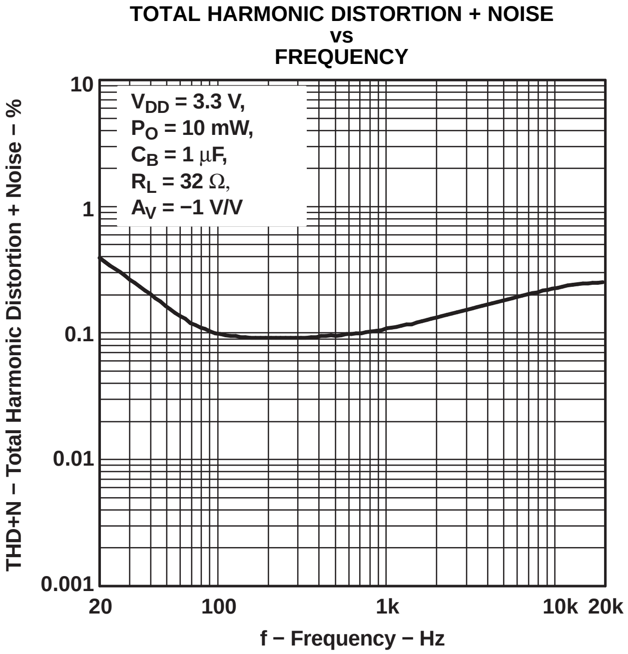
V_{DD} = 5 V, T_A = 25°C, R_L = 32 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%, f = 1 kHz		90		mW
THD+N	Total harmonic distortion + noise	P_O = 20 mW, 20 Hz – 20 kHz		2%		
B_{OM}	Maximum output power BW	G = 20 dB, THD < 2%		> 20		kHz
	Phase margin	Open loop		97°		
	Supply ripple rejection	f = 1 kHz, $C_{(BYP)}$ = 0.47 μF		61		dB
	Channel/channel output separation	f = 1 kHz, P_O = 20 mW		98		dB
SNR	Signal-to-noise ratio	P_O = 20 mW, A_V = 1		97		dB
V_n	Noise output voltage	A_V = 1		11.7		μV(rms)

TYPICAL CHARACTERISTICS

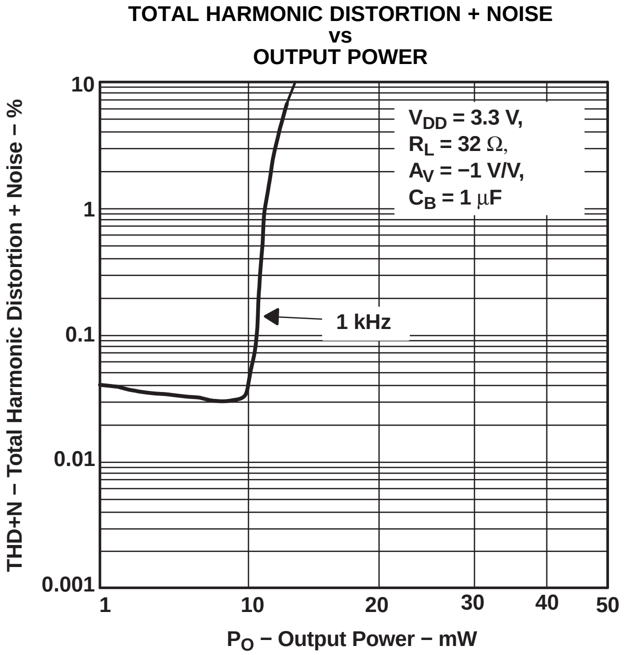
Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Frequency	1, 3, 5, 7
		vs Output power	2, 4, 6, 8
	Supply ripple rejection ratio	vs Frequency	9, 10
V_n	Output noise voltage	vs Frequency	11, 12
	Crosstalk	vs Frequency	13, 14, 15, 16
	Shutdown attenuation	vs Frequency	17, 18
	Output power	vs Load resistance	19
SNR	Signal-to-noise ratio	vs Voltage gain	20



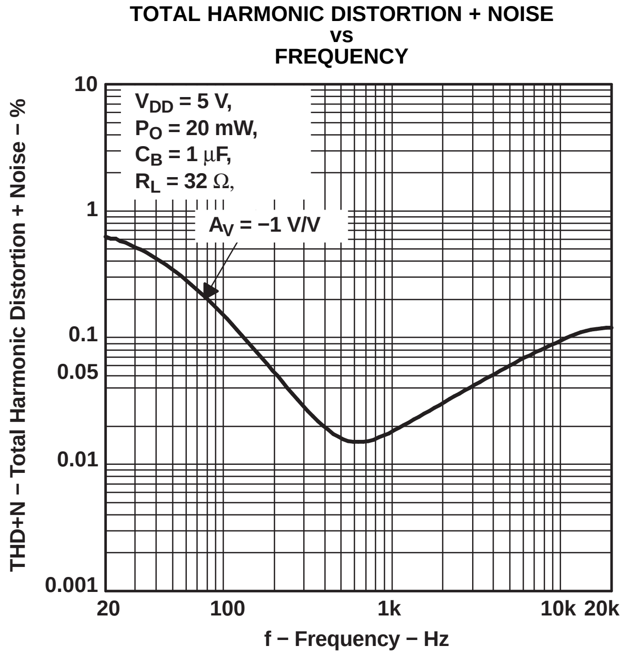
TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

Figure 1.



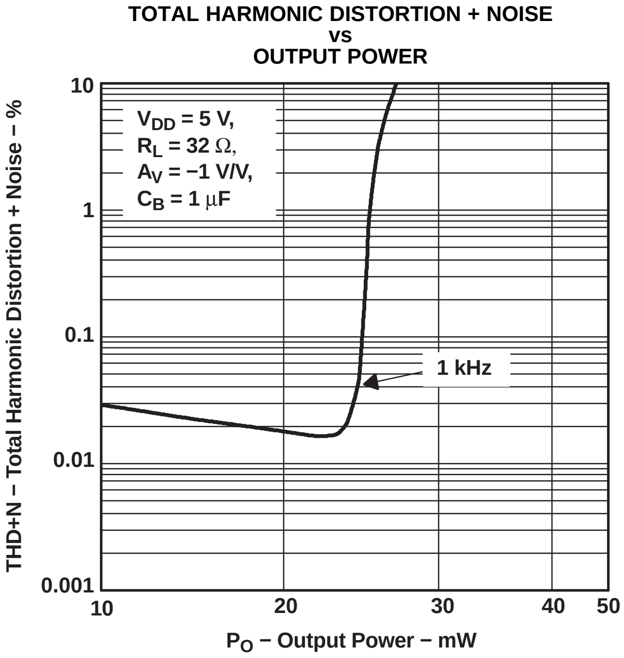
TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

Figure 2.



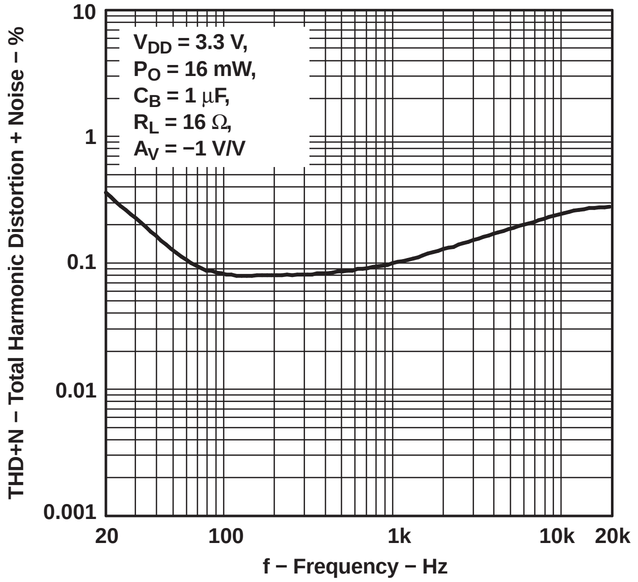
TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

Figure 3.



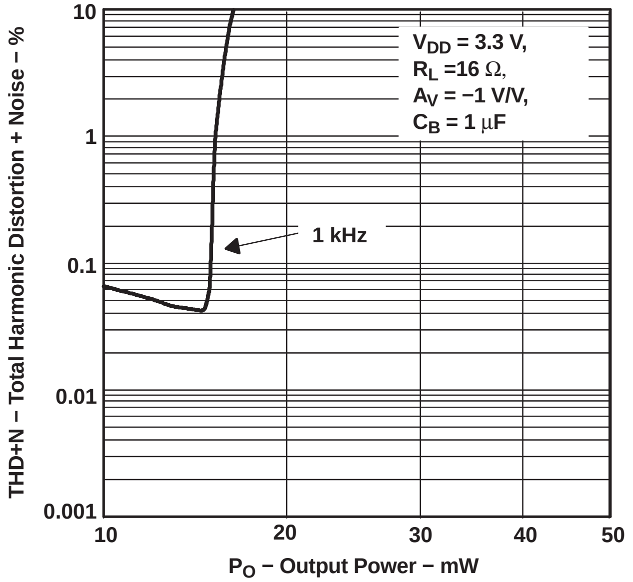
TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

Figure 4.



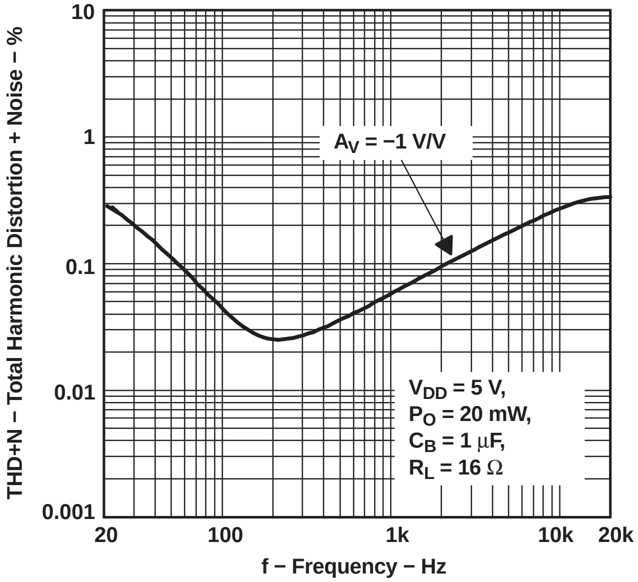
TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

Figure 5.



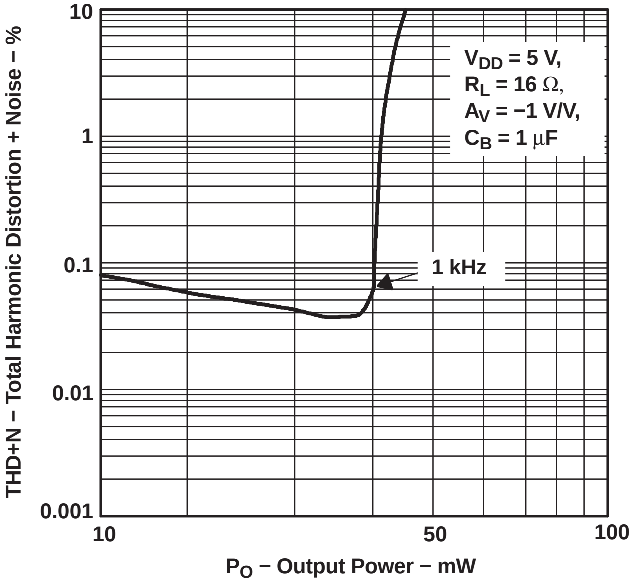
TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

Figure 6.



TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

Figure 7.



TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

Figure 8.

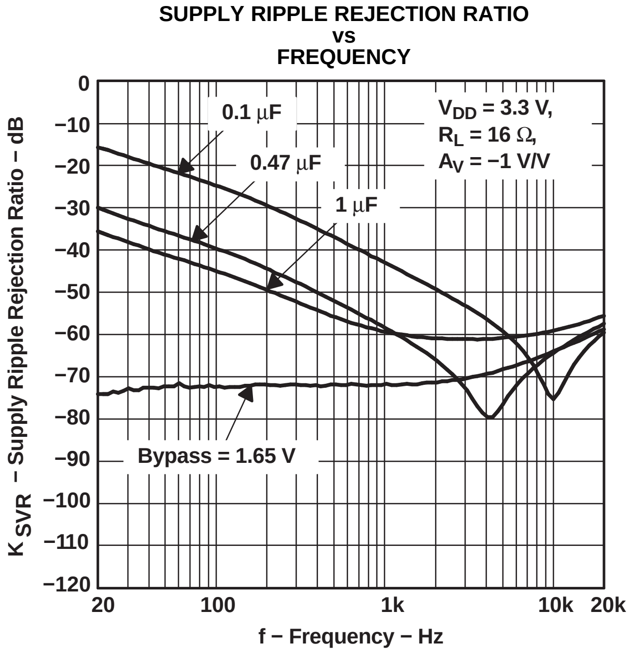

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

Figure 9.

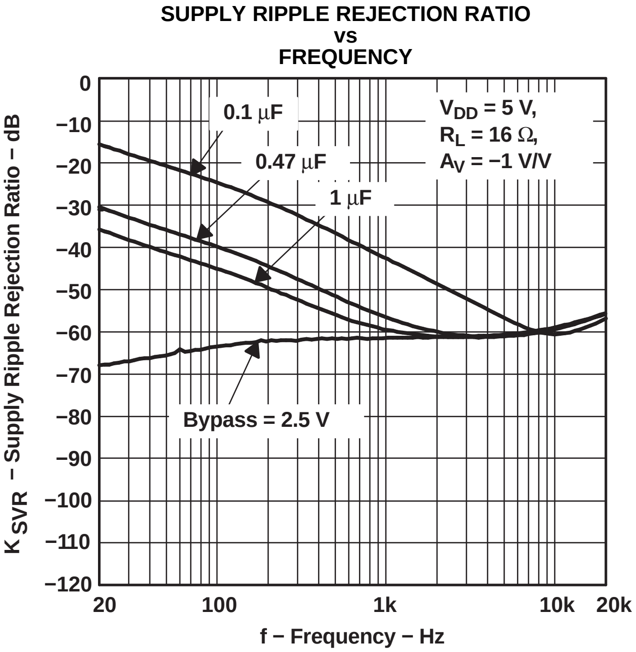

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

Figure 10.

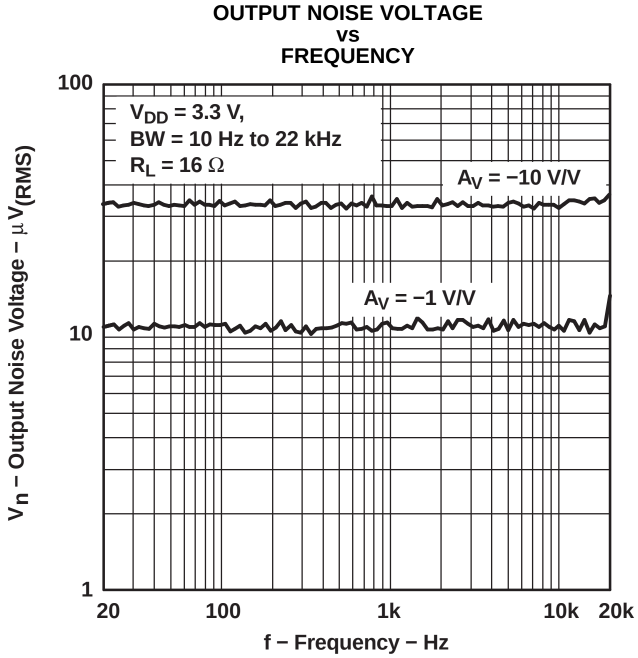

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

Figure 11.

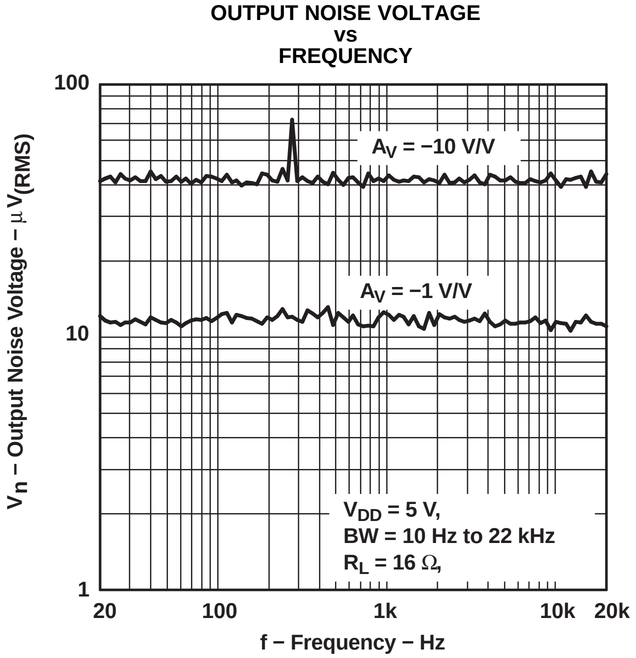

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

Figure 12.

CROSSTALK
vs
FREQUENCY

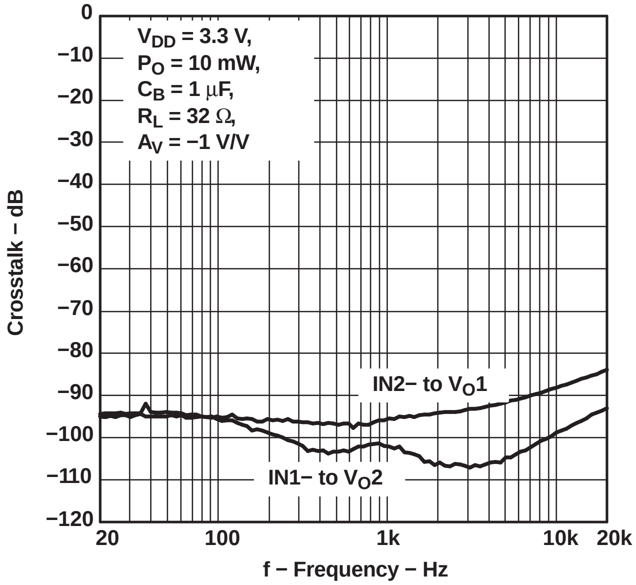


Figure 13.

CROSSTALK
vs
FREQUENCY

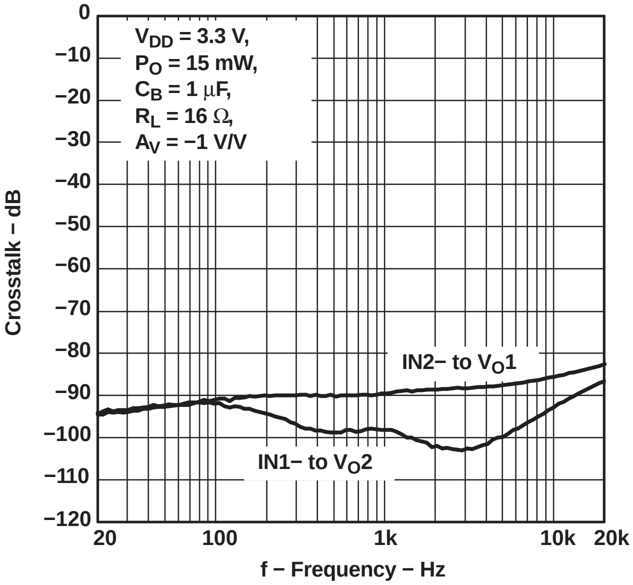


Figure 14.

CROSSTALK
vs
FREQUENCY

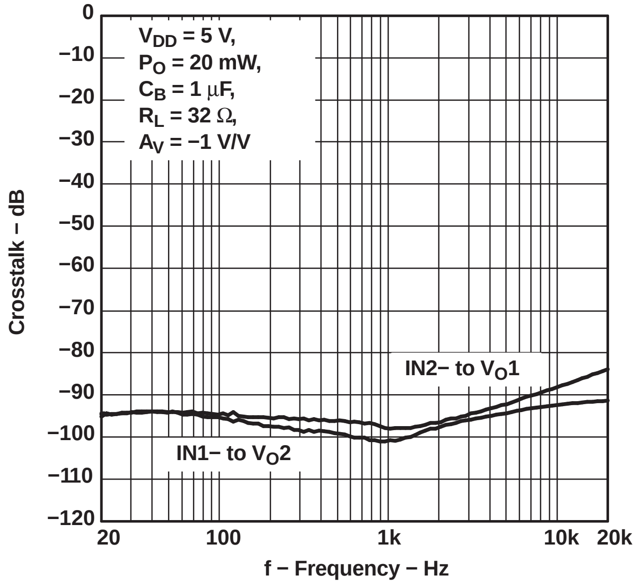


Figure 15.

CROSSTALK
vs
FREQUENCY

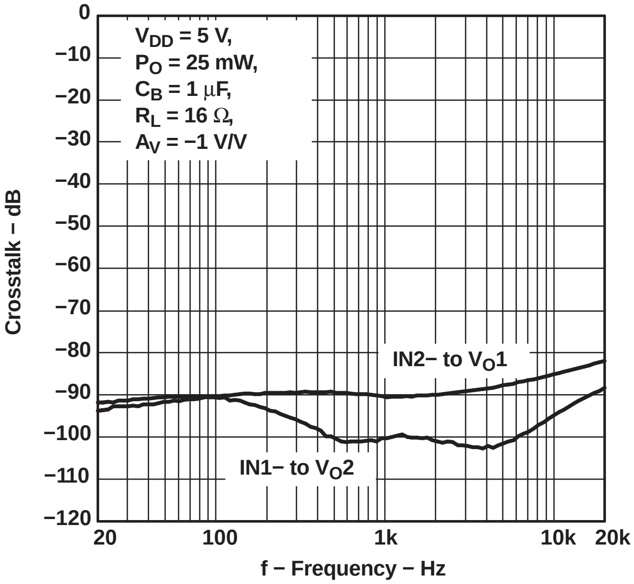


Figure 16.

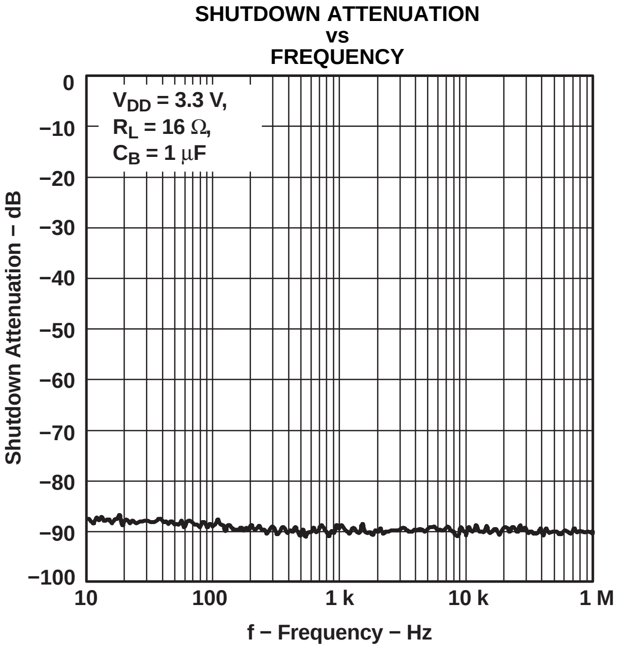


Figure 17.

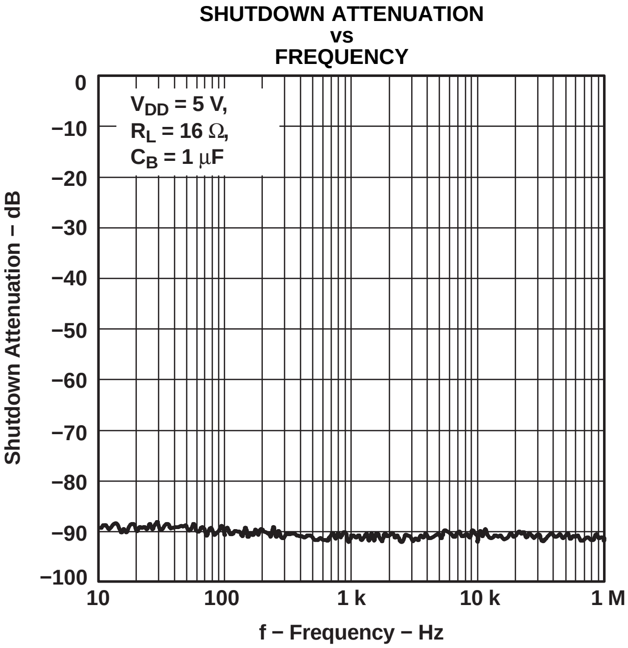


Figure 18.

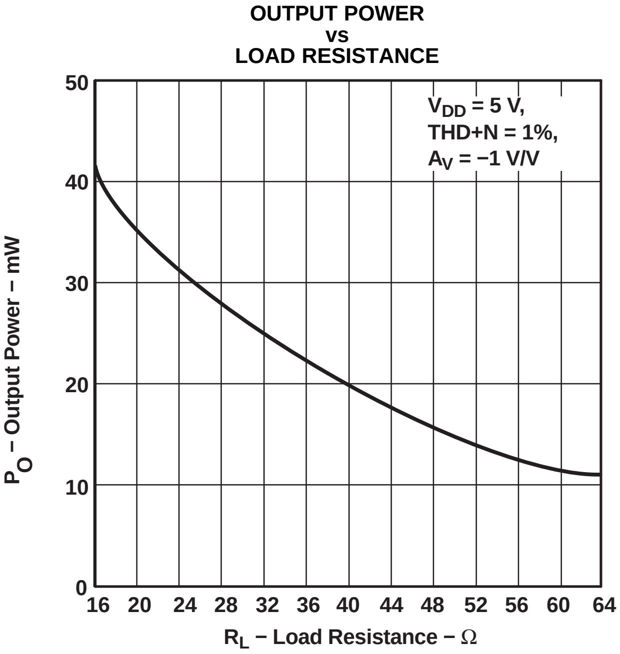


Figure 19.

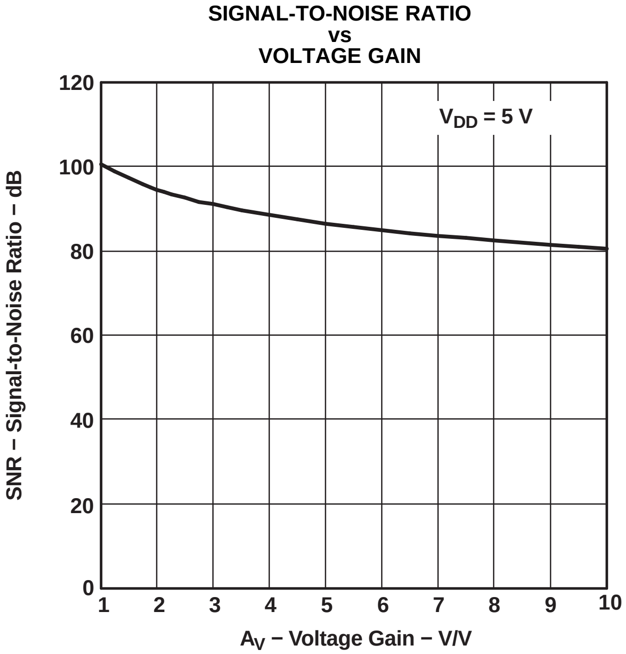


Figure 20.

APPLICATION INFORMATION

GAIN SETTING RESISTORS, R_F and R_i

The gain for the TPA6113A2 is set by resistors R_F and R_I according to Equation 1.

$$\text{Gain} = -\left(\frac{R_F}{R_I}\right) \tag{1}$$

Given that the TPA6113A2 is a MOS amplifier, the input impedance is high. Consequently, input leakage currents are not generally a concern, although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values is required for proper start-up operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in Equation 2.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \tag{2}$$

As an example, consider an input resistance of 20 kΩ and a feedback resistor of 20 kΩ. The gain of the amplifier would be –1 and the effective impedance at the inverting terminal would be 10 kΩ, which is within the recommended range.

For high-performance applications, metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ, the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F. In effect, this creates a low-pass filter network with the cutoff frequency defined in Equation 3.

$$f_{c(\text{lowpass})} = \frac{1}{2\pi R_F C_F} \tag{3}$$

For example, if R_F is 100 kΩ and C_F is 5 pF, then $f_{c(\text{lowpass})}$ is 318 kHz, which is well outside the audio range.

INPUT CAPACITOR, C_i

In the typical application, input capacitor C_I is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and R_I form a high-pass filter with the corner frequency determined in Equation 4.

$$f_{c(\text{highpass})} = \frac{1}{2\pi R_I C_I} \tag{4}$$

The value of C_I is important to consider, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where R_I is 20 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 4 is reconfigured as Equation 5.

$$C_I = \frac{1}{2\pi R_I f_{c(\text{highpass})}} \tag{5}$$

In this example, C_I is 0.40 μF, so one would likely choose a value in the range of 0.47 μF to 1 μF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications (> 10). For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

POWER SUPPLY DECOUPLING, $C_{(S)}$

The TPA6113A2 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF, placed as close as possible to the device V_{DD} lead, works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the power amplifier is recommended.

MIDRAIL BYPASS CAPACITOR, $C_{(BYP)}$

The midrail bypass capacitor, $C_{(BYP)}$, serves several important functions. During start-up, $C_{(BYP)}$ determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so low it cannot be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 230-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in Equation 6 should be maintained.

$$\frac{1}{\left(C_{(BYP)} \times 230\ \text{k}\Omega\right)} \le \frac{1}{\left(C_I R_I\right)} \qquad (6)$$

As an example, consider a circuit where $C_{(BYP)}$ is 1 µF, C_I is 1 µF, and R_I is 20 kΩ. Inserting these values into Equation 6 results in: 6.25 ≤ 50 which satisfies the rule. Recommended values for bypass capacitor $C_{(BYP)}$ are 0.1 µF to 1 µF, ceramic or tantalum low-ESR, for the best THD and noise performance.

OUTPUT COUPLING CAPACITOR, $C_{(C)}$

In the typical single-supply single-ended (SE) configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by Equation 7.

$$f_C = \frac{1}{2\pi R_L C_{(C)}} \qquad (7)$$

The main disadvantage, from a performance standpoint, is that the typically small load impedances drive the low-frequency corner higher. Large values of $C_{(C)}$ are required to pass low frequencies into the load. Consider the example where a $C_{(C)}$ of 68 F is chosen and loads vary from 32 Ω to 47 kΩ. Table 1 summarizes the frequency response characteristics of each configuration.

Table 1. Common Load Impedances vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	LOWEST FREQUENCY
32 Ω	68 µF	73 Hz
10,000 Ω	68 µF	0.23 Hz
47,000 Ω	68 µF	0.05 Hz

As Table 1 indicates, headphone response is adequate and drive into line level inputs (a home stereo for example) is good.

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. With the rules described earlier still valid, add the following relationship:

$$\frac{1}{\left(C_{(BYP)} \times 230\ k\Omega\right)} \leq \frac{1}{\left(C_I R_I\right)} \ll \frac{1}{R_L C_{(C)}} \tag{8}$$

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this application. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

5-V VERSUS 3.3-V OPERATION

The TPA6113A2 was designed for operation over a supply range of 2.5 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation, since these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation as far as supply bypassing, gain setting, or stability. The most important consideration is that of output power. Each amplifier in the TPA6113A2 can produce a maximum voltage swing of V_{DD} – 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V as opposed when $V_{O(PP)}$ = 4 V while operating at 5 V. The reduced voltage swing subsequently reduces maximum output power into the load before distortion begins to become significant.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA6113A2DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		6113A2	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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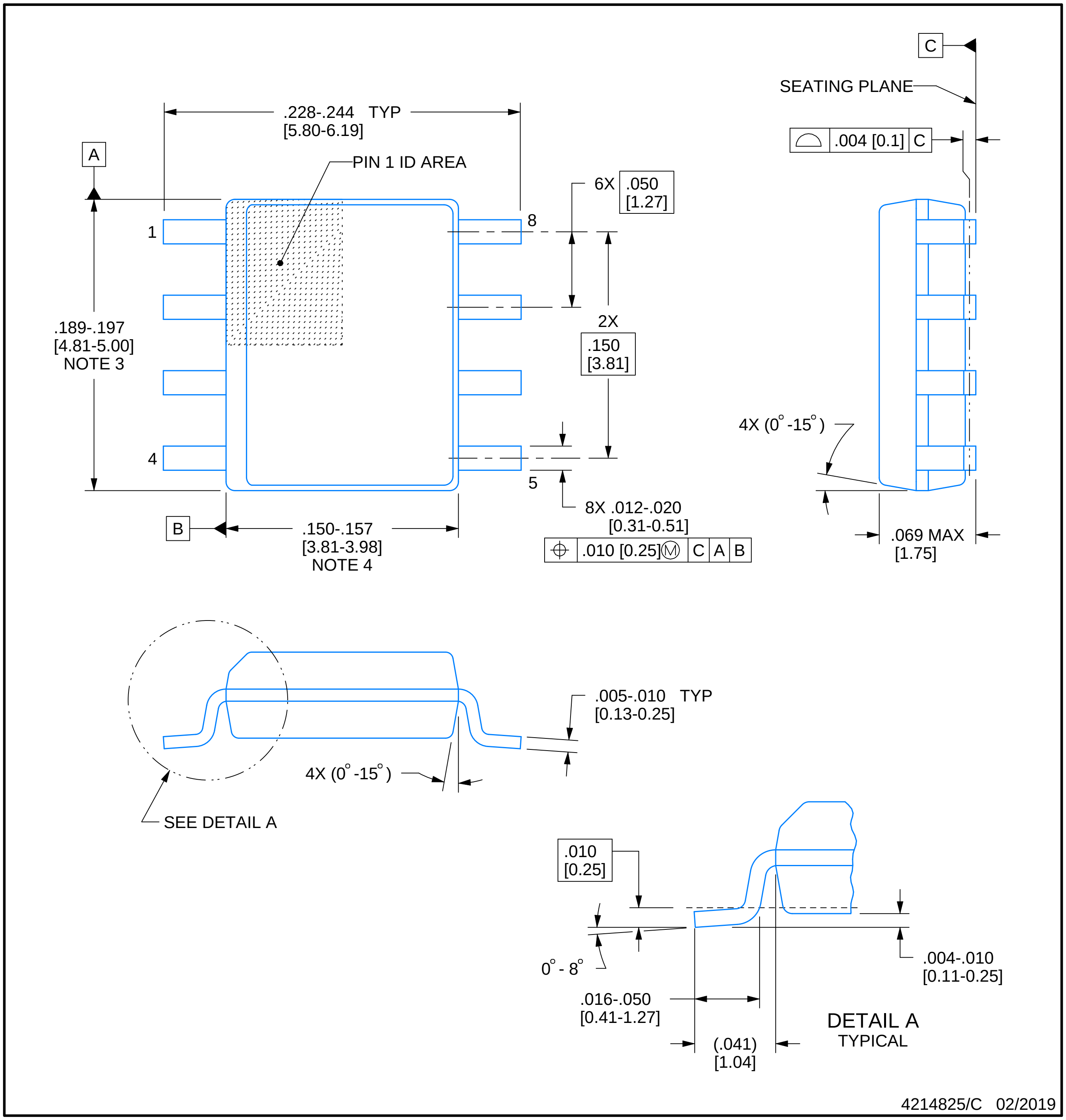
D0008A

PACKAGE OUTLINE

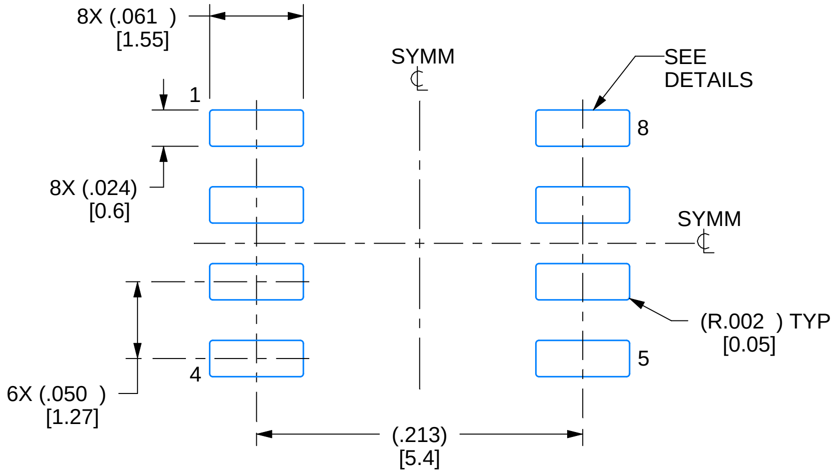
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

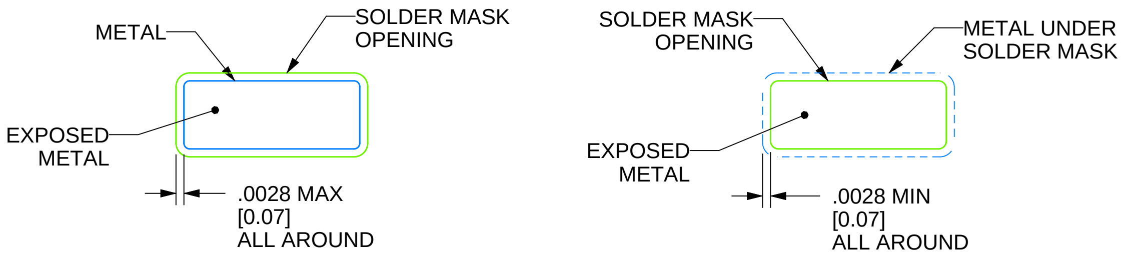


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



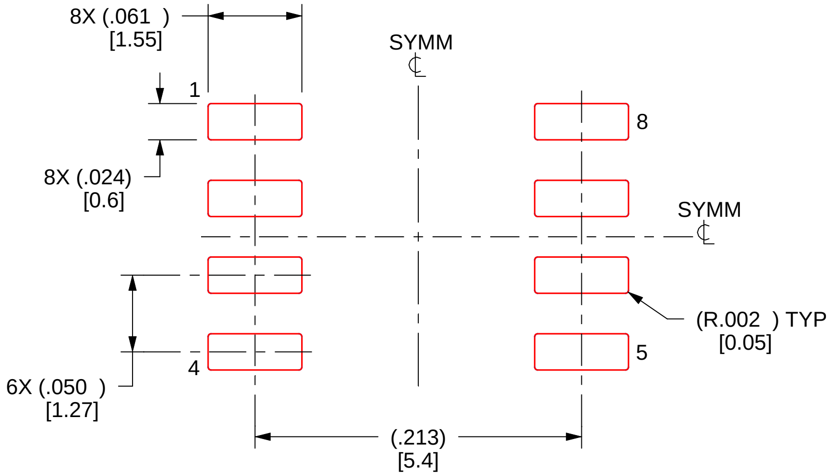
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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