THE DATASHEET OF

TMP275AIDGKR

TMP275 ±0.5°C Temperature Sensor With I^2C and SMBus Interface in Industry Standard LM75 Form Factor and Pinout

1 Features

- High Accuracy:
  - ±0.5°C (Maximum) From −20°C to 100°C
  - ±1°C (Maximum) From −40°C to 125°C
- Low Quiescent Current:
  - 50 µA (Typical)
  - 0.1-µA Standby
- Resolution: 9 to 12 Bits, User-Selectable
- Digital Output: SMBus™, Two-Wire, and I^2C Interface Compatibility
- 8 I^2C/SMBus Addresses
- Wide Supply Range: 2.7 V to 5.5 V
- Small VSSOP-8 and SOIC-8 Packages
- No Specified Power-up Sequence Required; Two-Wire Bus Pullups May Be Enabled Before V+

2 Applications

- Power-Supply Temperature Monitoring
- Computer Peripheral Thermal Protection
- Battery Management
- Office Machines
- Servers
- Thermostat Controls
- Environmental Monitoring and HVAC
- Electromechanical Device Temperature
- Data Logger

3 Description

The TMP275 is a ±0.5°C accurate integrated digital temperature sensor with a 12-bit analog-to-digital converter (ADC) that can operate as low as 2.7-V supply voltage and is pin- and register-compatible with the Texas Instruments LM75, TMP75, TMP75B, and TMP175 devices. This device is available in SOIC-8 and VSSOP-8 packages, and it requires no external components to sense the temperature. The TMP275 is capable of reading temperatures with a maximum resolution of 0.0625°C (12 bits) and as low as 0.5°C (9 bits), which allows the user to maximize efficiency by programming for higher resolution or faster conversion time. The device is specified over a temperature range of –40°C to 125°C.

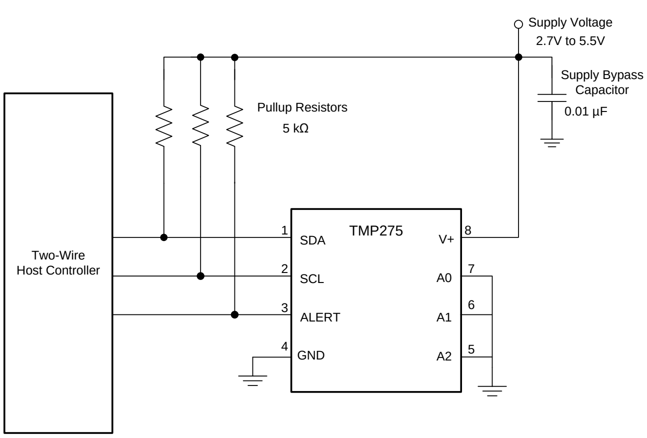
The TMP275 device features SMBus and two-wire interface compatibility, and allows up to eight devices on the same bus with the SMBus overtemperature alert function. The factory-calibrated temperature accuracy and the noise-immune digital interface make the TMP275 the preferred solution for temperature compensation of other sensors and electronic components, without the need for additional system-level calibration or elaborate board layout for distributed temperature sensing.

Device Information(1)

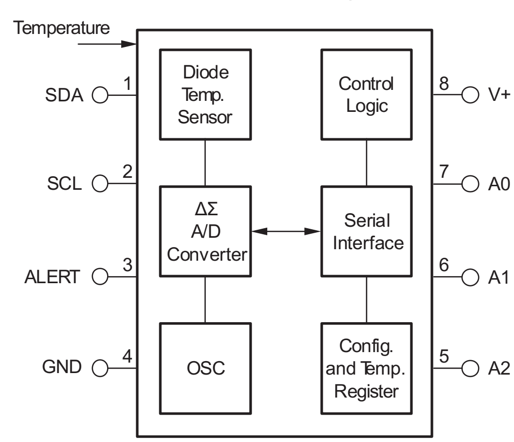
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMP275	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Simplified Schematic



Internal Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (November 2015) to Revision F — **Page**

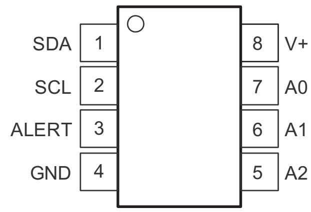
- Added repeatability parameter to the *Electrical Characteristics* table 5
- Added long-term drift parameter to the *Electrical Characteristics* table 5

Changes from Revision D (August 2007) to Revision E — **Page**

- Added *Handling Rating* table, *Feature Description* section, *Device Functional* Modes, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Changed the Timing Requirements table with new I^{2}C data. Updated affected values throughout the data sheet 6

5 Pin Configuration and Functions

D and DGK Packages
8-Pin SOIC and 8-Pin VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SDA	I/O	Serail data. Open-drain output; requires a pullup resistor.
2	SCL	I	Serial clock. Open-drain output; requires a pullup resistor.
3	ALERT	O	Overtemperature alert. Open-drain output; requires a pullup resistor.
4	GND	—	Ground
5	A2	I	Address select. Connect to GND or V+.
6	A1	I	Address select. Connect to GND or V+.
7	A0	I	Address select. Connect to GND or V+.
8	V+	I	Supply voltage, 2.7 to 5.5 V

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Power supply, V+		7	V
Input voltage(2)	–0.5	7	V
Input current		10	mA
Operating temperature	–55	127	°C
Junction temperature, T_J max,		150	°C
Storage temperature, T_{stg}	–60	130	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	
		Machine Model (MM)	±300	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage	2.7		5.5	V
Operating free-air temperature, T_A	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TMP275 D (SOIC) AND DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	59.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at T_A = −40°C to +125°C, and V+ = 2.7 V to 5.5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE INPUT					
Range		–40		125	°C
Accuracy (Temperature Error)	–20°C to 100°C, V+ = 3.3 V		±0.0625	±0.5	°C
	0°C to 100°C, V+ = 3 V to 3.6 V		±0.0625	±0.75	°C
	–40°C to 125°C, V+ = 3 V to 3.6 V		±0.0625	±1	°C
	25°C to 100°C, V+ = 3.3 V to 5.5 V		0.2	±1.5	°C
Resolution (1)	Selectable		0.0625		°C
Repeatability (2)	25°C, V+= 3.3 V (3)		±0.0625		°C
Long-term drift (4)	500 hours at 150°C		±0.0625		°C
DIGITAL INPUT/OUTPUT					
Input Capacitance			3		pF
Input logic level, HIGH, V_{IH}		0.7(V+)		6	V
Input logic level, LOW, V_{IL}		−0.5		0.3(V+)	V
Leakage Input Current, I_{IN}	0 V ≤ V_{IN} ≤ 6 V			1	µA
Input Voltage Hysteresis	SCL and SDA pins		500		mV
SDA Output logic level, LOW, V_{OL}	I_{OL} = 3 mA	0	0.15	0.4	V
ALERT Output logic level, HIGH, V_{OL}	I_{OL} = 4 mA	0	0.15	0.4	V
Resolution	Selectable		9 to 12		Bits
Coversion Time	9-Bit		27.5	37.5	ms
	10-Bit		55	75	ms
	11-Bit		110	150	ms
	12-Bit		220	300	ms
Time-out time		25	54	74	ms
POWER SUPPLY					
Operating range		2.7		5.5	V
Quiescent Current, I_Q	Serial bus inactive		50	85	µA
	Serial bus active, SCL freq = 400 kHz		100		µA
	Serial bus active, SCL freq = 3.4 MHz		410		µA
Shutdown Current, I_{SD}	Serial bus inactive		0.1	3	µA
	Serial bus active, SCL freq = 400 kHz		60		µA
	Serial bus active, SCL freq = 3.4 MHz		380		µA
TEMPERATURE RANGE					
Specified Range		–40		125	°C
Operating Range		–55		127	°C

(1) Specified for 12-bit resolution.
(2) Repeatability is the ability to reproduce a reading when the measured temperature is applied consecutively, under the same conditions.
(3) One-shot mode setup, 1 sample per minute for 24 hours.
(4) Long-term drift is determined using accelerated operational life testing at a junction temperature of 150°C.

6.6 Timing Requirements

See the *Timing Diagrams* section for timing diagrams.(1)

			FAST MODE		HIGH-SPEED MODE		UNIT
			MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency	V+	0.001	0.4	0.001	2.38	MHz
$t_{(BUF)}$	Bus-free time between STOP and START condition	See *Timing Diagrams*	1300		160		ns
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.	See *Timing Diagrams*	600		160		ns
$t_{(SUSTA)}$	Repeated start condition setup time	See *Timing Diagrams*	600		160		ns
$t_{(SUSTO)}$	STOP condition setup time	See *Timing Diagrams*	600		160		ns
$t_{(HDDAT)}$	Data hold time	See *Timing Diagrams*	4	900	4	120	ns
$t_{(SUDAT)}$	Data setup time	See *Timing Diagrams*	100		10		ns
$t_{(LOW)}$	SCL-clock low period	V+ , see *Timing Diagrams*	1300		280		ns
$t_{(HIGH)}$	SCL-clock high period	See *Timing Diagrams*	600		60		ns
t_FD	Data fall time	See *Timing Diagrams*		300		150	ns
t_RC	Clock rise time	See *Timing Diagrams*		300		40	ns
		SCLK ≤ 100 kHz, See *Timing Diagrams*		1000			ns
t_FC	Clock fall time	See *Timing Diagrams*		300		40	ns

(1) Values based on a statistical analysis of a one-time sample of devices. Minimum and maximum values are not specified and not production tested.

6.7 Typical Characteristics

at T_A = 25°C and V+ = 5 V (unless otherwise noted)

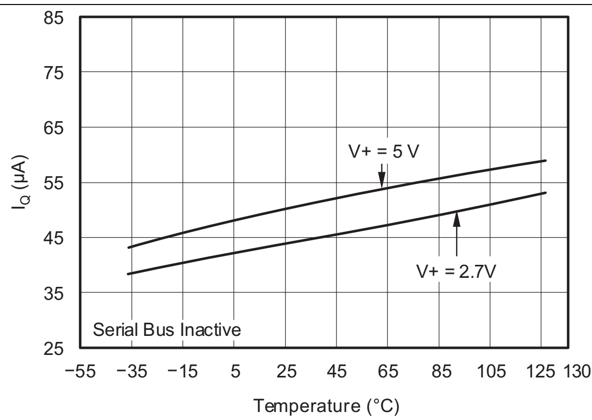


Figure 1. Quiescent Current vs Temperature

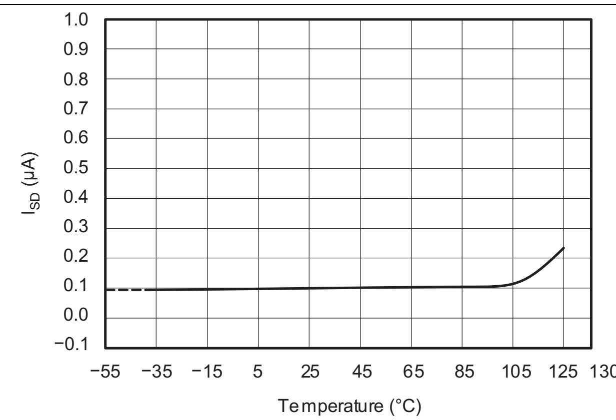


Figure 2. Shutdown Current vs Temperature

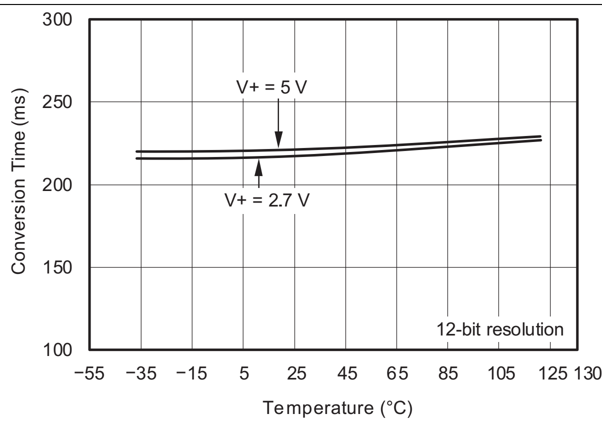


Figure 3. Conversion Time vs Temperature

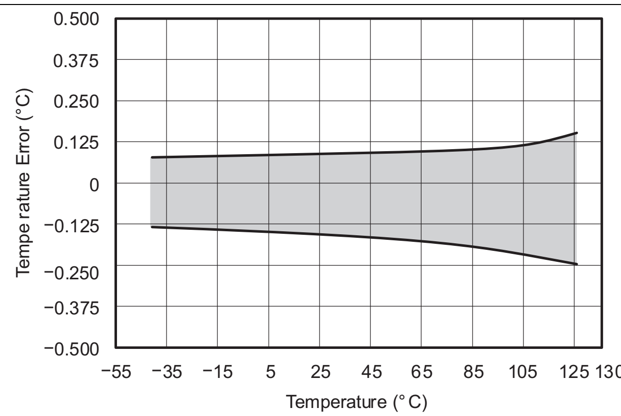


Figure 4. Temperature Error vs Temperature

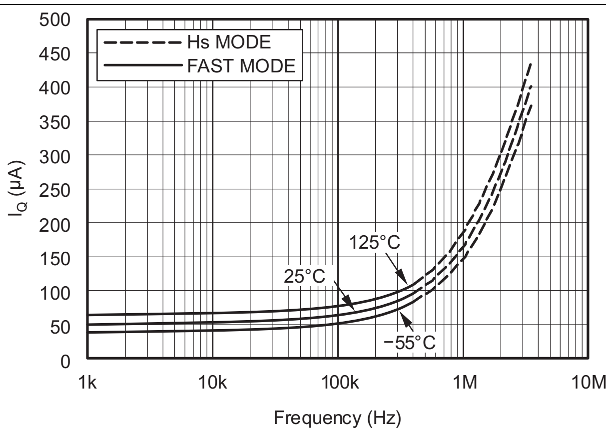


Figure 5. Quiescent Current with Bus Activity vs Temperature

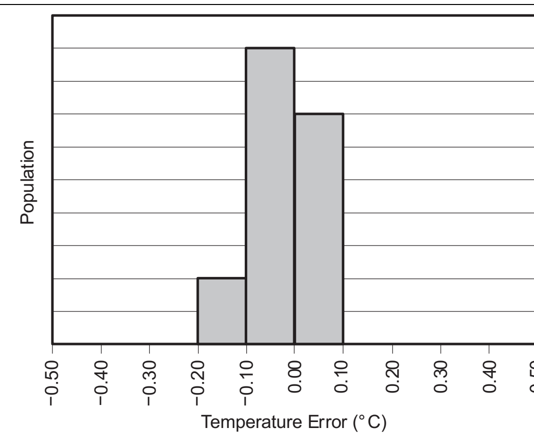


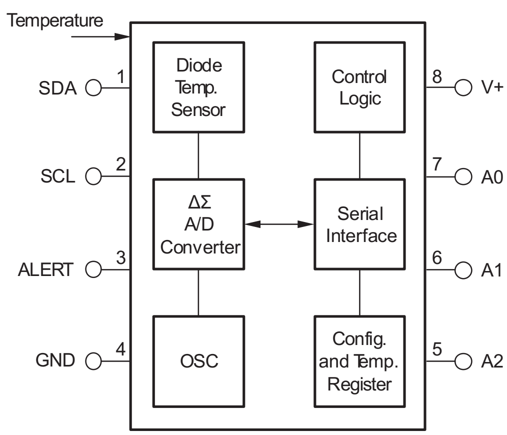
Figure 6. Temperature Error at 25°C

7 Detailed Description

7.1 Overview

The TMP275 is a digital temperature sensor that is optimal for thermal management and thermal protection applications. The TMP275 is Two-Wire, SMBus, and I^{2}C interface-compatible, and is specified over a temperature range of −40°C to 125°C. The temperature sensor in the TMP275 is the chip itself. Thermal paths run through the package leads as well as the plastic package. The package leads provide the primary thermal path because of the lower thermal resistance of the metal. See *Functional Block Diagram* for the internal block diagram of TMP275 device.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Digital Temperature Output

The temperature register of the TMP275 is a 12-bit, read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data, and are described in Figure 13 and Figure 14. Note that byte 1 is the most significant byte, followed by byte 2, the least significant byte. The first 12 bits are used to indicate temperature, with all remaining bits equal to zero. The least significant byte does not have to be read if that information is not needed. Data format for temperature is summarized in Table 1. Following power up or reset, the Temperature Register reads 0°C until the first conversion is complete. The user can obtain 9, 10, 11, or 12 bits of resolution by addressing the Configuration Register and setting the resolution bits accordingly. For 9-, 10-, or 11-bit resolution, the most significant bits in the Temperature Register are used with the unused LSBs set to zero

Table 1. Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
128	0111 1111 1111	7FF
127.9375	0111 1111 1111	7FF
100	0110 0100 0000	640
80	0101 0000 0000	500
75	0100 1011 0000	4B0
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0	0000 0000 0000	000
–0.25	1111 1111 1100	FFC
–25	1110 0111 0000	E70
–55	1100 1001 0000	C90

7.3.2 Serial Interface

The TMP275 operates only as slave devices on the SMBus, Two-Wire, and I^2C interface-compatible bus. Connections to the bus are made through the open-drain I/O lines SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP275 supports the transmission protocol for fast (up to 400 kHz) and high-speed (up to 2.38 MHz) modes. All data bytes are transmitted MSB first.

7.3.3 Bus Overview

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated, indicated by pulling the data-line (SDA) from a HIGH to LOW logic level while SCL is HIGH. All slaves on the bus shift in the slave address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA LOW.

Data transfer is then initiated and sent over eight clock pulses followed by an Acknowledge Bit. During data transfer SDA must remain stable while SCL is HIGH, as any change in SDA while SCL is HIGH will be interpreted as a control signal.

Once all data has been transferred, the master generates a STOP condition indicated by pulling SDA from LOW to HIGH, while SCL is HIGH.

7.3.4 Serial Bus Address

To communicate with the TMP275, the master must first address slave devices through a slave address byte. The slave address byte consists of 7 address bits, and a direction bit indicating the intent of executing a read or write operation.

The TMP275 features three address pins, allowing up to eight devices to be connected per bus. Pin logic levels are described in Table 2. The address pins of the TMP275 are read after reset, at start of communication, or in response to a Two-Wire address acquire request. Following reading the state of the pins the address is latched to minimize power dissipation associated with detection.

Table 2. Address Pins and Slave Addresses for the TMP275

A2	A1	A0	SLAVE ADDRESS
0	0	0	1001000
0	0	1	1001001
0	1	0	1001010
0	1	1	1001011
1	0	0	1001100
1	0	1	1001101
1	1	0	1001110
1	1	1	1001111

7.3.4.1 Writing and Reading to the TMP275

Accessing a particular register on the TMP275 is accomplished by writing the appropriate value to the Pointer Register. The value for the Pointer Register is the first byte transferred after the slave address byte with the R/W bit LOW. Every write operation to the TMP275 requires a value for the Pointer Register (see Figure 8).

When reading from the TMP275, the last value stored in the Pointer Register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the Pointer Register. This is accomplished by issuing a slave address byte with the R/W bit LOW, followed by the Pointer Register Byte. No additional data is required. The master can then generate a START condition and send the slave address byte with the R/W bit HIGH to initiate the read command. See Figure 9 for details of this sequence. If repeated reads from the same register are desired, it is not necessary to continually send the Pointer Register bytes, as the TMP275 remembers the Pointer Register value until it is changed by the next write operation.

Note that register bytes are sent most-significant byte first, followed by the least significant byte.

7.3.4.2 Slave Mode Operations

The TMP275 can operate as a slave receiver or slave transmitter.

7.3.4.2.1 Slave Receiver Mode

The first byte transmitted by the master is the slave address, with the R/$\overline{W}$ bit LOW. The TMP275 then acknowledges reception of a valid address. The next byte transmitted by the master is the Pointer Register. The TMP275 then acknowledges reception of the Pointer Register byte. The next byte or bytes are written to the register addressed by the Pointer Register. The TMP275 acknowledges reception of each data byte. The master may terminate data transfer by generating a START or STOP condition.

7.3.4.2.2 Slave Transmitter Mode

The first byte is transmitted by the master and is the slave address, with the R/$\overline{W}$ bit HIGH. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the Pointer Register. The master acknowledges reception of the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges reception of the data byte. The master may terminate data transfer by generating a Not-Acknowledge on reception of any data byte, or generating a START or STOP condition.

7.3.4.3 SMBus Alert Function

The TMP275 supports the SMBus Alert function. When the TMP275 is operating in Interrupt Mode (TM = 1), the ALERT pin of the TMP275 may be connected as an SMBus Alert signal. When a master senses that an ALERT condition is present on the ALERT line, the master sends an SMBus Alert command (00011001) on the bus. If the ALERT pin of the TMP275 is active, the device acknowledges the SMBus Alert command and responds by returning its slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates if the temperature exceeding T_{HIGH} or falling below T_{LOW} caused the ALERT condition. This bit will be HIGH if the temperature is greater than or equal to T_{HIGH}. This bit will be LOW if the temperature is less than T_{LOW}. Refer to Figure 10 for details of this sequence.

If multiple devices on the bus respond to the SMBus Alert command, arbitration during the slave address portion of the SMBus Alert command determines which device clears its ALERT status. If the TMP275 wins the arbitration, its ALERT pin becomes inactive at the completion of the SMBus Alert command. If the TMP275 loses the arbitration, its ALERT pin remains active.

7.3.4.4 General Call

The TMP275 responds to a Two-Wire General Call address (0000000) if the eighth bit is 0. The device acknowledges the General Call address and responds to commands in the second byte. If the second byte is 00000100, the TMP275 latches the status of their address pins, but will not reset. If the second byte is 00000110, the TMP275 latches the status of their address pins and reset their internal registers to their power-up values.

7.3.4.5 High-Speed Mode

For the Two-Wire bus to operate at frequencies above 400 kHz, the master device must issue an Hs-mode master code (00001XXX) as the first byte after a START condition to switch the bus to high-speed operation. The TMP1275 device will not acknowledge this byte, but will switch their input filters on SDA and SCL and their output filters on SDA to operate in Hs-mode, allowing transfers at up to 2.38 MHz. After the Hs-mode master code has been issued, the master will transmit a Two-Wire slave address to initiate a data transfer operation. The bus will continue to operate in Hs-mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the TMP275 switches the input and output filter back to fast-mode operation.

7.3.4.6 Time-Out Function

The TMP275 resets the serial interface if either SCL or SDA is held LOW for 54 ms (typical) between a START and STOP condition. The TMP275 releases the bus if it is pulled LOW and waits for a START condition. To avoid activating the time-out function, it is necessary to maintain a communication speed of at least 1 kHz for SCL operating frequency.

7.3.5 Timing Diagrams

The TMP275 is Two-Wire, SMBUs, and I^2C interface-compatible. Figure 7 to Figure 10 describe the various operations on the TMP275. Bus definitions are given below. Parameters for Figure 7 are defined in *Timing Requirements*.

Bus Idle: Both SDA and SCL lines remain HIGH.

Start Data Transfer: A change in the state of the SDA line, from HIGH to LOW, while the SCL line is HIGH, defines a START condition. Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from LOW to HIGH while the SCL line is HIGH defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, the termination of the data transfer can be signaled by the master generating a Not-Acknowledge on the last byte that has been transmitted by the slave.

7.3.6 Two-Wire Timing Diagrams

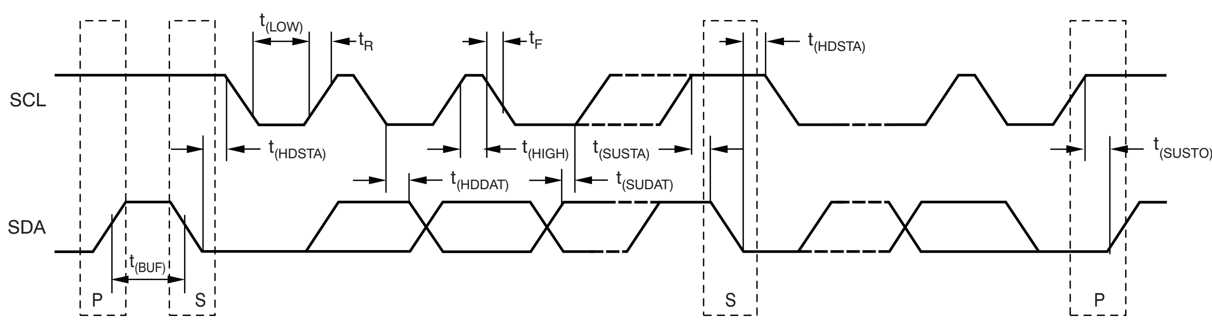


Figure 7. Two-Wire Timing Diagram

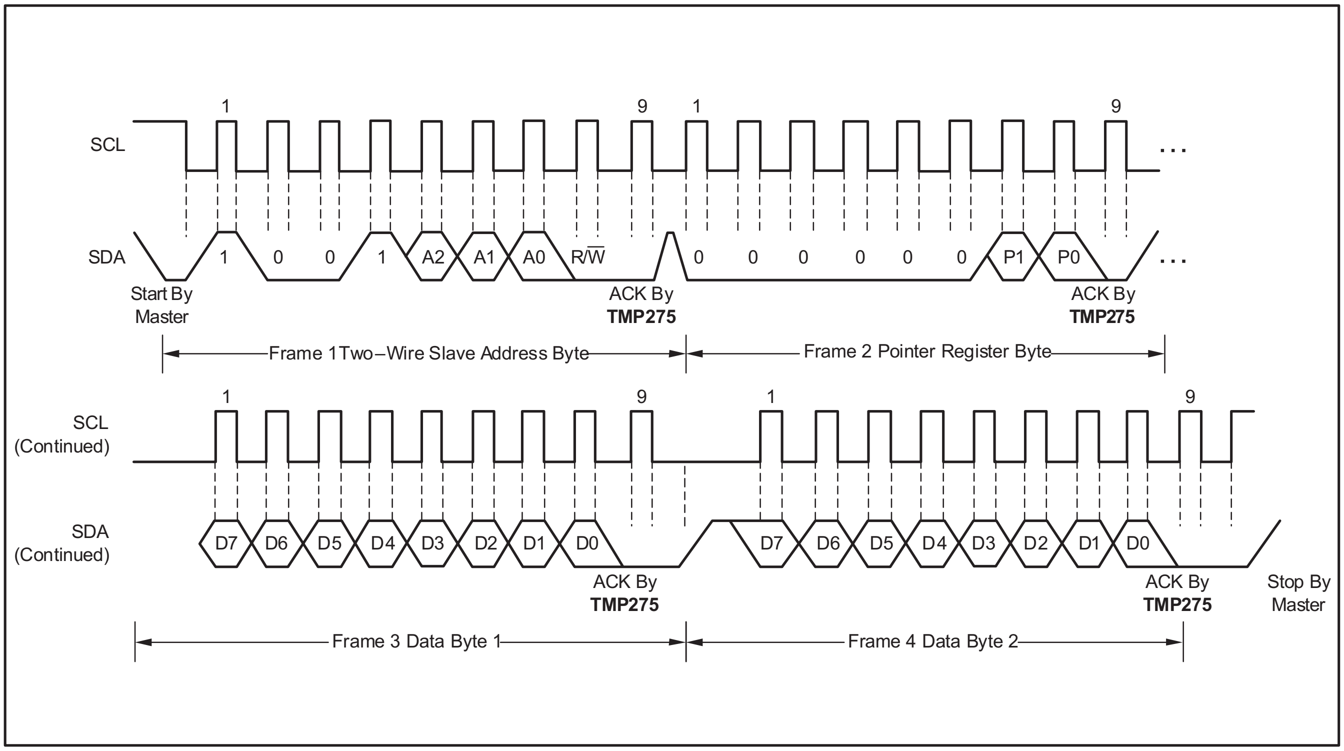


Figure 8. Two-Wire Timing Diagram for TMP275 Write Word Format

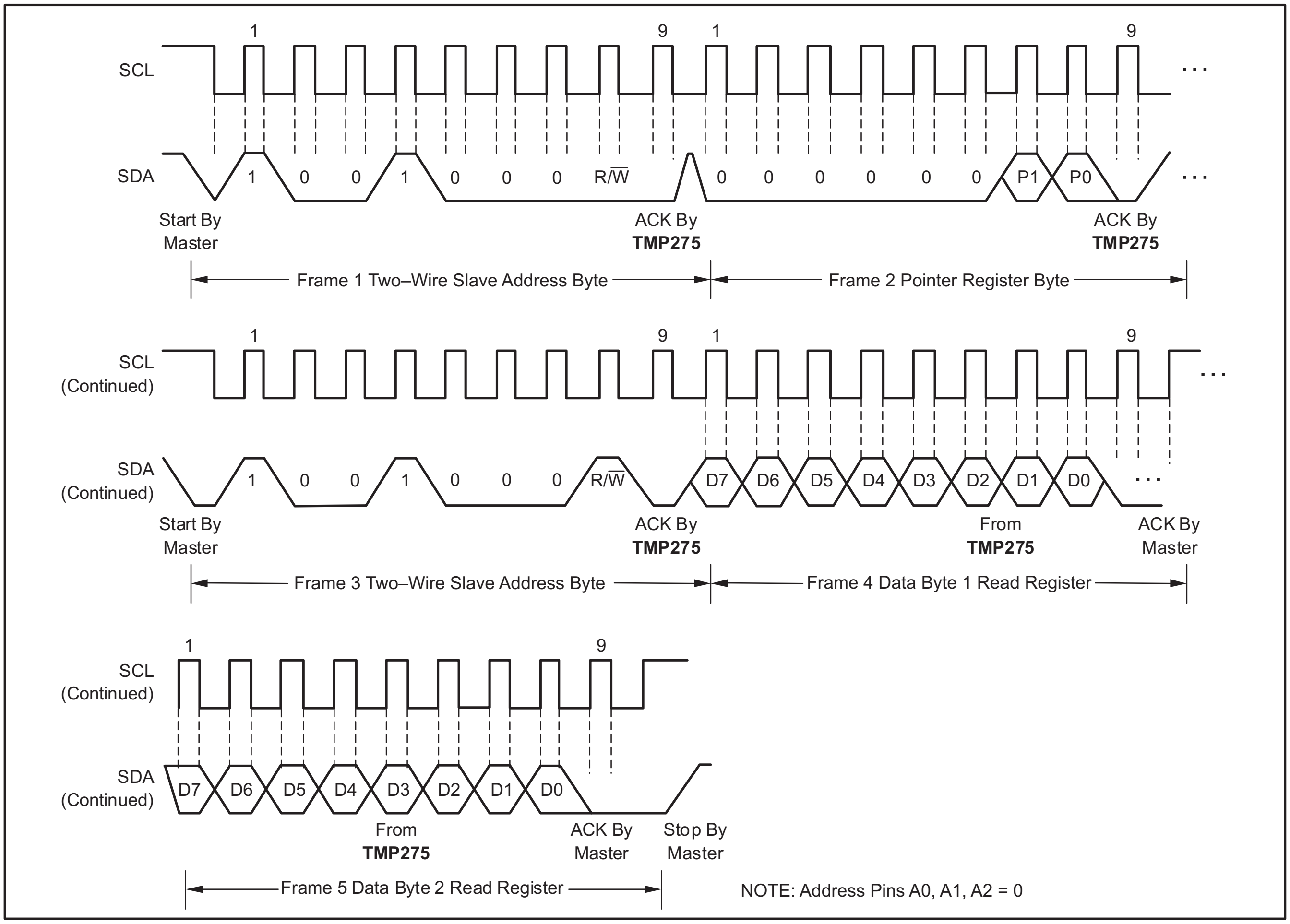


Figure 9. Two-Wire Timing Diagram for Read Word Format

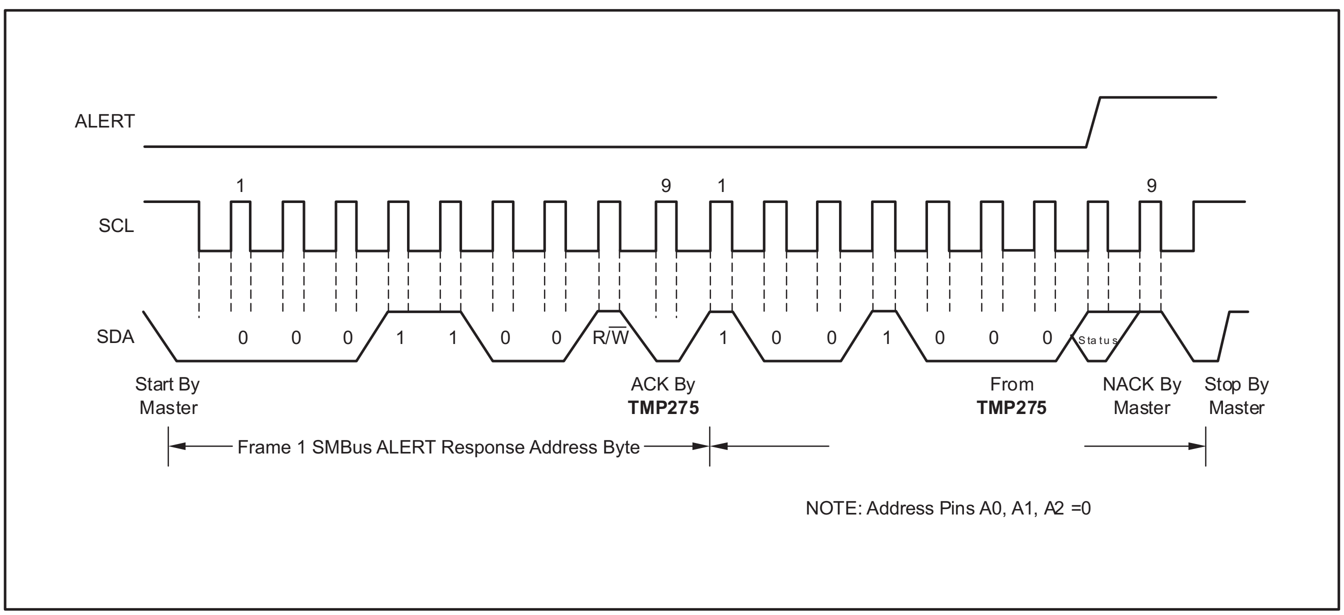


Figure 10. Timing Diagram for SMBus ALERT

7.4 Device Functional Modes

7.4.1 Shutdown Mode (SD)

The Shutdown Mode of the TMP275 allows the user to save maximum power by shutting down all device circuitry other than the serial interface, which reduces current consumption to typically less than 0.1 μA. Shutdown Mode is enabled when the SD bit is 1; the device will shut down once the current conversion is completed. When SD is equal to 0, the device maintains a continuous conversion state.

7.4.2 Thermostat Mode (TM)

The Thermostat Mode bit of the TMP275 indicates to the device whether to operate in Comparator Mode (TM = 0) or Interrupt Mode (TM = 1). For more information on comparator and interrupt modes, see the *High and Low Limit Registers* section.

7.4.2.1 Comparator Mode (TM = 0)

In Comparator mode (TM = 0), the ALERT pin is activated when the temperature equals or exceeds the value in the T(HIGH) register and it remains active until the temperature falls below the value in the T(LOW) register. For more information on the comparator mode, see the *High and Low Limit Registers* section.

7.4.2.2 Interrupt Mode (TM = 1)

In Interrupt mode (TM = 1), the ALERT pin is activated when the temperature exceeds T(HIGH) or goes below T(LOW) registers. The ALERT pin is cleared when the host controller reads the temperature register. For more information on the interrupt mode, see the *High and Low Limit Registers* section.

7.4.3 One-Shot (OS)

The TMP275 features a One-Shot Temperature Measurement Mode. When the device is in Shutdown Mode, writing a '1' to the OS bit starts a single temperature conversion. The device returns to the shutdown state at the completion of the single conversion. This mode is useful for reducing power consumption in the TMP275 when continuous temperature monitoring is not required. When the configuration register is read, the OS always reads zero.

7.5 Programming

7.5.1 Pointer Register

Figure 11 shows the internal register structure of the TMP275. The 8-bit Pointer Register of the devices is used to address a given data register. The Pointer Register uses the two LSBs to identify which of the data registers should respond to a read or write command. Figure 12 identifies the bits of the Pointer Register byte. Table 3 describes the pointer address of the registers available in the TMP275. Power-up reset value of P1/P0 is 00.

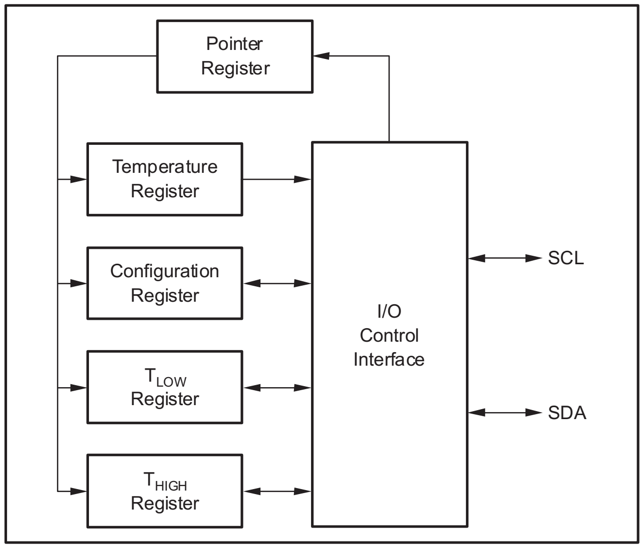


Figure 11. Internal Register Structure of the TMP275

7.5.1.1 Pointer Register Byte (offset = N/A) [reset = 00h]

Figure 12. Pointer Register Byte

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	0	Register Bits	

7.5.1.2 Pointer Addresses of the TMP275

Table 3. Pointer Addresses of the TMP275 Field Description

P1	P0	TYPE	REGISTER
0	0	R only, default	Temperature Register
0	1	R/W	Configuration Register
1	0	R/W	T_{LOW} Register
1	1	R/W	T_{HIGH} Register

7.5.2 Temperature Register

The Temperature Register of the TMP275 is a 12-bit, read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data, and are described in Figure 13 and Figure 14. Note that byte 1 is the most significant byte, followed by byte 2, the least significant byte. The first 12 bits are used to indicate temperature, with all remaining bits equal to zero. The least significant byte does not have to be read if that information is not needed. Data format for temperature is summarized in Table 1. Following power up or reset, the Temperature Register reads 0°C until the first conversion is complete.

Figure 13. Byte 1 of Temperature Register

D7	D6	D5	D4	D3	D2	D1	D0
T11	T10	T9	T8	T7	T6	T5	T4

Figure 14. Byte 2 of Temperature Register

D7	D6	D5	D4	D3	D2	D1	D0
T3	T2	T1	T0	0	0	0	0

7.5.3 Configuration Register

The Configuration Register is an 8-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read/write operations are performed MSB first. The format of the Configuration Register for the TMP275 is shown in Table 4, followed by a breakdown of the register bits. The power-up/reset value of the Configuration Register is all bits equal to 0.

Table 4. Configuration Register Format

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	OS	R1	R0	F1	F0	POL	TM	SD

7.5.4 Shutdown Mode (SD)

The Shutdown Mode of the TMP275 allows the user to save maximum power by shutting down all device circuitry other than the serial interface, which reduces current consumption to typically less than 0.1 μA. Shutdown Mode is enabled when the SD bit is 1; the device shuts down once the current conversion is completed. When SD is equal to 0, the device maintains a continuous conversion state.

7.5.5 Thermostat Mode (TM)

The Thermostat Mode bit of the TMP275 indicates to the device whether to operate in Comparator Mode (TM = 0) or Interrupt Mode (TM = 1). For more information on Comparator and Interrupt modes, see the *High and Low Limit Registers* section.

7.5.6 Polarity (POL)

The Polarity Bit of the TMP275 allows the user to adjust the polarity of the ALERT pin output. If POL = 0, the ALERT pin is active LOW, as shown in Figure 15. For POL = 1, the ALERT pin is active HIGH, and the state of the ALERT pin is inverted.

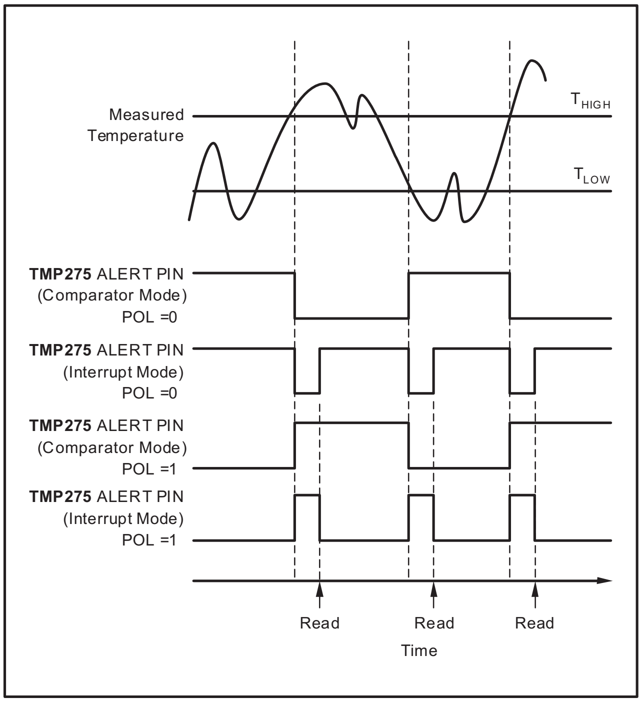


Figure 15. Output Transfer Function Diagrams

7.5.7 Fault Queue (F1/F0)

A fault condition is defined as when the measured temperature exceeds the user-defined limits set in the T_{HIGH} and T_{LOW} Registers. Additionally, the number of fault conditions required to generate an alert may be programmed using the fault queue. The fault queue is provided to prevent a false alert as a result of environmental noise. The fault queue requires consecutive fault measurements to trigger the alert function. Table 5 defines the number of measured faults that may be programmed to trigger an alert condition in the device. For T_{HIGH} and T_{LOW} register format and byte order, see the section *High and Low Limit Registers*.

Table 5. Fault Settings

F1	F0	CONSECUTIVE FAULTS
0	0	1
0	1	2
1	0	4
1	1	6

7.5.8 Converter Resolution (R1/R0)

The converter resolution bits control the resolution of the internal analog-to-digital (A/D) converter. This control allows the user to maximize efficiency by programming for higher resolution or faster conversion time. Table 6 identifies the Resolution Bits and the relationship between resolution and conversion time.

Table 6. Resolution of the TMP275

R1	R0	RESOLUTION	CONVERSION TIME (typical)
0	0	9 Bits (0.5°C)	27.5ms
0	1	10 Bits (0.25°C)	55ms
1	0	11 Bits (0.125°C)	110ms
1	1	12 Bits (0.0625°C)	220ms

7.5.9 One-Shot (OS)

The TMP275 features a One-Shot Temperature Measurement Mode. When the device is in Shutdown Mode, writing a ‘1’ to the OS bit starts a single temperature conversion. The device returns to the shutdown state at the completion of the single conversion. This mode is useful for reducing power consumption in the TMP275 when continuous temperature monitoring is not required. When the configuration register is read, the OS always reads zero.

7.5.10 High and Low Limit Registers

In Comparator Mode (TM = 0), the ALERT pin of the TMP275 becomes active when the temperature equals or exceeds the value in T_{HIGH} and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin remains active until the temperature falls below the indicated T_{LOW} value for the same number of faults.

In Interrupt Mode (TM = 1), the ALERT pin becomes active when the temperature equals or exceeds T_{HIGH} for a consecutive number of fault conditions. The ALERT pin remains active until a read operation of any register occurs, or the device successfully responds to the SMBus Alert Response Address. The ALERT pin is also cleared if the device is placed in Shutdown Mode. Once the ALERT pin is cleared, it only becomes active again by the temperature falling below T_{LOW}. When the temperature falls below T_{LOW}, the ALERT pin becomes active and remain active until cleared by a read operation of any register or a successful response to the SMBus Alert Response Address. Once the ALERT pin is cleared, the above cycle repeats, with the ALERT pin becoming active when the temperature equals or exceeds T_{HIGH}. The ALERT pin can also be cleared by resetting the device with the General Call Reset command. This command also clears the state of the internal registers in the device, returning the device to Comparator Mode (TM = 0).

Both operational modes are represented in Figure 15. Table 7, Table 8, Table 9, and Table 10 describe the format for the T_{HIGH} and T_{LOW} registers. Note that the most significant byte is sent first, followed by the least significant byte. Power-up reset values for T_{HIGH} and $_{TLOW}$ are:

T_{HIGH} = 80°C and T_{LOW} = 75°C

The format of the data for T_{HIGH} and T_{LOW} is the same as for the Temperature Register.

Table 7. Byte 1 T_{HIGH} Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	H11	H10	H9	H8	H7	H6	H5	H4

Table 8. Byte 2 of T_{HIGH} Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
2	H3	H2	H1	H0	0	0	0	0

Table 9. Byte 1 T_{LOW} Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	L11	L10	L9	L8	L7	L6	L5	L4

Table 10. Byte 2 of T_{LOW} Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
2	L3	L2	L1	L0	0	0	0	0

All 12 bits for the Temperature, T_{HIGH}, and T_{LOW} registers are used in the comparisons for the ALERT function for all converter resolutions. The three LSBs in T_{HIGH} and T_{LOW} can affect the ALERT output even if the converter is configured for 9-bit resolution.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TMP275 is digital output temperature sensor with SMBus, Two-Wire, and I^{2}C compatible interfaces. This device features three address pins (A0, A1, A2) allowing up to eight devices to be connected per bus. The TMP275 require no external components for operation except for pullup resistors on SCL, SDA, and ALERT, although TI recommends a 0.1-µF bypass capacitor. The TMP275 measures the PCB temperature of the location it is mounted. The sensing device of the device is the chip itself. Thermal paths run through the package leads as well as the plastic package. The lower thermal resistance of metal causes the leads to provide the primary thermal path.

8.2 Typical Applications

8.2.1 Typical Connections of the TMP275

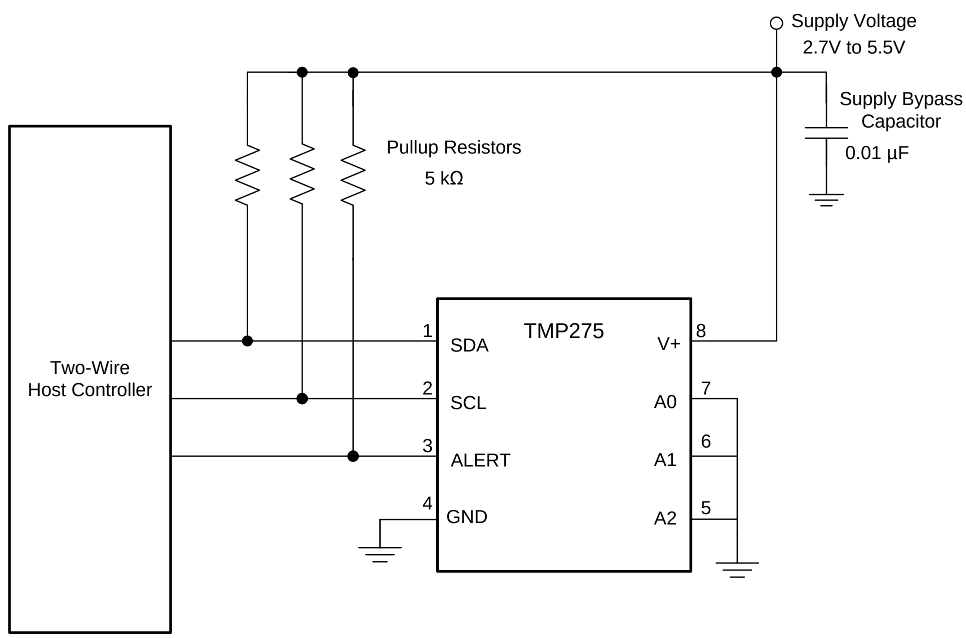


Figure 16. Typical Connections of the TMP275 Schematic

8.2.1.1 Design Requirements

Figure 16 shows TMP275 typical connections. The TMP275 device requires pullup resistors on the SCL, SDA, and ALERT pins. The recommended value for the pullup resistor is 5 kΩ. In some applications the pullup resistor can be lower or higher than 5 kΩ but must not exceed 3 mA of current on SCL and SDA pins, must not exceed 4 mA on ALERT pin. If the resistors are missing, the SCL and SDA lines will always be low (nearly 0 V) and the I^{2}C bus will not work. TI recommends a 0.1-µF bypass capacitor, as shown in Figure 16. The SCL, SDA, and ALERT lines can be pulled up to a supply that is equal to or higher than V+ through the pullup resistors.

The ALERT pin can be configured to respond to one of the two alert functions available, *Comparator Mode* and *Interrupt Mode*. To configure one of eight different addresses on the bus, connect A0, A1, and A2 to either a GND pin or V+ pin. In the circuit shown in Figure 16 the comparator mode is selected and the address pins (A0, A1, A2) are connected to ground.

Typical Applications (continued)

8.2.1.2 Detailed Design Procedure

The TMP275 device should be placed in close proximity to the heat source that must be monitored, with a proper layout for good thermal coupling. This placement ensures that temperature changes are captured within the shortest possible time interval. To maintain accuracy in applications that require air or surface temperature measurement, take care to isolate the package and leads from ambient air temperature. A thermally conductive adhesive is helpful in achieving accurate surface temperature measurement.

8.2.1.3 Application Curve

Figure 17 shows the step response of the TMP275 device to a submersion in an oil bath of 100ºC from room temperature (27ºC). The time-constant, or the time for the output to reach 63% of the input step, is 1.5 s. The time-constant result depends on the printed-circuit board (PCB) that the TMP275 devices are mounted. For this test, the TMP275 device was soldered to a two-layer PCB that measured 0.375 inches × 0.437 inches.

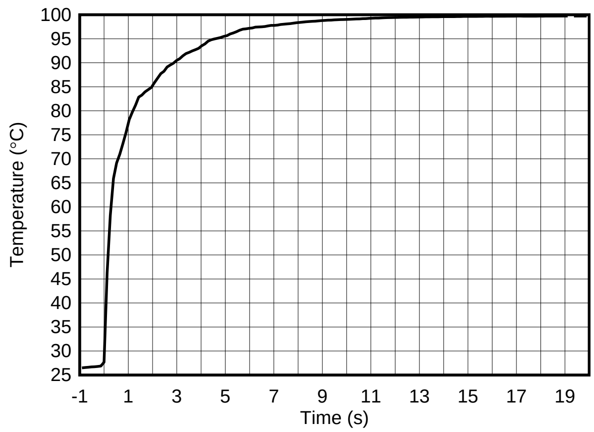


Figure 17. Temperature Step Response

8.2.2 Connecting Multiple Devices on a Single Bus

The TMP275 features three address pins allowing up to eight devices to be connected per bus. When the TMP275 is operating in Interrupt mode (TM = 1) , the ALERT pin of the TMP275 may be connected as an SMBus Alert signal. Figure 18 shows eight TMP275 devices connected to a MCU (master) using one single bus. Each device that exists as a slave on the SMBus has one unique seven bit address, see Table 2 for TMP275 address options. When a master senses that an ALERT condition is present on the ALERT line, the master sends an SMBus Alert command (00011001) on the bus. If the ALERT pin of the TMP275 is active, the device acknowledges the SMBus Alert command and responds by returning its slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates if the temperature exceeding T_{HIGH} or falling below $_{TLOW}$ caused the ALERT condition. This bit will be HIGH if the temperature is greater than or equal to T_{HIGH}. This bit will be LOW if the temperature is less than T_{LOW}.

This application have eight devices connected to the bus. If multiple devices on the bus respond to the SMBus Alert command, arbitration during the slave address portion of the SMBus Alert command determines which device clears its ALERT status. If the TMP275 wins the arbitration, its ALERT pin becomes inactive at the completion of the SMBus Alert command. If the TMP275 loses the arbitration, its ALERT pin remains active.

NOTE

Make sure you configure the device to operate in Interrupt Mode to enable the SMBus feature.

Typical Applications (continued)

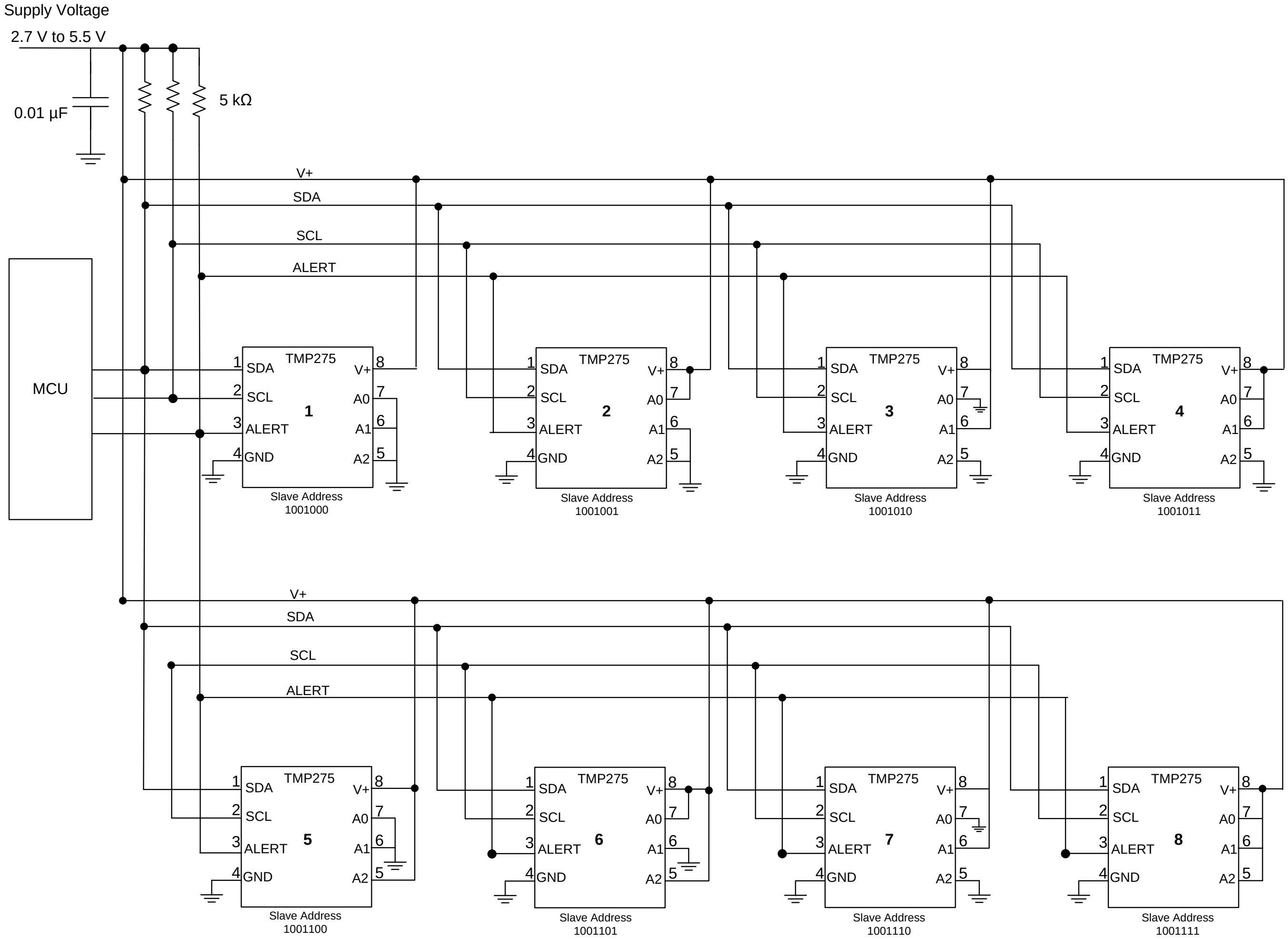


Figure 18. Connecting Multiple Devices on a Single Bus

Typical Applications (continued)

8.2.3 Temperature Data Logger for Cold Chain Management Applications

Cold chain management includes all of the means used to ensure a constant temperature for a product that is not heat stable from the time it is manufactured or farmed until the time it is used. This includes industries such as food, retail, medical, and pharmaceutical. Figure 19 implements a cold chain monitoring system that measures temperature, then logs the sensor data to nonvolatile (FRAM) memory in the MCU. Figure 19 uses a Near Field Communication (NFC) interface for wireless communication and is powered from a CR2032 coin cell battery with a focus on low power to maximize the battery lifetime.

The microcontroller communicates with all of the sensor devices through an I^2C-compatible interface. The MCU also communicates with the NFC transponder through this interface. An NFC enabled smartphone can be used to send configuration to the application board. For a detailed design procedure and requirements of this application, see *Ultralow Power Multi-Sensor Data Logger with NFC Interface Reference Design* (TIDU821).

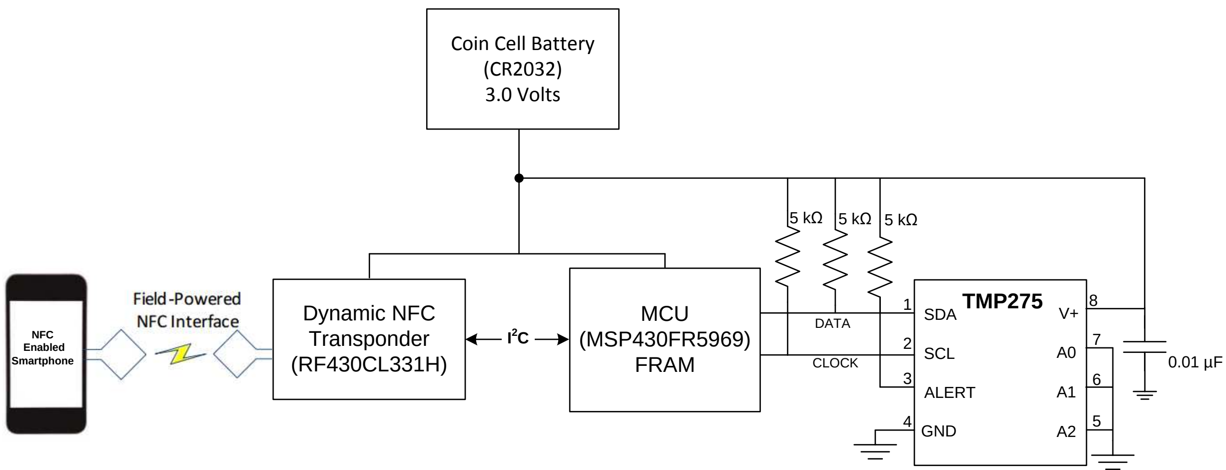


Figure 19. Temperature Data Logger

9 Power Supply Recommendations

The TMP275 device operates with power supply in the range of 2.7 V to 5.5 V. A power-supply bypass capacitor is required for stability. Place this capacitor as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.01 µF. Applications with noisy or high impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

10 Layout

10.1 Layout Guidelines

Mount the TMP275 to a PCB as shown in Figure 20. For this example the A0, A1, and A2 address pins are connected directly to ground. Connecting these pins to ground configures the device for slave address 1001000b.

- Bypass the V_S pin to ground with a low-ESR ceramic bypass-capacitor. The typical recommended bypass capacitance is a 0.1-µF ceramic capacitor with a X5R or X7R dielectric. The optimum placement is closest to the V_S and GND pins of the device. Take care in minimizing the loop area formed by the bypass-capacitor connection, the V_S pin, and the GND pin of the IC. Additional bypass capacitance can be added to compensate for noisy or high-impedance power supplies.
- Pull up the open-drain output pins SDA , SCL and ALERT through 5-kΩ pullup resistors.

10.2 Layout Example

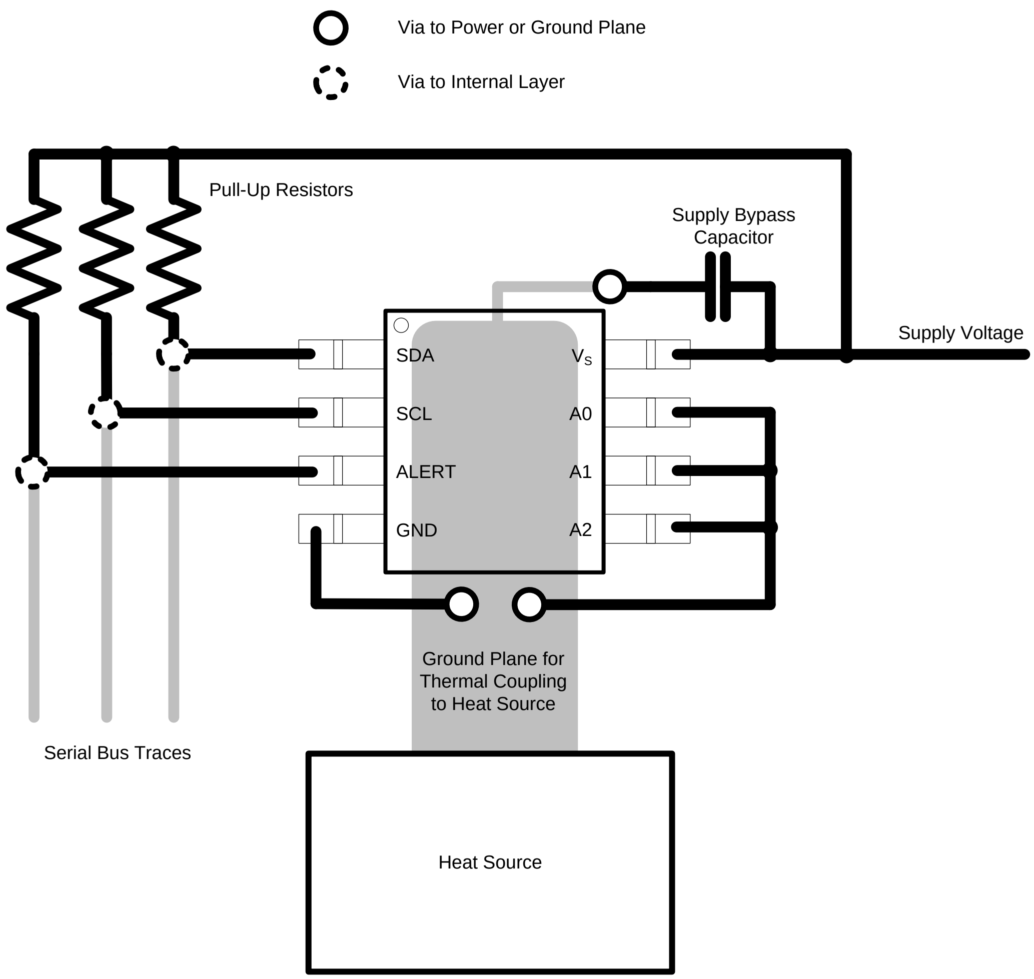


Figure 20. TMP275 Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Ultralow Power Multi-sensor Data Logger with NFC Interface Reference Design* (TIDU821)
- *Understanding the I^2C Bus* (SLVA704)

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
SMBus is a trademark of Intel Corporation.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP275AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMP275	Samples
TMP275AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	T275	Samples
TMP275AIDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	T275	Samples
TMP275AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	T275	Samples
TMP275AIDGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	T275	Samples
TMP275AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMP275	Samples
TMP275AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMP275	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

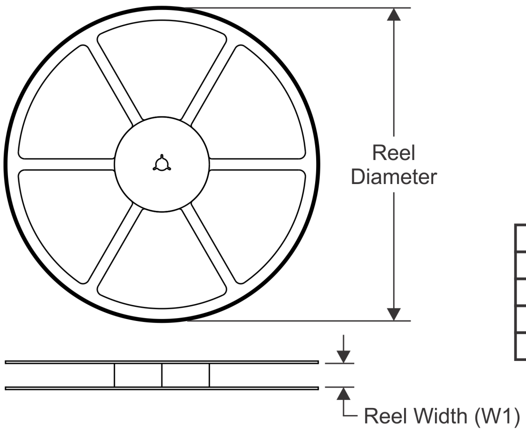
OTHER QUALIFIED VERSIONS OF TMP275 :

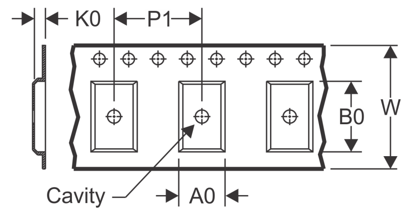
- Automotive: TMP275-Q1

NOTE: Qualified Version Definitions:

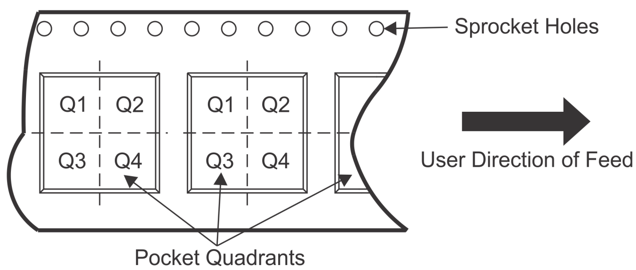
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION





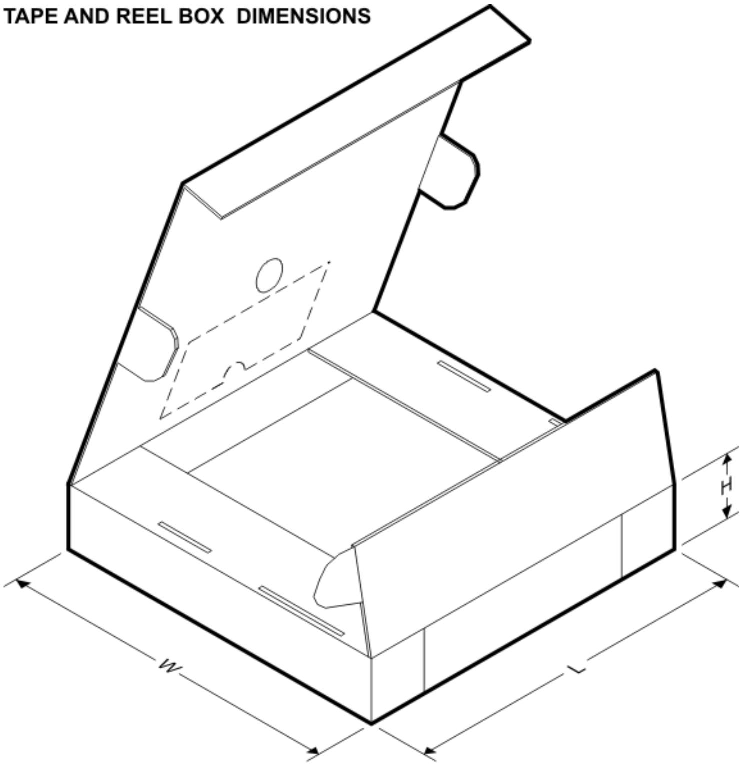
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

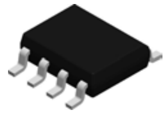
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP275AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TMP275AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP275AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP275AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

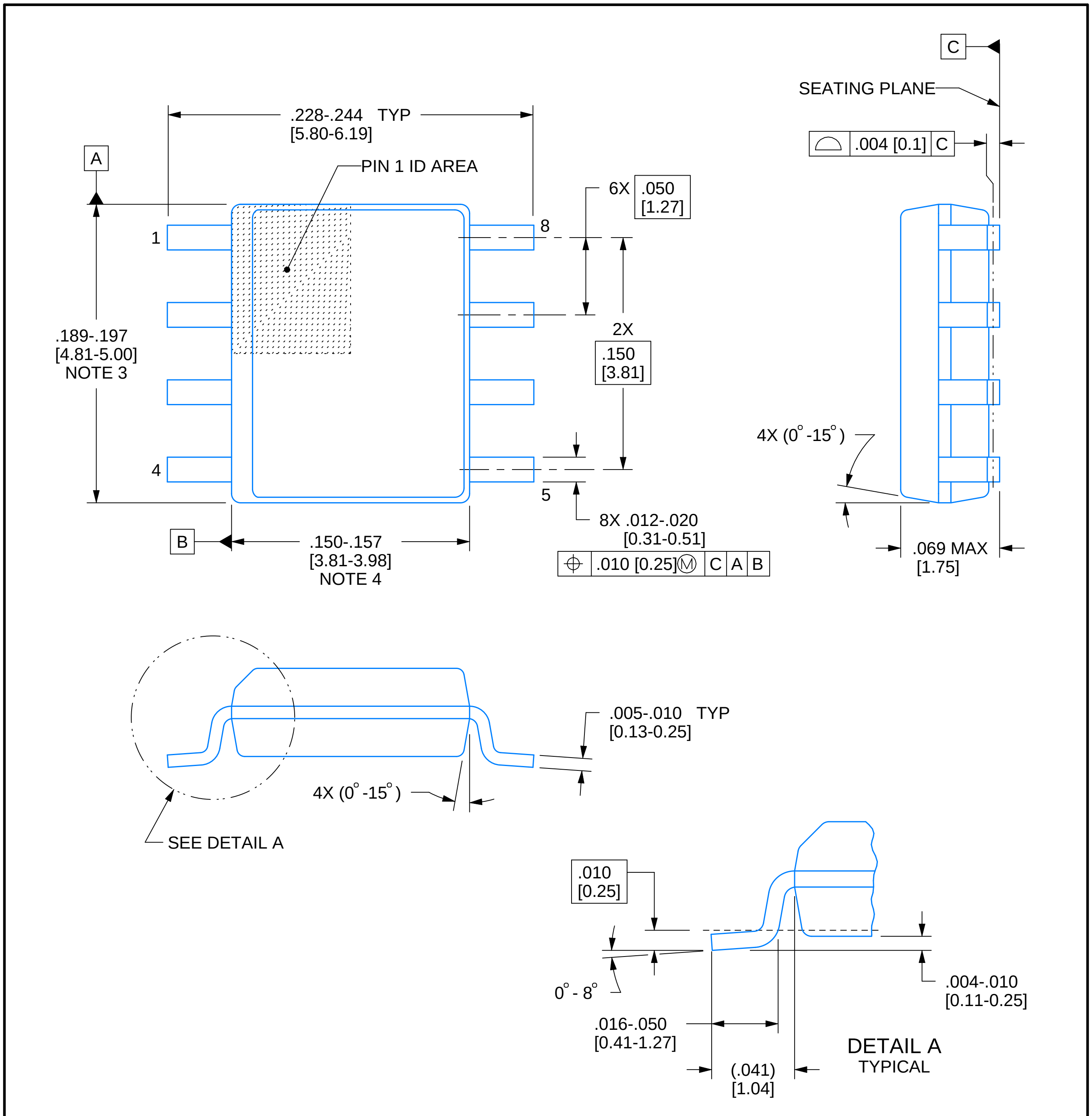
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP275AIDGKR	VSSOP	DGK	8	2500	370.0	355.0	55.0
TMP275AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TMP275AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
TMP275AIDR	SOIC	D	8	2500	367.0	367.0	35.0





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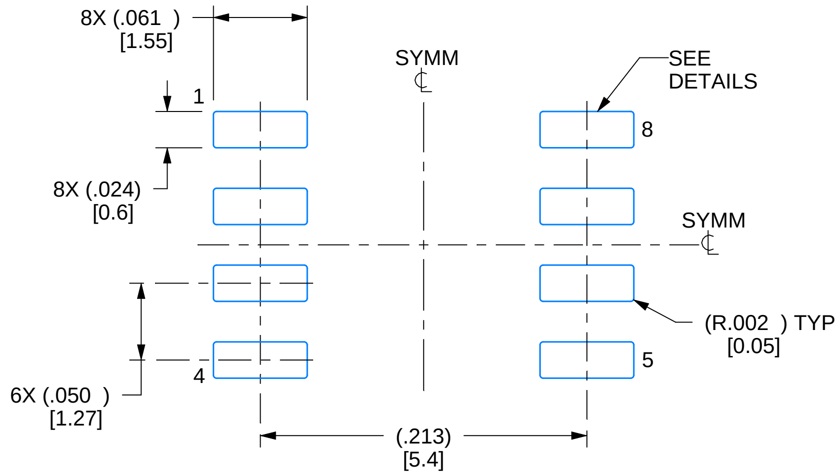
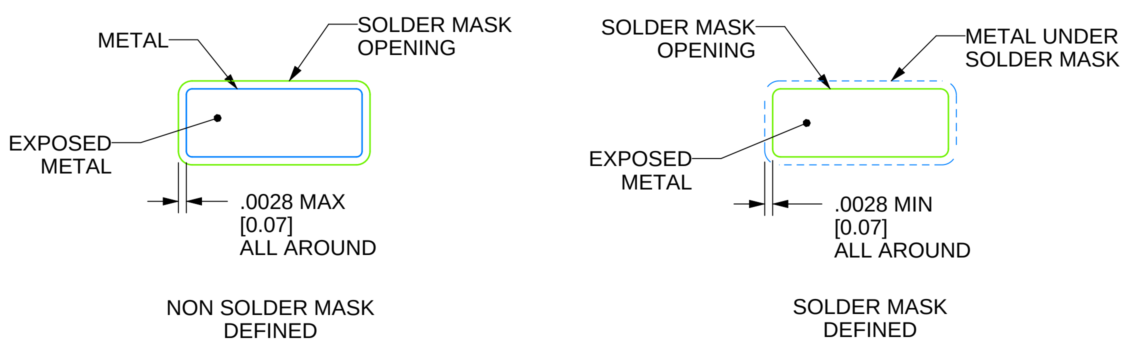
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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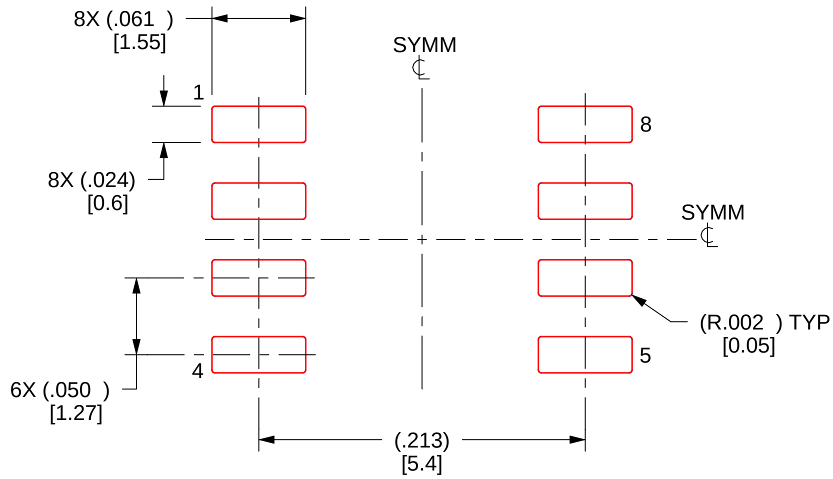
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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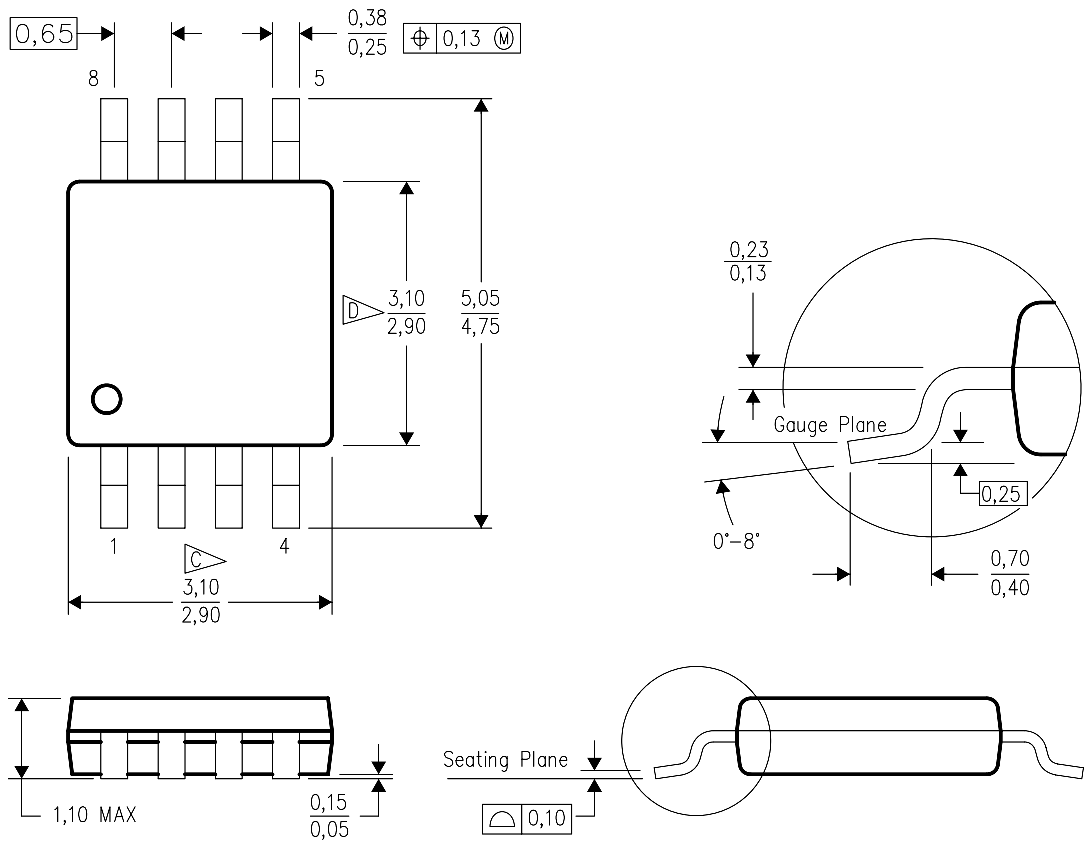
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

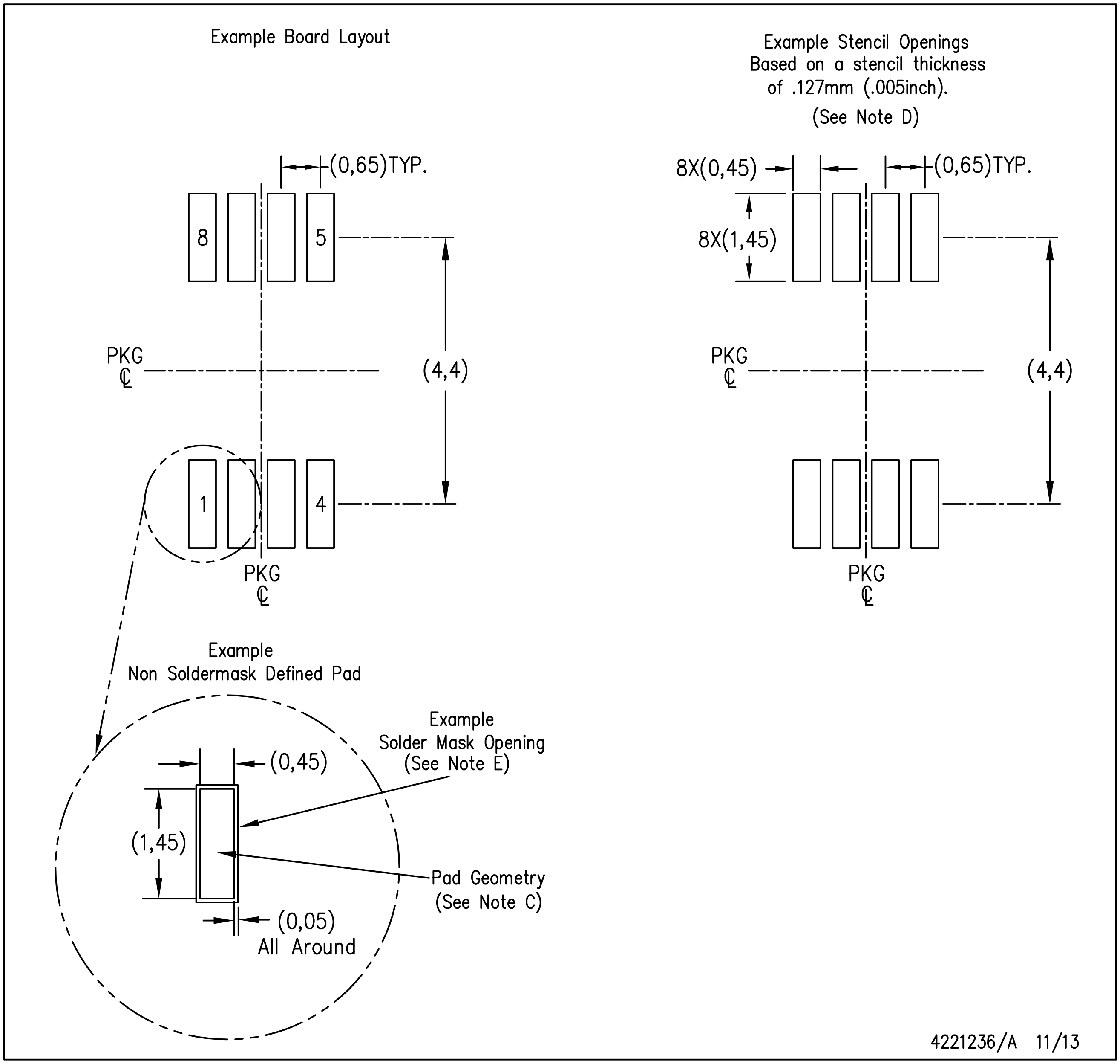
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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