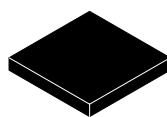
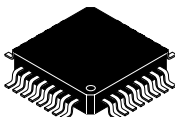




**THE DATASHEET OF
TLV320AIC1110PBS**





PCM CODEC

FEATURES

- 2.7-V to 3.3-V Operation
- Designed for Analog and Digital Wireless Handsets and Telecommunications Applications
- Two Differential Microphone Inputs
- Differential Earphone Outputs and One Single-Ended Earphone Output
- Earphone and Microphone Mute
- Programmable Transmit, Receive, and Sidetone Paths With Extended Gain and Attenuation Ranges
- Programmable for 15-Bit Linear Data or 8-Bit Companded (μ -law and A-law) Mode
- Supports PCM Clock Rates of 128 kHz and 2.048 MHz
- Pulse Density Modulated (PDM) Buzzer Output
- On-Chip I²C Bus, Which Provides Simple, Standard, Two-Wire Serial Interface With Digital ICs
- Dual-Tone Multifrequency (DTMF) and Single-Tone Generator Capable of up to 8-kHz Tone With Three Selectable Resolutions of 7.8125 Hz, 15.625 Hz, and 31.25 Hz
- 2-Channel Auxiliary Multiplexer (MUX) (Analog Switch)[†]

- Capable of Driving 32 Ω Down to a 8- Ω Speaker
- Programmable Power Down Modes
- Pin Compatible to the TLV320AIC1103 and TLV320AIC1109 Devices for TQFP Only
- Available in a 32-Pin Thin Quad Flatpack (TQFP) Package and MicroStar Junior™ BGA

APPLICATIONS

- Digital Handset
- Digital Headset
- Cordless Phones
- Digital PABX
- Digital Voice Recording

DESCRIPTION

The TLV320AIC1110 provides extended gain and attenuation flexibility for transmit, receive, and sidetone paths. A differential earphone output is capable of driving speaker loads as low as 8 Ω for use in speaker phone applications. The single tone function on the TLV320AIC1110 generates a single tone output of up to 8 kHz. The resolution of the DTMF tone is also selectable to 7.8125 Hz, 15.625 Hz, or 31.25 Hz through the interface control. The analog switch provides more control capabilities for voice-band audio processor (PCM codec).



This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

[†]These options are available on some devices. Please see the table of comparison for the last two generations of PCM codecs.

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DESCRIPTION (Continued)

The PCM codec is an analog-digital interface for voice band signals designed with a combination of coders and decoders (codecs) and filters. It is a low-power device with companding options and programming features, and it meets the requirements for communication systems, including the cellular phone. The device operates in either the 15-bit linear or 8-bit companded (μ -law or A-Law) mode, which is selectable through the I²C interface.

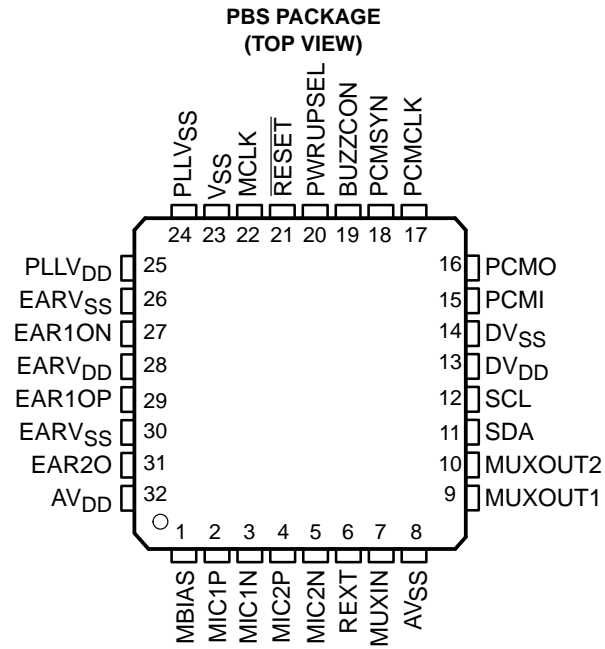
A coder, an analog-to-digital converter or ADC, digitizes the analog voice signal, and a decoder, a digital-to-analog converter or DAC, converts the digital-voice signal to an analog output. The PCM codec provides a companding option to overcome the bandwidth limitations of telephone networks without degrading the sound quality. The human auditory system is a logarithmic system in which high amplitude signals require less resolution than low amplitude signals. Therefore, an 8-bit code word with nonuniform quantization (μ -law or A-law) has the same quality as 13-bit linear coding. The PCM codec provides better digital code words by generating a 15-bit linear coding option.

The human voice is effective from a frequency range of 300 Hz to 3300 Hz in telephony applications. In order to eliminate unwanted signals, the PCM codec design has two types of filters that operate in both the transmit and receive path. A low-pass filter attenuates the signals over 4 kHz. A selectable high-pass filter cleans up the signals under 100 Hz. This reduces noise that may have coupled in from 50/60-Hz power cables. The high-pass filter is bypassed by selecting the corresponding register bit.

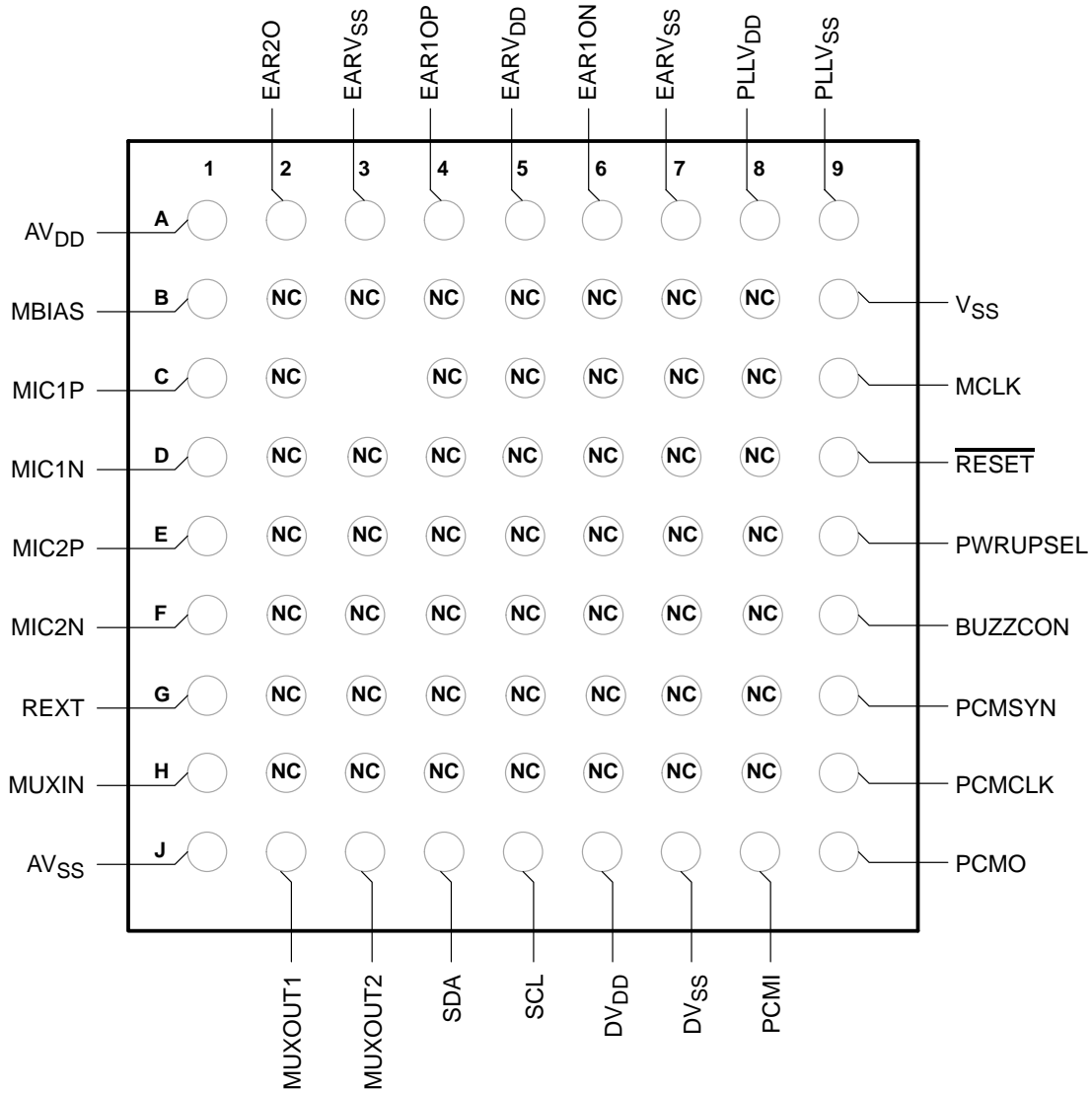
The PCM codec has many programming features that are controlled using a 2-wire standard serial I²C interface. This allows the device to interface with many digital ICs such as a DSP or a microprocessor. The device has seven registers: power control, mode control, transmit PGA, receive PGA, high DTMF, low DTMF, and auxiliary mode control. Some of the programmable features that can be controlled by I²C interface include:

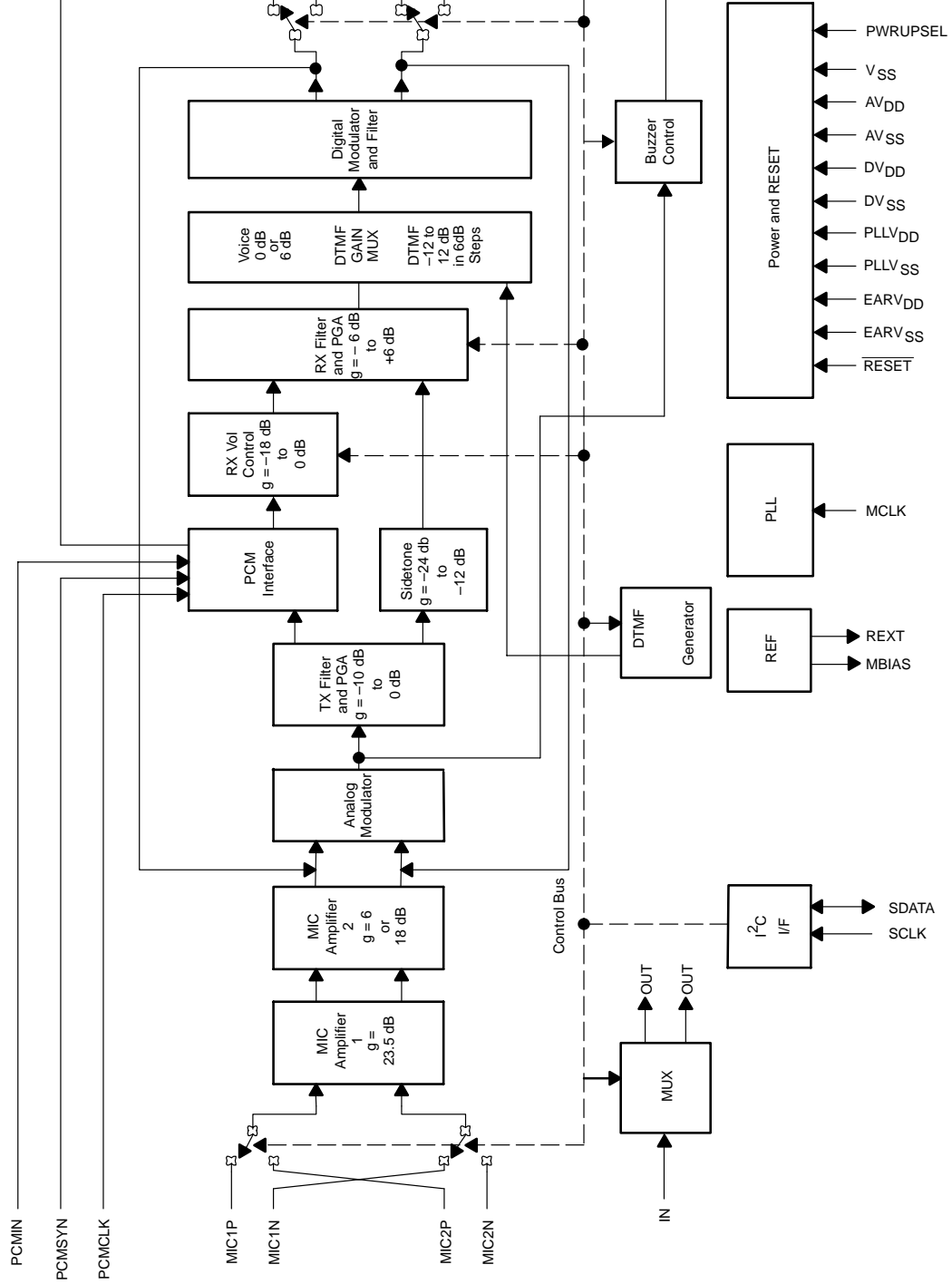
- Transmit amplifier gain
- Receive amplifier gain
- Sidetone gain
- Volume control
- Earphone control
- PLL power control
- Microphone selection
- Transmit channel high-pass filter control
- Receive channel high-pass filter control
- Companding options and selection control
- PCM loopback
- DTMF control
- Pulse density modulated control

The PCM codec is also capable of generating its own internal clocks from a 2.048-MHz master clock input.



MicroStar Junior™ (GQE) PACKAGE
(TOP VIEW)





detailed description

power on/reset

The power for the various digital and analog circuits is separated to improve the noise performance of the device. An external reset must be applied to the active low $\overline{\text{RESET}}$ terminal to assure reset upon power on and to bring the device to an operational state. After the initial power-on sequence, the device can be functionally powered up and powered down by writing to the power control register through the I²C interface. The device has a pin-selectable power up in the default mode option. The hardwired pin-selectable PWRUPSEL function allows the PCM codec to power up in the default mode and to be used without a microcontroller.

reference

A precision band gap reference voltage is generated internally and supplies all required voltage references to operate the transmit and receive channels. The reference system also supplies bias voltage for use with an electret microphone at terminal MBIAS. An external precision resistor is required for reference current setting at terminal REXT.

I²C control interface

The I²C interface is a two-wire bidirectional serial interface. The I²C interface controls the PCM codec by writing data to seven control registers:

- Power control
- Mode control
- Transmit PGA and sidetone control
- Receive PGA gain and volume control
- DTMF routing
- Tone selection control
- Auxiliary control

There are two power-up modes which may be selected at the PWRUPSEL terminal: (1) The PWRUPSEL state (V_{DD} at terminal 20) causes the device to power up in the default mode when power is applied. Without an I²C interface or controlling device, the programmable functions are fixed at the default gain levels, and functions such as the sidetone and DTMF are not accessible. (2) The PWRUPSEL state (ground at terminal 20) causes the device to go to a power-down state when power is applied. In this mode, an I²C interface is required to power up the device.

phase-locked loop (PLL)

The phase-lock loop generates the internal clock frequency required for digital filters and modulators by phase locking to 2.048-MHz master clock input.

PCM interface

The PCM interface transmits and receives data at the PCMO and PCMI terminals respectively. The data is transmitted or received at the PCMCLK speed once every PCMSYN cycle. The PCMCLK can be tied directly to the 128-kHz or 2.048-MHz master clock (MCLK). The PCMSYN can be driven by an external source or derived from the master clock and used as an interrupt to the host controller.

microphone amplifiers

The microphone input is a switchable interface for two differential microphone inputs. The first stage is a low-noise differential amplifier that provides a gain of 23.5 dB. The second-stage amplifier has a selectable gain of 6 dB or 18 dB.

detailed description (continued)

analog modulator

The transmit channel modulator is a third-order sigma-delta design.

transmit filter and PGA

The transmit filter is a digital filter designed to meet CCITT G.714 requirements. The device operates either in the 15-bit linear or 8-bit companded μ -law or in the A-law mode, which is selectable through the I²C interface. The transmit PGA defaults to 0 dB.

sidetone

A portion of the transmitted audio is attenuated and fed back to the receive channel through the sidetone path. The sidetone path defaults to the mute condition. The default gain of -12 dB is set in the sidetone control register. The sidetone path can be enabled by writing to the power control register.

receive volume control

The receive volume control block acts as an attenuator with a range of -18 dB to 0 dB in 2-dB steps for control of the receive channel volume. The receive volume control gain defaults to 0 dB.

receive filter and PGA

The receive filter is a digital filter that meets CCITT G.714 requirements with a high-pass filter that is selectable through the I²C interface. The device operates either in the 15-bit linear or the 8-bit μ -law or the A-law companded mode, which is selectable through the I²C interface. The gain defaults to -4 dB, representing a 3-dBm level for a 32- Ω load impedance and the corresponding digital full scale PCMI code.

digital modulator and filter

The second-order digital modulator and filter convert the received digital PCM data to the analog output required by the earphone interface.

earphone amplifiers

The analog signal can be routed to either of two earphone amplifiers, one with differential output (EAR1ON and EAR1OP) and one with single-ended output (EAR2O). Clicks and pops are suppressed for EAR1 differential output only.

tone generator

The tone generator provides generation of standard DTMF tones which are output to (1) the buzzer driver, as a PDM signal, (2) the receive path DAC for outputting through the earphone, or (3) as PCMO data. The integer value is loaded into one of two 8-bit registers, the high-tone register (04), or the low-tone register (05) (see the *Register Map Addressing* section). The tone output is 2 dB higher when applied to the high tone register (04). The high DTMF tones must be applied to the high-tone register, and the low DTMF tones to the low-tone register. The tone signals can be generated with three different resolutions at $\Delta F = 7.8125$ Hz, 15.625 Hz, and 31.250 Hz. The resolution option can be selected by setting the register (06).

analog mux

The analog switch can be used to source an analog signal to two different loads. The output can be reselected by setting the auxiliary register (06).

detailed description (continued)

DTMF gain MUX

The DTMF gain MUX selects the signal path and applies the appropriate gain setting. Therefore the device is either in tone mode or in voice mode. When set in the voice mode, the gain is controlled by the auxiliary register and is set to 0 dB or 6 dB. When set in the tone mode, the gain is from –12 dB to 12 dB in 6-dB steps which is set by the volume control register. The gain setting is controlled by the RXPGA register. This will not create any control contention since the device is working in one mode at a time.

Terminal Functions

| TERMINAL† | | | I/O | DESCRIPTION |
|-----------|--------|--------|-----|---|
| NAME | NO. | | | |
| | μBGA | TQFP | | |
| AVDD | A1 | 32 | I | Analog positive power supply |
| AVSS | J1 | 8 | I | Analog negative power supply (use for ground connection) |
| BUZZCON | F9 | 19 | O | Buzzer output, a pulse-density modulated signal to apply to external buzzer driver |
| DVDD | J6 | 13 | I | Digital positive power supply |
| DVSS | J7 | 14 | I | Digital negative power supply |
| EAR1ON | A6 | 27 | O | Earphone 1 amplifier output (–) |
| EAR1OP | A4 | 29 | O | Earphone 1 amplifier output (+) |
| EAR2O | A2 | 31 | O | Earphone 2 amplifier output |
| EARVDD | A5 | 28 | I | Analog positive power supply for the earphone amplifiers |
| EARVSS | A3, A7 | 30, 26 | I | Analog negative power supply for the earphone amplifiers |
| MBIAS | B1 | 1 | O | Microphone bias supply output, no decoupling capacitors |
| MCLK | C9 | 22 | I | Master system clock input (2.048 MHz, digital) |
| MIC1P | C1 | 2 | I | MIC1 input (+) |
| MIC1N | D1 | 3 | I | MIC1 input (–) |
| MIC2P | E1 | 4 | I | MIC2 input (+) |
| MIC2N | F1 | 5 | I | MIC2 input (–) |
| MUXIN | H1 | 7 | I | Analog MUX input |
| MUXOUT1 | J2 | 9 | I | Analog MUX output |
| MUXOUT2 | J3 | 10 | I | Analog MUX output |
| PCMI | J8 | 15 | I | Receive PCM input |
| PCMO | J9 | 16 | O | Transmit PCM output |
| PCMSYN | G9 | 18 | I | PCM frame sync |
| PCMCLK | H9 | 17 | I | PCM data clock |
| PLLVSS | A9 | 24 | I | PLL negative power supply |
| PLLVDD | A8 | 25 | I | PLL digital power supply |
| PWRUPSEL | E9 | 20 | I | Selects the power-up default mode |
| REXT | G1 | 6 | I/O | Internal reference current setting terminal (use precision 100-kΩ resistor and no filtering capacitors) |
| RESET | D9 | 21 | I | Active low reset |
| SCL | J5 | 12 | I | I ² C-bus serial clock. This input is used to synchronize the data transfer from and to the PCM codec. |
| SDA | J4 | 11 | I/O | I ² C-bus serial address/data input/output. This is a bidirectional terminal used to transfer register control addresses and data into and out of the codec. It is an open-drain terminal and therefore requires a pullup resistor to VDD (typical 10 kΩ for 100 kHz). |
| VSS | B9 | 23 | I | Ground return for bandgap internal reference (use for ground connection) |

† All MicroStar Junior BGA™ pins that are not mentioned have no internal connection.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|------------------------------|
| Supply voltage range, AV_{DD} , DV_{DD} , $PLL_{V_{DD}}$, $EAR_{V_{DD}}$ | -0.5 V to 3.6 V |
| Output voltage range, V_O | -0.5 V to 3.6 V |
| Input voltage range, V_I | -0.5 V to 3.6 V |
| Continuous total power dissipation | See Dissipation Rating Table |
| Operating free air temperature range (industrial temperature) | -40°C to 85°C |
| Storage temperature range, testing | -65°C to 150°C |
| Lead temperature 1,6 mm from case for 10 seconds | 260°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 85^\circ\text{C}$ POWER RATING | COMMENTS |
|----------------------|---|---|--|---|
| TQFP | 702 mW | 7.2 mW/°C | 270 mW | Low dissipation printed circuit board (PCB) |
| MicroStar Junior BGA | 660 mW | 164 mW/°C | 220 mW | Low dissipation PCB |
| MicroStar Junior BGA | 2.75 W | 36 mW/°C | 917 mW | High dissipation PCB |

recommended operating conditions (see Notes 1 and 2)

| | MIN | NOM | MAX | UNIT |
|---|---------------------|---------|---------------------|----------|
| Supply voltage, AV_{DD} , DV_{DD} , $PLL_{V_{DD}}$, $EAR_{V_{DD}}$ | 2.7 | | 3.3 | V |
| High-level input voltage, V_{IH} | $0.7 \times V_{DD}$ | | | V |
| Low-level input voltage, V_{IL} | | | $0.3 \times V_{DD}$ | V |
| Load impedance between EAR1OP and EAR1ON-RL | | 8 to 32 | | Ω |
| Load impedance for EAR2OP-RL | | 32 | | Ω |
| Operating free-air temperature, T_A | -40 | | 85 | °C |

- NOTES: 1. To avoid possible damage and resulting reliability problems to these CMOS devices, follow the *power-on initialization* paragraph, described in the *Principles of Operation*.
2. Voltages are with respect to AV_{SS} , DV_{SS} , $PLL_{V_{SS}}$, and $EAR_{V_{SS}}$.

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted)**supply current**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|-----|-----|-----|---------------|
| I_{DD} Supply current from V_{DD} | Operating, EAR1 selected, MicBias disabled | | 4.5 | 6 | mA |
| | Operating, EAR2 selected, MicBias disabled | | 4.5 | 6 | mA |
| | Power down room temperature, $V_{DD} = 3$ V, Reg 6 bit 7 = 1, MCik not present (see Note 3) | | 2 | 10 | μA |
| | Power down room temperature, $V_{DD} = 3$ V, , Reg 6 bit 7 = 0, MCik not present (see Note 3) | | 10 | 30 | μA |
| $t_{on(i)}$ Power-up time from power down | | | 5 | 10 | ms |

NOTE 3: $V_{IHMIN} = V_{DD}$, $V_{ILMAX} = V_{SS}$.

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (continued)

digital interface

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|---|--|------------------------|-----|------|------|
| V _{OH} | High-level output voltage PCMO (BUZZCON) | I _{OH} = -3.2 mA, V _{DD} = 3 V | DV _{DD} -0.25 | | | V |
| V _{OL} | Low-level output voltage PCMO | I _{OL} = 3.2 mA, V _{DD} = 3 V | | | 0.25 | V |
| I _{IH} | High-level input current, any digital input | V _I = V _{DD} | | | 10 | μA |
| I _{IL} | Low-level input current, any digital input | V _I = V _{SS} | | | 10 | μA |
| C _i | Input capacitance | | | | 10 | pF |
| C _o | Output capacitance | | | | 20 | pF |
| R _L | Load impedance (BUZZCON) | | | | 5 | kΩ |

microphone interface

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|---|---|------|-----|------|-------------------|
| V _{IO} | Input offset voltage at MIC1N, MIC2N | See Note 4 | -5 | | 5 | mV |
| I _{IB} | Input bias current at MIC1N, MIC2N | | -300 | | 300 | nA |
| C _i | Input capacitance at MIC1N, MIC2N | | | 5 | | pF |
| V _n | Microphone input referred noise, psophometrically weighted, (C-message weighted is similar) | MIC amp 1 gain = 23.5 dB MIC amp 2 gain = 0 dB | | 3 | 4.7 | μV _{rms} |
| I _{Omax} | Output source current—MBIAS | | 1 | | 1.2 | mA |
| V _(mbias) | Microphone bias supply voltage (see Note 5) | | 2.3 | 2.5 | 2.65 | V |
| | MICMUTE | | -80 | | | dB |
| | Input impedance | Fully differential | 35 | 60 | 100 | kΩ |

NOTES: 4. Measured while MIC1P and MIC1N are connected together. Less than 0.5-mV offset results in 0 value code on PCMOUT.
5. Not a JEDEC symbol.

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (continued)

speaker interface

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---------------------------------------|---|-----|---------|----------|------|
| Earphone AMP1 output power (see Note 6) | | $V_{DD} = 2.7$ V, fully differential, 8- Ω load, 3-dBm0 output, volume control = -3 dB, RXPGA = -4 dB level | | 161 | 200 | mW |
| | | $V_{DD} = 2.7$ V, fully differential, 16- Ω load, 3-dBm0 output, volume control = -3 dB, RXPGA = -2 dB level | | 128 | 160 | |
| | | $V_{DD} = 2.7$ V, fully differential, 32- Ω load, 3-dBm0 output, volume control = -3 dB, RXPGA = -1 dB level | | 81 | 100 | |
| Earphone AMP2 output power (see Note 6) | | $V_{DD} = 2.7$ V, single-ended, 32- Ω load, 3-dBm0 output | | 10 | 12.5 | mW |
| V_{OO} | Output offset voltage at EAR1 | Fully differential | | ± 5 | ± 30 | mV |
| I_{Omax} | Maximum output current for EAR1 (rms) | 3-dBm0 input, 8- Ω load | | 141 | 178 | mA |
| | | 3-dBm0 input, 16- Ω load | | 90 | 112 | |
| | | 3-dBm0 input, 32- Ω load | | 50 | 63 | |
| | Maximum output current for EAR2 (rms) | 3-dBm0 input | | 17.7 | 22.1 | |
| EARMUTE | | | -80 | | | dB |

NOTE 6: Maximum power is with a load impedance of -25%.

transmit gain and dynamic range, companded mode (μ -law or A-law) or linear mode selected, transmit slope filter bypassed (see Notes 7 and 8)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|--|------|-----|------|------------------|
| Transmit reference-signal level (0 dB) | | Differential | | | 87.5 | mV _{pp} |
| Overload-signal level (3 dBm0) | Differential, normal mode | | | | 124 | mV _{pp} |
| | Differential, extended mode | | | | 31.5 | |
| Absolute gain error | | 0-dBm0 input signal, $V_{DD} \pm 10\%$ | -1 | | 1 | dB |
| Gain error with input level relative to gain at -10 dBm0 MIC1N, MIC1P to PCMO | MIC1N, MIC1P to PCMO at 3 dBm0 to -30 dBm0 | | -0.5 | | 0.5 | dB |
| | MIC1N, MIC1P to PCMO at -31 dBm0 to -45 dBm0 | | -1 | | 1 | |
| | MIC1N, MIC1P to PCMO at -46 dBm0 to -55 dBm0 | | -1.2 | | 1.2 | |

NOTES: 7. Unless otherwise noted, the analog input is 0 dB, 1020-Hz sine wave, where 0 dB is defined as the zero-reference point of the channel under test.

8. The reference signal level, which is input to the transmit channel, is defined as a value 3 dB below the full-scale value of 88-mV_{rms}.

transmit gain and dynamic range, companded mode (μ -law or A-law) or linear mode selected, transmit slope filter enabled (see Notes 7 and 8)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|--|------|-----|------|------------------|
| Transmit reference-signal level (0 dB) | | Differential | | | 87.5 | mV _{pp} |
| Overload-signal level (3 dBm0) | Differential, normal mode | | | | 124 | mV _{pp} |
| | Differential, extended mode | | | | 31.5 | |
| Absolute gain error | | 0-dBm0 input signal, $V_{DD} \pm 10\%$ | -1 | | 1 | dB |
| Gain error with input level relative to gain at -10 dBm0 MIC1N, MIC1P to PCMO | MIC1N, MIC1P to PCMO at 3 dBm0 to -30 dBm0 | | -0.5 | | 0.5 | dB |
| | MIC1N, MIC1P to PCMO at -31 dBm0 to -45 dBm0 | | -1 | | 1 | |
| | MIC1N, MIC1P to PCMO at -46 dBm0 to -55 dBm0 | | -1.2 | | 1.2 | |

NOTES: 7. Unless otherwise noted, the analog input is 0 dB, 1020-Hz sine wave, where 0 dB is defined as the zero-reference point of the channel under test.

8. The reference signal level, which is input to the transmit channel, is defined as a value 3 dB below the full-scale value of 88-mV_{rms}.

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (continued)

transmit filter transfer, companded mode (μ -law or A-law) or linear mode selected, transmit slope filter bypassed (MCLK = 2.048 MHz)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|------|-----|-----|------|
| Gain relative to input signal gain at 1020 Hz, internal high-pass filter disabled | f_{MIC1} or $f_{MIC2} < 100$ Hz | -0.5 | | 0.5 | dB |
| | f_{MIC1} or $f_{MIC2} = 200$ Hz | -0.5 | | 0.5 | |
| | f_{MIC1} or $f_{MIC2} = 300$ Hz to 3 kHz | -0.5 | | 0.5 | |
| | f_{MIC1} or $f_{MIC2} = 3.4$ kHz | -1.5 | | 0 | |
| | f_{MIC1} or $f_{MIC2} = 4$ kHz | | | -14 | |
| | f_{MIC1} or $f_{MIC2} = 4.6$ kHz | | | -35 | |
| | f_{MIC1} or $f_{MIC2} = 8$ kHz | | | -47 | |
| Gain relative to input signal gain at 1020 Hz, internal high-pass filter enabled | f_{MIC1} or $f_{MIC2} < 100$ Hz | | | -15 | dB |
| | f_{MIC1} or $f_{MIC2} = 200$ Hz | | | -5 | |

transmit filter transfer, companded mode (μ -law or A-law) or linear mode selected, transmit slope filter selected, transmit high-pass filter enabled (MCLK = 2.048 MHz) (see Note 9)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|--|------------------------------------|-----|-------|-----|------|----|
| Gain relative to input signal gain at 1.02 kHz, with slope filter selected | f_{MIC1} or $f_{MIC2} = 100$ Hz | | | -27 | dB | |
| | f_{MIC1} or $f_{MIC2} = 200$ Hz | | | -8 | dB | |
| | f_{MIC1} or $f_{MIC2} = 250$ Hz | | | -4 | dB | |
| | f_{MIC1} or $f_{MIC2} = 300$ Hz | | -1.8 | | dB | |
| | f_{MIC1} or $f_{MIC2} = 400$ Hz | | -1.5 | | dB | |
| | f_{MIC1} or $f_{MIC2} = 500$ Hz | | -1.3 | | dB | |
| | f_{MIC1} or $f_{MIC2} = 600$ Hz | | -1.1 | | dB | |
| | f_{MIC1} or $f_{MIC2} = 700$ Hz | | -0.8 | | dB | |
| | f_{MIC1} or $f_{MIC2} = 800$ Hz | | -0.57 | | dB | |
| | f_{MIC1} or $f_{MIC2} = 900$ Hz | | -0.25 | | dB | |
| | f_{MIC1} or $f_{MIC2} = 1000$ Hz | | 0 | | dB | |
| | f_{MIC1} or $f_{MIC2} = 1500$ Hz | | 1.8 | | dB | |
| | f_{MIC1} or $f_{MIC2} = 2000$ Hz | | 4.0 | | dB | |
| | f_{MIC1} or $f_{MIC2} = 2500$ Hz | | 6.5 | | dB | |
| | f_{MIC1} or $f_{MIC2} = 3000$ Hz | | 7.6 | | dB | |
| | f_{MIC1} or $f_{MIC2} = 3100$ Hz | | 7.7 | | dB | |
| | f_{MIC1} or $f_{MIC2} = 3300$ Hz | | 8 | | dB | |
| | f_{MIC1} or $f_{MIC2} = 3500$ Hz | | 6.48 | | dB | |
| | f_{MIC1} or $f_{MIC2} = 4000$ Hz | | | | -13 | dB |
| | f_{MIC1} or $f_{MIC2} = 4500$ Hz | | | | -35 | dB |
| f_{MIC1} or $f_{MIC2} = 5000$ Hz | | | | -45 | dB | |
| f_{MIC1} or $f_{MIC2} = 8000$ Hz | | | | -50 | dB | |

NOTE 9: The pass-band tolerance is ± 0.25 dB from 300 Hz to 3500 Hz.

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (continued)

transmit idle channel noise and distortion, companded mode (μ -law or A-law) selected, slope filter bypassed

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|-----|-------|-----|-------------------|
| Transmit idle channel noise, psophometrically weighted | TXPGA gain= 0 dB, MIC Amp 1 gain = 23.5 dB, MIC Amp 2 gain = 6 dB | | -83.5 | -78 | dBm _{0p} |
| Transmit signal-to-distortion ratio with 1020-Hz sine-wave input | MIC1N, MIC1P to PCMO at 3 dBm0 | | 27 | | dBm0 |
| | MIC1N, MIC1P to PCMO at 0 dBm0 | | 30 | | |
| | MIC1N, MIC1P to PCMO at -5 dBm0 | | 33 | | |
| | MIC1N, MIC1P to PCMO at -10 dBm0 | | 36 | | |
| | MIC1N, MIC1P to PCMO at -20 dBm0 | | 35 | | |
| | MIC1N, MIC1P to PCMO at -30 dBm0 | | 26 | | |
| | MIC1N, MIC1P to PCMO at -40 dBm0 | | 24 | | |
| Intermodulation distortion, 2-tone CCITT method, composite power level, -13 dBm0 | CCITT G.712 (7.1), R2 | | 49 | | dB |
| | CCITT G.712 (7.2), R2 | | 51 | | |

transmit idle channel noise and distortion, companded mode (μ -law or A-law) selected, slope filter enabled

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|-----|-------|-----|-------------------|
| Transmit idle channel noise, psophometrically weighted | TXPGA gain= 0 dB, MIC Amp 1 gain = 23.5 dB, MIC Amp 2 gain = 6 dB | | -83.5 | -78 | dBm _{0p} |
| Transmit signal-to-total distortion ratio with 1020-Hz sine-wave input | MIC1N, MIC1P to PCMO at 3 dBm0 | | 27 | | dBm0 |
| | MIC1N, MIC1P to PCMO at 0 dBm0 | | 30 | | |
| | MIC1N, MIC1P to PCMO at -5 dBm0 | | 33 | | |
| | MIC1N, MIC1P to PCMO at -10 dBm0 | | 36 | | |
| | MIC1N, MIC1P to PCMO at -20 dBm0 | | 35 | | |
| | MIC1N, MIC1P to PCMO at -30 dBm0 | | 26 | | |
| | MIC1N, MIC1P to PCMO at -40 dBm0 | | 24 | | |
| Intermodulation distortion, 2-tone CCITT method, composite power level, -13 dBm0 | CCITT G.712 (7.1), R2 | | 49 | | dB |
| | CCITT G.712 (7.2), R2 | | 51 | | |

transmit idle channel noise and distortion, linear mode selected, slope filter bypassed

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-----|-------|-----|-------------------|
| Transmit idle channel noise | TXPGA gain = 0 dB, MIC Amp 1 gain = 23.5 dB, MIC Amp 2 gain = 6 dB | | -83.5 | -78 | dBm _{0p} |
| Transmit signal-to-total distortion ratio with 1020-Hz sine-wave input | MIC1N, MIC1P to PCMO at 3 dBm0 | 50 | 50 | | dB |
| | MIC1N, MIC1P to PCMO at 0 dBm0 | 50 | 65 | | |
| | MIC1N, MIC1P to PCMO at -5 dBm0 | 52 | 61 | | |
| | MIC1N, MIC1P to PCMO at -10 dBm0 | 56 | 65 | | |
| | MIC1N, MIC1P to PCMO at -20 dBm0 | 50 | 59 | | |
| | MIC1N, MIC1P to PCMO at -30 dBm0 | 51 | 63 | | |
| | MIC1N, MIC1P to PCMO at -40 dBm0 | 43 | 55 | | |
| | MIC1N, MIC1P to PCMO at -45 dBm0 | 38 | 52 | | |

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (continued)

transmit idle channel noise and distortion, linear mode selected, slope filter enabled

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-----|-------|-----|-------------------|
| Transmit idle channel noise | TXPGA gain = 0 dB, MIC Amp 1 gain = 23.5 dB, MIC Amp 2 gain = 6 dB | | -83.5 | -78 | dBm _{0p} |
| Transmit signal-to-total distortion ratio with 1020-Hz sine-wave input | MIC1N, MIC1P to PCMO at 3 dBm ₀ | 40 | 50 | | dB |
| | MIC1N, MIC1P to PCMO at 0 dBm ₀ | 50 | 65 | | |
| | MIC1N, MIC1P to PCMO at -5 dBm ₀ | 50 | 68 | | |
| | MIC1N, MIC1P to PCMO at -10 dBm ₀ | 64 | 70 | | |
| | MIC1N, MIC1P to PCMO at -20 dBm ₀ | 58 | 65 | | |
| | MIC1N, MIC1P to PCMO at -30 dBm ₀ | 50 | 60 | | |
| | MIC1N, MIC1P to PCMO at -40 dBm ₀ | 38 | 50 | | |
| | MIC1N, MIC1P to PCMO at -45 dBm ₀ | 30 | 45 | | |

receive gain and dynamic range, EAR1 selected, linear or companded (μ-law or A-law) mode selected (see Note 10)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|------|------|-----|-----------------|
| Overload signal level (3 dB) | 8-Ω load RXPGA = -4 dB | | 3.2 | | V _{pp} |
| | 16-Ω load RXPGA = -4 dB | | 4.05 | | |
| | 32-Ω load RXPGA = -4 dB | | 4.54 | | |
| Absolute gain error | 0 dBm ₀ input signal, V _{DD} ±10% | -1 | | 1 | dB |
| Gain error with output level relative to gain at -10 dBm ₀ | PCMIN to EAR1ON, EAR1OP at 3 dBm ₀ to -40 dBm ₀ | -0.5 | | 0.5 | dB |
| | PCMIN to EAR1ON, EAR1OP at -41 dBm ₀ to -50 dBm ₀ | -1 | | 1 | |
| | PCMIN to EAR1ON, EAR1OP at -51 dBm ₀ to -55 dBm ₀ | -1.2 | | 1.2 | |

NOTE 10: RXPGA = -4 dB for 32 Ω, 16 Ω, or 8 Ω, RXVOL = 0 dB, 1020-Hz input signal at PCMI, output measured differentially between EAR1ON and EAR1OP

receive gain and dynamic range, EAR2 selected, linear or companded (μ-law or A-law) mode selected (see Note 11)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|------|-------|-----|-----------------|
| Receive reference signal level (0 dB) | 0 dBm ₀ PCM input signal | | 1.36 | | V _{pp} |
| Overload-signal level (3 dB) | | | 1.925 | | V _{pp} |
| Absolute gain error | 0 dBm ₀ input signal, V _{DD} ±10% | -1 | | 1 | dB |
| Gain error with output level relative to gain at -10 dBm ₀ | PCMIN to EAR2O at 3 dBm ₀ to -40 dBm ₀ | -0.5 | | 0.5 | dB |
| | PCMIN to EAR2O at -41 dBm ₀ to -50 dBm ₀ | -1 | | 1 | |
| | PCMIN to EAR2O at -51 dBm ₀ to -55 dBm ₀ | -1.2 | | 1.2 | |

NOTE 11: RXPGA = -1 dB, RXVOL = 0 dB

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (continued)

receive filter transfer, companded mode (μ -law or A-law) or linear mode selected (MCLK = 2.048 MHz) (see Note 11)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|------|-----|-----|------|
| Gain relative to input signal gain at 1020 Hz, internal high-pass filter disabled | f_{EAR1} or $f_{\text{EAR2}} < 100$ Hz | -0.5 | | 0.5 | dB |
| | f_{EAR1} or $f_{\text{EAR2}} = 200$ Hz | -0.5 | | 0.5 | |
| | f_{EAR1} or $f_{\text{EAR2}} = 300$ Hz to 3 kHz | -0.5 | | 0.5 | |
| | f_{EAR1} or $f_{\text{EAR2}} = 3.4$ kHz | -1.5 | | 0 | |
| | f_{EAR1} or $f_{\text{EAR2}} = 4$ kHz | | | -14 | |
| | f_{EAR1} or $f_{\text{EAR2}} = 4.6$ kHz | | | -35 | |
| | f_{EAR1} or $f_{\text{EAR2}} = 8$ kHz | | | -47 | |
| Gain relative to input signal gain at 1020 Hz, internal high-pass filter enabled | f_{EAR1} or $f_{\text{EAR2}} < 100$ Hz | | | -15 | dB |
| | f_{EAR1} or $f_{\text{EAR2}} = 200$ Hz | | | -5 | |

NOTE 11: RXPGA = -1 dB, RXVOL = 0 dB

receive idle channel noise and distortion, EAR1 selected, companded mode (μ -law or A-law) selected (see Note 10)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|-----|-----|-----|------------------------|
| Receive noise, psophometrically weighted | PCMIN = 11010101 (A-law) | | -89 | -86 | dBm _{0p} |
| Receive noise, C-message weighted | PCMIN = 11111111 (μ -law) | | 36 | 50 | μ V _{rms} |
| Receive signal-to-distortion ratio with 1020-Hz sine-wave input | PCMIN to EAR1ON, EAR1OP at 3 dBm ₀ | 21 | | | dB |
| | PCMIN to EAR1ON, EAR1OP at 0 dBm ₀ | 25 | | | |
| | PCMIN to EAR1ON, EAR1OP at -5 dBm ₀ | 36 | | | |
| | PCMIN to EAR1ON, EAR1OP at -10 dBm ₀ | 43 | | | |
| | PCMIN to EAR1ON, EAR1OP at -20 dBm ₀ | 40 | | | |
| | PCMIN to EAR1ON, EAR1OP at -30 dBm ₀ | 38 | | | |
| | PCMIN to EAR1ON, EAR1OP at -40 dBm ₀ | 28 | | | |
| | PCMIN to EAR1ON, EAR1OP at -45 dBm ₀ | 23 | | | |

NOTE 10: RXPGA = -4 dB for 32 Ω , RXVOL = 0 dB, 1020-Hz input signal at PCMI, output measured differentially between EAR1ON and EAR1OP.

receive idle channel noise and distortion, EAR1 selected, linear mode selected (see Note 10)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|-----|-----|-----|------------------|
| Receive noise, (20-Hz to 20-kHz brickwall window) | PCMIN = 0000000000000000 | | -88 | -83 | dBm ₀ |
| Receive signal-to-distortion ratio with 1020-Hz sine-wave input | PCMIN to EAR1ON, EAR1OP at 3 dBm ₀ | 53 | 61 | | dB |
| | PCMIN to EAR1ON, EAR1OP at 0 dBm ₀ | 63 | 75 | | |
| | PCMIN to EAR1ON, EAR1OP at -5 dBm ₀ | 60 | 72 | | |
| | PCMIN to EAR1ON, EAR1OP at -10 dBm ₀ | 56 | 67 | | |
| | PCMIN to EAR1ON, EAR1OP at -20 dBm ₀ | 50 | 63 | | |
| | PCMIN to EAR1ON, EAR1OP at -30 dBm ₀ | 45 | 50 | | |
| | PCMIN to EAR1ON, EAR1OP at -40 dBm ₀ | 40 | 51 | | |
| Intermodulation distortion, 2-tone CCITT method, composite power level, -13 dBm ₀ | CCITT G.712 (7.1), R2 | 50 | | | dB |
| | CCITT G.712 (7.2), R2 | 54 | | | |

NOTE 10: RXPGA = -4 dB for 32 Ω , RXVOL = 0 dB, 1020-Hz input signal at PCMI, output measured differentially between EAR1ON and EAR1OP.

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (continued)

receive idle channel noise and distortion EAR2 selected, companded mode (μ -law or A-law) selected (see Note 11)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--------------------------------|-----|-----|-----|------------------------|
| Receive noise, psophometrically weighted | PCMIN = 11010101 (A-law) | | -82 | -78 | dBm _{op} |
| Receive noise, C-message weighted | PCMIN = 11111111 (μ -law) | | 36 | 50 | μ V _{rms} |
| Receive signal-to-distortion ratio with 1020-Hz sinewave input | PCMIN to EAR2O at 3 dBm0 | | 21 | | dB |
| | PCMIN to EAR2O at 0 dBm0 | | 25 | | |
| | PCMIN to EAR2O at -5 dBm0 | | 36 | | |
| | PCMIN to EAR2O at -10 dBm0 | | 43 | | |
| | PCMIN to EAR2O at -20 dBm0 | | 40 | | |
| | PCMIN to EAR2O at -30 dBm0 | | 38 | | |
| | PCMIN to EAR2O at -40 dBm0 | | 28 | | |
| | PCMIN to EAR2O at -45 dBm0 | | 23 | | |

NOTE 11. RXPGA = -1 dB, RXVOL = 0 dB

receive idle channel noise and distortion, EAR2 selected, linear mode selected (see Note 11)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|----------------------------|-----|-----|-----|------|
| Receive noise, (20-Hz to 20-kHz brickwall window) | PCMIN = 0000000000000000 | | -83 | -86 | dBm0 |
| Receive signal-to-noise + distortion ratio with 1020-Hz sinewave input | PCMIN to EAR2O at 3 dBm0 | | 53 | 60 | dB |
| | PCMIN to EAR2O at 0 dBm0 | | 60 | 65 | |
| | PCMIN to EAR2O at -5 dBm0 | | 58 | 62 | |
| | PCMIN to EAR2O at -10 dBm0 | | 55 | 60 | |
| | PCMIN to EAR2O at -20 dBm0 | | 53 | 60 | |
| | PCMIN to EAR2O at -30 dBm0 | | 51 | 58 | |
| | PCMIN to EAR2O at -40 dBm0 | | 50 | 57 | |
| Intermodulation distortion, 2-tone CCITT method | CCITT G.712 (7.1), R2 | | 50 | | dB |
| | CCITT G.712 (7.2), R2 | | 54 | | |

NOTE 11: RXPGA = -1 dB, RXVOL = 0 dB

power supply rejection and crosstalk attenuation

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|-----|-----|-----|------|
| Supply voltage rejection, transmit channel | MIC1N, MIC1P = 0 V, V _{DD} = 3 V _{dc} + 100 mV _{peak to peak} , f = 0 to 50 kHz | | -86 | -70 | dB |
| Supply voltage rejection, receive channel, EAR1 selected (differential) | PCM code = positive zero, V _{DD} = 3 V _{dc} + 100 mV _{peak to peak} , f = 0 to 50 kHz | | -98 | -70 | dB |
| Crosstalk attenuation, transmit-to-receive (differential) | MIC1N, MIC1P = 0 dB, f = 300 to 3400 Hz measured differentially between EAR1ON and EAR1OP | | 70 | | dB |
| Crosstalk attenuation, receive-to-transmit | PCMIN = 0 dBm0, f = 300 to 3400 Hz measured at PCMO, EAR1 amplifier | | 70 | | dB |

timing requirements**clock (2.048-MHz CLK)**

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---------------|--|-----|-------|-----|--------|
| t_t | Transition time, MCLK | | | 10 | ns |
| $f_{(mclk)}$ | MCLK frequency | | 2.048 | | MHz |
| | MCLK jitter | | | 37% | |
| | Number of PCMCLK clock cycles per PCMSYN frame | 256 | | 256 | cycles |
| $t_c(PCMCLK)$ | PCMCLK clock period | 156 | 488 | 512 | ns |
| | Duty cycle, PCMCLK | 45% | 50% | 68% | |

transmit (2.048-MHz CLK) (see Figure 1)

| PARAMETER | | MIN | MAX | UNIT |
|------------------|---|-----|------------------|------|
| $t_{su}(PCMSYN)$ | Setup time, PCMSYN high before falling edge of PCMCLK | 20 | $t_c(PCMCLK)-20$ | ns |
| $t_h(PCMSYN)$ | Hold time, PCMSYN high after falling edge of PCMCLK | 20 | $t_c(PCMCLK)-20$ | |

receive (2.048-MHz CLK) (see Figure 2)

| PARAMETER | | MIN | MAX | UNIT |
|-----------------|--|-----|------------------|------|
| $t_{su}(PCSYN)$ | Setup time, PCMSYN high before falling edge of PCMCLK | 20 | $t_c(PCMCLK)-20$ | ns |
| $t_h(PCSYN)$ | Hold time, PCMSYN high after falling edge of PCMCLK | 20 | $t_c(PCMCLK)-20$ | ns |
| $t_{su}(PCMI)$ | Setup time, PCMI high or low before falling edge of PCMCLK | 20 | | ns |
| $t_h(PCMI)$ | Hold time, PCMI high or low after falling edge of PCMCLK | 20 | | ns |

clock (128-kHz CLK)

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---------------|--|--------|--------|--------|---------|
| t_t | Transition time, MCLK | | | 10 | ns |
| $f_{(mclk)}$ | MCLK frequency | | 128 | | kHz |
| | MCLK jitter | | | 5% | |
| | Number of PCMCLK clock cycles per PCMSYN frame | 16 | | 16 | |
| $t_c(PCMCLK)$ | PCMCLK clock period | 742.19 | 781.25 | 820.31 | ns |
| | Duty cycle, PCMCLK | 40% | 50% | 60% | |
| $t_c(PCMSYN)$ | PCMSYN clock period | | 125 | | μ s |
| | Duty cycle, PCMCLK | 49.5% | 50% | 50.5% | |

transmit (128-kHz CLK) (see Figure 5)

| PARAMETER | | MIN | MAX | UNIT |
|------------------|--|-----|-----------------|------|
| $t_{su}(PCMSYN)$ | Setup time, PCMSYN high before PCMCLK \uparrow | 20 | $t_c(PCMCLK)/4$ | ns |
| $t_h(PCMSYN)$ | Hold time, PCMSYN high after PCMCLK \downarrow | 20 | $t_c(PCMCLK)/4$ | |
| $t_v(PCMO)$ | Data valid time after the rising edge of PCMSYNC | 50 | | ns |

receive (128-kHz CLK) (see Figure 4)

| PARAMETER | | MIN | MAX | UNIT |
|-----------------|--|-----|-----------------|------|
| $t_{su}(PCSYN)$ | Setup time, PCMSYN high before rising edge of PCMCLK | 20 | $t_c(PCMCLK)/4$ | ns |
| $t_h(PCSYN)$ | Hold time, PCMSYN high after falling edge of PCMCLK | 20 | $t_c(PCMCLK)/4$ | ns |
| $t_{su}(PCMI)$ | Setup time, PCMI high or low before falling edge of PCMCLK | 20 | | ns |
| $t_h(PCMI)$ | Hold time, PCMI high or low after falling edge of PCMCLK | 20 | | ns |

timing requirements (continued)

I²C bus timing requirements (see Figure 3)

| PARAMETER | | MIN | MAX | UNIT |
|-----------------------|---|------|-----|------|
| SCL | Clock frequency | | 400 | kHz |
| t _w (SCLH) | Pulse duration, SCL high | 600 | | ns |
| t _w (SCLL) | Pulse duration, SCL low | 1300 | | ns |
| t _h (STA) | Hold time, SCL high after SDA↓ (repeated START condition)† | 600 | | ns |
| t _{su} (STA) | Setup time, for SCL high before SDA↓ repeated START condition | 600 | | ns |
| t _h (DAT) | Hold time, SDA valid after SCL low | 0 | | ns |
| t _{su} (DAT) | Setup time, SDA valid before SCL↑ | 100 | | ns |
| t _{su} (STO) | Setup time, STOP condition | 600 | | ns |
| t _w (SDAT) | Pulse duration, SDA high (bus free time) | 1300 | | ns |
| t _r | Rise time (SDA and SCL) | | 300 | ns |
| t _f | Fall time (SDA and SCL) | | 300 | ns |

† After this period, the first block pulse is generated.

switching characteristics over recommended ranges of supply voltages and operating free-air temperature

propagation delay times, C_{L(max)} = 10 pF (see Figure 1)

| PARAMETER | | MIN | MAX | UNIT |
|------------------|--|-----|-----|------|
| t _{pd1} | PCMCLK bit 1 high to PCMO bit 1 valid | | 35 | ns |
| t _{pd2} | PCMCLK high to PCMO valid, bits 2 to n | | 35 | ns |
| t _{pd3} | PCMCLK bit n low to PCMO bit n Hi-Z | 30 | | ns |

DTMF generator

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|-------|-----|------|------|
| DTMF high to low tone relative amplitude (preemphasis) | | 1.5 | 2 | 2.5 | dB |
| Tone frequency accuracy (for DTMF) | Resolution of 7.8125 Hz | -1.5% | | 1.5% | |
| Harmonic distortion | Measured from lower tone group to highest parasitic | | | -20 | dB |

MICBIAS

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------|-----------------|-----|-----|-----|------|
| Load impedance (bias mode) | | | 5 | | kΩ |

PARAMETER MEASUREMENT INFORMATION

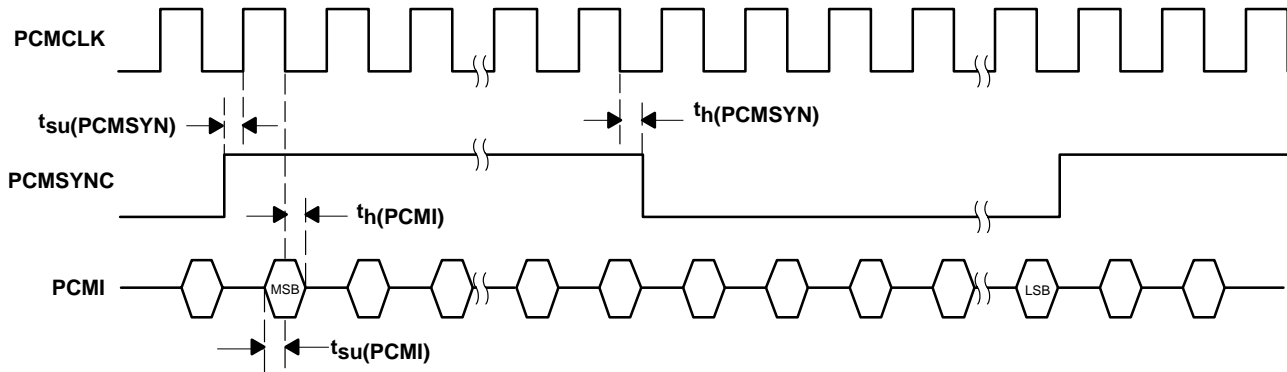


Figure 4. Receive Timing Diagram, 128 kHz

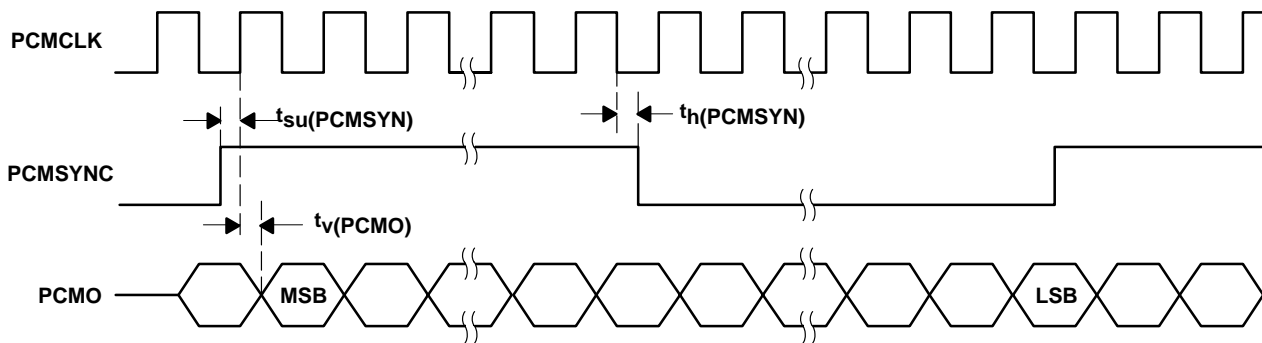


Figure 5. Transmit Timing Diagram, 128 kHz

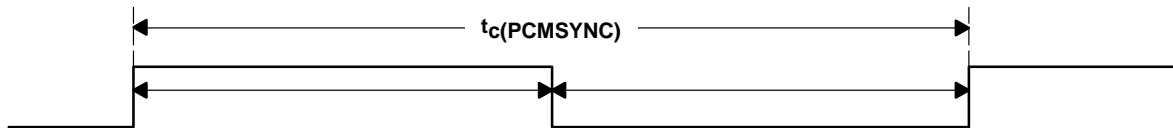
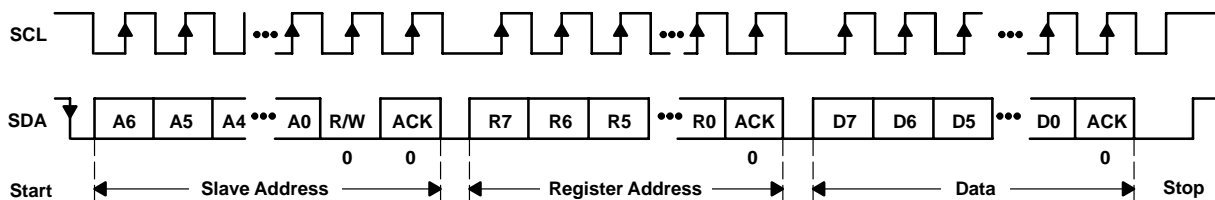


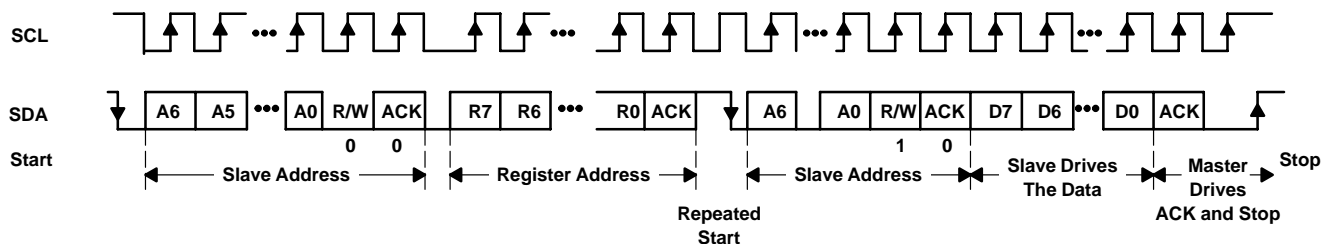
Figure 6. PCMSYNC Timing, 128 kHz

PARAMETER MEASUREMENT INFORMATION



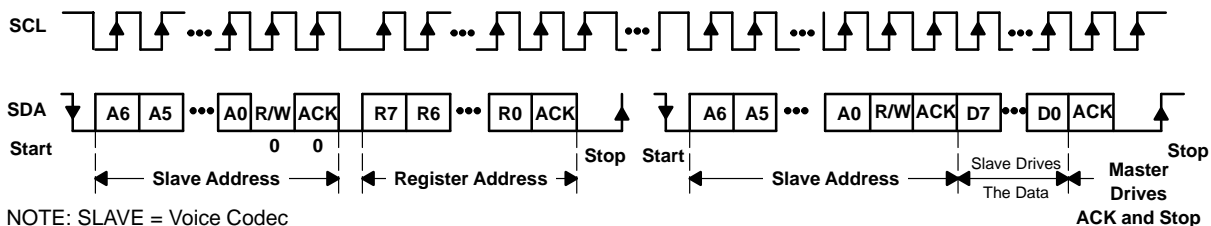
NOTE: SLAVE = Voice Codec

Figure 7. I²C-Bus Write to Voice Codec



NOTE: SLAVE = Voice Codec

Figure 8. I²C Read From Voice Codec: Protocol A



NOTE: SLAVE = Voice Codec

Figure 9. I²C Read From Voice Codec: Protocol B

TYPICAL CHARACTERISTICS

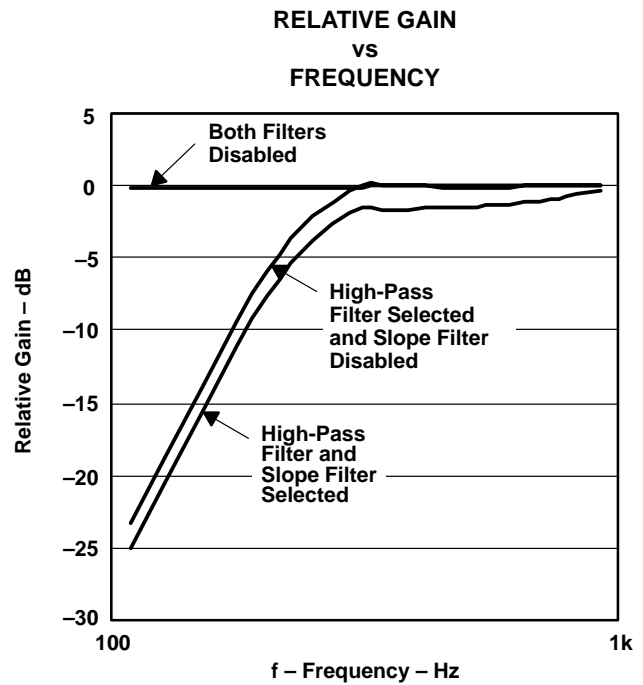
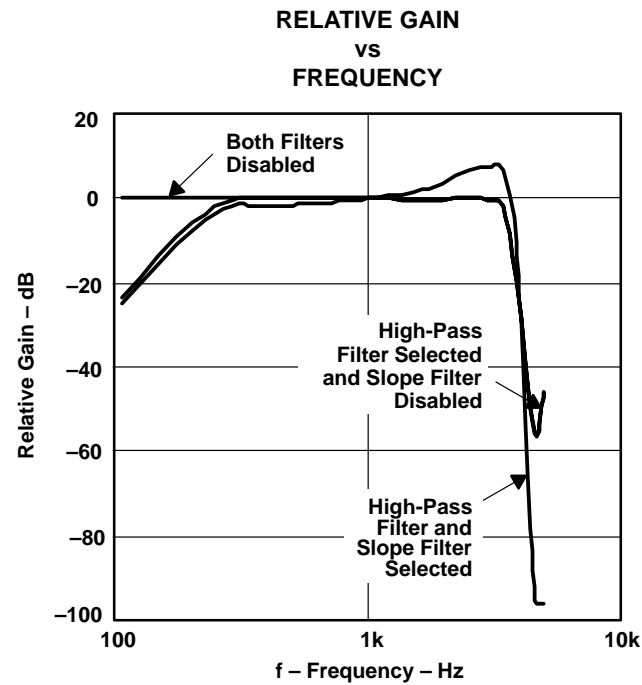
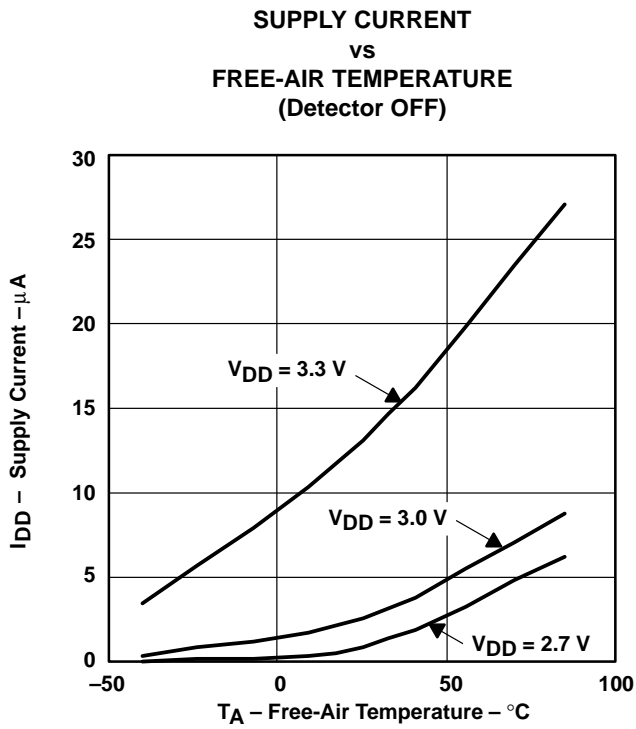
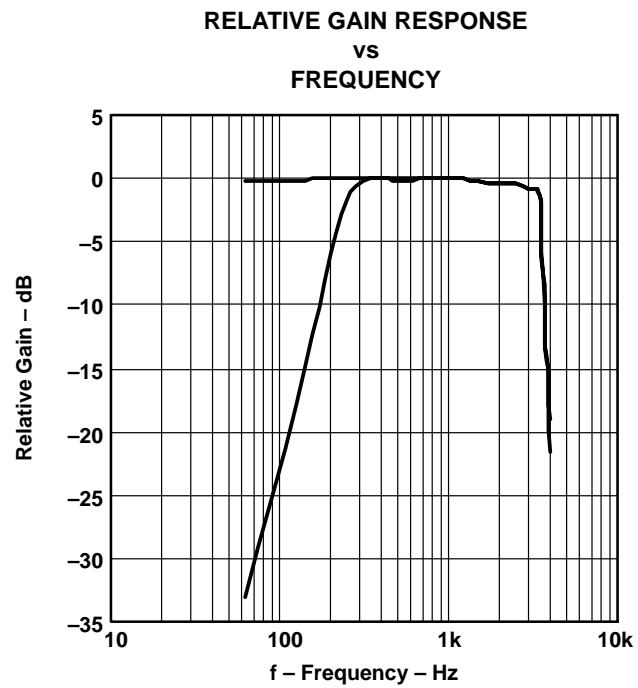


Figure 10. Transmit Gain Response With Respect to Gain of 1-kHz Tone

TYPICAL CHARACTERISTICS



**Figure 11. Receive Gain Response With Respect to Gain of 1-kHz Tone
With High-Pass Filter Selected and High-Pass Filter Disabled**

PRINCIPLES OF OPERATION

power-on initialization

An external reset with a minimum pulse width of 500 ns must be applied to the active low $\overline{\text{RESET}}$ terminal to assure reset upon power on. All registers are set with default values upon external reset initialization.

The desired selection for all programmable functions can be initialized prior to a power-up command using the control interface.

Table 1. Power-Up and Power-Down Procedures ($V_{DD} = 2.7 \text{ V}$, earphone amplifier unloaded)

| DEVICE STATUS | PROCEDURE | MAXIMUM POWER CONSUMPTION |
|---------------|---|---------------------------|
| Power up | Set bit 1 = 1 in power control register, EAR1 enabled | 16.2 mW |
| | Set bit 1 = 0 in power control register, EAR2 enabled | 14.6 mW |
| Power down | Set bit 7 = 1 in TXPGA control register and bit 0 = 0 | 1.35 μW |
| | Set bit 7 = 0 in TXPGA control register and bit 0 = 0 | 67.5 μW |

In addition to resetting the power down bit in the power control register, loss of MCLK (no transition detected) automatically enters the device into a power-down state with PCMO in the high impedance state. If during a pulse code modulation (PCM) data transmit cycle an asynchronous power down occurs, the PCM interface remains powered up until the PCM data is completely transferred.

An additional power-down mode overrides the MCLK detection function. This allows the device to enter the power down state without regard to MCLK. Setting bit 7 of the TXPGA sidetone register to logic high enables this function.

internal reference current setting terminal

Use a 100-k Ω precision resistor to connect the REXT pin to GND.

conversion laws

The device can be programmed for either a 15-bit linear or and 8-bit (μ -law or A-law) companding mode. The companding operation approximates the CCITT G.711 recommendation. The linear mode operation uses a 15-bit twos-complement format.

transmit operation

microphone input

The microphone input stage is a low-noise differential amplifier that provides a preamplifier gain of 23.5 dB. It is recommended that a microphone capacitively connected to the MIC1N and MIC1P inputs, while the MIC2N and MIC2P inputs can be used to capacitively connect a second microphone or an auxiliary audio circuit.

PRINCIPLES OF OPERATION

transmit operation (continued)

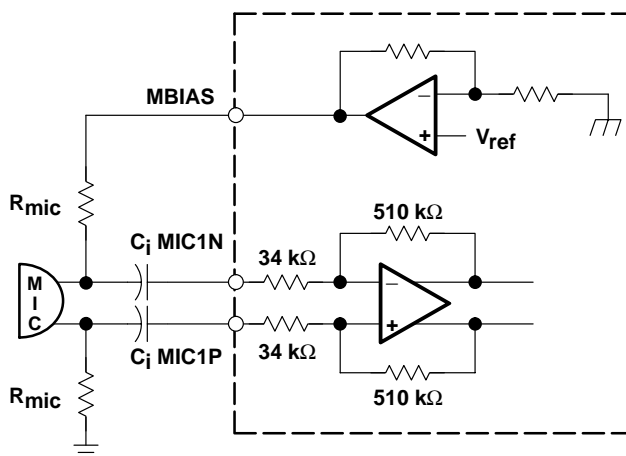


Figure 12. Typical Microphone Interface

microphone mute function

Transmit channel muting provides 80-dB attenuation of the input microphone signal. The MICMUTE function can be selected by setting bit 6 of the power control register through the I²C interface.

transmit channel gain control

The values in the transmit PGA control registers control the gain in the transmit path. The total TX channel gain can vary from 41.5 dB to 19.5 dB. The default total TX channel gain is 23.5 dB.

Table 2. Transmit Gain Control

| BIT NAME | | | | MIC AMP1 | MIC AMP2 | TX PGA | GAIN MODE | TOTAL TX GAIN | | | |
|----------|-----|-----|-----|----------|----------|--------|-----------|---------------|------|------|------|
| TP3 | TP2 | TP1 | TP0 | GAIN | GAIN | GAIN | | MIN | TYP | MAX | UNIT |
| 0 | 0 | 0 | 0 | 23.5 | 18 | 0 | Extended | 41.3 | 41.5 | 41.7 | dB |
| 0 | 0 | 0 | 1 | 23.5 | 18 | -2 | Extended | 39.3 | 39.5 | 39.7 | dB |
| 0 | 0 | 1 | 0 | 23.5 | 18 | -4 | Extended | 37.3 | 37.5 | 37.7 | dB |
| 0 | 0 | 1 | 1 | 23.5 | 18 | -6 | Extended | 35.3 | 35.5 | 35.7 | dB |
| 0 | 1 | 0 | 0 | 23.5 | 18 | -8 | Extended | 33.3 | 33.5 | 33.7 | dB |
| 0 | 1 | 0 | 1 | 23.5 | 18 | -10 | Extended | 31.3 | 31.5 | 31.7 | dB |
| 1 | 0 | 0 | 0 | 23.5 | 6 | 0 | Normal | 29.3 | 29.5 | 29.7 | dB |
| 1 | 0 | 0 | 1 | 23.5 | 6 | -2 | Normal | 27.3 | 27.5 | 27.7 | dB |
| 1 | 0 | 1 | 0 | 23.5 | 6 | -4 | Normal | 25.3 | 25.5 | 25.7 | dB |
| 1 | 0 | 1 | 1 | 23.5 | 6 | -6 | Normal | 23.3 | 23.5 | 23.7 | dB |
| 1 | 1 | 0 | 0 | 23.5 | 6 | -8 | Normal | 21.3 | 21.5 | 21.7 | dB |
| 1 | 1 | 0 | 1 | 23.5 | 6 | -10 | Normal | 19.3 | 19.5 | 19.7 | dB |

PRINCIPLES OF OPERATION

receive operation

receive channel gain control

The values in the receive PGA control registers control the gain in the receive path. PGA gain is set from -6 dB to 6 dB in 1-dB steps through the I²C interface. The default receive channel gain is -4 dB.

Table 3. Receive PGA Gain Control

| BIT NAME | | | | RELATIVE GAIN, VOICE MODE | | | | DTMF GAIN, TONE NODE |
|----------|-----|-----|-----|---------------------------|-----|------|------|----------------------|
| RP3 | RP2 | RP1 | RP0 | MIN | TYP | MAX | UNIT | |
| 0 | 0 | 0 | 0 | 5.8 | 6 | 6.2 | dB | 12 |
| 0 | 0 | 0 | 1 | 4.8 | 5 | 5.2 | dB | 12 |
| 0 | 0 | 1 | 0 | 3.8 | 4 | 4.2 | dB | 12 |
| 0 | 0 | 1 | 1 | 2.8 | 3 | 3.2 | dB | 6 |
| 0 | 1 | 0 | 0 | 1.8 | 2 | 2.2 | dB | 6 |
| 0 | 1 | 0 | 1 | 0.8 | 1 | 1.2 | dB | 6 |
| 0 | 1 | 1 | 0 | -0.2 | 0 | 0.2 | dB | 0 |
| 0 | 1 | 1 | 1 | -1.2 | -1 | -0.8 | dB | 0 |
| 1 | 0 | 0 | 0 | -2.2 | -2 | -1.8 | dB | 0 |
| 1 | 0 | 0 | 1 | -3.2 | -3 | -2.8 | dB | -6 |
| 1 | 0 | 1 | 0 | -4.2 | -4 | -3.8 | dB | -6 |
| 1 | 0 | 1 | 1 | -5.2 | -5 | -4.8 | dB | -6 |
| 1 | 1 | 0 | 0 | -6.2 | -6 | -5.8 | dB | -12 |
| 1 | 1 | 0 | 1 | | X | | dB | -12 |
| 1 | 1 | 1 | 0 | | X | | dB | -12 |

sidetone gain control

The values in the sidetone PGA control registers control the sidetone gain. Sidetone gain is set from -12 dB to -24 dB in 2-dB steps through the I²C interface. Sidetone can be muted by setting bit 7 of the power control register. The default sidetone gain is -12 dB.

Table 4. Sidetone Gain Control

| BIT NAME | | | RELATIVE GAIN | | | |
|----------|-----|-----|---------------|-----|-------|------|
| ST2 | ST1 | ST0 | MIN | TYP | MAX | UNIT |
| 0 | 0 | 0 | -12.2 | -12 | -11.8 | dB |
| 0 | 0 | 1 | -14.2 | -14 | -13.8 | dB |
| 0 | 1 | 0 | -16.2 | -16 | -15.8 | dB |
| 0 | 1 | 1 | -18.2 | -18 | -17.8 | dB |
| 1 | 0 | 0 | -20.2 | -20 | -19.8 | dB |
| 1 | 0 | 1 | -22.2 | -22 | -21.8 | dB |
| 1 | 1 | 0 | -24.2 | -24 | -23.8 | dB |

PRINCIPLES OF OPERATION
receive operation (continued)**receive volume control**

The values in the volume control PGA control registers provide volume control for the earphone. Volume control gain is set from 0 dB to –18 dB in 2-dB steps through the I²C interface. The default RX volume control gain is 0 dB.

Table 5. RX Volume Control

| BIT NAME | | | | RELATIVE GAIN | | | UNIT |
|----------|-----|-----|-----|---------------|-----|-------|------|
| RV3 | RV2 | RV1 | RV0 | MIN | TYP | MAX | |
| 0 | 0 | 0 | 0 | –0.2 | 0 | 0.2 | dB |
| 0 | 0 | 0 | 1 | –2.2 | –2 | –1.8 | dB |
| 0 | 0 | 1 | 0 | –4.2 | –4 | –3.8 | dB |
| 0 | 0 | 1 | 1 | –6.2 | –6 | –5.8 | dB |
| 0 | 1 | 0 | 0 | –8.2 | –8 | –7.8 | dB |
| 0 | 1 | 0 | 1 | –10.2 | –10 | –9.8 | dB |
| 0 | 1 | 1 | 0 | –12.2 | –12 | –11.8 | dB |
| 0 | 1 | 1 | 1 | –14.2 | –14 | –13.8 | dB |
| 1 | 0 | 0 | 0 | –16.2 | –16 | –15.8 | dB |
| 1 | 0 | 0 | 1 | –18.2 | –18 | –17.8 | dB |

earphone amplifier

The analog signal can be routed to either of two earphone amplifiers: one with a differential output (EAR1ON and EAR1OP) capable of driving a 8-Ω load, or one with a single-ended output (EAR2O) capable of driving a 8-Ω load.

earphone mute function

Muting can be selected by setting bit 3 of the power control register through the I²C interface.

receive PCM data format

- Companded mode: 8 bits are received, the most significant (MSB) first.
- Linear mode: 15 bits are received, MSB first.

PRINCIPLES OF OPERATION

receive operation (continued)

Table 6. Receive-Data Bit Definitions

| BIT NO. | COMPANDED MODE | LINEAR MODE |
|---------|----------------|-------------|
| 1 | CD7 | LD14 |
| 2 | CD6 | LD13 |
| 3 | CD5 | LD12 |
| 4 | CD4 | LD11 |
| 5 | CD3 | LD10 |
| 6 | CD2 | LD9 |
| 7 | CD1 | LD8 |
| 8 | CD0 | LD7 |
| 9 | – | LD6 |
| 10 | – | LD5 |
| 11 | – | LD4 |
| 12 | – | LD3 |
| 13 | – | LD2 |
| 14 | – | LD1 |
| 15 | – | LD0 |
| 16 | – | — |

Transmit channel gain control bits always follow the PCM data in time:

CD7-CD0 = data word in companded mode

LD14-LD0 = data word in linear mode

DTMF generator operation and interface

The DTMF circuit generates the summed DTMF tones for push button dialing and provides the PDM output for the BUZZCON user-alert tone. The integer value is determined by the formula round tone [Freq (Hz)/resolution (Hz)]. The integer value is loaded into one of two 8-bit registers, high-tone register (04) or low-tone register (05). The tone output is 2 dB higher when applied to the high-tone register (04). When generating DTMF tones, the high-frequency value must be applied to the high tone register (04) and the low DTMF value to the low-tone register.

The DTMF frequency resolution is controlled by the auxiliary register (06) bits 2, 3, 4, and 5. When the resolution is set to 7.8125 Hz, the frequency range can be up to 1992.2 Hz. A wider range can be accomplished (for example, 2x or 4x) by selecting lower resolutions of 15.625 Hz or 31.250 Hz. The gain setting is controlled by the RXPGA gain control. This register applies the required gain to obtain MUX control during tone mode operation. Table 3 shows the relationship of the two gain settings.

PRINCIPLES OF OPERATION
DTMF generator operation and interface (continued)**Table 7. Typical DTMF and Single Tone Control**

| DT7 | DT6 | DT5 | DT4 | DT3 | DT2 | DT1 | DT0 | INTEGER VALUE | TONE FUNCTION | TONE/Hz |
|-----|-----|-----|-----|-----|-----|-----|-----|---------------|---------------|---------|
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 89 | DTMF Low | 697 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 99 | DTMF Low | 770 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 109 | DTMF Low | 852 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 120 | DTMF Low | 941 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 155 | DTMF High | 1209 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 171 | DTMF High | 1336 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 189 | DTMF High | 1477 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 209 | DTMF High | 1633 |

Tones from the DTMF generator block are present at all outputs and are controlled by enabling or disabling the individual output ports. The values that determine the tone frequency are loaded into the tone registers (high and low) as two separate values.

The values loaded into the tone registers initiate an iterative table look-up function, placing a 6-bit or 7-bit in twos-complement value into the the tone registers. There is a 2-dB difference in the resulting output of the two registers, the high-tone register having the greater result.

In the case of low-tone signal, the tone generator outputs a 6-bit integer with a maximum code of 31 (011111). However, the DTMF output is an 8-bit integer. Therefore, two zeros are padded to the MSB position, which results in 31 (00011111). On the other hand, the receive channel requires a 15-bit integer, the input 3968 (000111110000000). Since the maximum digital value of receive channel is 16383 (011111111111111), the maximum low-tone signal is designed to be –12.32 dB below the full digital scale.

$$20 \log \left(\frac{3968}{16383} \right)^2 = -12.32 \text{ dB} \quad (1)$$

In the case of high-tone signal, the tone generator outputs a 7-bit integer with a maximum code of 39 (0100111). The DTMF, therefore, pads a zero to the MSB and generates an 8-bit integer (00100111). In order to send the digital code to receive channel, it is converted to a 15-bit integer with seven more zeros padded to LSB position and biased as 4992 (001001110000000). Therefore, the maximum high-tone signal is designed to be –10.32 dB below the full digital scale.

$$20 \log \left(\frac{4992}{16383} \right)^2 = -10.32 \text{ dB} \quad (2)$$

In the case of DTMF output, the tone generator outputs an 8-bit integer with the maximum code level of 70 (01000110). This output is converted to a 15-bit code with the value of 8960 (010001100000000). Therefore, the maximum output of DTMF is designed to be –5.24 dB below the full digital scale.

$$20 \log \left(\frac{8960}{16383} \right)^2 = -5.24 \text{ dB} \quad (3)$$

PRINCIPLES OF OPERATION

buzzer logic section

The single-ended output BUZZCON is a PDM signal intended to drive a buzzer through an external driver transistor. The PDM begins as a selected DTMF tone, generated and passed through the receive D/A channel and fed back to the transmit channel analog modulator, where a PDM signal is generated and routed to the BUZZCON output.

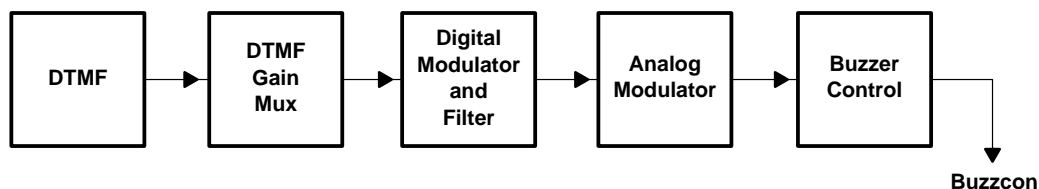


Figure 13. Buzzer Driver System Architecture

support section

The clock generator and control circuit use the master clock input (MCLK) to generate internal clocks to drive internal counters, filters, and convertors. Register control data is written into and read back from the PCM codec registers via the control interface.

I²C-bus protocols

The PCM codec serial interface is designed to be I²C bus-compatible and operates in the slave mode when CE is high. This interface consists of the following terminals:

- SCL: I²C-bus serial clock. This input synchronizes the control data transfer to and from the codec.
- SDA: I²C-bus serial address/data input/output. This is a bidirectional terminal that transfers register control addresses and data into and out of the codec. It is an open drain terminal and therefore requires a pullup resistor to V_{CC} (typical 10 kΩ for 100 kHz).

TLV320AIC1110 has a fixed device select address of (E2)HEX for write mode and (E3)HEX for read mode.

For normal data transfer, SDA is allowed to change only when SCL is low. Changes when SCL is high are reserved for indicating the start and stop conditions.

Data transfer may be initiated only when the bus is not busy. During data transfer, the data line must remain stable whenever the clock line is at high. Changes in the data line while the clock line is at high are interpreted as a start or stop condition.

Table 8. I²C-Bus Conditions

| CONDITION | STATUS | DESCRIPTION |
|-----------|---------------------|--|
| A | Bus not busy | Both data and clock lines remain at high. |
| B | Start data transfer | A high to low transition of the SDA line while the clock (SCL) is high determines a start condition. All commands must proceed from a start condition. |
| C | Stop data transfer | A low to high transition of the SDA line while the clock (SCL) is high determines a stop condition. All operations must end with a stop condition. |
| D | Data valid | The state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the high period of the clock signal. |

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

PRINCIPLES OF OPERATION

I²C-bus protocols (continued)

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes, transferred between the start and stop conditions, is determined by the master device (microprocessor).

When addressed, the PCM codec generates an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

The PCM codec must pull down the SDA line during the acknowledge clock pulse so that the SDA line is at stable low state during the high period of the acknowledge related clock pulse. Setup and hold times must be taken into account. During read operations, the master device must signal an end of data to the slave by not generating an acknowledge bit on the last byte that was clocked out of the slave. In this case, the slave (PCM codec) must leave the data line high to enable the master device to generate the stop condition.

clock frequencies and sample rates

A fixed PCMSYN rate of 8 kHz determines the sampling rate.

register map addressing

| | REG | BITS | | | | | | | |
|---------------|-----|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| | | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
| Power control | 00 | Sidetone En | TXEn | RX TX En | MICSEL | BIASEn | RXEn | EAROUT Sel | PWRUP |
| Mode control | 01 | Comp Sel | TMEEn | PCMLB | Comp En | BUZZEn | RXFLTR En | TXFLTR En | TXSLOPE En |
| TXPGA | 02 | X | TP3 | TP2 | TP1 | TP0 | ST2 | ST1 | ST0 |
| RXPGA | 03 | RP3 | RP2 | RP1 | RP0 | RV3 | RV2 | RV1 | RV0 |
| High DTMF | 04 | HIFREQ Sel7 | HIFREQ Sel6 | HIFREQ Sel5 | HIFREQ Sel4 | HIFREQ Sel3 | HIFREQ Sel2 | HIFREQ Sel1 | HIFREQ Sel0 |
| Low DTMF | 05 | LOFREQ Sel7 | LOFREQ Sel6 | LOFREQ Sel5 | LOFREQ Sel4 | LOFREQ Sel3 | LOFREQ Sel2 | LOFREQ Sel1 | LOFREQ Sel0 |
| AUX | 06 | MCLK Detect | RXPGA2† | DTMFH1 | DTMFH0 | DTML1 | DTMFL0 | AMVX | MCLK sel |

† For voice mode only

register power-up defaults

| | REG | BITS | | | | | | | |
|--------------------|-----|------|----|----|----|----|----|----|----|
| | | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
| Power control (1)† | 00 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| Power control (2)‡ | 00 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Mode control | 01 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| TXPGA | 02 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| RXPGA | 03 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| High DTMF | 04 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Low DTMF | 05 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| AUX | 06 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

† 1. Value when PWRUPSEL = 0

‡ 2. Value when PWRUPSEL = 1

PRINCIPLES OF OPERATION

register map

Table 9. Power Control Register: Address (00) HEX

| BIT NUMBER | | | | | | | | DEFINITIONS |
|------------|---|---|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | Default setting PWRUPSEL = 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | Default setting PWRUPSEL = 1 |
| X | X | X | X | X | X | X | 0 | Reference system, power down |
| X | X | X | X | X | X | X | 1 | Reference system, power up |
| X | X | X | X | X | X | 1 | X | EAR AMP1 selected, EAR AMP2 power down |
| X | X | X | X | X | X | 0 | X | EAR AMP2 selected, EAR AMP1 power down |
| X | X | X | X | X | 0 | X | X | Receive channel enabled |
| X | X | 0 | X | X | 1 | X | X | Receive channel muted |
| X | X | 1 | X | X | 1 | X | 0 | Receive channel, power down |
| X | X | X | X | 1 | X | X | X | Micbias enable |
| X | X | X | X | 0 | X | X | X | Micbias disable |
| X | X | X | 1 | X | X | X | X | MIC1 selected |
| X | X | X | 0 | X | X | X | X | MIC2 selected |
| X | 0 | X | X | X | X | X | X | Transmit channel enabled |
| X | 1 | 0 | X | X | X | X | X | Transmit channel muted |
| X | 1 | 1 | X | X | X | X | X | Transmit channel power down |
| 0 | X | X | X | X | X | X | X | Sidetone enabled |
| 1 | X | X | X | X | X | X | X | Sidetone muted |

Table 10. Mode Control Register: Address (01) HEX

| BIT NUMBER | | | | | | | | DEFINITIONS |
|------------|---|---|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | Default setting |
| X | X | X | X | X | X | 0 | 0 | TX channel high-pass filter enabled and slope filter enabled |
| X | X | X | X | X | X | 0 | 1 | TX channel high-pass filter enabled and slope filter disabled |
| X | X | X | X | X | X | 1 | 0 | TX channel high-pass filter disabled and slope filter enabled |
| X | X | X | X | X | X | 1 | 1 | TX channel high-pass filter disabled and slope filter disabled |
| X | X | X | X | X | 0 | X | X | RX channel high-pass filter disabled (low pass only) |
| X | X | X | X | X | 1 | X | X | RX channel high-pass filter enabled |
| X | X | X | X | 0 | X | X | X | BUZZCON disabled |
| X | X | X | X | 1 | X | X | X | BUZZCON enabled |
| X | X | X | 0 | X | X | X | X | Linear mode selected |
| 1 | X | X | 1 | X | X | X | X | A-law companding mode selected |
| 0 | X | X | 1 | X | X | X | X | μ-law companding mode selected |
| X | X | 0 | X | X | X | X | X | TX and RX channels normal mode |
| X | X | 1 | X | X | X | X | X | PCM loopback mode |
| X | 0 | X | X | X | X | X | X | Tone mode disabled |
| X | 1 | X | X | X | X | X | X | Tone mode enabled |

PRINCIPLES OF OPERATION
register map (continued)

Transmit PGA and sidetone control register: Address (02)HEX

Bit definitions:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFINITION |
|---|-----|-----|-----|-----|-----|-----|-----|-------------------------|
| X | TP3 | TP2 | TP1 | TP0 | ST2 | ST1 | ST0 | See Table 2 and Table 4 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Default setting |

Receive volume control register: Address (03)HEX

Bit definitions:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFINITION |
|-----|-----|-----|-----|-----|-----|-----|-----|-------------------------|
| RP3 | RP2 | RP1 | RP0 | RV3 | RV2 | RV1 | RV0 | See Table 3 and Table 5 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Default setting |

High tone selection control register: Address (04)HEX

Bit definitions:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFINITION |
|---|---|---|---|---|---|---|---|--------------------|
| X | X | X | X | X | X | X | X | DTMF (see Table 7) |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Default setting |

Low tone selection control register: Address (05)HEX

Bit definitions :

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFINITION |
|---|---|---|---|---|---|---|---|--------------------|
| X | X | X | X | X | X | X | X | DTMF (see Table 7) |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Default setting |

Auxiliary register: Address (06)HEX

Bit definitions:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFINITION |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Default |
| X | X | X | X | X | X | X | 0 | MCLK is set to 2.048 MHz |
| X | X | X | X | X | X | X | 1 | MCLK is set to 128 MHz |
| X | X | X | X | X | X | 0 | X | Analog switch output is set to OUT2 |
| X | X | X | X | X | X | 1 | X | Analog switch output is set to OUT1 |
| X | X | X | X | 0 | 0 | X | X | Low tone frequency resolution is set to 7.8125 Hz |
| X | X | X | X | 0 | 1 | X | X | Low tone frequency resolution is set to 15.625 Hz |
| X | X | X | X | 1 | 0 | X | X | Low tone frequency resolution is set to 31.250 Hz |
| X | X | 0 | 0 | X | X | X | X | High tone frequency resolution is set to 7.8125 Hz |
| X | X | 0 | 1 | X | X | X | X | High tone frequency resolution is set to 15.625 Hz |
| X | X | 1 | 0 | X | X | X | X | High tone frequency resolution is set to 31.250 Hz |
| X | 0 | X | X | X | X | X | X | Receiver channel gain, RXPGA2 is equal to 0 dB, voice mode only |
| X | 1 | X | X | X | X | X | X | Receiver channel gain, RXPGA2 is equal to 6 dB, voice mode only |
| 0 | X | X | X | X | X | X | X | MCLK detector is powered ON |
| 1 | X | X | X | X | X | X | X | MCLK detector is powered OFF |

PRINCIPLES OF OPERATION

using PCM codec as a general-purpose PCM codec

In situations when a general-purpose PCM codec is needed and programming features are not necessary, the receive and transmit channels can be enabled for voice mode only by setting the powerup select pin to V_{CC} level.

When set to default, the following features are activated:

- REF is powered up
- Ear amp1 selected, Ear amp 2 = OFF
- Receive channel enabled
- MIC bias enabled
- MIC 2 selected
- Transmit channel enabled
- Side tone enabled, Gain = -12 dB
- TX channel high pass filter disabled
- TX channel slope filter enabled
- RX channel HP filter disabled (low pass only)
- Buzzcon disabled
- Linear mode only
- TX and RX channel normal mode (no loopback)
- Tone mode disabled (voice mode only)
- MIC amp 1 gain = 23.5 dB
 MIC amp 2 gain = 6 dB
TX PGA gain = 0 dB
 Total TX gain = 29.5 dB
- Receive PGA = -4 dB
 Receive PGA 2 = 0 dB
Volume = 0 dB
 Total RX gain = -4 dB
- Clock = 2.048 MHz

PRINCIPLES OF OPERATION
PCM codec device comparisons

| | TLV320AIC1103 | TLV320AIC1110 |
|-----------------------------|----------------------------|--------------------------------|
| Single tone frequency range | To 2 kHz | To 8 kHz |
| Transmit channel gain range | 13.5 dB to 35.5 dB | 19.5 dB to 41.5 dB |
| Receive channel gain range | – 24 dB to 6 dB | – 24 dB to 12 dB |
| PCMCLK rate | 2.048 MHz | 128 kHz or 2.048 MHz |
| Device pin out | Backward compatible (TQFP) | |
| Control registers | Backward compatible | |
| Number of registers | 6 | 7 |
| Control interface | I ² C | I ² C |
| Analog switch | No | Yes |
| Earout driving impedance | 32 Ω | 8-32 Ω |
| DTMF | Yes | Yes |
| Tone resolution (Hz) | 7.8125 | 7.8125 15.625 31.25 |
| Packages | TQFP | TQFP, MicroStar Junior BGA™ |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|----------------------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLV320AIC1110PBS | ACTIVE | TQFP | PBS | 32 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | AIC1110 | Samples |
| TLV320AIC1110PBSR | ACTIVE | TQFP | PBS | 32 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | AIC1110 | Samples |
| TLV320AIC1110ZQER | LIFEBUY | BGA MICROSTAR JUNIOR | ZQE | 80 | 2500 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 85 | AIC1110 | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



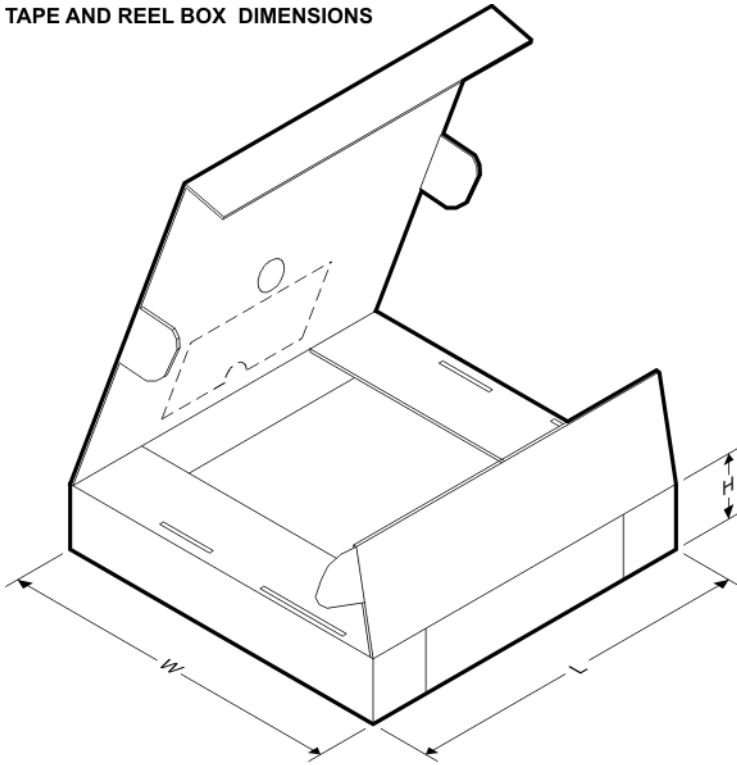
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|----------------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV320AIC1110PBSR | TQFP | PBS | 32 | 1000 | 330.0 | 16.4 | 7.2 | 7.2 | 1.5 | 12.0 | 16.0 | Q2 |
| TLV320AIC1110ZQER | BGA MICROSTAR JUNIOR | ZQE | 80 | 2500 | 330.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|----------------------|-----------------|------|------|-------------|------------|-------------|
| TLV320AIC1110PBSR | TQFP | PBS | 32 | 1000 | 350.0 | 350.0 | 43.0 |
| TLV320AIC1110ZQER | BGA MICROSTAR JUNIOR | ZQE | 80 | 2500 | 350.0 | 350.0 | 43.0 |

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