



**THE DATASHEET OF
TLC7701IDRG4**



Micropower Supply Voltage Supervisors

 Check for Samples: [TLC7701](#), [TLC7725](#), [TLC7703](#), [TLC7733](#), [TLC7705](#)

FEATURES

- Power-On Reset Generator
- Automatic Reset Generation After Voltage Drop
- Precision Voltage Sensor
- Temperature-Compensated Voltage Reference
- Programmable Delay Time by External Capacitor
- Supply Voltage Range . . . 2 V to 6 V
- Defined RESET Output from $V_{DD} \geq 1$ V
- Power-Down Control Support for Static RAM With Battery Backup
- Maximum Supply Current of 16 μ A
- Power Saving Totem-Pole Outputs
- Temperature Range . . . Up to -55°C to 125°C

APPLICATIONS

- Medical Imaging

DESCRIPTION

The TLC77xx family of micropower supply voltage supervisors provide reset control, primarily in microcomputer and microprocessor systems.

During power-on, $\overline{\text{RESET}}$ is asserted when V_{DD} reaches 1 V. After minimum V_{DD} (≥ 2 V) is established, the circuit monitors SENSE voltage and keeps the reset outputs active as long as SENSE voltage ($V_{I(\text{SENSE})}$) remains below the threshold voltage. An internal timer delays return of the output to the inactive state to ensure proper system reset. The delay time, t_d , is determined by an external capacitor:

$$t_d = 2.1 \times 10^4 \times C_T$$

Where

C_T is in farads

t_d is in seconds

Except for the TLC7701, which can be customized with two external resistors, each supervisor has a fixed sense threshold voltage set by an internal voltage divider. When SENSE voltage drops below the threshold voltage, the outputs become active and stay in that state until SENSE voltage returns above threshold voltage and the delay time, t_d , has expired.

DRB PACKAGE
(TOP VIEW)



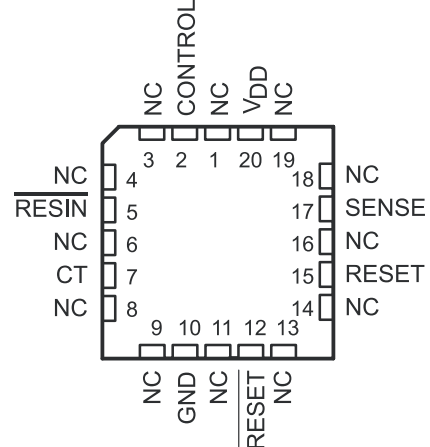
D, JG, P OR PW PACKAGE
(TOP VIEW)



U PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

In addition to the power-on-reset and undervoltage-supervisor function, the TLC77xx adds power-down control support for static RAM. When CONTROL is tied to GND, RESET will act as active high. The voltage monitor contains additional logic intended for control of static memories with battery backup during power failure. By driving the chip select (\overline{CS}) of the memory circuit with the RESET output of the TLC77xx and with the CONTROL driven by the memory bank select signal ($\overline{CSH1}$) of the microprocessor (see Figure 10), the memory circuit is automatically disabled during a power loss. (In this application the TLC77xx power has to be supplied by the battery.)

The TLC77xxL is characterized for operation over a temperature range of -40°C to 85°C ; the TLC77xxQ is characterized for operation over a temperature range of -40°C to 125°C ; and the TLC77xxM is characterized for operation over the full Military temperature range of -55°C to 125°C .

The 3x3 mm DRB package is also available as a non-magnetic package for medical imaging application.

AVAILABLE OPTIONS

| T_A | THRESHOLD VOLTAGE (V) | PACKAGED DEVICES | | | | | | |
|--|-----------------------|----------------------------------|-------------------|------------------|---------------------------|-----------------|---|-----------------------------|
| | | SMALL OUTLINE (D) ⁽¹⁾ | CHIP CARRIER (FK) | CERAMIC DIP (JG) | CERAMIC DUAL FLATPACK (U) | PLASTIC DIP (P) | THIN SHRINK SMALL OUTLINE (PW) ⁽²⁾ | SMALL OUTLINE NO LEAD (DRB) |
| -40°C to 85°C | 1.1 | TCLC7701ID | — | — | — | TCLC7701IP | TCLC7701IPWR | — |
| | 2.25 | TLC7725ID | — | — | — | TLC7725IP | TLC7725IPWR | — |
| | 2.63 | TLC7703ID | — | — | — | TLC7703IP | TLC7703IPWR | — |
| | 2.93 | TLC7733ID | — | — | — | TLC7733IP | TLC7733IPWR | — |
| | 4.55 | TLC7705ID | — | — | — | TLC7705IP | TLC7705IPWR | — |
| | 1.1 | TLC7701IDBR | — | — | — | — | — | TLC7701IDRBT-NM |
| -40°C to 125°C | 1.1 | TLC7701QD | — | — | — | TLC7701QP | TLC7701QPWR | — |
| | 2.25 | TLC7725QD | — | — | — | TLC7725QP | TLC7725QPWR | — |
| | 2.63 | TLC7703QD | — | — | — | TLC7703QP | TLC7703QPWR | — |
| | 2.93 | TLC7733QD | — | — | — | TLC7733QP | TLC7733QPWR | — |
| | 4.55 | TLC7705QD | — | — | — | TLC7705QP | TLC7705QPWR | — |
| -55°C to 125°C | 2.93 | — | — | — | — | — | — | — |
| | 4.55 | — | — | — | — | — | — | — |

(1) The D package is available taped and reeled. Add the suffix R to the device type when ordering (e.g., TLC7705QDR).

(2) The PW package is only available left-end taped and reeled (indicated by the R suffix on the device type; e.g., TLC7705QPWR).

Table 1. FUNCTION TABLE

| CONTROL | \overline{RESIN} | $V_{I(SENSE)} > V_{IT+}$ | \overline{RESET} | RESET |
|---------|--------------------|--------------------------|--------------------|------------------|
| L | L | False | H | L |
| L | L | True | H | L |
| L | H | False | H | L |
| L | H | True | L ⁽¹⁾ | H ⁽¹⁾ |
| H | L | False | H | L |
| H | L | True | H | L |
| H | H | False | H | L |
| H | H | True | H | H ⁽¹⁾ |

(1) RESET and \overline{RESET} states shown are valid for $t > t_d$.

LOGIC SYMBOL



(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

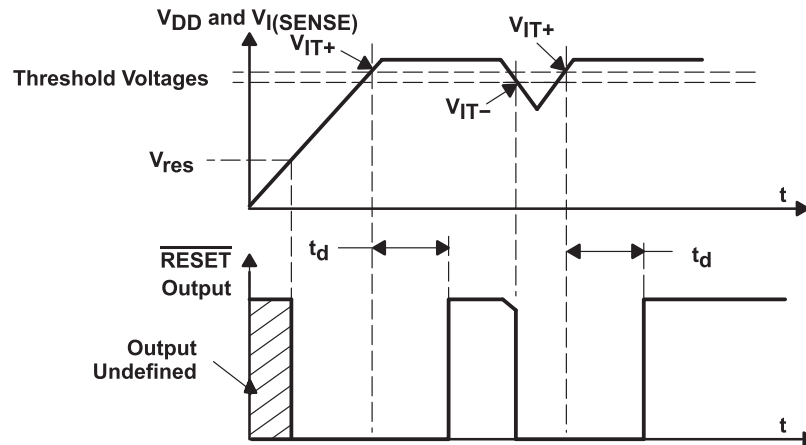
FUNCTIONAL BLOCK DIAGRAM



† Outputs are totem-pole configuration. External pullup or pulldown resistors are not required.
‡ Nominal values:

| | R1 (Typ) | R2 (Typ) |
|---------|----------------|----------------|
| TLC7701 | 0 | ∞ |
| TLC7725 | 600 k Ω | 600 k Ω |
| TLC7703 | 698 k Ω | 502 k Ω |
| TLC7733 | 750 k Ω | 450 k Ω |
| TLC7705 | 910 k Ω | 290 k Ω |

TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | VALUE | UNIT |
|------------------|---|------------------------------|---------------|
| V _{DD} | Supply voltage ⁽²⁾ | 7 | V |
| | Input voltage range, CONTROL, RESIN, SENSE ⁽²⁾ | –0.3 to 7 | V |
| I _{OL} | Maximum low output current | 10 | mA |
| I _{OH} | Maximum high output current, | –10 | mA |
| I _{IK} | Input clamp current, (VI < 0 or VI > VDD) | ±10 | mA |
| I _{OK} | Output clamp current, (VO 0 or VO > VDD) | ±10 | mA |
| | Continuous total power dissipation | See Dissipation Rating Table | |
| T _A | Operating free-air temperature range | TL77xxI | –40 to 84 °C |
| | | TL77xxQ | –40 to 125 °C |
| | | TL77xxM | –55 to 125 °C |
| T _{stg} | Storage temperature range | –65 to 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.

DISSIPATION RATINGS

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE T _A = 25°C | T _A = 85°C POWER RATING | T _A = 125°C POWER RATING |
|---------|---------------------------------------|--|---------------------------------------|--|
| D | 725 mW | 5.8 mW/°C | 377 mW | 145 mW |
| DRB | | | | |
| FK | 1375 mW | 11.0 mW/°C | 715 mW | 275 mW |
| JG | 1050 mW | 8.4 mW/°C | 546 mW | 210 mW |
| P | 1000 mW | 8.0 mW/°C | 520 mW | 200 mW |
| PW | 525 mW | 4.2 mW/°C | 273 mW | 105 mW |
| U | 700 mW | 5.5 mW/°C | 370 mW | 150 mW |

RECOMMENDED OPERATING CONDITIONS

at specified temperature range

| | | MIN | MAX | UNIT |
|-----------------|--|---------------------|---------------------|-------|
| V _{DD} | Supply voltage | 2 | 6 | V |
| V _I | Input voltage | 0 | V _{DD} | V |
| V _{IH} | High-level input voltage at $\overline{\text{RESIN}}$ and CONTROL ⁽¹⁾ | 0.7×V _{DD} | | V |
| V _{IL} | Low-level input voltage at $\overline{\text{RESIN}}$ and CONTROL ⁽¹⁾ | | 0.2×V _{DD} | V |
| I _{OH} | High-level output current | | –2 | mA |
| I _{OL} | Low-level output current | | 2 | mA |
| Δt/ΔV | input transition rise and fall rate at $\overline{\text{RESIN}}$ and CONTROL | | 100 | ns/ V |
| T _A | Operating free-air temperature range | TL77xxI | –40 | 85 |
| | | TL77xxQ | –40 | 125 |
| | | TL77xxM | –55 | 125 |

- (1) To ensure a low supply current, V_{IL} should be kept < 0.3 V and V_{IH} > V_{DD} – 0.3 V.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions⁽¹⁾ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TLC77xx | | | UNIT | |
|--------------------|--|---|---|------|------|------|----|
| | | | MIN | TYP | MAX | | |
| V _{OH} | High-level output voltage | I _{OH} = -20 μA | V _{DD} = 2 V | 1.8 | | V | |
| | | | V _{DD} = 2.7 V | 2.5 | | | |
| | | I _{OH} = 2 -mA | V _{DD} = 4.5 V | 4.3 | | | |
| | | | V _{DD} = 4.5 V | 3.7 | | | |
| V _{OL} | Low-Level output voltage | I _{OL} = 20 μA | V _{DD} = 2 V | | 0.2 | V | |
| | | | V _{DD} = 2.7 V | | 0.2 | | |
| | | I _{OL} = 2 mA | V _{DD} = 4.5 V | | 0.2 | | |
| | | | V _{DD} = 4.5 V | | 0.5 | | |
| V _{IT-} | Negative-going input threshold voltage, SENSE ⁽²⁾ | V _{DD} = 2 V to 6 V | TCLC7701 | 1.04 | 1.1 | 1.16 | mV |
| | | | TLC7725 | 2.18 | 2.25 | 2.32 | |
| | | | TLC7703 | 2.56 | 2.63 | 2.70 | |
| | | | TLC7733 | 2.86 | 2.93 | 3 | |
| | | | TLC7705 | 4.47 | 4.55 | 4.63 | |
| V _{hus} | Hysteresis voltage, SENSE | V _{DD} = 2 V to 6 V | TCLC7701 | 30 | | mV | |
| | | | TLC7725 | | | | |
| | | | TLC7703 | 70 | | | |
| | | | TLC7733 | | | | |
| | | | TLC7705 | | | | |
| V _{res} | Power-up reset voltage ⁽³⁾ | I _{OL} = 20 μA | | | 1 | V | |
| I _i | Input current | RESIN | V _I = 0 V to V _{DD} | | 2 | μA | |
| | | CONTROL | V _I = V _{DD} | 7 | 15 | | |
| | | SENSE | V _I = 5 V | 5 | 10 | | |
| | | SENSE, TLC7701 only | V _I = 5 V | | 2 | | |
| I _{DD} | Supply current | RESIN = V _{DD} , SENSE = V _{DD} ≥ V _{ITmax} + 0.2 V, CONTROL = 0 V, Outputs open | | 9 | 16 | μA | |
| I _{DD(d)} | Supply current during t _d | V _{DD} = 5 V, V _{CT} = 0, RESIN = V _{DD} , SENSE = V _{DD} , CONTROL = 0 V, Outputs open | | 120 | 150 | μA | |
| C _i | Input capacitance, SENSE | V _I = 0 V to V _{DD} | | 50 | | pF | |

(1) All characteristics are measured with C_T = 0.1 μF.

(2) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 mF) should be connected near the supply terminals.

(3) The lowest supply voltage at which RESET becomes active. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology. Rise time of V_{DD} ≥ 15 μs/V.

ELECTRICAL CHARACTERISTICS

 over recommended operating conditions⁽¹⁾ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | TLC77xxM | | | UNIT | |
|---------------------|--|---|--|---|---|-----|---------|-----|
| | | | | MIN | TYP ⁽²⁾ | MAX | | |
| V_{OH} | High-level output voltage | $I_{OH} = -20 \mu A$ | $V_{DD} = 2 V$ | $T_A = 25^\circ C$ | 1.8 | | V | |
| | | | | $T_A = -55^\circ C \text{ to } 125^\circ C$ | 1.7 | | | |
| | | | $V_{DD} = 2.7 V$ | $T_A = 25^\circ C$ | 2.5 | | V | |
| | | | | $T_A = -55^\circ C \text{ to } 125^\circ C$ | 2.3 | | | |
| | | | $V_{DD} = 4.5 V$ | $T_A = 25^\circ C$ | 4.3 | | V | |
| | | | | $T_A = -55^\circ C \text{ to } 125^\circ C$ | 4.2 | | | |
| $I_{OH} = -2 \mu A$ | $V_{DD} = 4.5 V$ | $T_A = 25^\circ C$ | 3.7 | | V | | | |
| | | $T_A = -55^\circ C \text{ to } 125^\circ C$ | 3.6 | | | | | |
| V_{OL} | Low-level output voltage | $I_{OL} = -20 \mu A$ | $V_{DD} = 2 V$ | $T_A = 25^\circ C$ | | 0.2 | V | |
| | | | | $T_A = -55^\circ C \text{ to } 125^\circ C$ | | 0.2 | | |
| | | | $V_{DD} = 2.7 V$ | $T_A = 25^\circ C$ | | 0.2 | V | |
| | | | | $T_A = -55^\circ C \text{ to } 125^\circ C$ | | 0.2 | | |
| | | | $V_{DD} = 4.5 V$ | $T_A = 25^\circ C$ | | 0.2 | V | |
| | | | | $T_A = -55^\circ C \text{ to } 125^\circ C$ | | 0.2 | | |
| | | | $I_{OL} = 2 mA$ | $V_{DD} = 4.5 V$ | $T_A = 25^\circ C$ | | 0.5 | V |
| | | | | | $T_A = -55^\circ C \text{ to } 125^\circ C$ | | 0.5 | |
| V_{IT-} | Negative-going input threshold voltage, SENSE ⁽³⁾ | TLC7733 | $V_{DD} = 2 V \text{ to } 6 V$ | 2.86 | 2.93 | 3.1 | V | |
| | | TLC7705 | | 4.3 | 4.5 | 4.8 | | |
| V_{hys} | Hysteresis voltage, SENSE | | $V_{DD} = 2 V \text{ to } 6 V$ | | 70 | | mV | |
| V_{res} | Power-up reset voltage ⁽²⁾ | | $I_{OL} = 20 \mu A$ | | | 1 | V | |
| I_i | Input current | RESIN | $V_i = 0 V \text{ to } V_{DD}$ | | | 2 | μA | |
| | | CONTROL | $V_i = V_{DD}$ | | 7 | 15 | | |
| | | SENSE | $V_i = 5 V$ | | 5 | 10 | | |
| | | SENSE, TLC7701 only | $V_i = 5 V$ | | | 2 | | |
| I_{DD} | Supply current | | RESIN = VDD, SENSE = $V_{DD} \geq V_{ITmax} + 0.2 V$ CONTROL = 0 V, Outputs open | | 9 | 16 | μA | |
| $I_{DD(d)}$ | Supply current during t_d | TLC7733 | $V_{CT} = 0$, RESIN = V_{DD} , CONTROL = 0 V, SENSE = V_{DD} , Outputs open | $V_{DD} = 3.3 V$ | | 250 | μA | |
| | | TLC7705 | | $V_{DD} = 5 V$ | | 120 | | 150 |
| C_i | Input capacitance, SENSE | | $V_i = 0 V \text{ to } V_{DD}$ | | | 50 | pF | |

 (1) All characteristics are measured with $C_T = 0.1 \mu F$.

 (2) Typical values apply at $T_A = 25^\circ C$.

(3) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 mF) should be connected near the supply terminals.

SWITCHING CHARACTERISTICS

at $V_{DD} = 5\text{ V}$, $R_L = 2\text{ k}\Omega$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | MEASURED | | TEST CONDITIONS | TLC77xx | | | UNIT |
|--|------------------------------------|---------------------------|--|---------|-----|-----|---------------|
| | FROM (INPUT) | TO (OUTPUT) | | MIN | TYP | MAX | |
| t_d Delay time | $V_{I(\text{SENSE})} \geq V_{IT+}$ | RESET and RESET | $\overline{\text{RESIN}} = 0.7 \times V_{DD}$, CONTROL = $0.2 \times V_{DD}$, $C_T = 100\text{ nF}$, $T_A = \text{Full range}$, See timing diagram | 1.1 | 2.1 | 4.2 | ms |
| t_{PLH} Propagation delay time, low-to-high-level output | SENSE | $\overline{\text{RESET}}$ | $V_{IH} = V_{IT+max} + 0.2\text{ V}$, $V_{IL} = V_{IT.min} - 0.2\text{ V}$, $\overline{\text{RESIN}} = 0.7 \times V_{DD}$, CONTROL = $0.2 \times V_{DD}$, CT = NC ⁽¹⁾ | 20 | | | μs |
| t_{PHL} Propagation delay time, high-to-low-level output | | $\overline{\text{RESET}}$ | | 5 | | | |
| t_{PLH} Propagation delay time, low-to-high-level output | | RESET | | 5 | | | |
| t_{PHL} Propagation delay time, high-to-low-level output | | RESET | | 20 | | | |
| t_{PLH} Propagation delay time, low-to-high-level output | $\overline{\text{RESIN}}$ | $\overline{\text{RESET}}$ | $V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.2 \times V_{DD}$, SENSE = $V_{IT+max} + 0.2\text{ V}$, CONTROL = $0.2 \times V_{DD}$, CT = NC ⁽¹⁾ | 20 | | | μs |
| t_{PHL} Propagation delay time, high-to-low-level output | | $\overline{\text{RESET}}$ | | 40 | | | |
| t_{PLH} Propagation delay time, low-to-high-level output | | RESET | | 45 | | | |
| t_{PHL} Propagation delay time, high-to-low-level output | | RESET | | 20 | | | |
| t_{PLH} Propagation delay time, low-to-high-level output | CONTROL | RESET | $V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.2 \times V_{DD}$, SENSE = $V_{IT+max} + 0.2\text{ V}$, $\overline{\text{RESIN}} = 0.7 \times V_{DD}$, CT = NC ⁽¹⁾ | 38 | | | ns |
| t_{PHL} Propagation delay time, high-to-low-level output | | | | 38 | | | |
| Low-level minimum pulse duration to switch RESET and $\overline{\text{RESET}}$ | SENSE | | $V_{IH} = V_{IT+max} + 0.2\text{ V}$, $V_{IL} = V_{IT.min} - 0.2\text{ V}$, $V_{IL} = 0.2 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$ | | | | |
| | $\overline{\text{RESIN}}$ | | | | | | |
| t_r Rise time | | RESET and RESET | 10% to 90% | | | | |
| t_f Fall time | | RESET and RESET | 90% to 10% | | | | |

(1) NC = No capacitor, and includes up to 100-pF probe and jig capacitance.

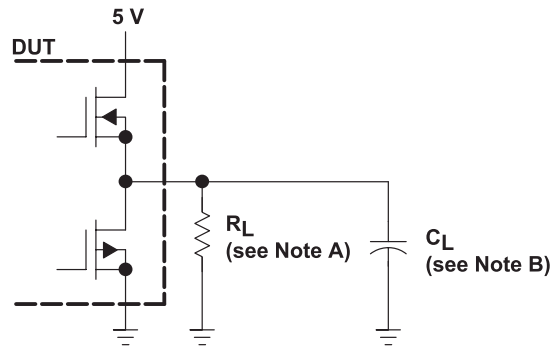
SWITCHING CHARACTERISTICS

 at $V_{DD} = 5\text{ V}$, $R_L = 2\text{ k}\Omega$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | MEASURED | | TEST CONDITIONS | T_A | TLC77xxM | | | UNIT |
|--|------------------------------------|-----------------|---|------------|---|-----|-----|---------------|
| | FROM (INPUT) | TO (OUTPUT) | | | MIN | TYP | MAX | |
| t_d Delay time | $V_{I(\text{SENSE})} \geq V_{IT+}$ | RESET and RESET | RESIN = 2.7 V, CONTROL = 0.4 V, $C_T = 100\text{ nF}$, See timing diagram | Full range | 1.1 | 2.1 | 4.2 | ms |
| t_{PLH} Propagation delay time, low-to-high-level output | SENSE | RESET | $V_{IH} = V_{IT+max} + 0.2\text{ V}$, $V_{IL} = V_{IT-min} - 0.2\text{ V}$, RESIN = 2.7 V, CONTROL = 0.4 V, CT = NC ⁽¹⁾ | 25°C | | | 20 | μs |
| | | Full range | | | | 24 | | |
| | | RESET | | 25°C | | | 5 | μs |
| | | Full range | | | | 7 | | |
| t_{PHL} Propagation delay time, high-to-low-level output | SENSE | RESET | $V_{IH} = V_{IT+max} + 0.2\text{ V}$, $V_{IL} = V_{IT-min} - 0.2\text{ V}$, RESIN = 2.7 V, CONTROL = 0.4 V, CT = NC ⁽¹⁾ | 25°C | | | 5 | μs |
| | | Full range | | | | 7 | | |
| | | RESET | | 25°C | | | 20 | μs |
| | | Full range | | | | 24 | | |
| t_{PLH} Propagation delay time, low-to-high-level output | RESIN | RESET | $V_{IH} = 2.7\text{ V}$, $V_{IL} = 0.4\text{ V}$, SENSE = $V_{IT+max} + 0.2\text{ V}$, CONTROL = 0.4 V, CT = NC ⁽¹⁾ | 25°C | | | 20 | μs |
| | | Full range | | | | 24 | | |
| | | RESET | | 25°C | | | 45 | ns |
| | | Full range | | | | 65 | | |
| t_{PHL} Propagation delay time, high-to-low-level output | RESIN | RESET | $V_{IH} = 2.7\text{ V}$, $V_{IL} = 0.4\text{ V}$, SENSE = $V_{IT+max} + 0.2\text{ V}$, CONTROL = 0.4 V, CT = NC ⁽¹⁾ | 25°C | | | 40 | ns |
| | | Full range | | | | 60 | | |
| | | RESET | | 25°C | | | 20 | μs |
| | | Full range | | | | 24 | | |
| t_{PLH} Propagation delay time, low-to-high-level output | CONTROL | RESET | $V_{IH} = 2.7\text{ V}$, $V_{IL} = 0.4\text{ V}$, SENSE = $V_{IT+max} + 0.2\text{ V}$, RESIN = 2.7 V, CT = NC ⁽¹⁾ | 25°C | | | 38 | ns |
| Full range | | | | | | 58 | | |
| t_{PHL} Propagation delay time, high-to-low-level output | CONTROL | RESET | $V_{IH} = 2.7\text{ V}$, $V_{IL} = 0.4\text{ V}$, SENSE = $V_{IT+max} + 0.2\text{ V}$, RESIN = 2.7 V, CT = NC ⁽¹⁾ | 25°C | | | 38 | ns |
| Full Range | | | | | | 58 | | |
| Low-level minimum pulse duration | SENSE | | $V_{IH} = V_{IT+max} + 0.2\text{ V}$, $V_{IL} = V_{IT-min} - 0.2\text{ V}$ | Full range | | | 3 | μs |
| | RESIN | | | | $V_{IL} = 0.4\text{ V}$, $V_{IH} = 2.7\text{ V}$ | | | |
| t_r Rise time | | RESET and RESET | 10% to 90% | Full range | | | 8 | ns/V |
| t_f Fall time | | | 90% to 10% | | | | 4 | |

(1) NC = No capacitor, and includes up to 100-pF probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. For switching characteristics, $R_L = 2\text{ k}\Omega$.
B. $C_L = 50\text{ pF}$ includes jig and probe capacitance.

Figure 1. RESET and $\overline{\text{RESET}}$ Output Configurations

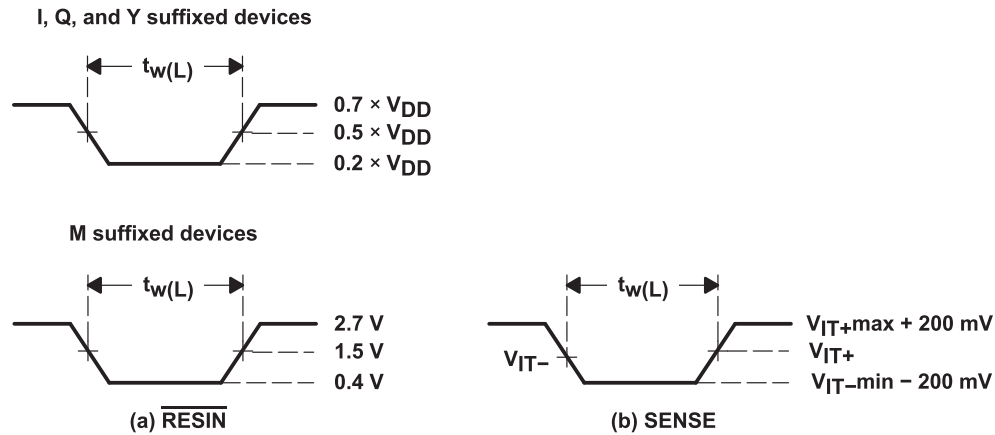


Figure 2. Input Pulse Definition Waveforms

TYPICAL CHARACTERISTICS

NORMALIZED INPUT THRESHOLD VOLTAGE
vs
TEMPERATURE



Figure 3.

SUPPLY CURRENT
vs
SUPPLY VOLTAGE



Figure 4.

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT



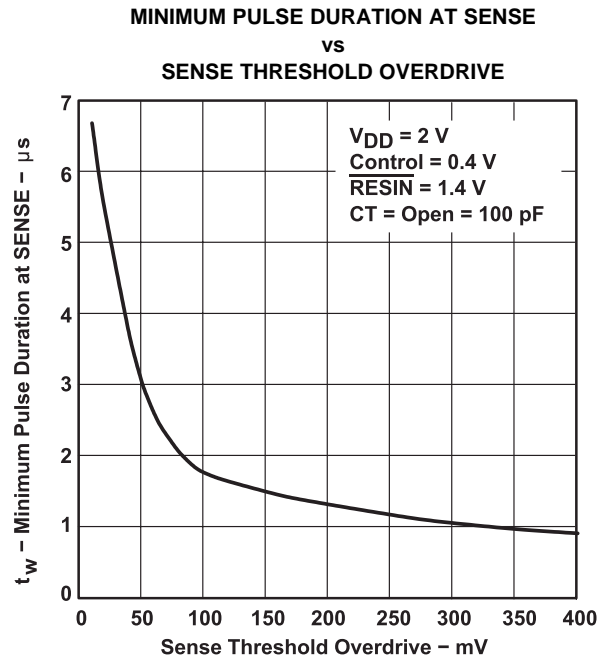
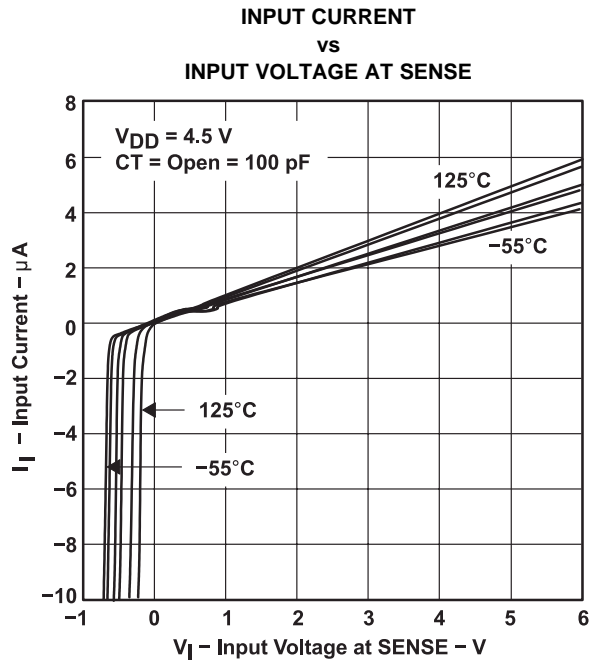
Figure 5.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT



Figure 6.

TYPICAL CHARACTERISTICS (continued)



APPLICATION INFORMATION

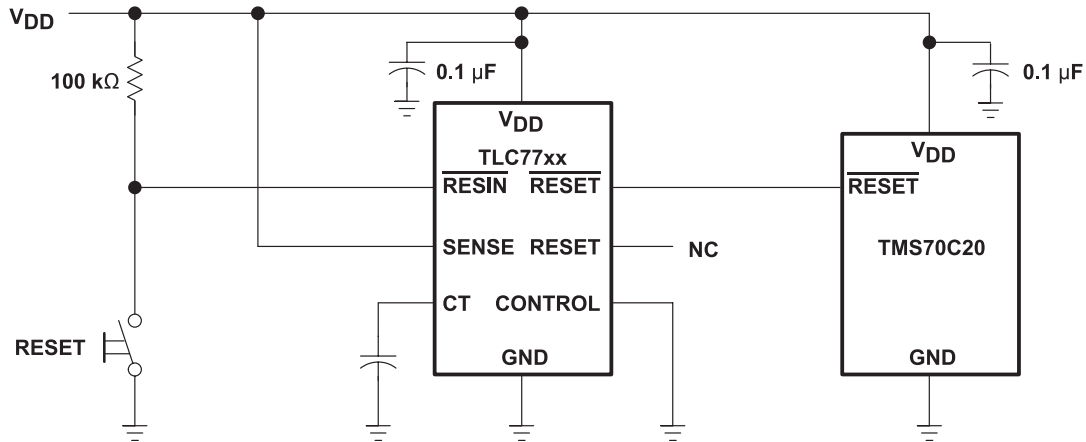


Figure 9. Reset Controller in a Microcomputer System

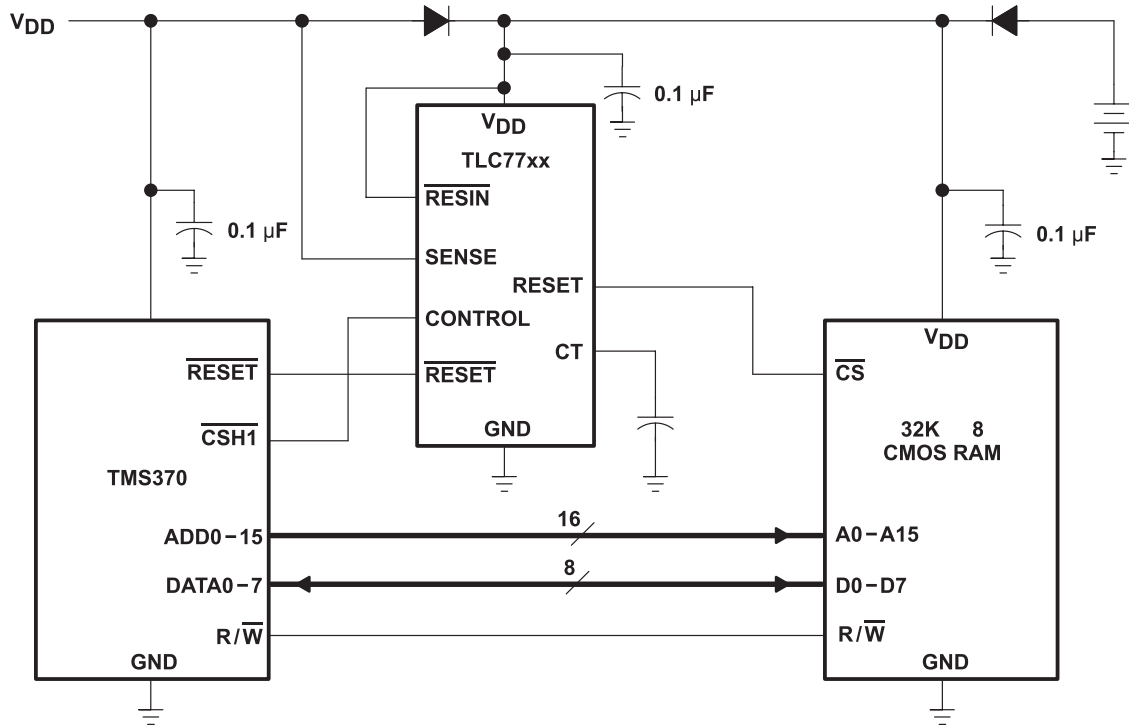


Figure 10. Data Retention During Power Down Using Static CMOS RAMs

Changes from Revision L (February 2003) to Revision M

Page

-
- Updated the DRB package Pin Out dimensions and Ordering Information. 1
-

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|--|-------------------------|
| 5962-9750901Q2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962- 9750901Q2A TLC7733 MFKB | Samples |
| 5962-9750901QPA | ACTIVE | CDIP | JG | 8 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 9750901QPA TLC7733M | Samples |
| 5962-9751301Q2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962- 9751301Q2A TLC7705 MFKB | Samples |
| 5962-9751301QHA | ACTIVE | CFP | U | 10 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 9751301QHA TLC7705M | Samples |
| 5962-9751301QPA | ACTIVE | CDIP | JG | 8 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 9751301QPA TLC7705M | Samples |
| TLC7701ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C7701I | Samples |
| TLC7701IDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C7701I | Samples |
| TLC7701IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C7701I | Samples |
| TLC7701IDRBT-NM | ACTIVE | SON | DRB | 8 | 250 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR | -40 to 125 | 7701N | Samples |
| TLC7701IDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C7701I | Samples |
| TLC7701IP | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | TLC7701IP | Samples |
| TLC7701IPW | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | Y7701 | Samples |
| TLC7701IPWR | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | Y7701 | Samples |
| TLC7701IPWRG4 | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | Y7701 | Samples |
| TLC7701QD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C7701Q | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLC7701QDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C7701Q | Samples |
| TLC7701QDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C7701Q | Samples |
| TLC7701QP | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLC7701QP | Samples |
| TLC7701QPW | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TD701 | Samples |
| TLC7701QPWG4 | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TD701 | Samples |
| TLC7701QPWR | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TD701 | Samples |
| TLC7701QPWRG4 | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TD701 | Samples |
| TLC7703ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C7703I | Samples |
| TLC7703IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C7703I | Samples |
| TLC7703IP | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | TLC7703IP | Samples |
| TLC7703IPW | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | Y7703 | Samples |
| TLC7703IPWG4 | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | Y7703 | Samples |
| TLC7703IPWR | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | Y7703 | Samples |
| TLC7703QD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C7703Q | Samples |
| TLC7703QDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C7703Q | Samples |
| TLC7703QPW | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TD703 | Samples |
| TLC7703QPWG4 | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TD703 | Samples |
| TLC7705ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C7705I | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|------------------------------------|-------------------------|
| TLC7705IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C7705I | Samples |
| TLC7705IP | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | TLC7705IP | Samples |
| TLC7705IPE4 | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | TLC7705IP | Samples |
| TLC7705IPW | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | Y7705 | Samples |
| TLC7705IPWR | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | Y7705 | Samples |
| TLC7705MFKB | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-9751301Q2A TLC7705 MFKB | Samples |
| TLC7705MJG | ACTIVE | CDIP | JG | 8 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | TLC7705 MJG | Samples |
| TLC7705MJGB | ACTIVE | CDIP | JG | 8 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 9751301QPA TLC7705M | Samples |
| TLC7705MUB | ACTIVE | CFP | U | 10 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 9751301QHA TLC7705M | Samples |
| TLC7705QD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C7705Q | Samples |
| TLC7705QDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C7705Q | Samples |
| TLC7705QPW | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TD705 | Samples |
| TLC7705QPWR | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TD705 | Samples |
| TLC7705QPWRG4 | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TD705 | Samples |
| TLC7725ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C7725I | Samples |
| TLC7725IDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C7725I | Samples |
| TLC7725IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C7725I | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLC7725IDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C7725I | Samples |
| TLC7725IPW | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | Y7725 | Samples |
| TLC7725IPWR | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | Y7725 | Samples |
| TLC7725QD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C7725Q | Samples |
| TLC7725QDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C7725Q | Samples |
| TLC7725QDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C7725Q | Samples |
| TLC7725QPWR | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TD725 | Samples |
| TLC7725QPWRG4 | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TD725 | Samples |
| TLC7733ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C7733I | Samples |
| TLC7733IDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C7733I | Samples |
| TLC7733IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C7733I | Samples |
| TLC7733IDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C7733I | Samples |
| TLC7733IP | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | TLC7733IP | Samples |
| TLC7733IPE4 | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | TLC7733IP | Samples |
| TLC7733IPW | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | Y7733 | Samples |
| TLC7733IPWR | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | Y7733 | Samples |
| TLC7733IPWRG4 | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | Y7733 | Samples |
| TLC7733MFKB | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962- 9750901Q2A | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| | | | | | | | | | | TLC7733 MFKB | |
| TLC7733MJG | ACTIVE | CDIP | JG | 8 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | TLC7733 MJG | Samples |
| TLC7733MJGB | ACTIVE | CDIP | JG | 8 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 9750901QPA TLC7733M | Samples |
| TLC7733QD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C7733Q | Samples |
| TLC7733QDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C7733Q | Samples |
| TLC7733QP | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLC7733QP | Samples |
| TLC7733QPW | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TD733 | Samples |
| TLC7733QPWR | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TD733 | Samples |
| TLC7733QPWRG4 | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TD733 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLC77 :

- Automotive: [TLC77-Q1](#)
- Enhanced Product: [TLC77-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLC7701IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLC7701IDRBT-NM | SON | DRB | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TLC7701IPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLC7701QDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLC7701QPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLC7703IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLC7703IPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLC7705IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLC7705IPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLC7705QDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLC7705QPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLC7725IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLC7725IPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLC7725QDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLC7725QPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLC7733IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLC7733IPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLC7733QDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLC7733QPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLC7701IDR | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| TLC7701IDRBT-NM | SON | DRB | 8 | 250 | 210.0 | 185.0 | 35.0 |
| TLC7701IPWR | TSSOP | PW | 8 | 2000 | 367.0 | 367.0 | 35.0 |
| TLC7701QDR | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| TLC7701QPWR | TSSOP | PW | 8 | 2000 | 367.0 | 367.0 | 35.0 |
| TLC7703IDR | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| TLC7703IPWR | TSSOP | PW | 8 | 2000 | 367.0 | 367.0 | 35.0 |
| TLC7705IDR | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| TLC7705IPWR | TSSOP | PW | 8 | 2000 | 367.0 | 367.0 | 35.0 |
| TLC7705QDR | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| TLC7705QPWR | TSSOP | PW | 8 | 2000 | 367.0 | 367.0 | 35.0 |
| TLC7725IDR | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| TLC7725IPWR | TSSOP | PW | 8 | 2000 | 367.0 | 367.0 | 35.0 |
| TLC7725QDR | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| TLC7725QPWR | TSSOP | PW | 8 | 2000 | 367.0 | 367.0 | 35.0 |
| TLC7733IDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLC7733IPWR | TSSOP | PW | 8 | 2000 | 367.0 | 367.0 | 35.0 |
| TLC7733QDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| TLC7733QPWR | TSSOP | PW | 8 | 2000 | 367.0 | 367.0 | 35.0 |

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

DRB 8

GENERIC PACKAGE VIEW

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

EXAMPLE BOARD LAYOUT

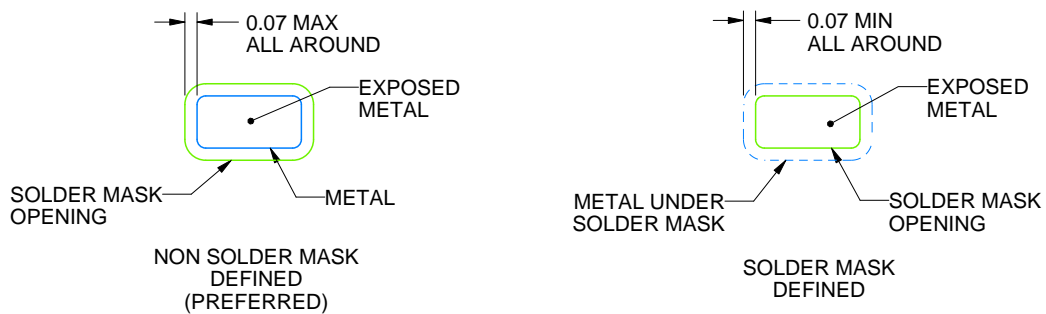
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

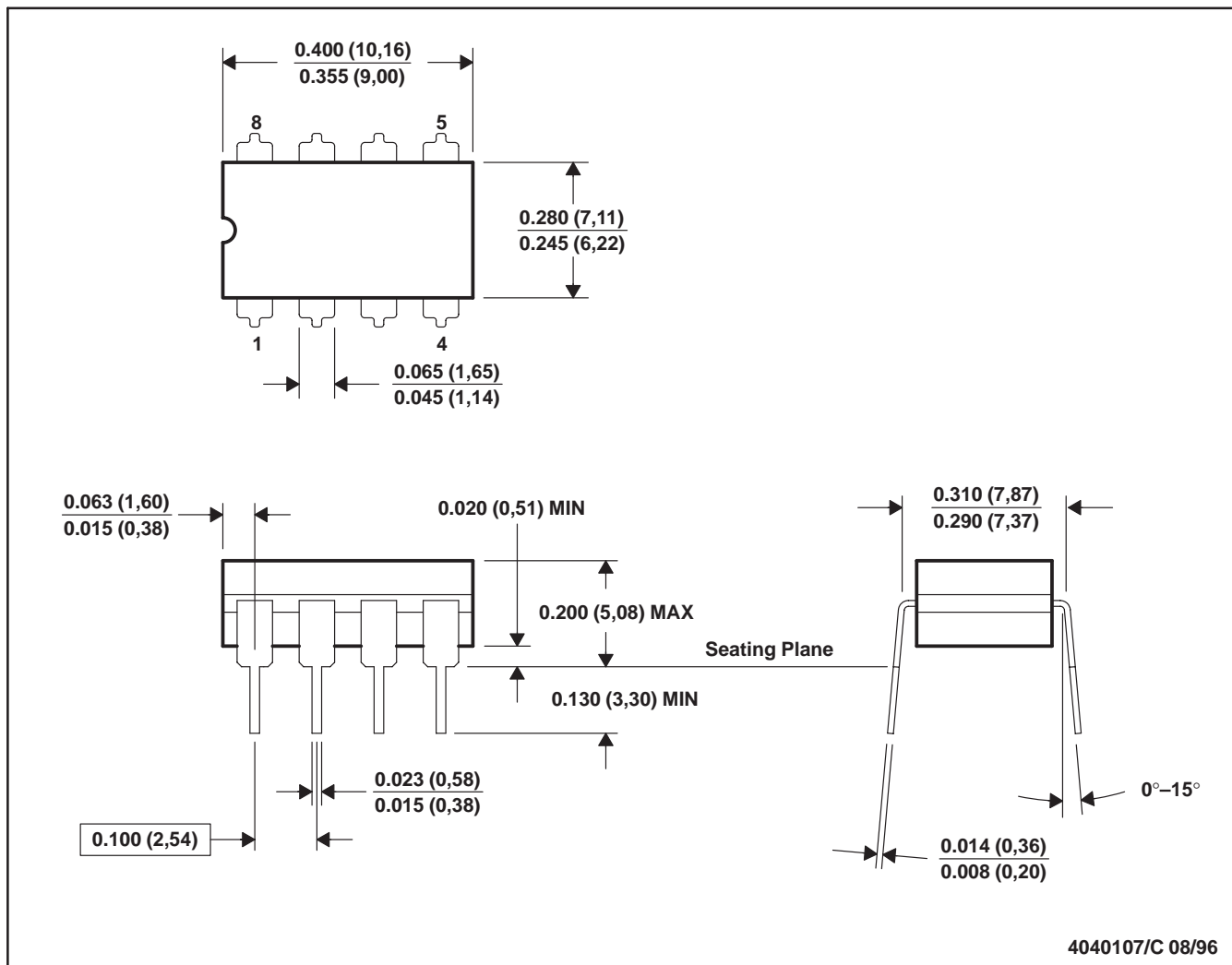
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T8

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

PW0008A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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