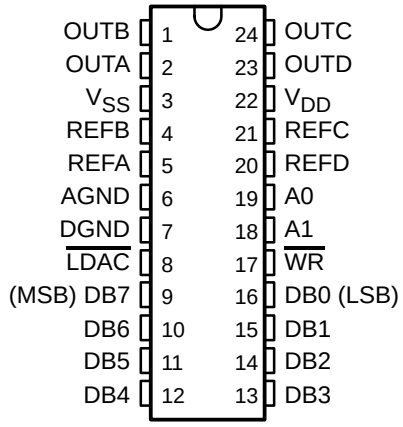
THE DATASHEET OF

TLC7225CDW

- **Four 8-Bit D/A Converters With Individual References**
- **Direct Bipolar Operation Without an External Level-Shift Amplifier**
- **Microprocessor Compatible**
- **TTL/CMOS Compatible**
- **Single Supply Operation Possible**
- **Simultaneous Update Facility**
- **Binary Input Coding**

DW PACKAGE
(TOP VIEW)



applications

- **Process Control**
- **Automatic Test Equipment**
- **Automatic Calibration of Large System Parameters e.g., Gain/Offset**

description

The TLC7225 consists of four 8-bit voltage-output digital-to-analog converters (DACs), with output buffer amplifiers and interface logic with double register-buffering.

Separate on-chip latches are provided for each of the DACs. Data is transferred into one of these data latches through a common 8-bit TTL/CMOS-compatible (5 V) input port. Control inputs A0 and A1 determine which DAC is loaded when $\overline{WR}$ goes low. Only the data held in the DAC registers determines the analog outputs of the converters. The double register buffering allows simultaneous update of all four outputs under control of $\overline{LDAC}$. All logic inputs are TTL- and CMOS-level compatible and the control logic is speed compatible with most 8-bit microprocessors. Each DAC includes an output buffer amplifier capable of driving up to 5 mA of output current.

The TLC7225 performance is specified for input reference voltages from 2 V to V_{DD} – 4 V with dual supplies. The voltage-mode configuration of the DACs allow the TLC7225 to be operated from a single power-supply rail at a reference of 10 V.

The TLC7225 is fabricated in a LinBiCMOS™ process that has been specifically developed to allow high-speed digital logic circuits and precision analog circuits to be integrated on the same chip. The TLC7225 has a common 8-bit data bus with individual DAC latches. This provides a versatile control architecture for simple interface to microprocessors. All latch-enable signals are level triggered.

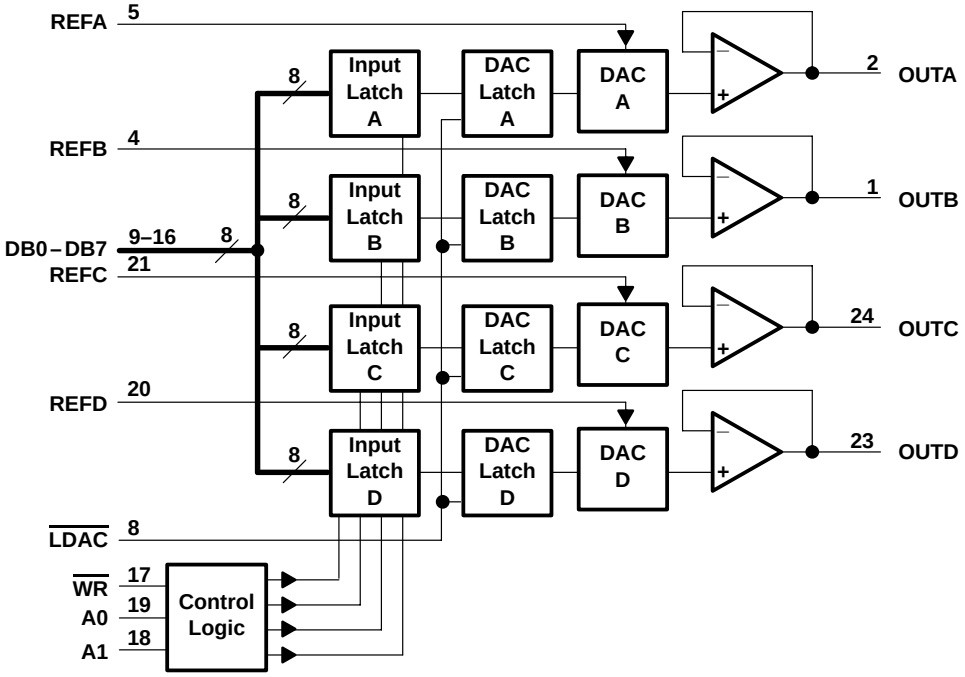
Combining four DACs, four operational amplifiers, and interface logic into a small, 0.3-inch wide, 24-terminal SOIC allows significant reduction in board space requirements and offers increased reliability in systems using multiple converters. The pinout optimizes board layout with all of the analog inputs and outputs at one end of the package and all of the digital inputs at the other.

The TLC7225C is characterized for operation from 0°C to 70°C. The TLC7225I is characterized for operation from –25°C to 85°C.

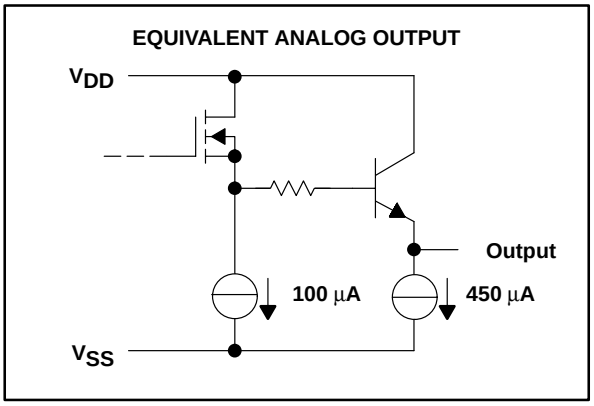
AVAILABLE OPTIONS

PACKAGED DEVICES	
T_A	SMALL OUTLINE (DW)
0°C to 70°C	TLC7225CDW
–25°C to 85°C	TLC7225IDW

functional block diagram



schematic of outputs



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	6		Analog ground
A0, A1	18, 19	I	DAC select inputs
DGND	7		Digital ground
DB0 – DB7	9 – 16	I	Digital DAC data inputs
$\overline{\text{LDAC}}$	8		Load DAC. A high level simultaneously loads all four DAC registers. DAC registers are transparent when $\overline{\text{LDAC}}$ is low.
OUTA	2	O	DACA output
OUTB	1	O	DACB output
OUTC	24	O	DACC output
OUTD	23	O	DACD output
REFA	5	I	Voltage reference input to DACA
REFB	4	I	Voltage reference input to DACB
REFC	21	I	Voltage reference input to DACC
REFD	20	I	Voltage reference input to DACD
V_{DD}	22		Positive supply voltage
V_{SS}	3		Negative supply voltage
$\overline{\text{WR}}$	17	I	Write input selects DAC transparency or latch mode

absolute maximum ratings over operating free-air temperature range (unless otherwise note)†

Supply voltage range, V_{DD}: to AGND or DGND . . . . . –0.3 V to 17 V
to V_{SS} . . . . . –0.3 V to 24 V
Supply voltage range, V_{SS}: to AGND or DGND . . . . . –7 V to V_{DD}
Voltage range between AGND and DGND . . . . . –0.3 V to V_{DD}
Input voltage range, V_I (to DGND) . . . . . –0.3 V to V_{DD} + 0.3 V
Reference voltage range, V_{ref} (to AGND) . . . . . –0.3 V to V_{DD}
Output voltage range, V_O (to AGND) (see Note 1) . . . . . V_{SS} to V_{DD}
Continuous total power dissipation at (or below) T_A = 25°C (see Note 2) . . . . . 500 mW
Operating free-air temperature range: C suffix . . . . . 0°C to 70°C
I suffix . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Output voltages may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typically short circuit current to AGND is 50 mA.
2. For operation above T_A = 75°C derate linearly at the rate of 2.0 mW/°C.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		11.4	16.5	V
Supply voltage, V_{SS}		–5.5	0	V
High-level input voltage, V_{IH}		2		V
Low-level input voltage, V_{IL}			0.8	V
Reference voltage, V_{ref}		2	$V_{DD}-4$	V
Load resistance, R_L		2		kΩ
Operating free-air temperature, T_A	C suffix	0	70	°C
	I suffix	–25	85	°C

timing requirements (see Figure 1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{su(AW)}$	Setup time, address valid before $\overline{WR}\downarrow$		0		ns
$t_{su(DW)}$	Setup time, data valid before $\overline{WR}\uparrow$	V_{DD} = 11.4 V to 16.5 V, V_{SS} = 0 or –5 V	45		ns
$t_{h(AW)}$	Hold time, address valid after $\overline{WR}\uparrow$	V_{DD} = 11.4 V to 16.5 V, V_{SS} = 0 or –5 V	0		ns
$t_{h(DW)}$	Hold time, data valid after $\overline{WR}\uparrow$	V_{DD} = 11.4 V to 16.5 V, V_{SS} = 0 or –5 V	10		ns
t_{w1}	Pulse duration, $\overline{WR}$ low	V_{DD} = 11.4 V to 16.5 V, V_{SS} = 0 or –5 V	50		ns
t_{w2}	Pulse duration, $\overline{LDAC}$ low	V_{DD} = 11.4 V to 16.5 V, V_{SS} = 0 or –5 V	50		ns

electrical characteristics over recommended operating free-air temperature range

reference inputs (all supply ranges)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
r_i	Input resistance, REFA, REFB, REFC, REFD		1.5	4		kΩ
C_i	Input capacitance, REFA, REFB, REFC, REFD	DAC loaded with all 1s			300	pF
		DAC loaded with all 0s	65			pF
	Channel-to-channel isolation	V_{ref} = 10 V_{pp} sine wave at 10 kHz	60			dB
	AC feedthrough		70			dB

dual power supply over recommended supply and reference voltage ranges, AGND = DGND = 0 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_I	Input current, digital		V_I = 0 or V_{DD}			±1	µA
I_{DD}	Supply current, V_{DD}		V_I = V_{IL} or V_{IH}, No load		10	16	mA
I_{SS}	Supply current, V_{SS}		V_I = V_{IL} or V_{IH}, No load		4	10	mA
	Power supply sensitivity		ΔV_{DD} = ±5%			0.01	%/%
C_i	Input capacitance	Digital inputs				8	pF

single power supply, V_{DD} = 14.25 V to 15.75 V, V_{SS} = AGND = DGND = 0 V, V_{ref} (A, B, C, D) = 10 V

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_I	Input current, digital		V_I = 0 or V_{DD}			±1	µA
I_{DD}	Supply current, V_{DD}		V_I = V_{IL} or V_{IH}, No load		5	13	mA
	Power supply sensitivity		ΔV_{DD} = ±5%			0.01	%/%
C_i	Input capacitance	Digital inputs				8	pF

operating characteristics over recommended operating free-air temperature range

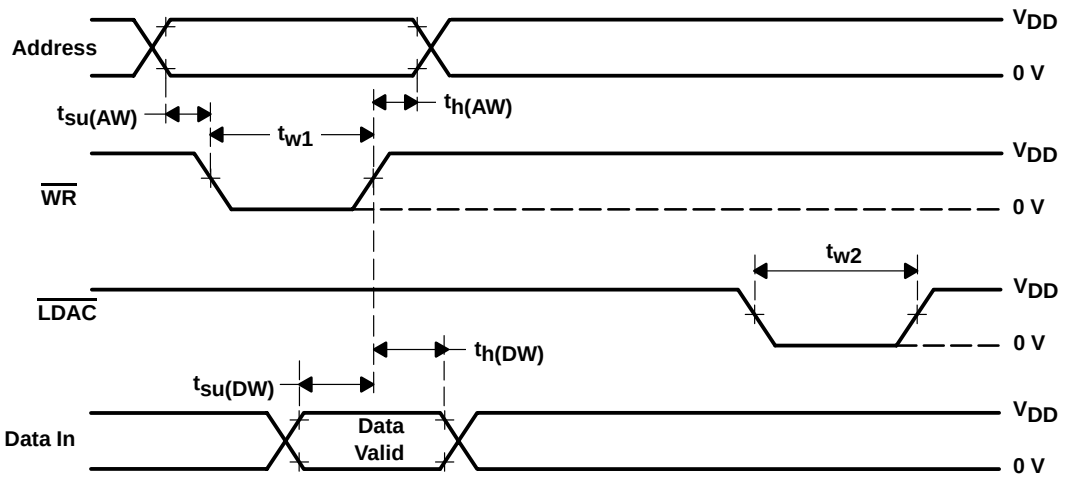
dual power supply over recommended supply and reference voltage ranges, AGND = DGND = 0 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Slew rate				2.5			V/µs
t_S	Settling time to 1/2 LSB	Positive full scale	$V_{ref(A, B, C, D)}$ = 10 V				5	µs
		Negative full scale					7	
	Resolution					8		Bits
	Total unadjusted error		V_{DD} = 15 V ±5%,	$V_{ref(A, B, C, D)}$ = 10 V			±2	LSB
	Integral nonlinearity (INL)		V_{DD} = 15 V ±5%,	$V_{ref(A, B, C, D)}$ = 10 V			±1	LSB
	Differential nonlinearity (DNL)		V_{DD} = 15 V ±5%,	$V_{ref(A, B, C, D)}$ = 10 V			±1	LSB
E_{FS}	Full-scale error		V_{DD} = 15 V ±5%,	$V_{ref(A, B, C, D)}$ = 10 V			±2	LSB
E_G	Gain error		V_{DD} = 15 V ±5%,	$V_{ref(A, B, C, D)}$ = 10 V		±0.25		LSB
	Temperature coefficient of gain	Full-scale error	V_{DD} = 14 V to 16.5 V,	$V_{ref(A, B, C, D)}$ = 10 V		±20		ppm/°C
		Zero-code error				±50		µV/°C
	Zero-code error					±20	±80	mV
	Digital crosstalk or feedthrough glitch impulse area		$V_{ref(A, B, C, D)}$ = 0			50		nV–s

single power supply, V_{DD} = 14.25 V to 15.75 V, V_{SS} = AGND = DGND = 0 V, $V_{ref(A, B, C, D)}$ = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Slew rate			2			V/µs
t_S	Settling time to 1/2 LSB	Positive full scale				5	µs
		Negative full scale				20	
	Resolution				8		Bits
	Total unadjusted error					±2	LSB
E_{FS}	Full-scale error					±2	LSB
	Temperature coefficient of gain	Full-scale error	V_{DD} = 14 V to 16.5 V, $V_{ref(A, B, C, D)}$ = 10 V		±20		ppm/°C
		Zero-code error			±50		µV/°C
	Differential nonlinearity error (DNL)					±1	LSB
	Digital crosstalk or feedthrough glitch impulse area				50		nV–s

PARAMETER MEASUREMENT INFORMATION



NOTES: A. $t_r = t_f = 20$ ns over V_{DD} range.
B. The timing-measurement reference level is equal to $V_{IH} + V_{IL}$ divided by 2.
C. If $\overline{LDAC}$ is activated prior to the rising edge of $\overline{WR}$, then it must remain low for at least t_{w2} after $\overline{WR}$ goes high.

Figure 1. Write-Cycle Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT CURRENT vs OUTPUT VOLTAGE

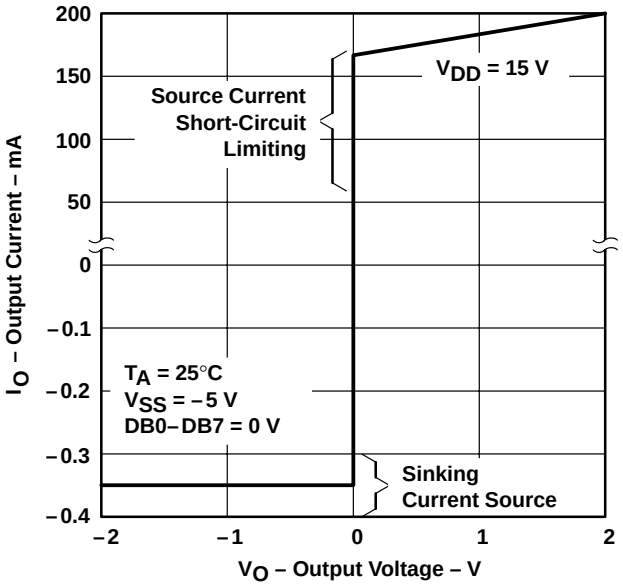


Figure 2

OUTPUT CURRENT (SINK) vs OUTPUT VOLTAGE

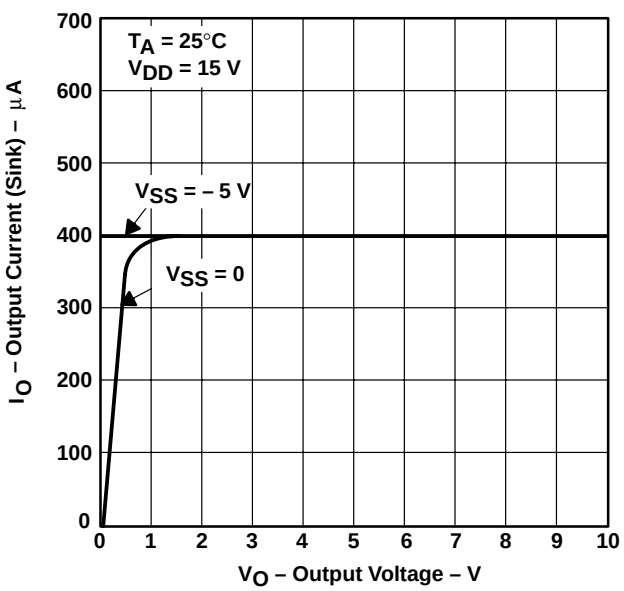


Figure 3

APPLICATION INFORMATION

specification ranges

For the TLC7225 to operate to rated specifications, the input reference voltage must be at least 4 V below the power supply voltage at the V_{DD} terminal. This voltage differential is the overhead voltage required by the output amplifiers.

The TLC7225 is specified to operate over a V_{DD} range from 12 V ± 5% to 15 V ± 10% (i.e., from 11.4 V to 16.5 V) with a V_{SS} of – 5 V ± 10%. Operation is also specified for a single supply with a V_{DD} of 15 V ± 5%. Applying a V_{SS} of – 5 V results in improved zero-code error, improved output sink capability with outputs near AGND, and improved negative-going settling time.

Performance is specified over the range of reference voltages from 2 V to (V_{DD} – 4 V) with dual supplies. This allows a range of standard refence generators to be used such as the TL1431, with an adjustable 2.5-V bandgap reference. Note that an output voltage range of 0 V to 10 V requires a nominal 15 V ± 5% power supply voltage.

DAC section

The TLC7225 contains four, identical, 8-bit voltage-mode DACs. Each converter has a separate reference input. The output voltages from the converters have the same polarity as the reference voltages, thus allowing single supply operation.

The simplified circuit diagram for channel A is shown in Figure 4. Note that AGND (terminal 6) is common to all four DACs.

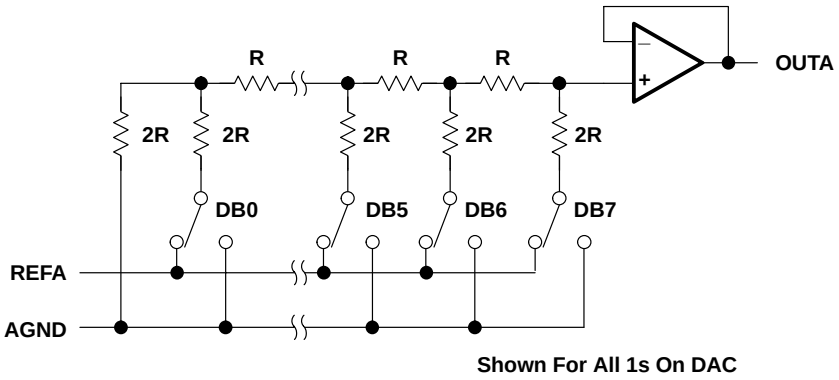


Figure 4. DAC Simplified-Circuit Diagram

The input impedance at any of the reference inputs is code dependent and can vary from 1.4 kΩ minimum to an open circuit. The lowest input impedance at any reference input occurs when that DAC is loaded with the digital code 01010101. Therefore, it is important that the reference source presents a low output impedance under changing load conditions. The nodal capacitance at the reference terminals is also code dependent and typically varies from 60 pF to 300 pF.

Each OUTx terminal can be considered as a digitally programmable voltage source with an output voltage of:

$$V_{OUTx} = D_x \times V_{REFx}$$

where D_x is the fractional representation of the digital input code and can vary from 0 to 255/256.

The output impedance is that of the output buffer amplifier.

APPLICATION INFORMATION

output buffer

Each voltage-mode DAC output is buffered by a unity-gain noninverting amplifier. This buffer amplifier is capable of developing 10 V across a 2-kΩ load and can drive capacitive loads of 3300 pF.

The TLC7225 can be operated as a single or dual supply; operating with dual supplies results in enhanced performance in some parameters which cannot be achieved with a single-supply operation. In a single supply operating (V_{SS} = 0 V = AGND) the sink capability of the amplifier, which is normally 400 μA, is reduced as the output voltage nears AGND. The full sink capability of 400 μA is maintained over the full output voltage range by tying V_{SS} to –5 V. This is indicated in Figure 3.

Settling time for negative-going output signals approaching AGND is similarly affected by V_{SS}. Negative-going settling time for single supply operation is longer than for dual supply operation. Positive-going settling-time is not affected by V_{SS}.

Additionally, the negative V_{SS} gives more headroom to the output amplifiers which results in better zero code performance and improved slew rate at the output than can be obtained in the single-supply mode.

digital inputs

The TLC7225 digital inputs are compatible with either TTL or 5-V CMOS levels. To minimize power supply currents, it is recommended that the digital input voltages be driven as close to the supply rails (V_{DD} and DGND) as practically possible.

interface logic information

The TLC7225 contains two registers per DAC, an input register and a DAC register. Address lines A0 and A1 select which input register accepts data from the input port. When the $\overline{WR}$ signal is low, the input latches of the selected DAC are transparent. The data is latched into the addressed input register on the rising edge of $\overline{WR}$. Table 1 shows the addressing for the input registers on the TLC7225.

Table 1. TLC7225 Addressing

CONTROL INPUTS		SELECTED INPUT REGISTER
A1	A0	
L	L	DAC A input register
L	H	DAC B input register
H	L	DAC C input register
H	H	DAC D input register

Only the data held in the DAC register determines the analog output of the converter. The $\overline{LDAC}$ signal is common to all four DACs and controls the transfer of information from the input registers to the DAC registers. Data is latched into all four DAC registers simultaneously on the rising edge of $\overline{LDAC}$. The $\overline{LDAC}$ signal is level triggered and, therefore, the DAC registers may be made transparent by tying $\overline{LDAC}$ low (the outputs of the converters responds to the data held in their respective input latches). $\overline{LDAC}$ is an asynchronous signal and is independent of $\overline{WR}$. This is useful in many applications. However, in systems where the asynchronous $\overline{LDAC}$ can occur during a write cycle (or vice versa) care must be taken to ensure that incorrect data is not latched through to the output. In other words, if $\overline{LDAC}$ is activated prior to the rising edge of $\overline{WR}$ (or $\overline{WR}$ occurs during $\overline{LDAC}$), then $\overline{LDAC}$ must stay low for a time of t_{w2} or longer after $\overline{WR}$ goes high to ensure that the correct data is latched through to the output. Table 2 shows the truth table for TLC7225 operation. Figure 5 shows the input control logic for the device and the write cycles timing diagram is shown in Figure 1.

APPLICATION INFORMATION

Table 2. TLC7225 Truth Table

CONTROL INPUTS		FUNCTION
$\overline{WR}$	$\overline{LDAC}$	
H	H	No operation. Device not selected
L	H	Input register of selected DAC is transparent.
↑	H	Input register of selected DAC is latched.
H	L	All four DAC registers are transparent (i.e., outputs respond to data held in respective input registers) input registers are latched.
H	↑	All four DAC registers are latched.
L	L	DAC registers and selected input register are transparent. Output follows input data for selected channel.

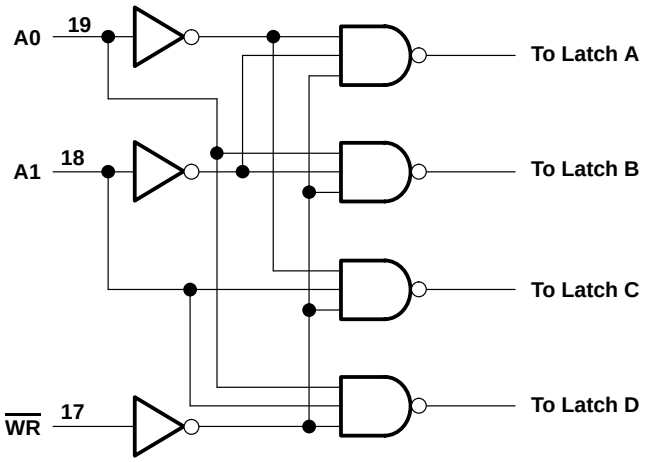


Figure 5. Input Control Logic

APPLICATION INFORMATION

ground management and layout

The TLC7225 contains four reference inputs that can be driven from ac sources (see multiplying DAC using ac input to the REF terminals section) so careful layout and grounding is important to minimize analog crosstalk between the four channels. The dynamic performance of the four DACs depends upon the optimum choice of board layout. Figure 6 shows the relationship between input frequency and channel-to-channel isolation. Figure 7 shows a printed circuit board layout that minimizes crosstalk and feedthrough. The four input signals are screened by AGND. V_{ref} was limited between 2 V and 3.24 V to avoid slew-rate limiting effects from the output amplifier during measurements.

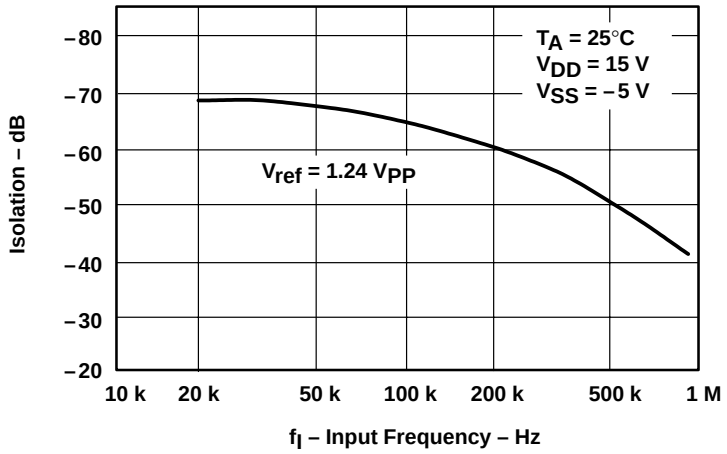


Figure 6. Channel-to-Channel Isolation

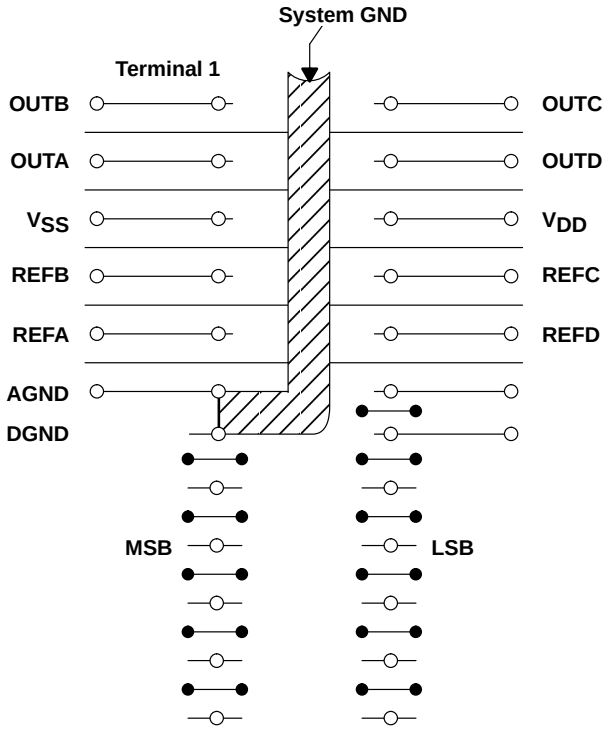


Figure 7. Suggested PCB Layout (Top View)

APPLICATION INFORMATION

unipolar output operation

The unipolar output operation is the basic mode of operation for each channel of the TLC7225, with the output voltages having the same positive polarity as V_{ref}. The TLC7225 can be operated with a single supply (V_{SS} = AGND) or with positive or negative supplies. The voltage at V_{ref} must never be negative with respect to DGND to prevent parasitic transistor turnon. Connections for the unipolar output operation are shown in Figure 8. The transfer values are shown in Table 3.

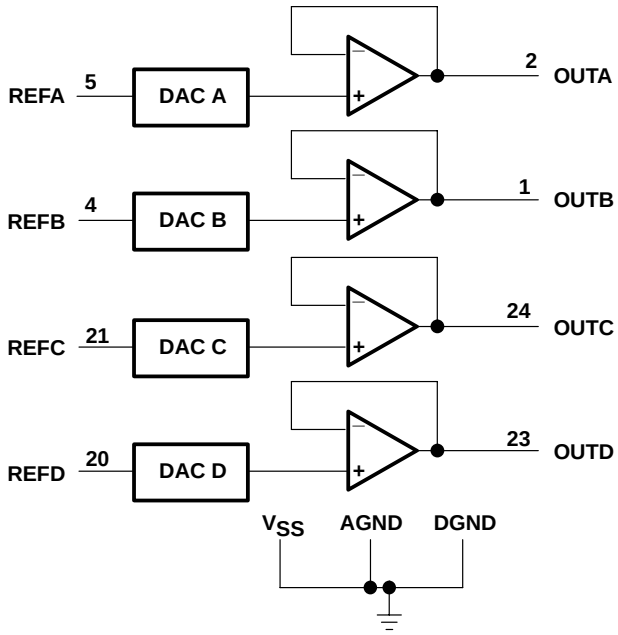


Figure 8. Unipolar Output Circuit

Table 3. Unipolar Code

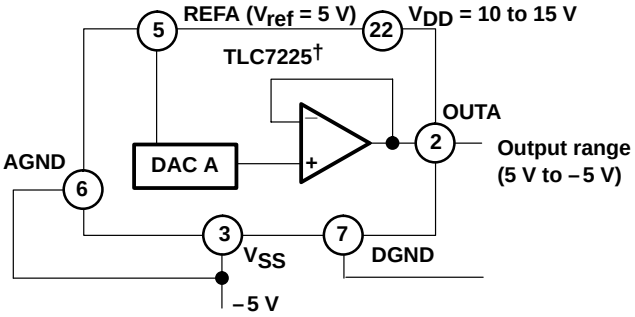
DAC LATCH CONTENTS MSB	DAC LATCH CONTENTS LSB	ANALOG OUTPUT
1111	1111	$+ V_{ref}\left(\frac{255}{256}\right)$
1000	0001	$+ V_{ref}\left(\frac{129}{256}\right)$
1000	0000	$+ V_{ref}\left(\frac{128}{256}\right) = + \frac{V_{ref}}{2}$
0111	1111	$+ V_{ref}\left(\frac{127}{256}\right)$
0000	0001	$+ V_{ref}\left(\frac{1}{256}\right)$
0000	0000	0 V

NOTE 3: 1 LSB = $\left(V_{ref}\ 2^{-8}\right) = V_{ref}\left(\frac{1}{256}\right)$

APPLICATION INFORMATION

AGND bias for direct bipolar-output operation

The TLC7225 can be used in bipolar operation without adding additional external operational amplifiers by biasing AGND to V_{SS} as shown in Figure 9. This configuration provides an excellent method for providing a direct bipolar output with no additional components. The transfer values are shown in Table 4.



† Digital inputs omitted for clarity.

Figure 9. AGND Bias for Direct Bipolar-Output Operation

Table 4. Bipolar (Offset Binary) Code

DAC LATCH CONTENTS MSB	LSB	ANALOG OUTPUT
1111	1111	$+ V_{ref}\left(\frac{127}{128}\right)$
1000	0001	$+ V_{ref}\left(\frac{1}{128}\right)$
1000	0000	0 V
0111	1111	$- V_{ref}\left(\frac{1}{128}\right)$
0000	0001	$- V_{ref}\left(\frac{127}{128}\right)$
0000	0000	$-V_{ref}\left(\frac{128}{128}\right) = - V_{ref}$

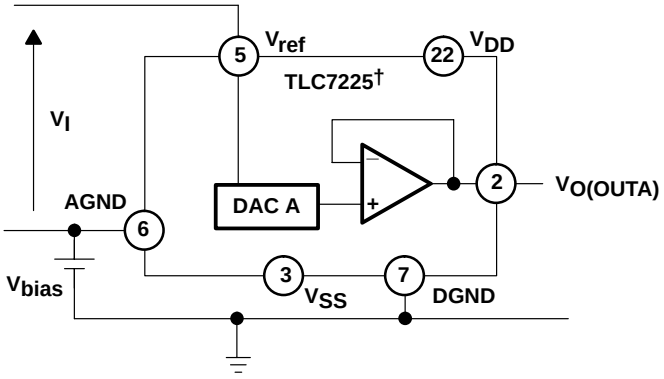
APPLICATION INFORMATION

AGND bias for positive output offset

The TLC7225 AGND terminal can be biased above or below the system ground terminal, DGND, to provide an offset-zero analog-output voltage level. Figure 10 shows a circuit configuration to achieve this for channel A of the TLC7225. The output voltage, V_O at OUTA, can be expressed as:

$$V_O = V_{bias} + D_A \left(V_I\right)$$

where D_A is a fractional representation of the digital input word ($0 \le D \le 255/256$).



† Digital inputs omitted for clarity.

Figure 10. AGND Bias Circuit

Increasing AGND above system ground reduces the output range. $V_{DD} – V_{ref}$ must be at least 4 V to ensure specified operation. Since the AGND terminal is common to all four DACs, this method biases up the output voltages of all the DACs in the TLC7225. Supply voltages V_{DD} and V_{SS} for the TLC7225 should be referenced to DGND.

APPLICATION INFORMATION

bipolar-output operation using external amplifier

Each of the DACs of the TLC7225 can also be individually configured to provide bipolar output operation using an external amplifier and two resistors per channel. Figure 11 shows a circuit used to implement offset binary coding (bipolar operation) with DAC A of the TLC7225. In this case (see equation 1):

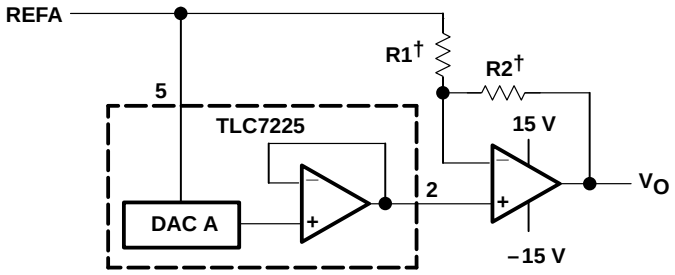
$$V_O = 1 + \frac{R2}{R1}\left(D_A\ V_{ref}\right) - \frac{R2}{R1}\left(V_{ref}\right) \quad (1)$$

with $R1 = R2$

$$V_O = \left(2D_A - 1\right) V_{ref}$$

where D_A is a fractional representation of the digital word in latch A.

Mismatch between R1 and R2 causes gain and offset errors. Therefore, these resistors must match and track over temperature. The TLC7225 can be operated with a single supply or from positive and negative supplies.



† R1 = R2 = 10 kΩ ±0.1%

Figure 11. Bipolar-Output Circuit

multiplying DAC using ac input to the REF terminals

The TLC7225 can be used as a multiplying DAC when the reference signal is maintained between 2 V and V_{DD} – 4 V. When this configuration is used, V_{DD} should be 14.25 V to 15.75 V. A low output-impedance buffer should be used so that the input signal is not loaded by the resistor ladder. Figure 12 shows the general schematic.

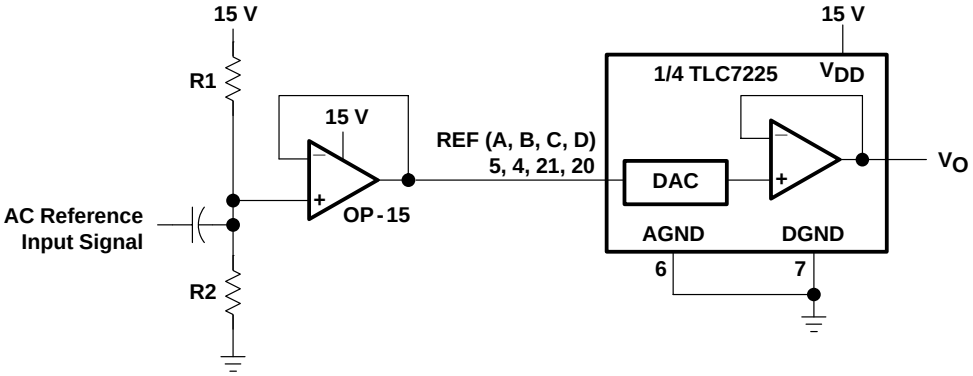


Figure 12. AC Signal-Input Scheme

APPLICATION INFORMATION

digital word multiplication

Since each DAC of the TLC7225 has a separate reference input, the output of one DAC can be used as the reference input for another. Therefore, multiplication of digital words can be performed (with the result given in analog form). For example, when the output from DAC A is applied to REFB then the output from DAC B, V_{OUTB}, can be expressed as given in equation 2:

$$V_{OUTB} = (D_A)\ (D_B)\ (V_{REFA}) \quad (2)$$

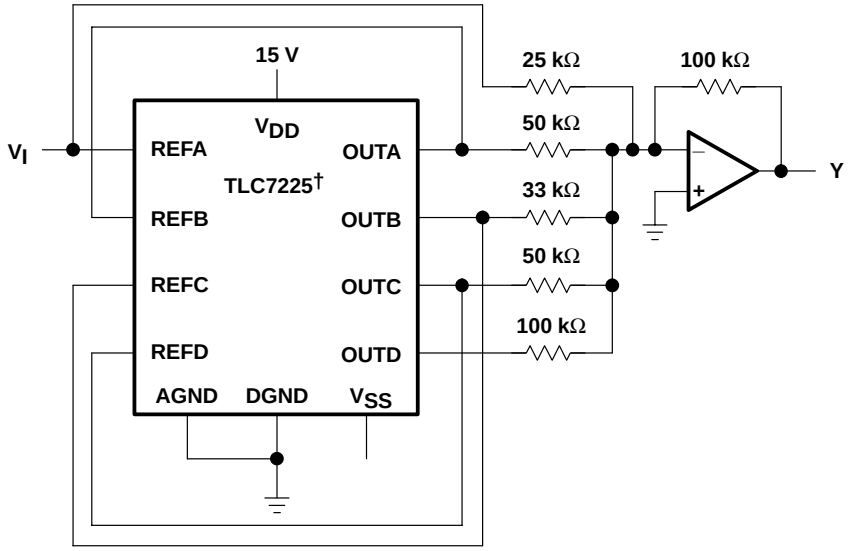
where D_A and D_B are the fractional representations of the digital words in DAC latches A and B respectively.

If $D_A = D_B = D$ then the result is $D^2\ (V_{REFA})$

In this manner, the four DACs can be used on their own or in conjunction with an external summing amplifier to generate complex waveforms. Figure 13 shows one such application with the output waveform, Y, which is represented by equation 3:

$$Y = -(x^4 + 2x^3 + 3x^2 + 2x + 4)\ V_I \quad (3)$$

where x is the digital code that is applied to all four DAC latches.



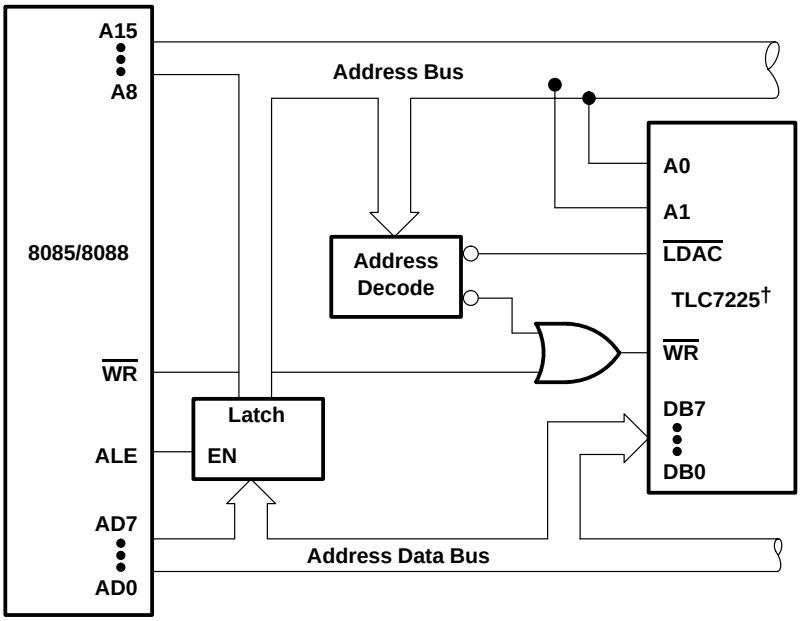
† Digital inputs omitted for clarity

Figure 13. Complex-Waveform Generation

APPLICATION INFORMATION

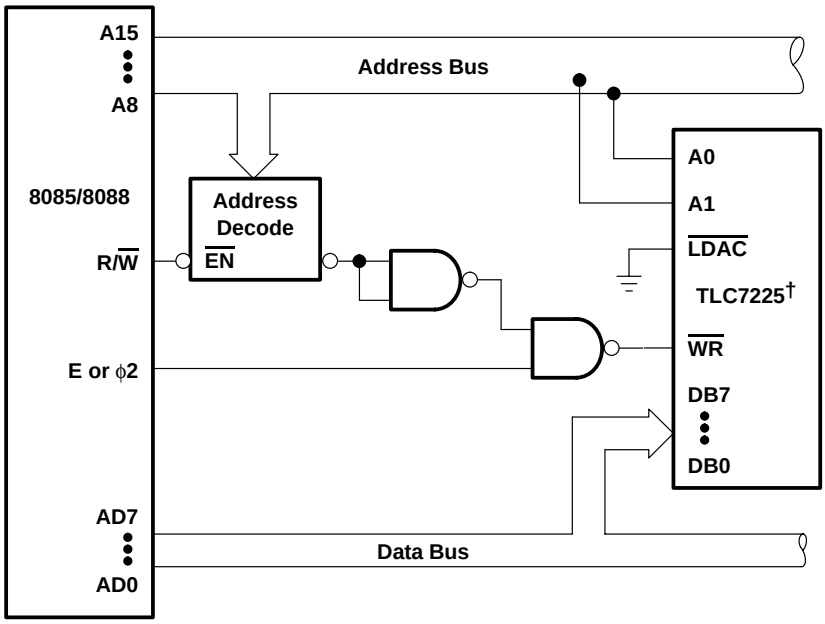
microprocessor interface

Figures 14, 15, 16, and 17 show the hardware interface to some of the standard processors.



† Linear circuitry omitted for clarity

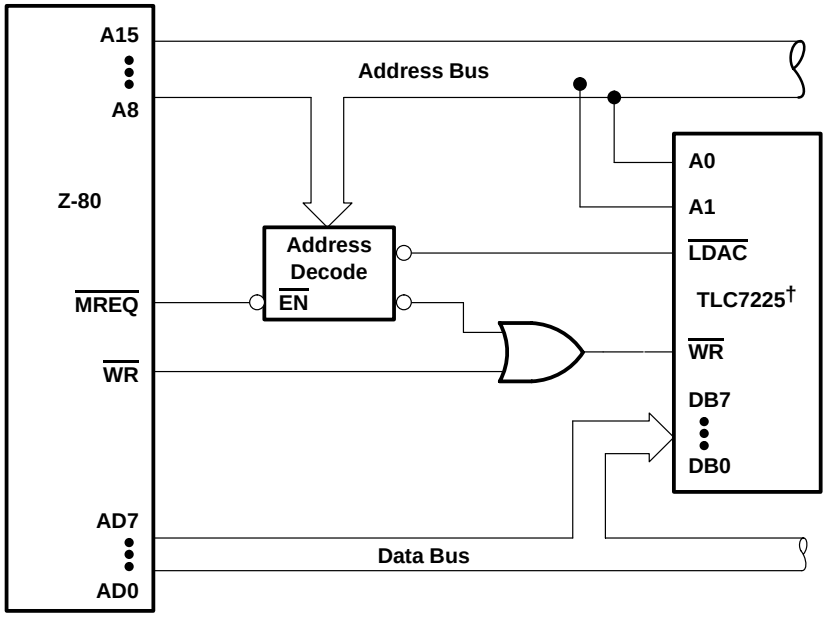
Figure 14. TLC7225 to 8085A/8088 Interface, Double-Buffered Mode



† Linear circuitry omitted for clarity

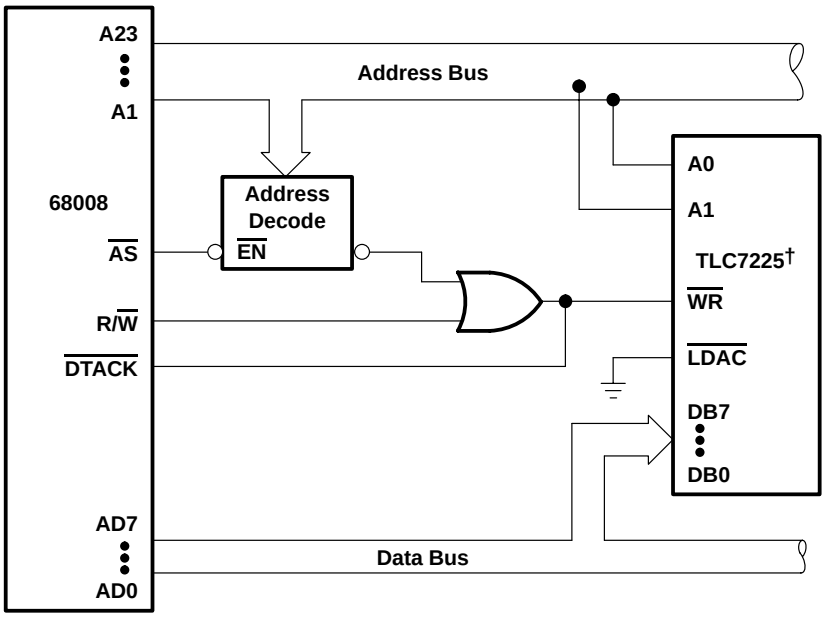
Figure 15. TLC7225 to 6809/6502 Interface, Single-Buffered Mode

APPLICATION INFORMATION



† Linear circuitry omitted for clarity

Figure 16. TLC7225 to Z-80 Interface, Double-Buffered Mode



† Linear circuitry omitted for clarity

Figure 17. TLC7225 to 68008 Interface, Single-Buffered Mode

APPLICATION INFORMATION

linearity, offset, and gain error using single-ended supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, since the most negative supply rail is ground, the output cannot drive below ground.

So with this output offset voltage, the output voltage remains at zero until the input-code value produces a sufficient output voltage to overcome the inherent offset voltage, resulting in a transfer function shown in Figure 18.

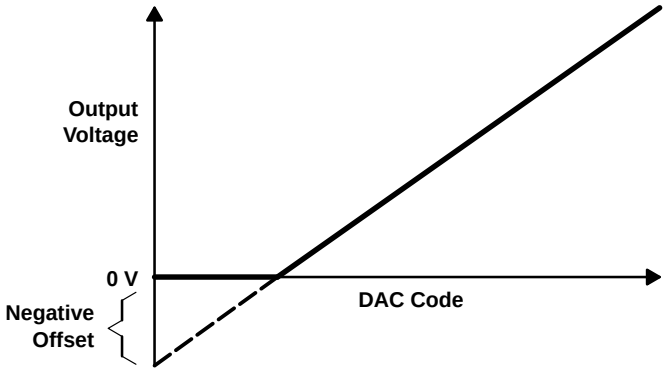


Figure 18. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below ground.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale is adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity in the unipolar mode is measured between full-scale code and the lowest code, which produces a positive output voltage.

The code is calculated from the maximum specification for the zero offset error.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC7225CDW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC7225C	Samples
TLC7225CDWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC7225C	Samples
TLC7225CDWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC7225C	Samples
TLC7225IDW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	TLC7225I	Samples
TLC7225IDWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	TLC7225I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

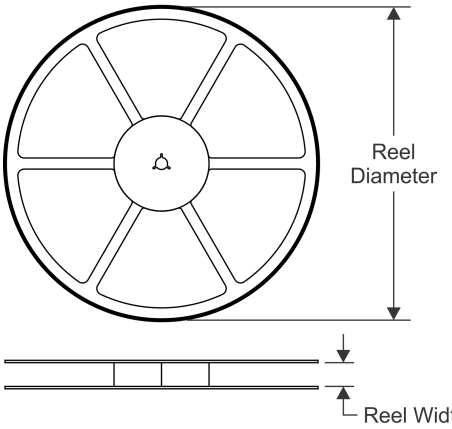
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

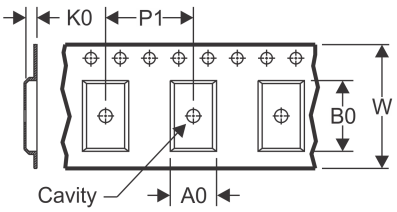
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

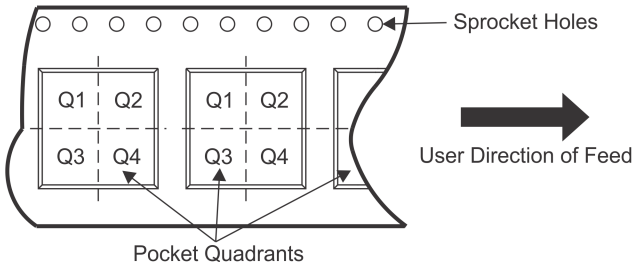


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

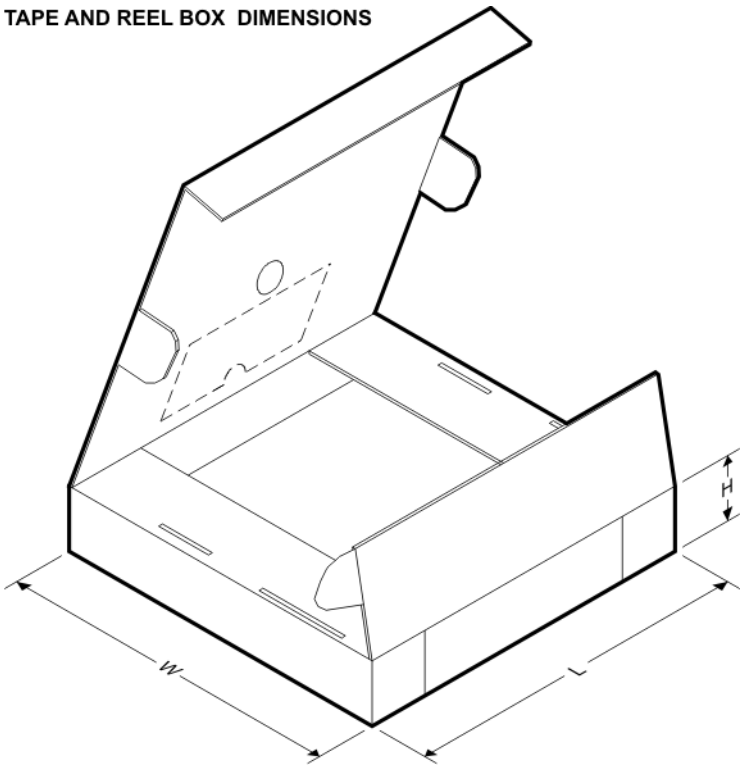
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC7225CDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
TLC7225IDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

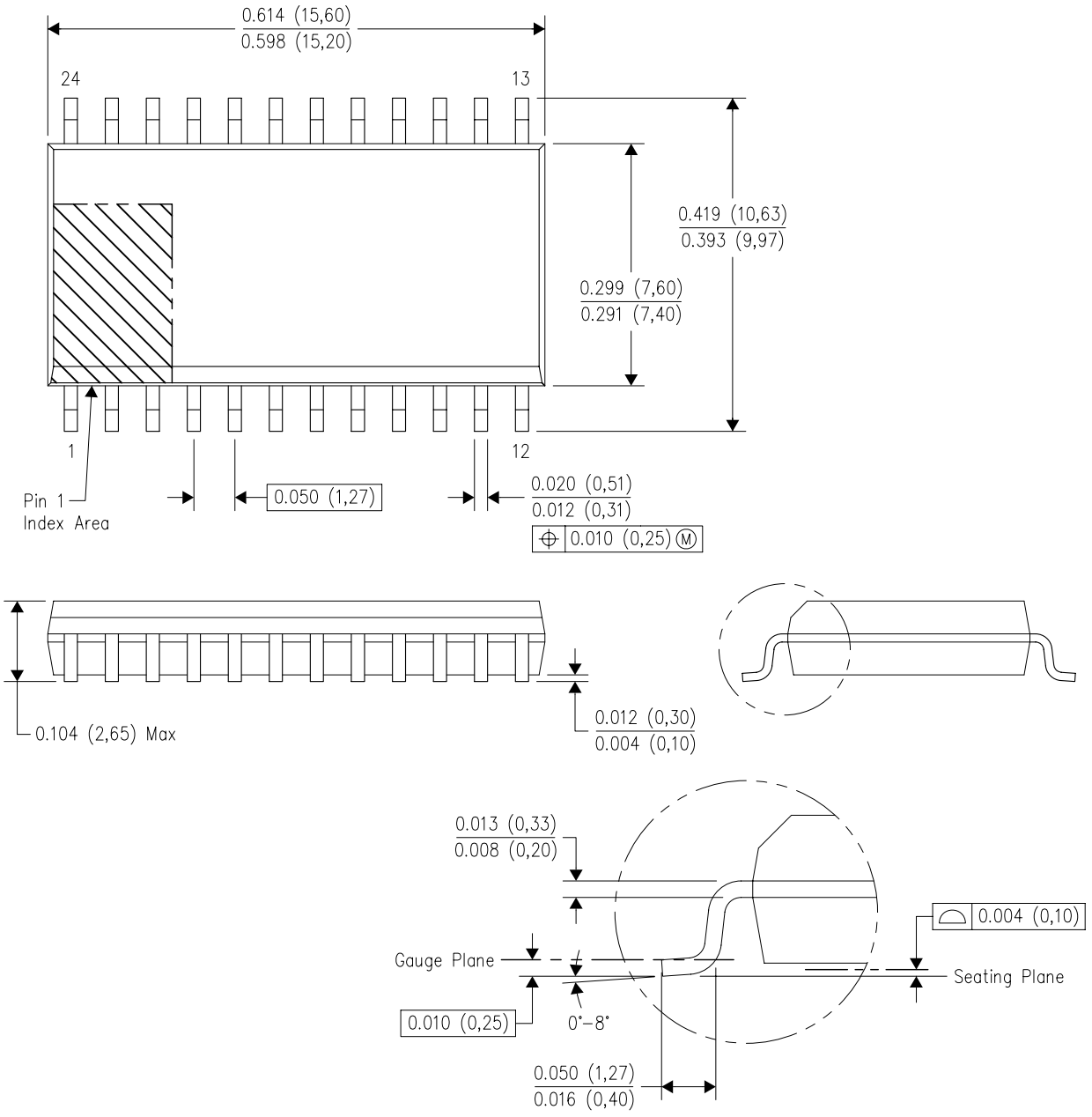
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC7225CDWR	SOIC	DW	24	2000	350.0	350.0	43.0
TLC7225IDWR	SOIC	DW	24	2000	350.0	350.0	43.0

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

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