THE DATASHEET OF

TLC5960DAR

Eight-Channel LED Driver with Intelligent Headroom Voltage Monitor (iHVM™)

Check for Samples: TLC5960

FEATURES

- 250kHz PWM Dimming
- Four Intelligent Headroom Voltage Monitor (iHVM) Outputs
- Eight-Channel, High-Voltage LED Driver:
  - 0.3% (typ) Accuracy Between Channels
- Control Interface with Four PWM Inputs
- Easy-To-Use Analog Dimming Interface
- 10% to 100% Analog Brightness Dimming
- Integrated 5V Internal Regulator
- Integrated Power-On Reset (POR) Circuitry
- Full Protection/Diagnostic Functions:
  - LOD: LED Open Detection
  - LSD: LED Short Detection
  - FOD: FET Open Detection
  - FSD: FET Short Detection
- Built-In Phase Shift Function
- 38-Pin TSSOP Package

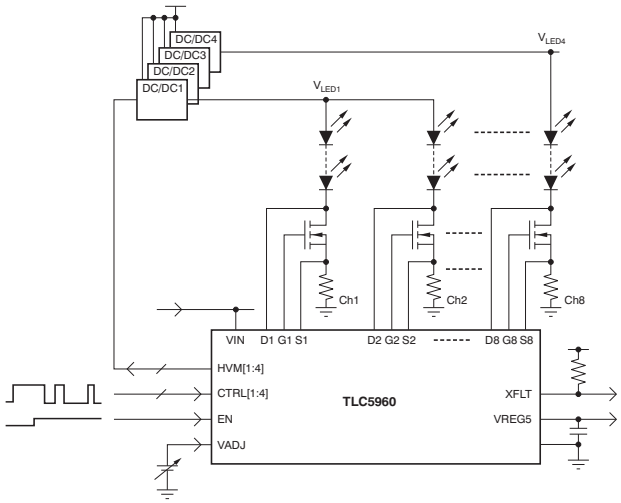
APPLICATIONS

- LED Backlights for LCD-TV
- High-Current LED Lighting

DESCRIPTION

The TLC5960 is an eight-channel PWM LED driver with four intelligent headroom voltage monitor (iHVM) outputs. The LED drivers have scalable, high-voltage capability and provide 1% maximum current matching accuracy between LED strings. To achieve optimal efficiency, the iHVM automatically optimizes the external dc/dc converter output voltage to compensate for the forward-voltage variations of the LED

Compared to a conventional HVM solution that requires several MOSFETs, capacitors, and resistors, the iHVM is designed to use only a single external resistor. The LED driver design is capable of up to 250kHz PWM dimming, and also provides an analog brightness dimming interface. This device easily adapts to various LED and power configurations with a single voltage input rail. Full protection and diagnostic functions are provided to protect the entire system, such as LED open/short detection (LOD/LSD), FET open/short detection (FOD/FSD) and thermal shutdown (TSD). In case of failure, the TLC5960 automatically disconnects the failed channel(s) from the operating channels and pulls down the open drain fault buffer (XFLT) to signal an error status.



Typical Application Circuit

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	ORDERING NUMBER
TLC5960	TSSOP-38	DA	TLC5960DA

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		VALUE		UNIT
		MIN	MAX	
Voltage(2)	VIN, CTRL2, CTRL4	–0.3	30	V
	S1 to S8, D1 to D8	–0.3	38	V
	EN, CTRL1, CTRL3, VADJ, VREG5, G1 to G8, XFLT, HVM1 to HVM4	–0.3	6.0	V
Temperature	Operating virtual junction, T_J	–40	+150	°C
	Storage, T_{stg}	–55	+150	°C
Electrostatic Discharge Rating(3)	Human Body Model (HBM, JESD22-A114)		2	kV
	Charged Device Model (CDM. JESD22-C101)		1000	V
	Machine Model (MM)		200	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL INFORMATION

THERMAL METRIC(1)		TLC5960 DA 38 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	71.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	21.8	
θ_{JB}	Junction-to-board thermal resistance	43.6	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	38.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

DISSIPATION RATINGS

PACKAGE	OPERATING FACTOR ABOVE T_A = +25°C	T_A < +25°C POWER RATING	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
TSSOP-38 (DA)	14mW/°C	1404mW	770mW	560mW

RECOMMENDED OPERATING CONDITIONS

PARAMETER		TLC5960			UNIT
		MIN	NOM	MAX	
DC Characteristics					
V_{IN}	Supply voltage	10	24	28	V
V_D	Voltage applied to sense input (D1 to D8, S1 to S8)	GND		34	V
V_{IH}	High-level input voltage (CTRL1 to CTRL4)	1.2		5.5	V
V_{IL}	Low-level input voltage (CTRL1 to CTRL4)	GND		0.4	V
I_{SINK}	Low-level output current (XFLT)			1	mA
C_{LOAD}	Capacitive load of Gn outputs (G1 to G8)		100	500	pF
V_G	MOSFET threshold voltage (G1 to G8)			2.8	V
C_{VREG5}	Regulator output capacitor (VREG5)	1.0	2.2		µF
T_A	Operating free-air temperature range	–40		+85	°C
T_J	Operating junction temperature range	–40		+125	°C
AC Characteristics: At VIN = 10V to 28V and T_A = –40°C to +85°C					
t_{WH0}/t_{WL0}	CTRLn pulse duration (CTRL1, 2, 3, 4 = high or low)	4			µs
t_{WH1}/t_{WL1}	EN pulse duration (EN = high or low)	50			µs
t_{SU0}	Setup time (EN to CTRL1, 2, 3, 4)	50			µs
t_{H0}	Hold time (EN to CTRL1, 2, 3, 4)	2			µs

ELECTRICAL CHARACTERISTICS

At VIN = 10.0V to 28.0V and T_A = –40°C to +85°C. Typical values at VIN = 24V and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5960 MIN	TLC5960 TYP	TLC5960 MAX	UNIT
V_{OL}	Open-drain low-level output voltage	I_{OL} = 1mA at XFLT			0.8	V
R_{PD}	Internal pull-down resistance	EN		100		kΩ
		CTRL1 to CTRL4		500		kΩ
		HVM4, CTRL2 > 7.0V		2		MΩ
I_{IN}	VIN supply current	VIN < V_{POR} (1)		20	40	µA
		VIN > V_{POR}, EN = high or low, CTRL1 to CTRL4 = high or low		10	16	mA
I_{OH}	High-level output current (G1 to G8)	EN = CTRL1 to CTRL4 = high	2			mA
V_{OFFSET}	Input offset voltage of output amplifier (S1 to S8)	VADJ = 1.2V	–10		10	mV
V_{DREF+}	HVM upper threshold (D1 to D8)	EN = CTRL1 to CTRL4 = high	2.5	2.6	2.7	V
$V_{DREF–}$	HVM lower threshold (D1 to D8)	EN = CTRL1 to CTRL4 = high	1.55	1.6	1.65	V
V_{HVM}	HVM output voltage range (HVM1 to HVM4)	EN = high or low, CTRL1 to CTRL4 = high or low	0.1	0.7	1.3	V
I_{HVM}	HVM output source current	HVM1 to HVM4 = 1.25V			–1.5	mA
	HVM output sink current	HVM1 to HVM4 = 0.14V	1.5			mA
V_{LOD}	LED open detection threshold (D1 to D8 undervoltage detection)	EN = CTRL1 to CTRL4 = high	0.7	0.8	0.9	V
V_{LSD}	LED short detection threshold (D1 to D8 overvoltage detection)	EN = CTRL1 to CTRL4 = high, CTRL2,4 < 6V, HVM 2CH mode	18.0	19.2	20.4	V
V_{FOD}	FET open detection threshold (S1 to S8 undervoltage detection)	EN = high, CTRL1 to CTRL4 = high, VADJ = 5.0V	300			mV
V_{FSD}	FET short detection threshold (S1 to S8 overvoltage detection)	EN = high	0.8	0.9	1.0	V
V_{FSDHYS}	FET short detection hysteresis (S1 to S8 overvoltage detection)		150	200	250	mV
T_{STD}	Thermal shutdown junction temperature (2)			+160		°C
5V LDO		**C_{VREG5} = 2.2µF**				
V_{REG}	Regulator output voltage	10V < VIN < 28V, I_{VREG5} < 25mA	4.75	5.00	5.25	V
I_{LIM}	Current limit	VIN = 24V, VREG5 = 4.5V	20	40	80	mA
		VIN = 24V, VREG5 = 0V	10	20	40	mA
POWER-ON RESET (POR)						
V_{POR}	Undervoltage lockout on VIN	Negative going threshold on VIN	6.5	7.0	7.5	V
V_{PORHYS}	Undervoltage lockout hysteresis			500		mV
AC CHARACTERISTICS		**T_A = +25°C**				
t_{DET}	Protection time after channel enabled		21	26	31	µs
t_{DET1}	Detection time after channel enable			13		µs
t_{DET2}	Protection/XFLT indication wait time after detection (3)			13		µs
t_D	Built-in phase shift unit delay time			13		µs

(1) V_{POR} is the power-on reset voltage.
(2) Specified by design.
(3) XFLT is the fault indicator; protection means that the failed channel shuts off. $t_{DET} = t_{DET1} + t_{DET2}$.

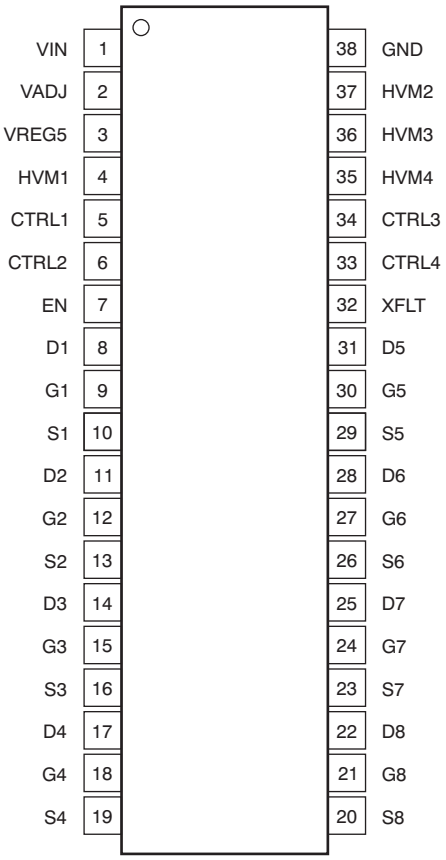
SWITCHING CHARACTERISTICS

At VIN = 10.0V to 28.0V and T_A = –40°C to +85°C, with typical values at V_{IN} = 24V and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5960 MIN	TLC5960 TYP	TLC5960 MAX	UNIT
t_{SW}	Switching time of output current	S1 to S8, from 10% to 90% or 90% to 10%, C_{LOAD} < 100pF		1.5	2	µs

PIN CONFIGURATIONS

DA PACKAGE
TSSOP-38
(TOP VIEW)



PIN DESCRIPTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN	1	I	Supply voltage input
VADJ	2	I	Analog dimming input
VREG5	3	O	Internal linear regulator 5V output
HVM1, 2, 3, 4	4, 35, 36, 37	IO	DC/DC feedback interface for thermal control. HVM4 is also used to set LED short detection threshold during 4CH and 8CH HVM modes (see the *Flexible Configurations of the iHVM* section).
CTRL1, 2, 3, 4	5, 6, 33, 34	I	Parallel PWM input control interface. High turns on corresponding channels. Configuration depends on the HVM mode.
EN	7	I	High enables driver control from CTRL1 to CTRL4. Low disables driver control from CTRL inputs
D1 to D8	8, 11, 14, 17, 22, 25, 28, 31	I	External FET drain node sense voltage input
G1 to G8	9, 12, 15, 18, 21, 24, 27, 30	IO	External FET gate driver output
S1 to S8	10, 13, 16, 19, 20, 23, 26, 29	I	External FET source node sense voltage input
XFLT	32	O	Fault detection notifying buffer output (open drain)
GND	38	—	Common ground

FUNCTIONAL BLOCK DIAGRAM

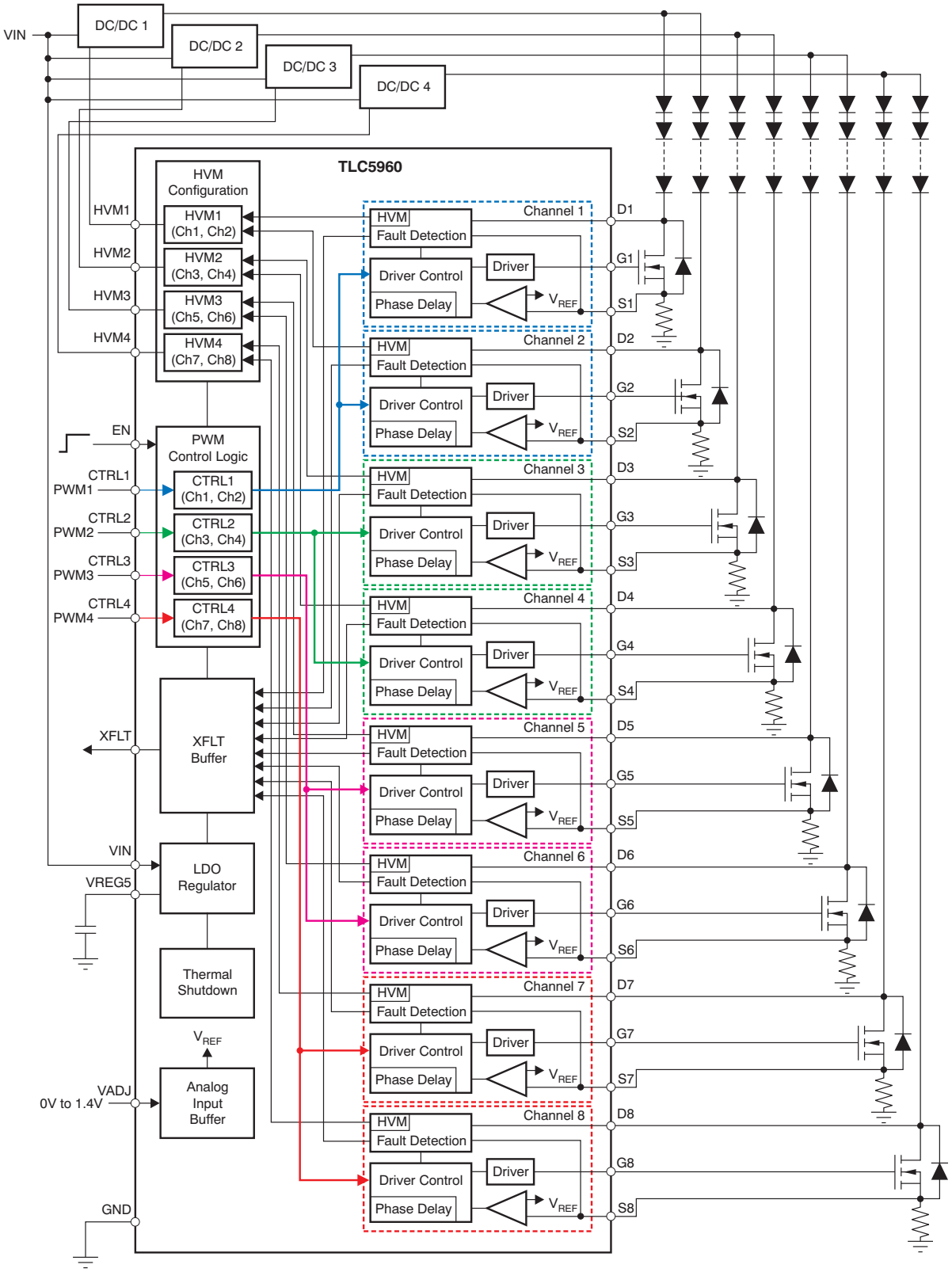


Figure 1. Configuration with Four PWM Inputs and Four DC/DC Converters

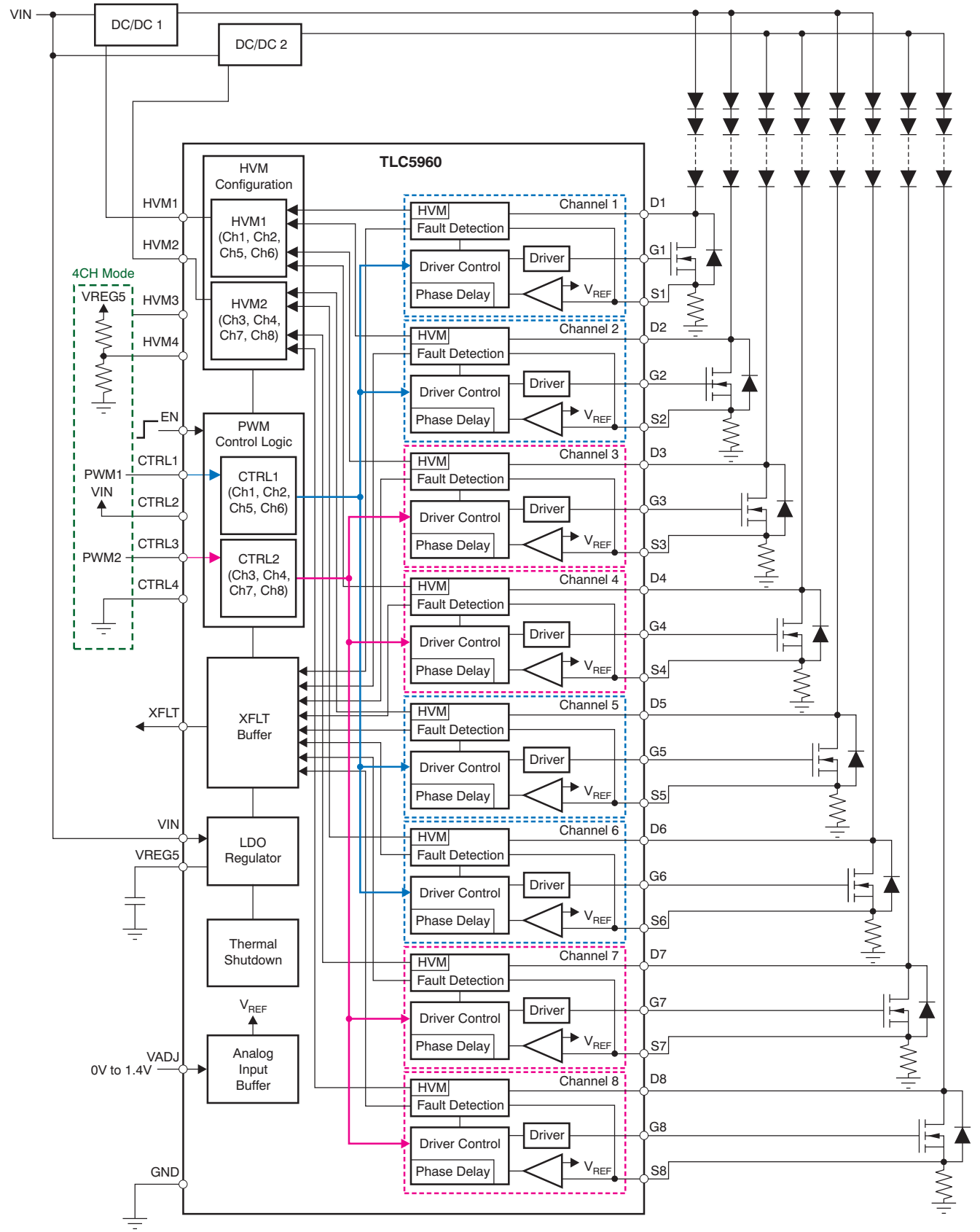


Figure 2. Configuration with Two PWM Inputs and Two DC/DC Converters

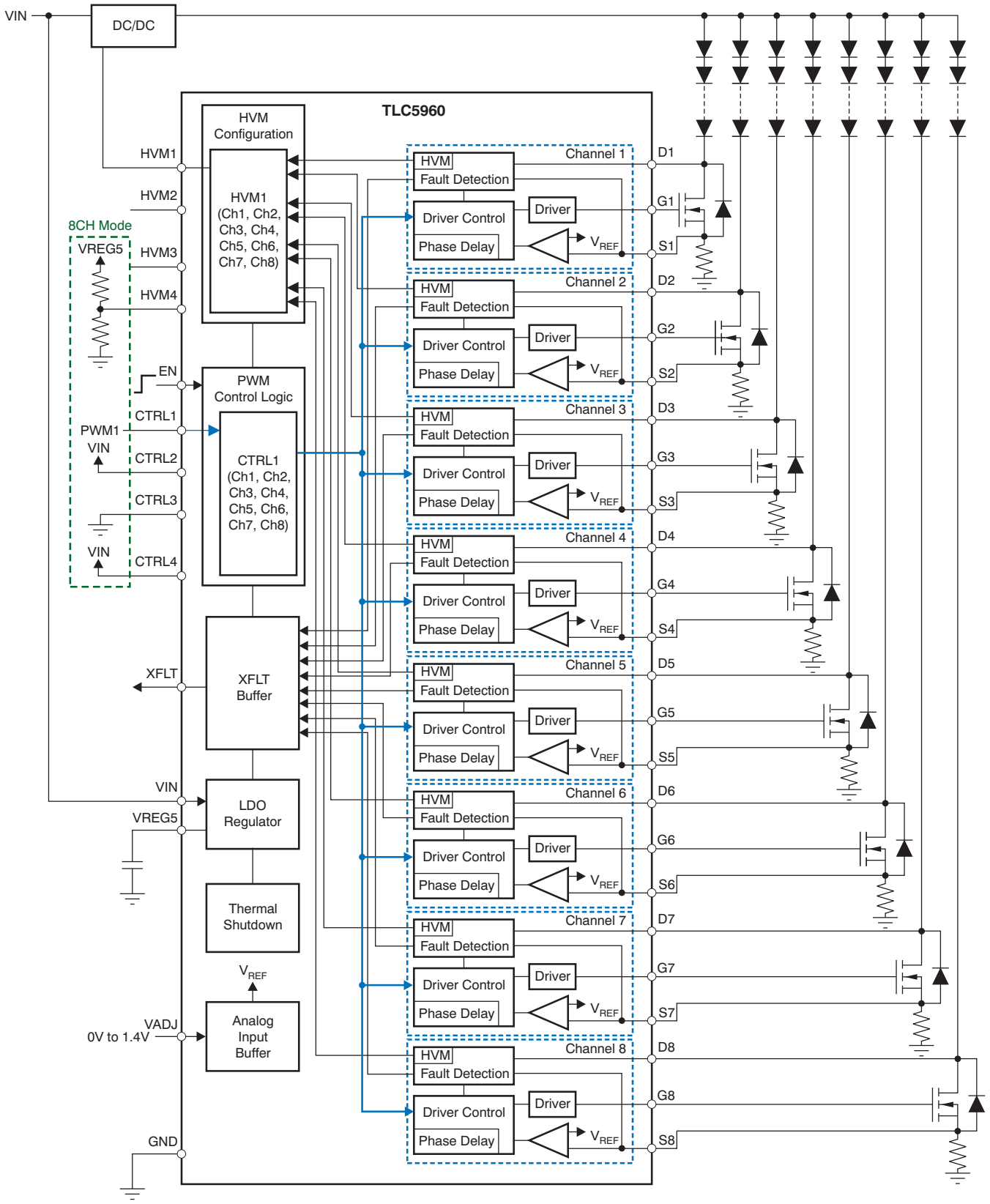
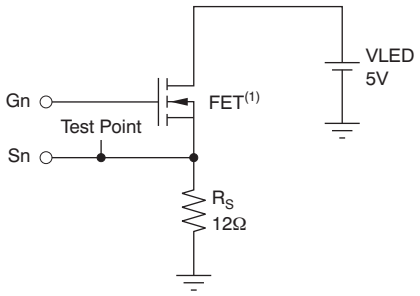


Figure 3. Configuration with One PWM Input and One DC/DC Converter

MEASUREMENT CIRCUIT



(1) Suggested FET: Sanyo MCH6440.

Figure 4. Constant Current Switching Speed (t_{SW}) Measurement Circuit

TYPICAL CHARACTERISTICS

ANALOG DIMMING LINEARITY (I_{LED} vs VADJ)

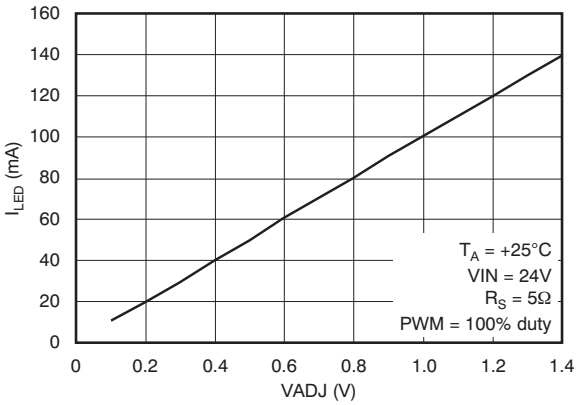


Figure 5.

PWM DIMMING LINEARITY (I_{LED} vs CTRL PULSE DURATION)

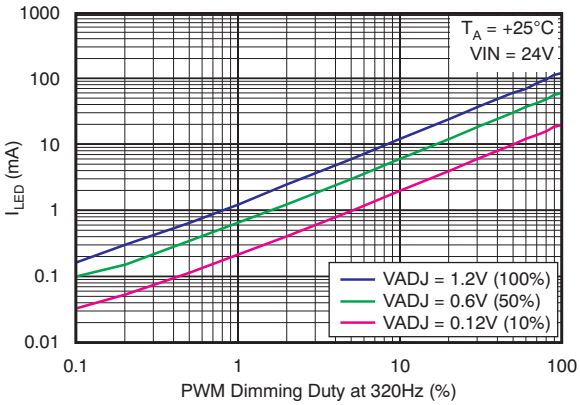


Figure 6.

TYPICAL TURN-ON WAVEFORM

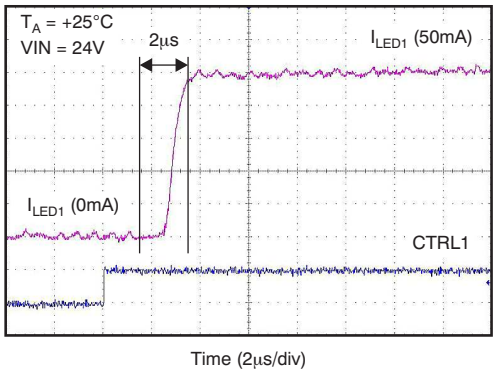


Figure 7.

TYPICAL TURN-OFF WAVEFORM

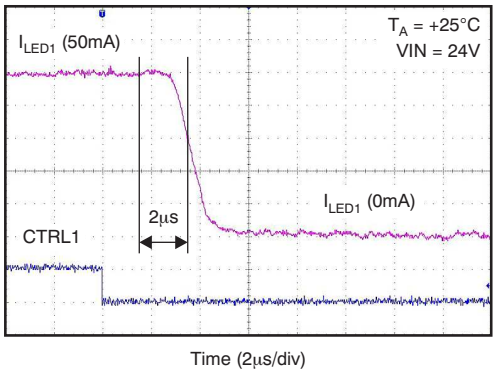


Figure 8.

LDO LOAD REGULATION

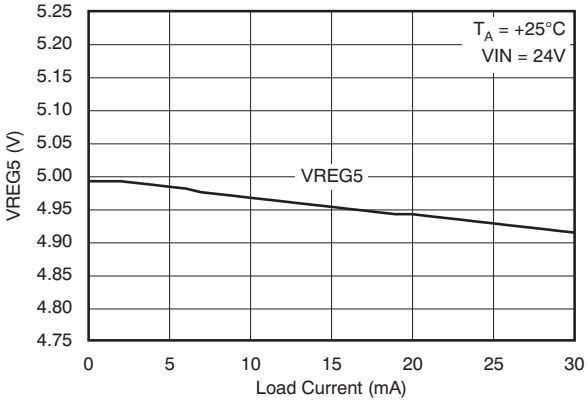


Figure 9.

LDO LINE REGULATION

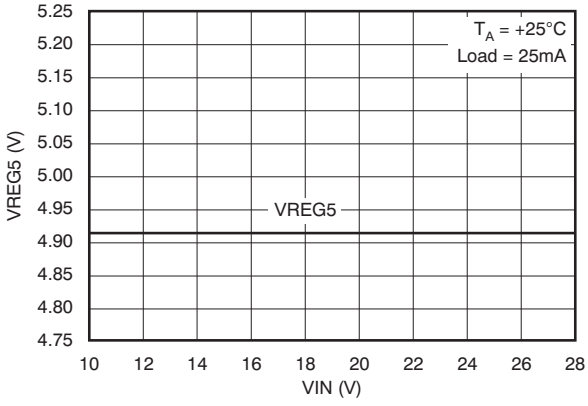


Figure 10.

TYPICAL CHARACTERISTICS (continued)

GATE OUTPUT VOLTAGE LINE REGULATION

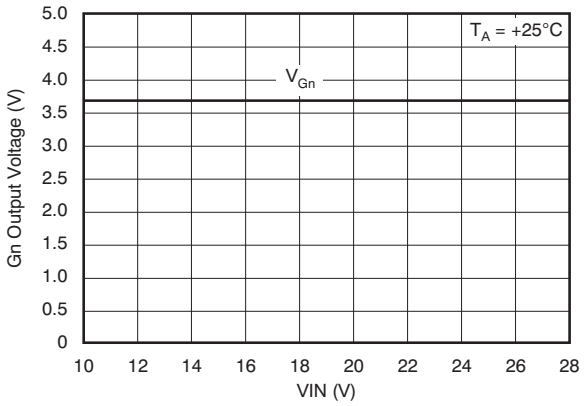


Figure 11.

VIN SUPPLY CURRENT DURING SHUTDOWN MODE (VIN < V_{POR})

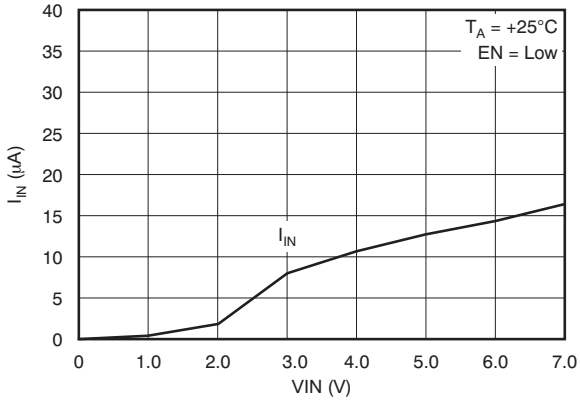


Figure 12.

VIN SUPPLY CURRENT WHEN CHANNELS ARE ENABLED

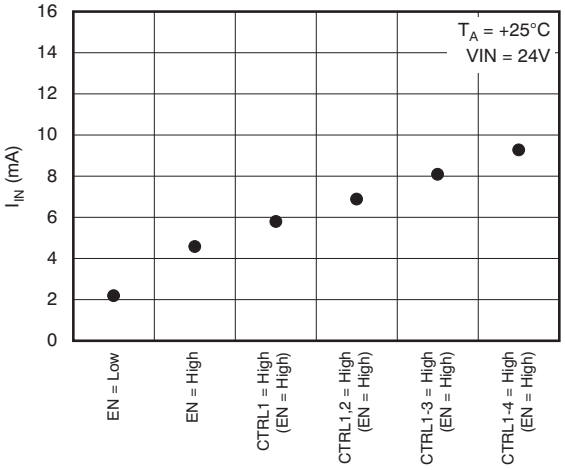


Figure 13.

FUNCTIONAL DESCRIPTION

CONTROLLING THE EXTERNAL-FET GATE DRIVERS

The eight-channel TLC5960 is equipped with eight external-FET gate drivers (one per channel) to drive FETs in series with the LED strings. In normal mode, a CTRL input enables/disables the corresponding two-channel drivers. That is, CTRL1 turns on the channel 1 (ch1) and ch2 gate drive outputs (G1 and G2) sequentially. A total of four parallel inputs (CTRL1 to CTRL4) are used to provide eight channels of PWM control. EN high enables this CTRLn PWM interface, and EN low shuts down all channels simultaneously. The control interface logic truth table is shown in Table 1.

Table 1. Output Channel Control Truth Table (Normal Mode)

EN	CTRL1	CTRL2	CTRL3	CTRL4	OUTPUT STATUS
Low	X	X	X	X	All channels disabled
High	Low	Low	Low	Low	All channels disabled
	High	Low	Low	Low	Ch1 (G1)/Ch2 (G2) enabled
	Low	High	Low	Low	Ch3 (G3)/Ch4 (G4) enabled
	Low	Low	High	Low	Ch5 (G5)/Ch6 (G6) enabled
	Low	Low	Low	High	Ch7 (G7)/Ch8 (G8) enabled
	High	High	High	High	All channels enabled

Figure 14 shows the on and off timing of the control input CTRL1 and the related gate driver outputs of ch1 and ch2. The TLC5960 integrates an internal phase shift function between the channels; therefore, the G1 and G2 outputs on-off timing have an internal unit delay time (t_D). Refer to the *Built-In Phase Shift and PWM Input Minimum On-Time Requirement* section for more details. The EN signal polarity change, on the other hand, immediately applies to all channel outputs.

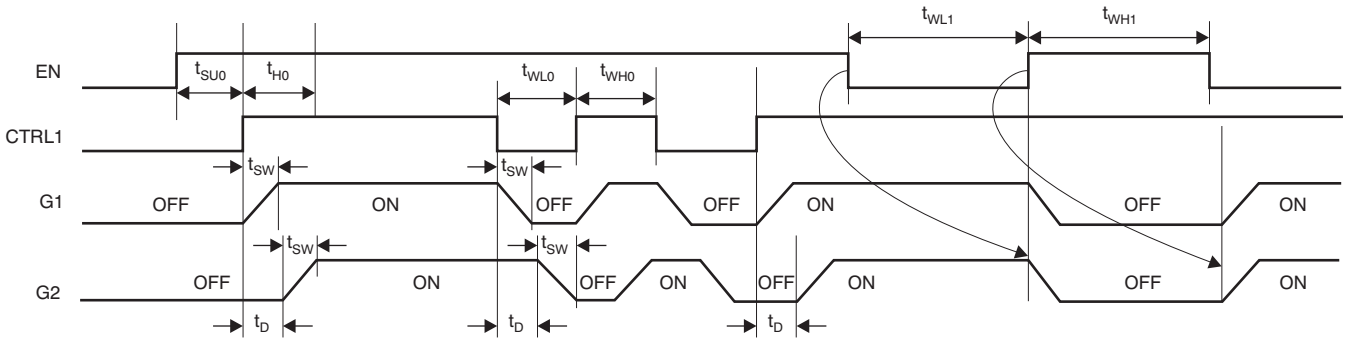


Figure 14. Gate Driver On and Off Timing Sequence

CONSTANT CURRENT CONTROL: PWM AND ANALOG DIMMING

The dedicated FET gate drivers help regulate the constant currents on the LED strings, as shown in Figure 15. A sense resistor (R_S) sets the constant current value on the corresponding LED channel. The gate driver regulates this source node (Sn) voltage to be the same as the internal reference voltage (V_{REF}). The default setting of V_{REF} is 0.6V. This internal reference voltage can be configured through the external input, VADJ. This function can be used as a linear or analog dimming function for all LED strings simultaneously. As shown in Figure 16, the TLC5960 uses halved VADJ input as the internal V_{REF}. If VADJ is greater than 1.4V, the internal V_{REF} falls back to the typical 0.6V (100% analog dimming). Here, 1.4V is a positive-going threshold and is designed to have 100mV negative-going hysteresis as a noise margin. The V_{REF} fallback mechanism is also applied in case VADJ = open. The analog dimming linearity range is specified from 10% to 100%.

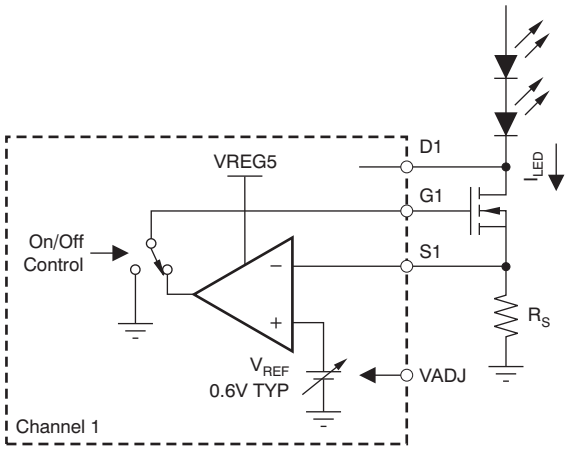


Figure 15. Constant Current Drive Amplifier

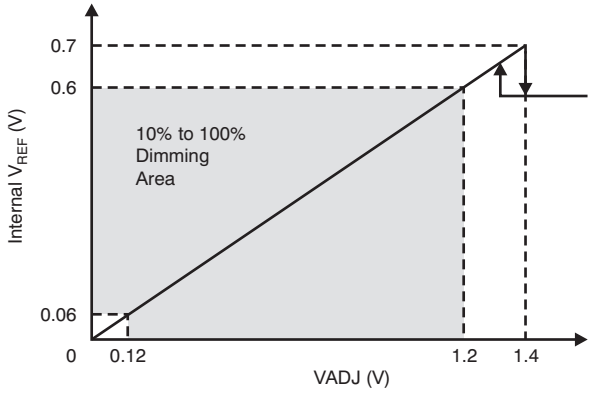


Figure 16. VADJ vs Internal Reference Voltage

The constant current value in the LED strings is set using the following equations:

$$\text{If VADJ} < 1.4\text{V, then } I_{LED} = \frac{VADJ/2}{R_S} \quad (1)$$

$$\text{If VADJ} > 1.4\text{V, then } I_{LED} = \frac{0.6V}{R_S} \quad (2)$$

CHANNEL-TO-CHANNEL CONSTANT CURRENT MISMATCH RATING

The current mismatch rate between channels is primarily induced by the external sense resistor mismatch rating. Additionally, the TLC5960 driver input offset contributes to the current mismatch rating between the channels. The gate drive amplifier offset (V_{OFFSET}) is specified in the *Electrical Characteristics*.

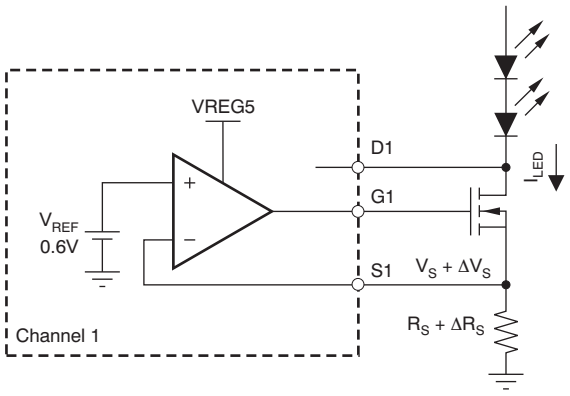


Figure 17. Channel-to-Channel Mismatch Factors

Figure 17 shows the mismatch contributing factors on this system. ΔR_S represents the resistor mismatch. ΔV_S denotes the contribution of the gate amplifier input equivalent offset, V_{OFFSET}. Using these two external and internal error factors, the total mismatch rate is estimated in Equation 3. In this case, with a 1% accurate R_S used, the total current mismatch value is estimated within 1.9%.

$$I_{LED} = \frac{V_S + \Delta V_S}{R_S + \Delta R_S} \approx \frac{V_S}{R_S}\left(1 + \frac{\Delta V_S}{V_S} - \frac{\Delta R_S}{R_S}\right)$$

$$\Delta I_{LED} = \frac{V_S}{R_S}\left(\frac{\Delta V_S}{V_S} - \frac{\Delta R_S}{R_S}\right) \quad (3)$$

BUILT-IN PHASE SHIFT AND PWM INPUT MINIMUM *ON*-TIME REQUIREMENT

The TLC5960 is equipped with a built-in phase shift function to prevent noise from affecting all eight channels. The gate drive timing has a sequential delay time between each combination of channels. This built-in delay time (t_D) is typically 13µs, and consists of four internal clock cycles. Figure 18 describes the phase shift sequence. G1 turns on immediately after the CTRL1 input goes high. After the unit delay of t_D, the G2 output powers on. On the other hand, G3, which is driven by control input CTRL2, already has twice the unit delay from the turn-on timing of CTRL2. G4 turns on after G3 with a sequential unit delay. CTRL3 turns on G5 and G6; these outputs have a built-in (t_D × 4) and (t_D × 5) phase shift, respectively. Finally, CTRL4 turns on G7 and G8; these outputs have built-in (t_D × 6) and (t_D × 7) phase shift, respectively, from CTRL4 *on*-timing. This description is for the HVM 2CH mode; however, the phase shift function is available in all of the HVM modes. In 4CH HVM mode, CTRL1 drives G1, G2, G6, and G7. These output delays are fixed at 0, t_D, (t_D × 5), and (t_D × 6), respectively. CTRL3 turns on the other four channels, G3, G4, G7, and G8. These phase shifts are also fixed at (t_D × 2), (t_D × 3), (t_D × 6), and (t_D × 7), respectively. The phase shift function works in the same manner in the 8CH HVM mode.

The internal clock cycle is equal to the minimum on-time of the TLC5960 gate driver. The gate drivers are designed to drive the external FET turn-on and turn-off within 1µs for both rise and fall times, typically. Therefore, the internal clock cycle of 3.2µs defines the minimum on-time pulse width on the LED strings in the TLC5960-based system.

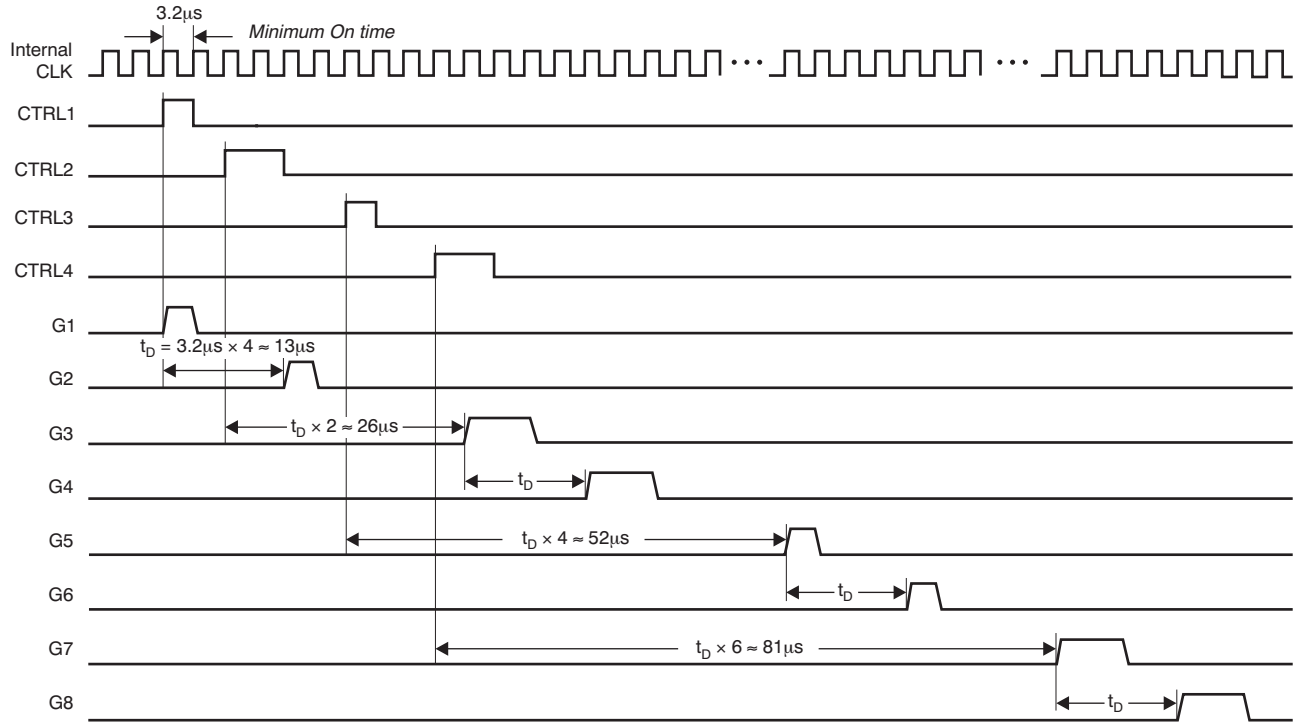


Figure 18. Built-In Phase Shift Output Sequence

PROTECTION FEATURES

The TLC5960 provides protection features to keep the entire system safe. The TLC5960 internal error recognition routine is triggered when the detection comparator detects an abnormal system status. After the error recognition, the TLC5960 first shuts off the corresponding error channel and separates the channel from the other normal operating channels; then, the TLC5960 indicates the error status through the XFLT buffer drive. In cases of LED failure, the TLC5960 provides protection for both the LED open detection (LOD) and LED short detection (LSD). Also, if the external FET fails, the FET open detection (FOD) and FET short detection (FSD) features are provided, as shown in Figure 19.

The error status can be easily identified by monitoring the XFLT output. The XFLT output drive is designed to toggle with a different duty ratio, each with a fixed frequency corresponding to the failure mode. The XFLT toggle frequency is approximately 80kHz. The duty ratio is 25%, 50%, 75% ,and 100% for each of the respective failure modes: LOD, LSD, FOD, and FSD. Table 2 summarizes the indications and the protective actions to take for all protection modes.

The appropriate LED short detection (LSD) threshold can be selected in 4/8CH HVM mode through the HVM4 input voltage. Other detection thresholds are automatically determined internally by the TLC5960.

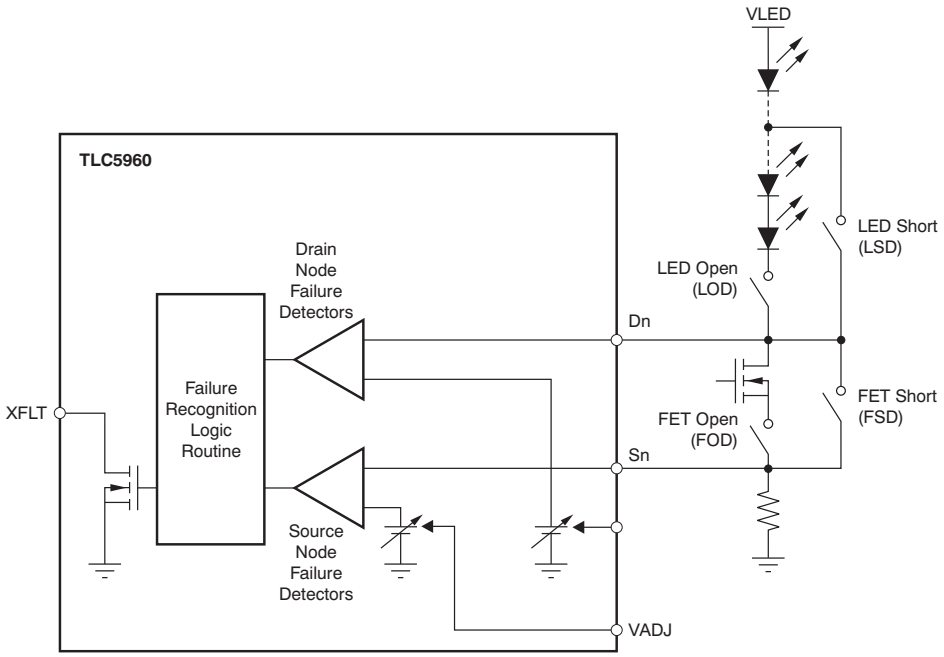


Figure 19. Protection Features on the TLC5960 Driver System

Table 2. Protection Feature Summary

PROTECTION FUNCTION	DETECTION THRESHOLD	MONITOR	LATCH	INDICATION	PROTECTIVE ACTION	RECOVERY CONDITION
LED open detection (LOD)	Dn < 0.8V	During on	Yes	XFLT = low 25% duty	Channel off	VIN < V_{POR} or toggle EN high, low, high
LED short detection (LSD)	See Note (1)	During on	Yes	XFLT = low 50% duty	Channel off	
FET open detection (FOD)	Sn < VADJ/4 (VADJ < 1.4V)	During on	Yes	XFLT = low 75% duty	Channel off	
FET short detection (FSD) (2)	Sn > 0.9V	Continuous	No	XFLT = low 100% duty	N/A	Sn < 0.7V
Thermal shutdown (TSD)	Temp > +160°C	Continuous	Yes	XFLT = low 100% duty	VREG5 off, all channels off	VIN < V_{POR} or toggle EN high, low, high

(1) Detection threshold is Dn > 19.2V for HVM 2CH mode, and Dn > 8 × HVM4(V) for 4/8CH mode.
(2) In the case of FSD, the TLC5960 has already driven Gn to a lower level so that the failed channel is shut off and no additional protection is needed.

FAILURE MODE DETECTION AND RELEASE TIMING

When the FET is on, the TLC5960 protects the system by monitoring the triggers of the LOD, LSD, and FOD detectors. After the LED channel is on (EN = CTRLn = high), the TLC5960 waits for a detection time of t_{DET1} before capturing the drain and source node information on the external FETs.

In case the error comparator(s) detect an abnormal status, the TLC5960 starts to determine whether this state is a true error condition or not. If the status is determined as an error in system with a processing time of t_{DET2}, the TLC5960 shuts off the corresponding channel(s), separates it from the operating channels, and the XFLT notification sequence is started.

After the abnormal situation is recovered, toggling of the EN pin (high-to-low-to-high) reverts the TLC5960 to the default operating status. Otherwise, the device remains in the error status until VIN is less than V_{POR}. The detection time (t_{DET1}) and error processing time (t_{DET2}) are both set to 13µs. Figure 20 shows the case of CTRL1, D1, and D2.

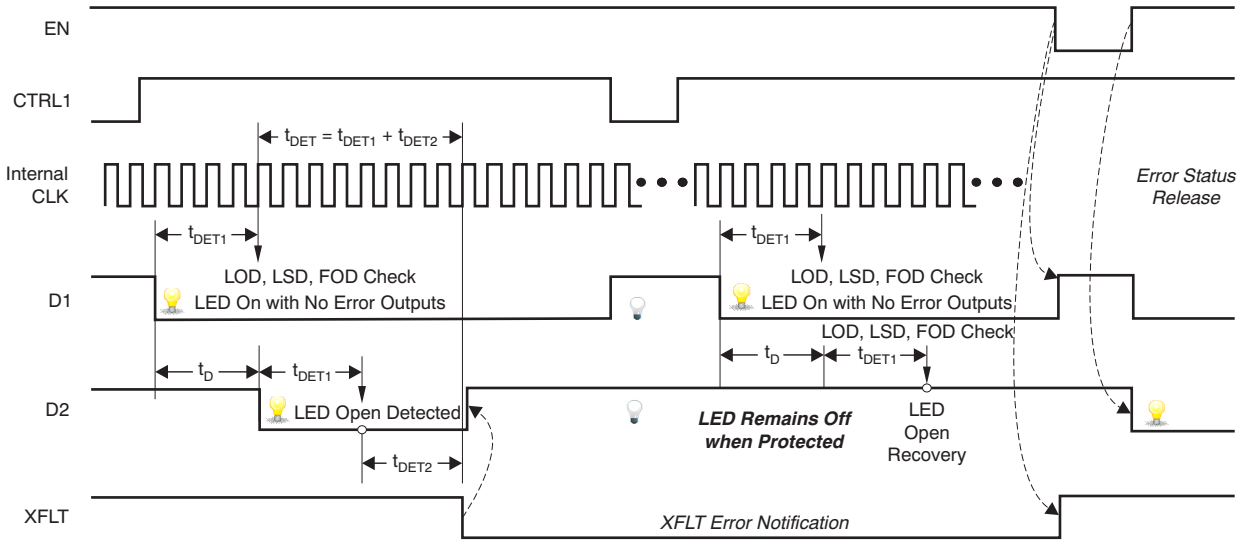


Figure 20. LOD, LSD, and FOD Detection and Error Status Release

LED OPEN DETECTION (LOD) AND LED SHORT DETECTION (LSD)

The TLC5960 senses the drain node of the external FET when the FET is on, as shown in Figure 21. When the LED is open, the drain voltage falls below the default detection level (0.8V). The LED short detection (LSD) triggers at an abnormal overvoltage detection threshold of 19.2V, typically. This LSD detection threshold can be redefined in the 4CH and 8CH HVM modes according to the various system configurations. The threshold is defined by Equation 4 and Equation 5.

For example, when detecting two shorted LEDs on an 15-LED string, this voltage range can be set to ~10V (HVM4 input = 1.25V) in 4CH and 8CH HVM modes. This ~10V voltage setting can be calculated by multiplying V_F by the two failed LEDs (~3.5V x 2 = 7V) and adding the result to the normal regulating Dn voltage range (1.6V to 2.6V). In the case of LDO and LSD, the TLC5960 shuts off the failed LED string(s) and automatically separates the failed string(s) from the operating strings.

For 2CH HVM mode: V_{LSD} = 19.2V (4)

For 4/8CH HVM modes: V_{LSD} = 8 × HVM4 (V) (5)

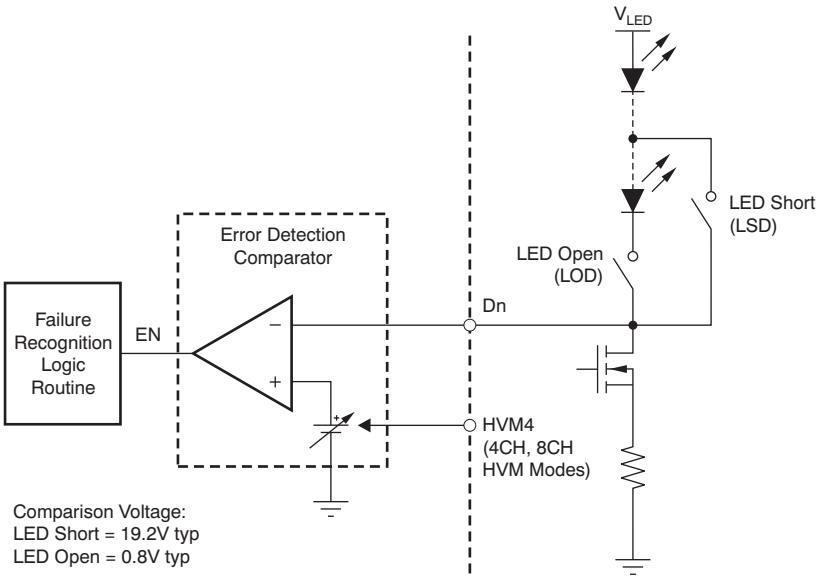


Figure 21. TLC5960 Drain Terminals Sensing to Protect LED Failure

FET OPEN DETECTION (FOD) AND FET SHORT DETECTION (FSD)

The TLC5960 monitors the source terminal of the FETs to detect any abnormal status of the external FETs, as shown in Figure 22. In case a FET is open (FOD), the source node stays at a lower level, even if the TLC5960 drives the gate voltage higher and higher. To detect this error status, the default threshold is set to 0.3V. The TLC5960 automatically adjusts the detection threshold internally, as described in Equation 6 and Equation 7, depending on the analog dimming setting.

$$\text{If VADJ} < 1.4\text{V, then } V_{FOD} = \frac{\text{VADJ}}{4}\ (\text{V}) \quad (6)$$

$$\text{If VADJ} > 1.4\text{V, then } V_{FOD} = 0.3\text{V} \quad (7)$$

The FET short detection (FSD) detects overvoltage sensed at the source node. This failure mode usually implies that the overcurrent is in the entire system and it may induce a critical situation because of potential thermal-related issues. The TLC5960 always monitors the FSD threshold to keep the entire system safe. The detection threshold is typically set at 0.9V.

In the case of FOD, the TLC5960 shuts off the failed LED string(s) and automatically separates the failed string(s) from the operating strings. In the case of FSD, the TLC5960 normal function already shut off the failed LED string(s), and then the TLC5960 delivers the failure notification signal through the XFLT output buffer. If the failure phenomenon is removed, the FSD is automatically recovered, unlike LOD, LSD, and FOD, as shown in Table 2.

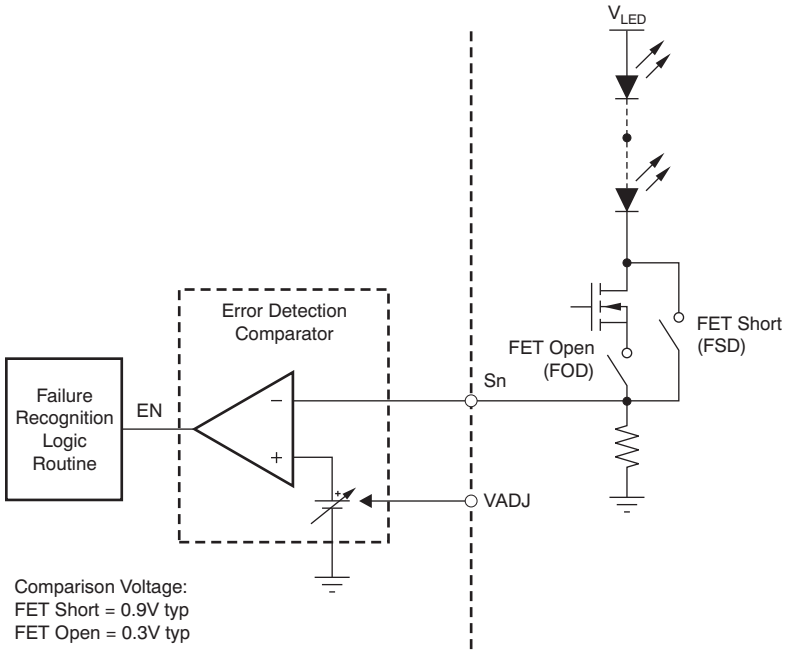


Figure 22. TLC5960 Source Terminal Sensing to Protect FET Failure

THERMAL SHUTDOWN

The TLC5960 includes integrated internal temperature sensors for providing thermal shutdown protection. If an over-temperature state is detected, the TLC5960 automatically shuts down all the functions, including the internal low-dropout regulator (LDO). This status is latched until VIN < V_{POR}, or the EN input signal toggles from high to low to high.

POWER-ON RESET (POR)

The TLC5960 is equipped with internal power-on reset circuitry. When VIN < 7.0V, the remaining circuit blocks are all locked to stay in standby mode. This function is also called *undervoltage lockout* (UVLO). The specifications for V_{POR} and V_{PORHYS} are listed in the *Electrical Characteristics*.

HEADROOM VOLTAGE MONITOR FEEDBACKS (iHVM)

The TLC5960 provides an intelligent feedback mechanism of the headroom voltage information to automatically adjust the dc/dc converter output voltage. Up to four dc/dc converter outputs can be optimized using the TLC5960 iHVM buffers; the output levels are automatically adjusted through the internal iHVM mechanism.

Figure 23 shows a basic configuration of one dc/dc converter for a two-channel output (HVM 2CH mode). Only one additional external resistor is required to modify the dc/dc converter output voltage.

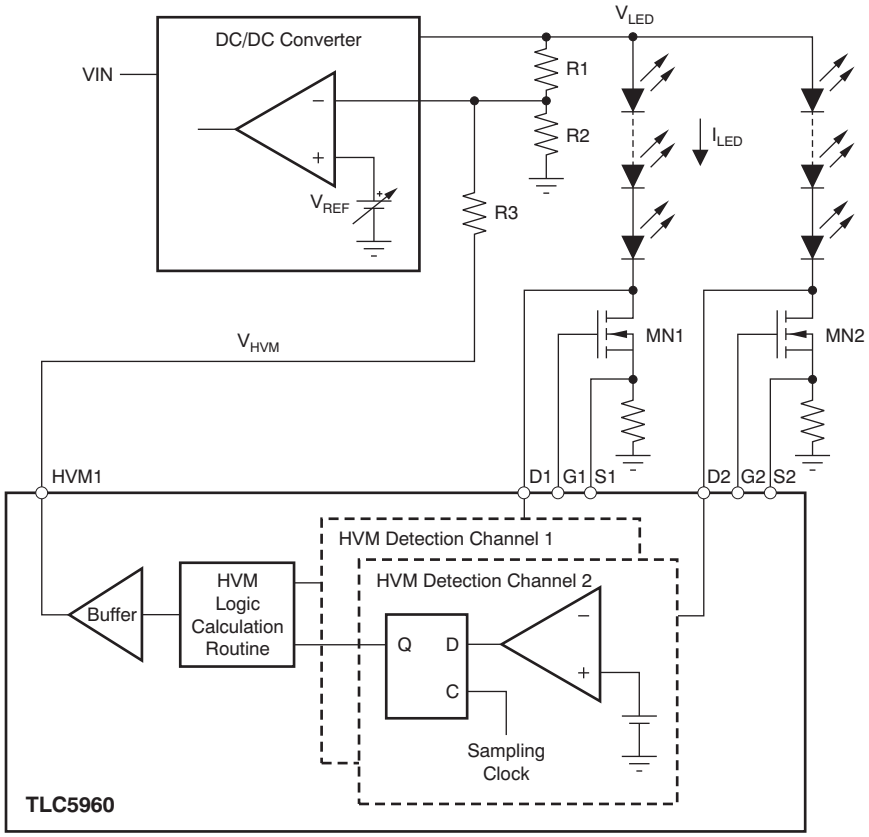


Figure 23. Headroom Voltage Monitor Feedback Mechanism

SETTING THE DC/DC CONVERTER OUTPUT RANGE

The given V_{LED} voltage setting by the iHVM system is shown in Equation 8. V_{REF} is the internal reference voltage of the dc/dc converter. V_{HVM} is the regulated voltage output from the HVM buffer, which outputs 0.7V initially and is automatically adjusted by the internal iHVM mechanism.

$$V_{LED} = \frac{R1 + R2}{R2} \times V_{REF} + \frac{R1}{R3} \times (V_{REF} - V_{HVM}) \quad (8)$$

The voltage range for V_{HVM} is 0.14V (min) to 1.25V (max) with a typical value of 0.7V. Given these values, the available V_{LED} range with iHVM is calculated as shown in Equation 9 through Equation 11:

$$V_{LEDMIN} = \frac{R1 + R2}{R2} \times V_{REF} + \frac{R1}{R3} \times (V_{REF} - 1.25) \quad (9)$$

$$V_{LEDTYP} = \frac{R1 + R2}{R2} \times V_{REF} + \frac{R1}{R3} \times (V_{REF} - 0.7) \quad (10)$$

$$V_{LEDMAX} = \frac{R1 + R2}{R2} \times V_{REF} + \frac{R1}{R3} \times (V_{REF} - 0.14) \quad (11)$$

In this case, if V_{REF} = 0.7V, R1 = 200kΩ, R2 = 1kΩ, and R3 = 20kΩ, then the variable range on the dc/dc output, V_{LED}, is 140V ±6V. The appropriate V_{LED} voltage range can easily be set by selecting the values of R1, R2, and R3.

BASIC POWER DISSIPATION CONSIDERATIONS

The most critical components for power consumption are the external FETs in the system. These components are critical because the forward voltage variance of all the LED strings are concentrated in these components. For optimal system performance with the appropriate thermal dissipation, the LED selection and iHVM V_{LED} range must be set accordingly. The iHVM V_{LED} range should be determined from the V_{LED} worst-case variance without turning off the LED strings. Here, the FET power dissipation rating (P_{FET}) is defined as shown in Equation 12:

$$P_{FET} = (V_D - 0.6) \times I_{LED} \quad (12)$$

If the FET is supposed to tolerate 1W, then the V_D should be 10.6V under worst-case conditions with a 100mA I_{LED} setting.

FLEXIBLE CONFIGURATIONS OF THE iHVM

The TLC5960 provides flexible configurations for the dc/dc converter and LED driver channel count. By default, the TLC5960 has four PWM inputs, eight LED strings, and four dc/dc converter control outputs (2CH mode). In this case, the best thermal capability is provided with dc/dc peripherals overhead; see Figure 24. The TLC5960 provides drain node voltage control within the range of 1.6V to 2.6V on at least four out of eight channels. The upper-right side of Figure 24 illustrates this four-channel control capability that automatically minimizes the FET power dissipation.

The TLC5960 integrates two other configuration modes: 4CH HVM mode and 8CH HVM mode. In these modes, the TLC5960 is capable of controlling the headroom voltage range in two out of the eight channels, or one out of eight channels. Also in these modes, the total V_D variance that is coming from the LED V_F variance is much larger than in 2CH mode, as shown in the upper-right side of Figure 25. If the LED components are not appropriately selected, only one LED string is well-controlled within the HVM range of 1.6V to 2.6V. It is more important to have a better selection criteria on LEDs instead of than less peripheral overhead in order to better handle the thermal rating.

Application of voltage greater than 7.0V on CTRL2 drives the TLC5960 HVM mode into 4CH mode. CTRL1 and CTRL3 PWM inputs are used to control Ch1, Ch2, Ch5, Ch6 and Ch3, Ch4, Ch7, Ch8, respectively. Two HVM outputs are used to control two dc/dc converter output voltages. If voltage greater than 7.0V is placed on both CTRL2 and CTRL4, the TLC5960 HVM logic goes into 8CH mode. CTRL1 controls all of the LED string outputs and the HVM output is consolidated into one HVM1 output. Table 3 summarizes the HVM mode configurations. The applicable voltage on CTRL2 and CTRL4 is defined up to the VIN level. It is recommended to tie CTRL2 and/or CTRL4 to VIN through a 10kΩ resistor.

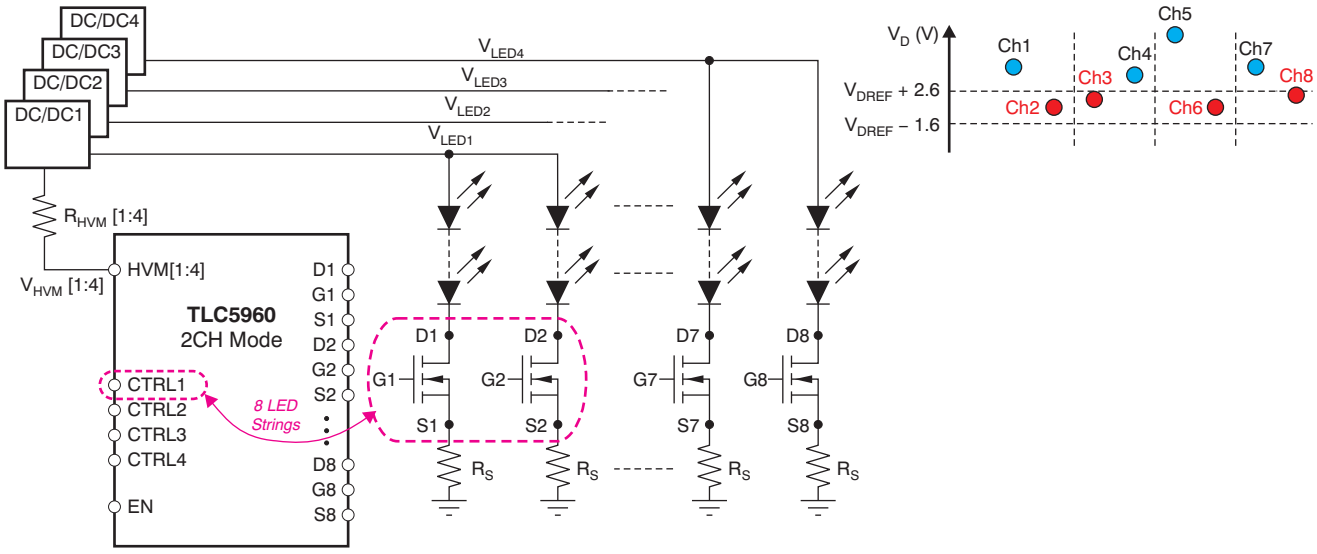


Figure 24. HVM 2CH Mode Typical Configuration

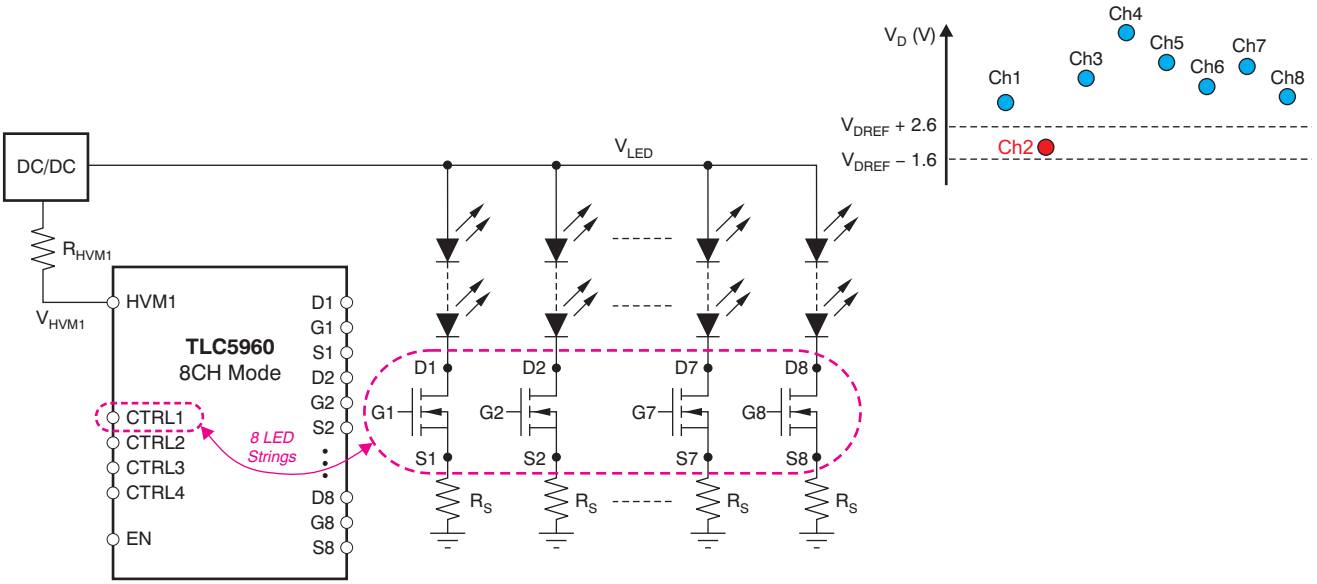


Figure 25. HVM 8CH Mode Typical Configuration

On the 4CH mode and 8CH mode, the TLC5960 LED-Short-Detection threshold voltage can be adjusted by setting the external input voltage to the HVM4 pin. The threshold calculation is shown in Equation 5.

Table 3. HVM Configuration Modes

HVM LOGIC MODE	IN				OUT			
	CTRL1	CTRL2	CTRL3	CTRL4	HVM1	HVM2	HVM3	HVM4
2CH	Ch1, 2	Ch3, 4	Ch5, 6	Ch7, 8	Ch1, 2	Ch3, 4	Ch5, 6	Ch7, 8
4CH	Ch1, 2, 5, 6	> 7.0V	Ch3, 4, 7, 8	GND	Ch1, 2, 5, 6	Ch3, 4, 7, 8	N/A	REFLSD (Input)
8CH	Ch1 to Ch8	> 7.0V	GND	> 7.0V	Ch1 to Ch8	N/A	N/A	REFLSD (Input)

APPLICATION INFORMATION

CASCADING SYSTEM USING iHVM

iHVM provides flexibility to the application configuration with a minimum of external components. Figure 26 shows an example for using a diode-OR to configure multiple iHVM controllers. This configuration can be applicable to as many controllers as a daisy-chain configuration allows. Care must be taken regarding the available HVM voltage range affected by the dc/dc converter reference voltage shown in Equation 13 through Equation 16. For example, the TPS40210 internal reference voltage is 700mV. In case of this combination, the diode-OR operation achieves the minimum voltage of the HVM buffer outputs, and the V_{LED} adjustable range is limited to the upper-half region compared to the normal configuration.

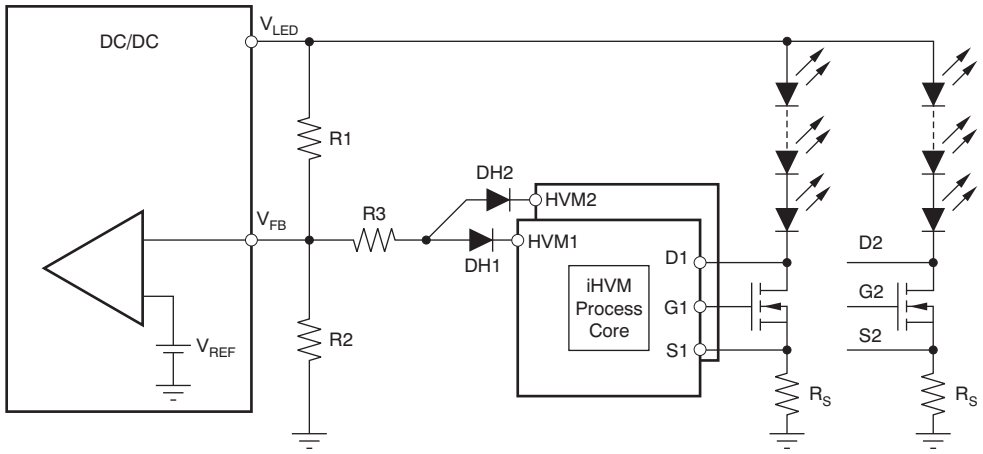


Figure 26. iHVM System Cascade Configuration through a Diode-OR

$$V_{LED} = \frac{R1 + R2}{R2} \times V_{REF} + \frac{R1}{R3} \times (V_{REF} - V_F - V_H)$$

Where:

$V_H = \text{Min}(V_{H1}, V_{H2})$

$V_{REF} - V_F - V_H \geq 0$

V_F = forward voltage of DH1 and DH2 (13)

$$V_{LEDMIN} = \frac{R1 + R2}{R2} \times V_{REF} + \frac{R1}{R3} \times (V_{REF} - V_F - 1.25) \quad (14)$$

$$V_{LEDTYP} = \frac{R1 + R2}{R2} \times V_{REF} + \frac{R1}{R3} \times (V_{REF} - V_F - 0.7) \quad (15)$$

$$V_{LEDMAX} = \frac{R1 + R2}{R2} \times V_{REF} + \frac{R1}{R3} \times (V_{REF} - V_F - 0.14) \quad (16)$$

In this case, if V_{REF} = 0.7V, R1 = 200kΩ, R2 = 1kΩ, and R3 = 20kΩ, then the diode forward voltage of V_F = 0.3V and the available V_{LED} output range would be 138V to 143V. Refer to Equation 9 to compare with normal conditions.

UNUSED DRIVER OUTPUT CONNECTION

Figure 27 shows the recommended connection when not all eight channels are needed. Basically, Dn should be connected to the adjacent pin of the corresponding D terminal in order to prevent the TLC5960 protection routine from activating these unneeded output pins. The Gn and Sn pins should be tied together.

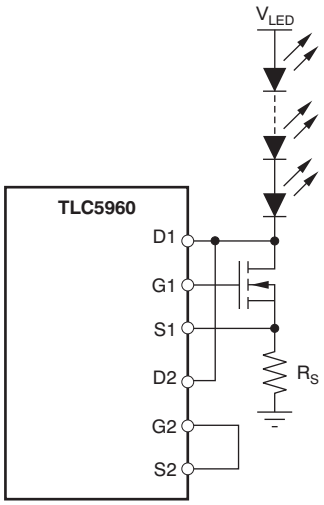


Figure 27. Unused Driver Output Recommended Connection

BIPOLAR DRIVE CAPABILITY

The TLC5960 integrated driver is designed to work with not only FETs, but also with bipolar devices, as shown in Figure 28. In this case, the amount of the base current must be considered when you define the LED current. The amount of base current is deducted from the LED current, based on Equation 17. The output current capability of Gn is specified as I_{OH} in the *Electrical Characteristics*.

$$I_{LED} = \frac{V_{REF}}{R_S} - I_B \tag{17}$$

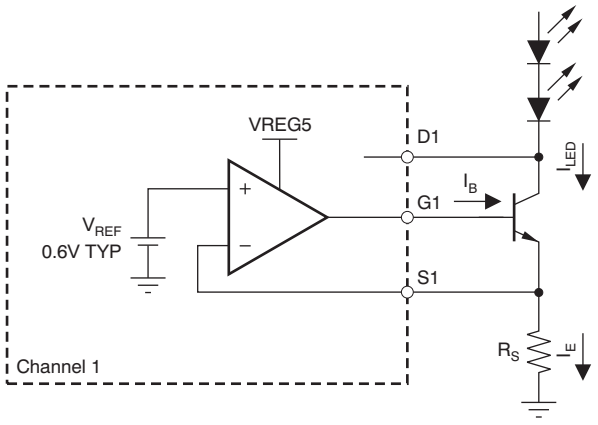


Figure 28. Bipolar Output Capability

iHVM: STABILITY ANALYSIS ON CONVENTIONAL SYSTEM

Figure 29 shows a *dual loop*, a conventional dc/dc output topology adjustment enabled by the information of the drain node feedback mechanism. This system basically consists of two feedback loops. The primary feedback loop is a voltage feedback loop for the dc/dc converter. The additional secondary feedback loop is established to integrate the cathode node information of the LED string to optimize thermal dissipation regarding LED string voltage change as a result of variance of LED component forward voltage.

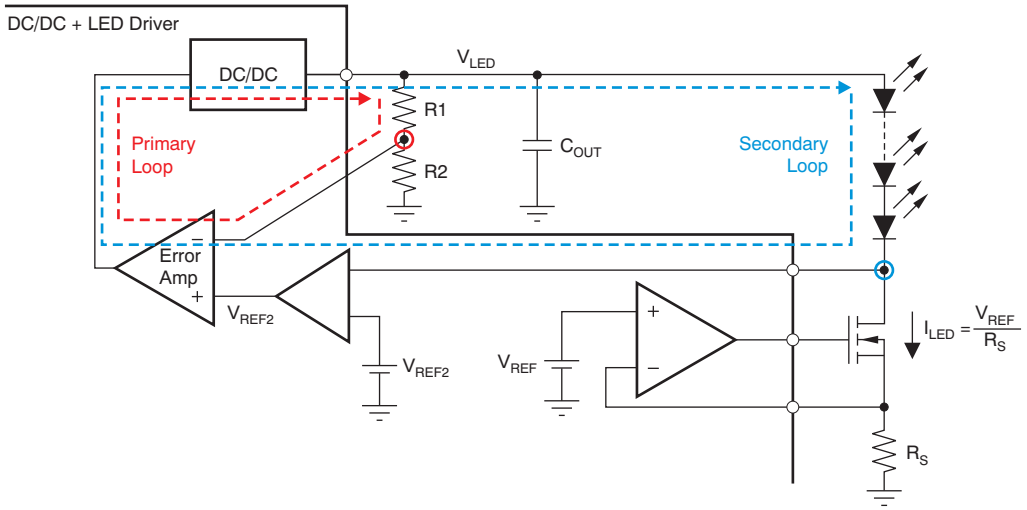


Figure 29. Conventional Drain Information Feedback Loop Structure

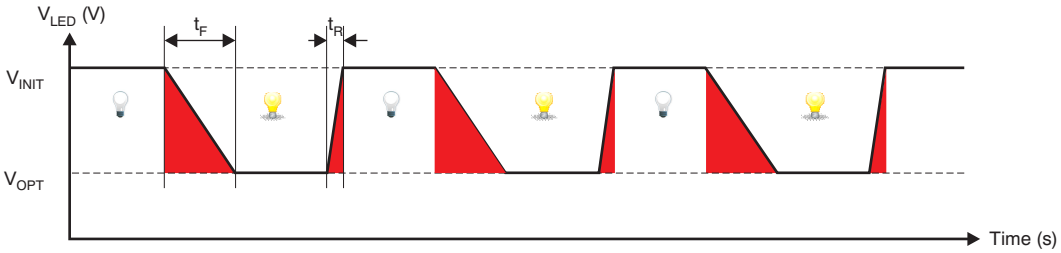
In order to keep this total system stable, the circuit constants are appropriately set so that they do not conflict with these feedback loops. The primary loop frequency response must be set faster than the secondary loop; typically, a 10x faster setting is known to generate a stable system.

The conventional approach restricts total system performance on the following:

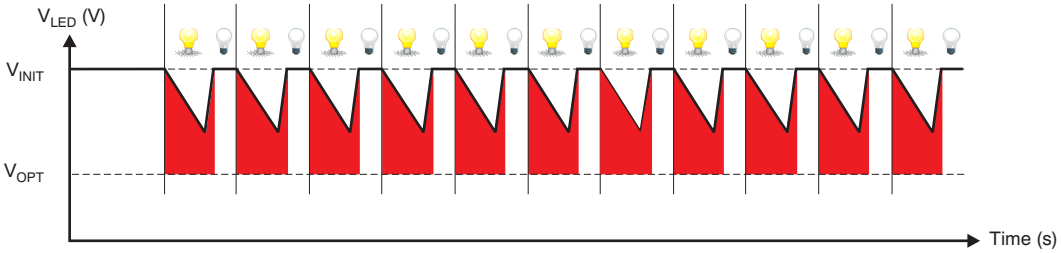
1. The LED drive dimming speed must be as slow as the secondary loop response; or,
2. If faster dimming LED switching is needed, then the dc/dc output capacitance must be larger (sometimes over 1000µF) in order to keep the V_{LED} line stable enough, with tight LED forward voltage selection criteria to maintain required thermal performance.

Figure 30(a) shows a typical switching of the on-off sequence in this conventional system. Here, V_{LED} (the output voltage of the dc/dc converter) starts from a higher point (V_{INIT}). As the drain node information feedback loops, the V_{LED} is driven lower to the appropriate voltage level (V_{OPT}) for lower power consumption while maintaining the constant current regulation. After the signal feedback, the V_{LED} transient speed is limited by the primary loop response speed and the slowest timing in this sequence is normally the falling edge of V_{LED}. The maximum speed of the falling time (t_F) is calculated in Equation 18, and only the constant current of I_{LED} is available to lower the V_{LED} in an LED backlight system.

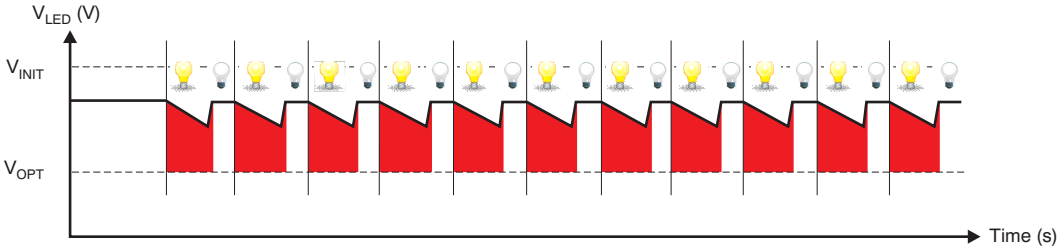
$$t_F = \frac{C_{OUT}}{I_{LED}} \times (V_{INIT} - V_{HVM}) \quad (18)$$



(a) Typical Setting with Appropriate LED Switching



(b) Faster LED Switching: Not Enough Settling Time



(c) Faster LED Switching with Large C_{OUT}: Tight LED Selection Needed

Figure 30. V_{LED} Voltage Regulation Sequence on Conventional System

In this case, with C_{OUT} = 100µF, I_{LED} = 100mA, V_{INIT} = 180V and V_{OPT} = 155V, the maximum speed of t_F is calculated as 25ms. This slower transient speed absolutely limits the LED switching speed. If maximum t_F is 25ms, the fastest dimming cycle with a full dual-loop system advantage is limited to only 40Hz. If the LED switching speed is faster than that value, the V_{LED} regulation voltage would appear as shown in Figure 30(b). HVM power saving is only achievable with one-fourth of the typical case (a).

To solve this situation on a conventional system, C_{OUT} can sometimes be increased to keep the voltage stable. Figure 30(c) shows that switching waveform. These possible power-savings are achieved by lowering V_{INIT} using tightly selected LEDs in relation to its forward voltage specification.

STABILITY ANALYSIS OF PROPOSED iHVM SYSTEM

Figure 31 shows the feedback system with the proposed iHVM control mechanism. The biggest difference (and advantage) compared to a conventional system is that the iHVM processing core controls the secondary loop. With this system, there are no limitations on the primary loop and secondary loop settings. The FETs drain node voltage information is processed easily and can be automatically adjusted to fit the primary loop feedback response, as long as the primary loop unity gain frequency is approximately 1kHz. See Equation 8 for the iHVM output voltage setting calculation. The second term is the variable portion of V_{LED} output voltage and is well-regulated by the iHVM mechanism.

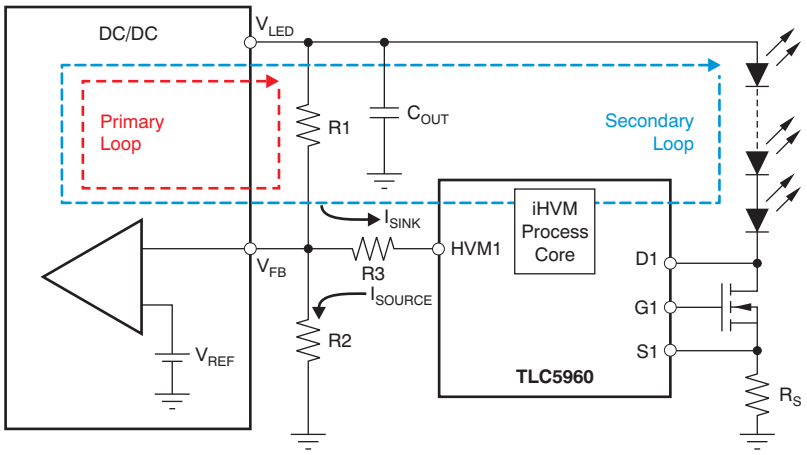


Figure 31. iHVM Loop Structure

Here, focusing on the appropriate minimal time range, the only condition required to maintain the total iHVM feedback system stability is shown in Equation 19.

$$\frac{R1}{R3} \times dv(iHVM) < \frac{I_{LED}}{C_{OUT}} \times dt(iHVM) \quad (19)$$

The left-hand term describes the value of the output voltage range by iHVM during the minimal time of dt(iHVM). Therefore, in an iHVM system, the slowest response in the entire system can be designated by the values of I_{LED} and C_{OUT}, as long as the primary system unity gain frequency is set at a minimum of 1kHz. Here, the derivation of the iHVM circuit response is already known as 10V/s. The resulting equation to keep the entire iHVM system stable is shown in Equation 20.

$$C_{OUT} < \frac{I_{LED}}{10V/s} \times \frac{R3}{R1}$$

Where the unity gain frequency of the primary loop > 1kHz. (20)

In this case, I_{LED} = 100mA, R1 = 400kΩ, and R3 = 40kΩ, C_{OUT} should be less than 1000µF to retain the transient response to achieve 100% power saving by iHVM caused by LED V_F variance. In a typical application, this value is large enough. Therefore, we can conclude that the only condition required to keep iHVM stable is to set the primary feedback loop unity-gain frequency greater than 1kHz with a minimum amount of C_{OUT} (typically 100µF to 300µF, depending on the required LED current value) to keep the V_{LED} line stable when the LED is switching. Refer to the dc/dc controller manual for setting the appropriate minimum output capacitance value.

Figure 32 shows the iHVM transient response. Only the first cycle of the HVM cycle is needed to set the appropriate voltage for the V_{LED} corresponding to the LED strings total V_F. Therefore, the first t_F should be a similar transient with conventional system; however, from the next cycle, the intelligent iHVM mechanism reuses the once-settled value. As shown in the results, the second falling edge can be much faster than the first cycle, and almost zero transient power consumption is achievable in Figure 32(a).

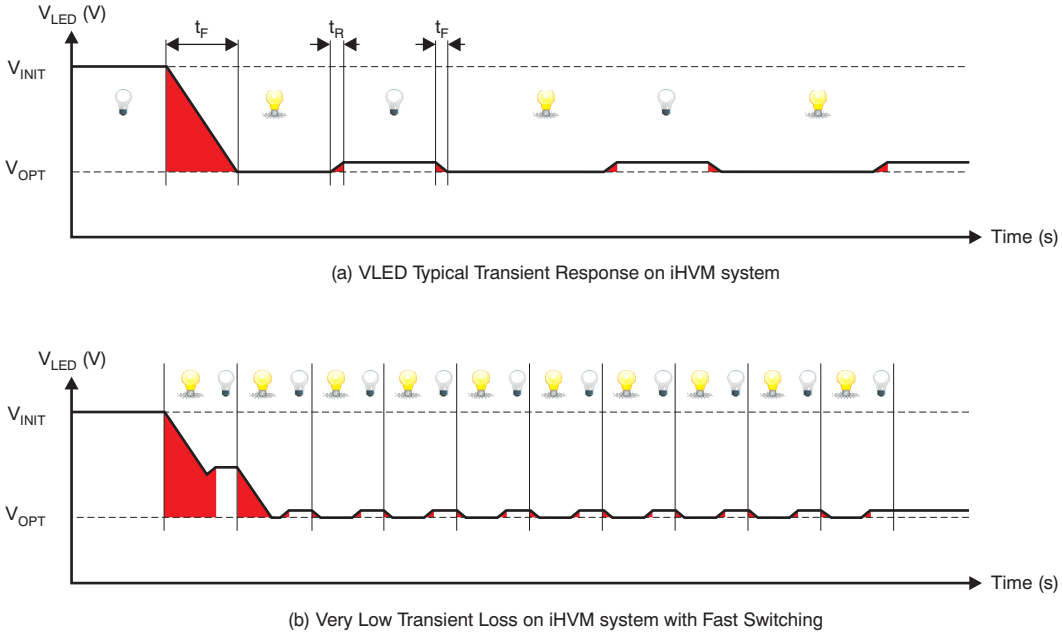


Figure 32. Transient Response of the iHVM-Based System

In addition to this power saving, faster LED switching speeds can be set up to 250kHz. The transient response in this case is shown in Figure 32(b). The power-saving iHVM mechanism is designed to work perfectly with that faster switching speed, as well.

Figure 33 shows the application evaluation results of an iHVM system. As the dc/dc portion, the TPS40210 SEPIC configuration (supply voltage = 170V, V_{LED} ~150V) is employed. 48 LEDs are series connected and R_S is set to 12Ω in order to achieve a 50mA constant current. The iHVM system works well to keep the once-settled V_{LED} voltage well-regulated with a constant current value.

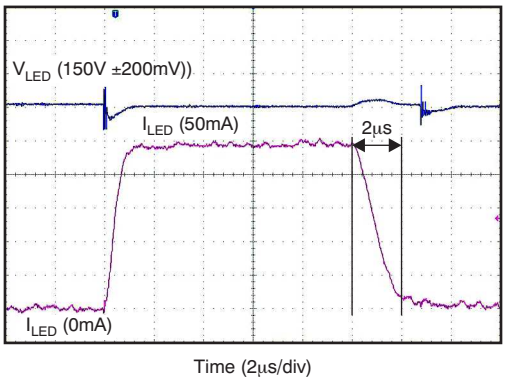


Figure 33. Switching Characteristics for 1% PWM Dimming on 240Hz

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLC5960DA	ACTIVE	TSSOP	DA	38	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5960	Samples
TLC5960DAR	ACTIVE	TSSOP	DA	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5960	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

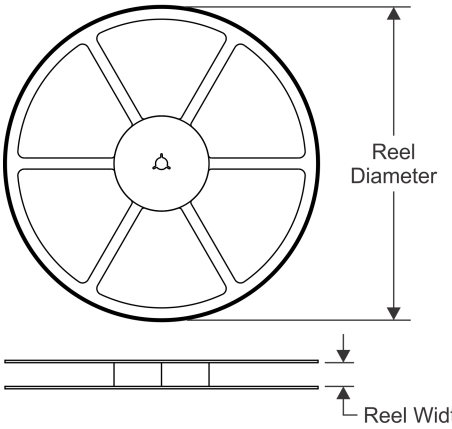
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

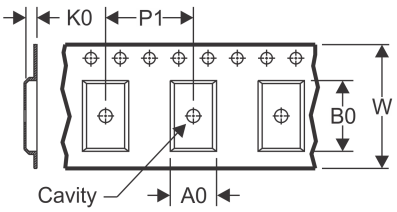
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

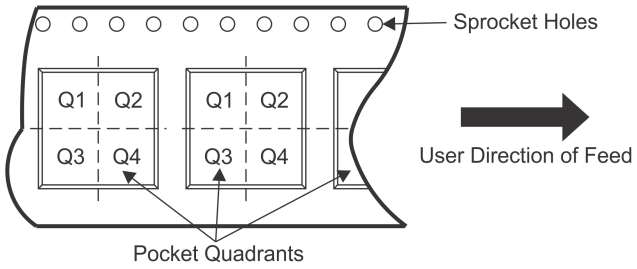


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

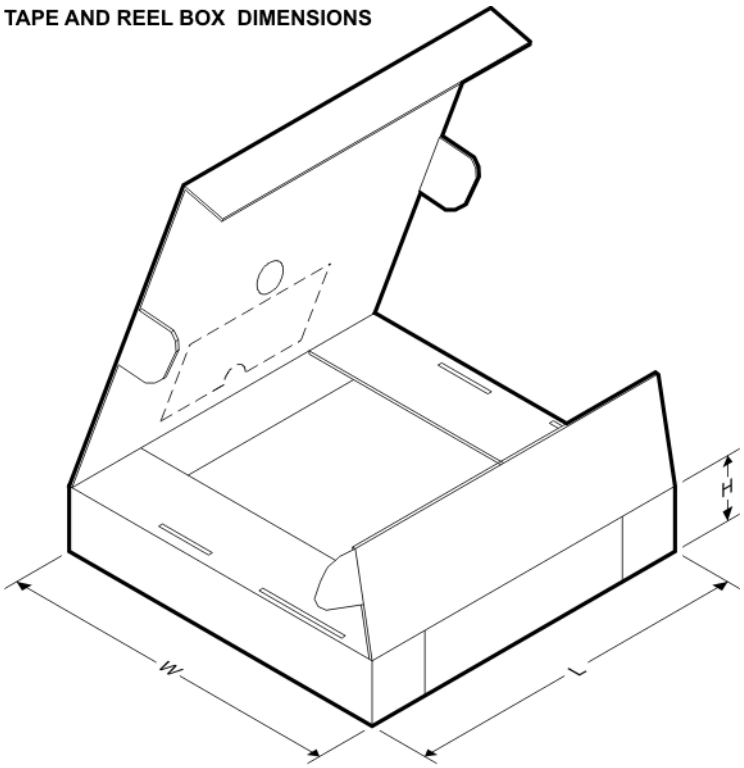
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5960DAR	TSSOP	DA	38	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

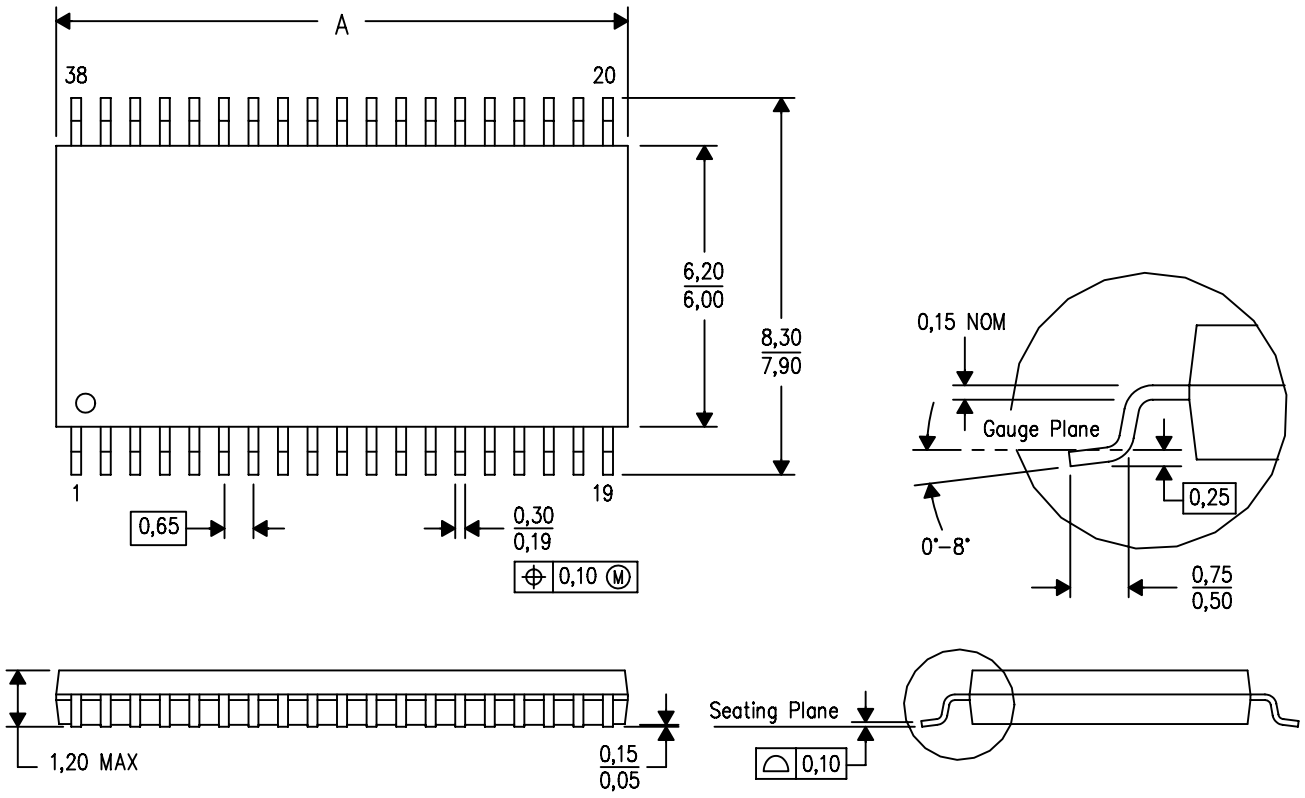


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5960DAR	TSSOP	DA	38	2000	350.0	350.0	43.0

DA (R–PDSO–G**) PLASTIC SMALL–OUTLINE PACKAGE

38 PIN SHOWN



DIM \ PINS **	30	32	38
A MAX	11,10	11,10	12,60
A MIN	10,90	10,90	12,40
△D MO–153 Variation	DB–1	DC	DD–1

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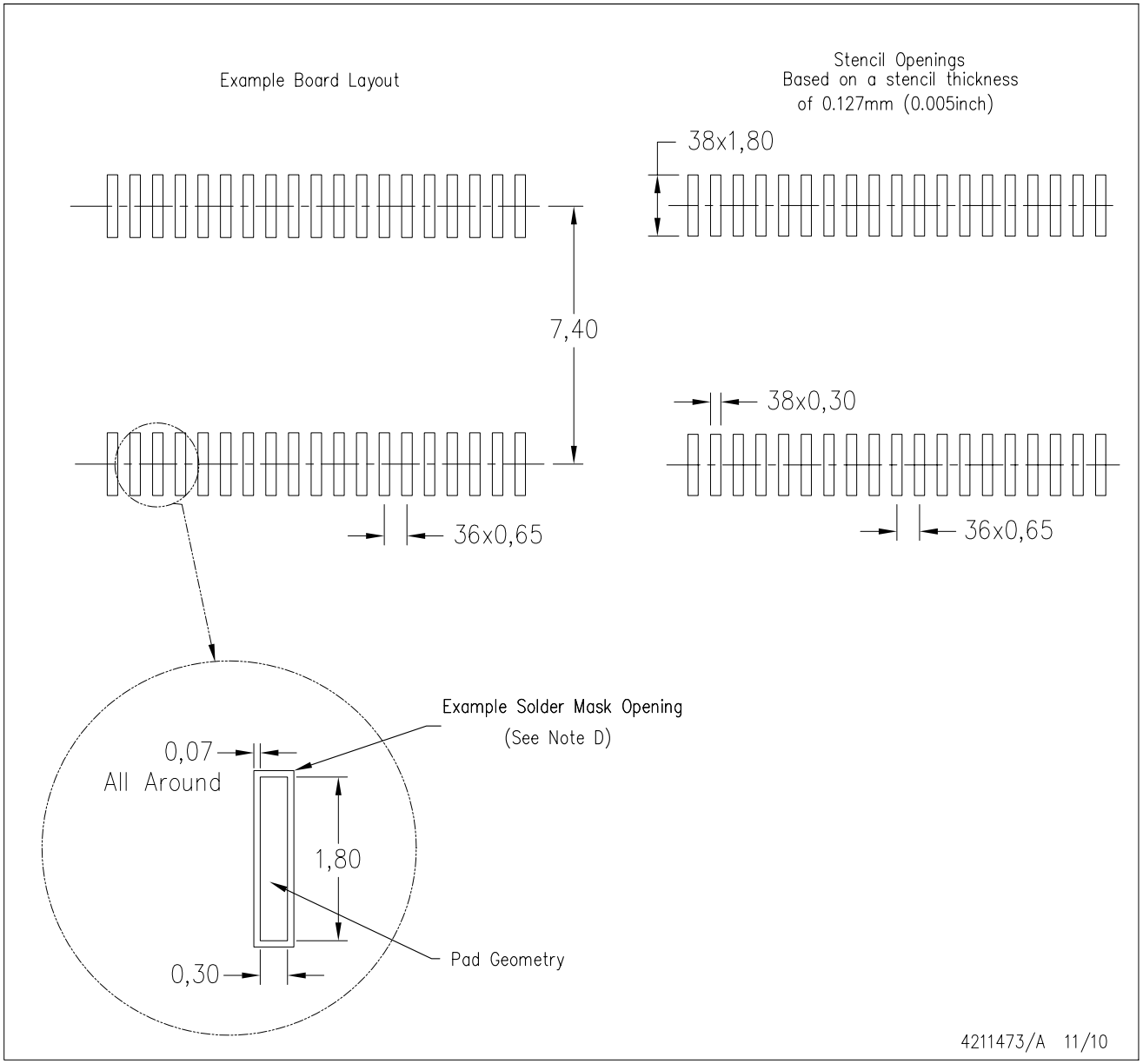
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
△D Falls within JEDEC MO–153, except 30 pin body length.

DA (R–PDSO–G38) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Contact the board fabrication site for recommended soldermask tolerances.

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