THE DATASHEET OF

TLC555QDR

TLC555-Q1 LinCMOS™ TIMER

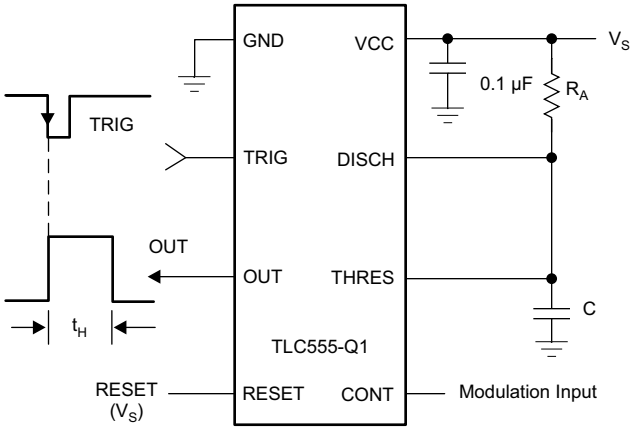
1 Features

- Qualified for Automotive Applications
- Very Low Power Consumption
  - 1 mW (Typical) at V_{DD} = 5 V
- Capable of Operation in Astable Mode
- CMOS Output Capable of Swinging Rail to Rail
- High-Output-Current Capability
  - Sink 100 mA (Typical)
  - Source 10 mA (Typical)
- Output Fully Compatible With CMOS, TTL, and MOS
- Low Supply Current Reduces Spikes During Output Transitions
- Single-Supply Operation From 2 V to 15 V
- Functionally Interchangeable With the NE555; Has Same Pinout

2 Applications

- Precision Timing
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation
- Pulse Position Modulation
- Linear Ramp Generators
- Automotive Lamp/LED Lighting
- Telematics

Pulse Width Modulator



3 Description

The TLC555-Q1 is a monolithic timing circuit fabricated using the TI LinCMOS™ process. The timer is fully compatible with CMOS, TTL, and MOS logic and operates at frequencies up to 2 MHz. Because of its high input impedance, this device uses smaller timing capacitors than those used by the NE555. As a result, more accurate time delays and oscillations are possible. Power consumption is low across the full range of power-supply voltage.

Like the NE555, the TLC555-Q1 has a trigger level equal to approximately one-third of the supply voltage and a threshold level equal to approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal (CONT).

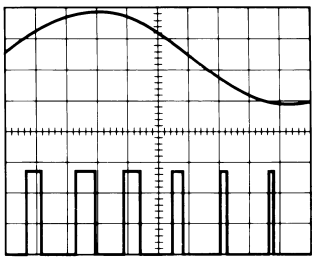
When the trigger input (TRIG) falling below the trigger level sets the flip-flop, and the output goes high. Having TRIG above the trigger level and the threshold input (THRES) above the threshold level resets the flip-flop, and the output is low. The reset input (RESET) can override all other inputs, and a possible use is to initiate a new timing cycle. RESET going low resets the flip-flop, and the output is low. Whenever the output is low, a low-impedance path exists between the discharge terminal (DISCH) and GND. Tie all unused inputs to an appropriate logic level to prevent false triggering.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC555-Q1	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Pulse Width Modulator Waveform:
Top Waveform - Modulation
Bottom Waveform - Output Voltage



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2012) to Revision B — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Original (October 2006) to Revision A — **Page**

- Changed next-to-last paragraph in Description and Ordering Information section ... 1
- In the 5-V and 15-V Electrical Characteristics tables, changed all "MAX" entries in the T_A column to "Full range" ... 5
- Deleted the last Electrical Characteristics table, which contained only redundant data ... 6

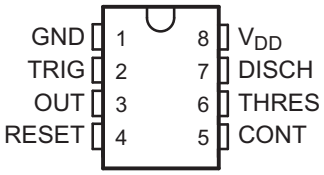
5 Description (continued)

The advantage of the TLC555-Q1 is that it exhibits greatly reduced supply-current spikes during output transitions. Although the CMOS output is capable of sinking over 100 mA and sourcing over 10 mA, the main reason the TLC555-Q1 is able to have low current spikes is due to its edge rates. This minimizes the need for the large decoupling capacitors required by the NE555.

The TLC555-Q1 is characterized for operation over the full automotive temperature range of –40°C to 125°C.

6 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CONT	5	I/O	Controls comparator thresholds, Outputs 2/3 VDD, allows bypass capacitor connection
DISCH	7	O	Open collector output to discharge timing capacitor
GND	1	—	Ground
OUT	3	O	High current timer output signal
RESET	4	I	Active low reset input forces output and discharge low
THRES	6	I	End of timing input. THRES > CONT sets output low and discharge low
TRIG	2	I	Start of timing input. TRIG < ½ CONT sets output high and discharge open
VDD	8	—	Input supply voltage, 2 V to 15 V

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{DD}	Supply voltage(2)			18	V
V_I	Input voltage	Any input	–0.3	V_{DD}	V
	Sink current, discharge or output			150	mA
I_O	Source current, output			15	mA
	Continuous total power dissipation		See *Dissipation Ratings*		
T_A	Operating free-air temperature		–40	125	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network GND.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±1000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 4, 5, and 8)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{DD}	Supply voltage	2	15	V
T_A	Operating free-air temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TLC555-Q1 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	113.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: V_{DD} = 5 V

V_{DD} = 5 V, at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	MIN	TYP	MAX	UNIT
V_{IT}	Threshold voltage		25°C	2.8	3.3	3.8	V
			Full range	2.7		3.9	
I_{IT}	Threshold current		25°C		10		pA
			Full range		5000		
$V_{I(TRIG)}$	Trigger voltage		25°C	1.36	1.66	1.96	V
			Full range	1.26		2.06	
$I_{I(TRIG)}$	Trigger current		25°C		10		pA
			Full range		5000		
$V_{I(RESET)}$	Reset voltage		25°C	0.4	1.1	1.5	V
			Full range	0.3		1.8	
$I_{I(RESET)}$	Reset current		25°C		10		pA
			Full range		5000		
	Control voltage (open-circuit) as a percentage of supply voltage		Full range		66.7%		
	Discharge-switch on-state voltage	I_{OL} = 10 mA	25°C		0.14	0.5	V
			Full range			0.6	
	Discharge-switch off-state current		25°C		0.1		nA
			Full range		120		
V_{OH}	High-level output voltage	I_{OH} = –1 mA	25°C	4.1	4.8		V
			Full range	4.1			
V_{OL}	Low-level output voltage	I_{OL} = 8 mA	25°C		0.21	0.4	V
			Full range			0.6	
		I_{OL} = 5 mA	25°C		0.13	0.3	
			Full range			0.45	
		I_{OL} = 3.2 mA	25°C		0.08	0.3	
			Full range			0.4	
I_{DD}	Supply current (2)		25°C		170	350	µA
			Full range			700	

(1) Full-range T_A is –40°C to 125°C.
(2) These values apply for the expected operating configurations in which THRES is connected directly to DISCH or TRIG.

7.6 Electrical Characteristics: V_{DD} = 15 V

V_{DD} = 15 V, at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	MIN	TYP	MAX	UNIT
V_{IT}	Threshold voltage		25°C	9.45	10	10.55	V
			Full range	9.35		10.65	
I_{IT}	Threshold current		25°C		10		pA
			Full range		5000		
$V_{I(TRIG)}$	Trigger voltage		25°C	4.65	5	5.35	V
			Full range	4.55		5.45	
$I_{I(TRIG)}$	Trigger current		25°C		10		pA
			Full range		5000		
$V_{I(RESET)}$	Reset voltage		25°C	0.4	1.1	1.5	V
			Full range	0.3		1.8	
$I_{I(RESET)}$	Reset current		25°C		10		pA
			Full range		5000		
	Control voltage (open-circuit) as a percentage of supply voltage		Full range		66.7%		
	Discharge-switch on-state voltage	I_{OL} = 100 mA	25°C		0.77	1.7	V
			Full range			1.8	
	Discharge switch off-state current		25°C		0.1		nA
			Full range		120		
V_{OH}	High-level output voltage	I_{OH} = –10 mA	25°C	12.5	14.2		V
			Full range	12.5			
		I_{OH} = –5 mA	25°C	13.5	14.6		
			Full range	13.5			
		I_{OH} = –1 mA	25°C	14.2	14.9		
			Full range	14.2			
V_{OL}	Low-level output voltage	I_{OL} = 100 mA	25°C		1.28	3.2	V
			Full range			3.8	
		I_{OL} = 50 mA	25°C		0.63	1	
			Full range			1.5	
		I_{OL} = 10 mA	25°C		0.12	0.3	
			Full range			0.45	
I_{DD}	Supply current(2)		25°C		360	600	µA
			Full range			1000	

(1) Full-range T_A is –40°C to 125°C.
(2) These values apply for the expected operating configurations in which THRES is connected directly to DISCH or TRIG.

7.7 Operating Characteristics

V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Initial error of timing interval(1)	V_{DD} = 5 V to 15 V, C_T = 0.1 µF, R_A = R_B = 1 kΩ to 100 kΩ(2)		1%	3%	
	Supply voltage sensitivity of timing interval	V_{DD} = 5 V to 15 V, C_T = 0.1 µF, R_A = R_B = 1 kΩ to 100 kΩ(2)		0.1	0.5	%/V
t_r	Output pulse rise time	R_L = 10 MΩ, C_L = 10 pF		20	75	ns
t_f	Output pulse fall time	R_L = 10 MΩ, C_L = 10 pF		15	60	ns
f_{max}	Maximum frequency in astable mode	R_A = 470 Ω, C_T = 200 pF, R_B = 200 Ω(2)	1.2	2.1		MHz

(1) Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.
(2) R_A, R_B, and C_T are as defined in Figure 1.

7.8 Dissipation Ratings

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	145 mW

7.9 Typical Characteristics

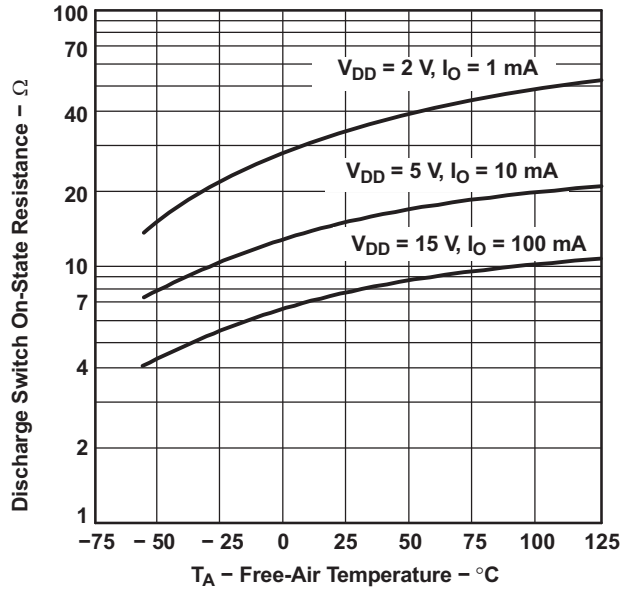
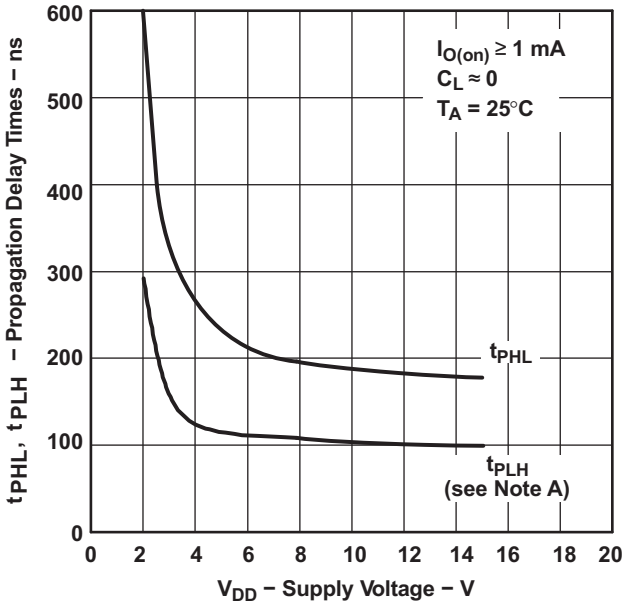


Figure 1. Discharge Switch ON-State Resistance vs Free-Air Temperature



The effects of the load resistance on these values must be taken into account separately.

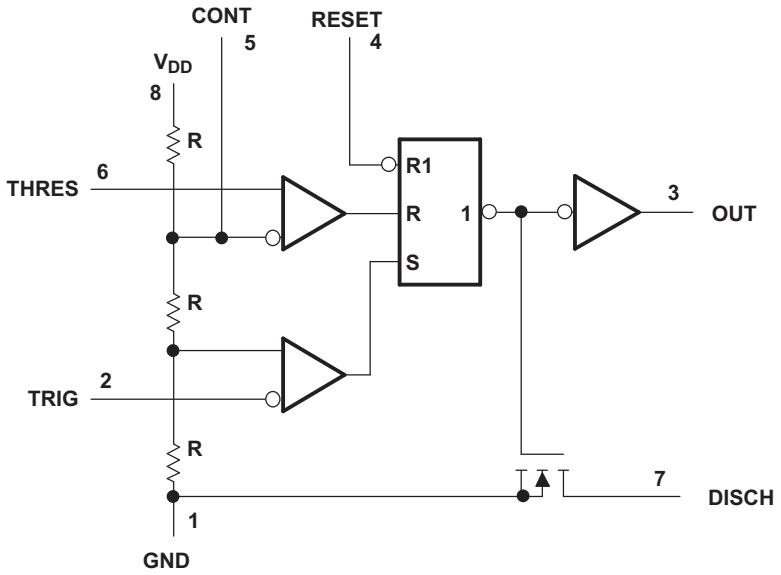
Figure 2. Propagation Delay Times to Discharge Output from Trigger and Threshold Shorted Together vs Supply Voltage

8 Detailed Description

8.1 Overview

The TLC555-Q1 timer is used for general purpose timing applications from 476 ns to hours or from < 1 mHz to 2.1 MHz.

8.2 Functional Block Diagram



RESET can override TRIG, which can override THRES.

8.3 Feature Description

8.3.1 Mono-stable Operation

For mono-stable operation, any of these timers can be connected as shown in Figure 3. If the output is low, application of a negative-going pulse to the trigger (TRIG) sets the flip-flop ($\overline{Q}$ goes low), drives the output high, and turns off Q1. Capacitor C then is charged through R_A until the voltage across the capacitor reaches the threshold voltage of the threshold (THRES) input. If TRIG has returned to a high level, the output of the threshold comparator resets the flip-flop ($\overline{Q}$ goes high), drives the output low, and discharges C through Q1.

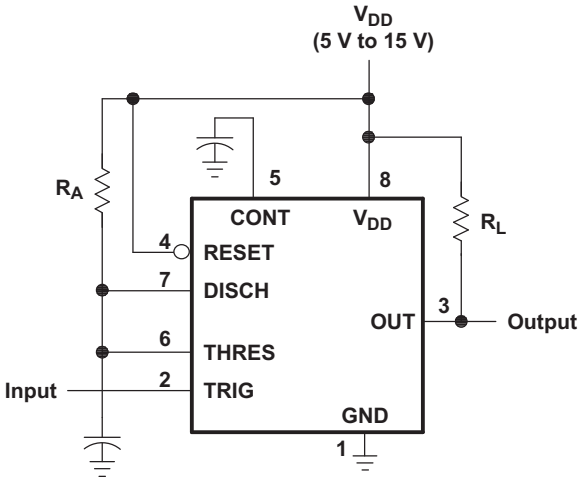


Figure 3. Circuit for Monostable Operation

Feature Description (continued)

Monostable operation is initiated when TRIG voltage falls below the trigger threshold. Once initiated, the sequence ends only if TRIG is high for at least 10 µs before the end of the timing interval. When the trigger is grounded, the comparator storage time can be as long as 10 µs, which limits the minimum monostable pulse width to 10 µs. Because of the threshold level and saturation voltage of Q1, the output pulse duration is approximately $t_w = 1.1R_AC$. Figure 4 is a plot of the time constant for various values of R_A and C. The threshold levels and charge rates both are directly proportional to the supply voltage, V_{CC}. The timing interval is, therefore, independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges C and reinitiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is not used, it should be connected to V_{CC}.

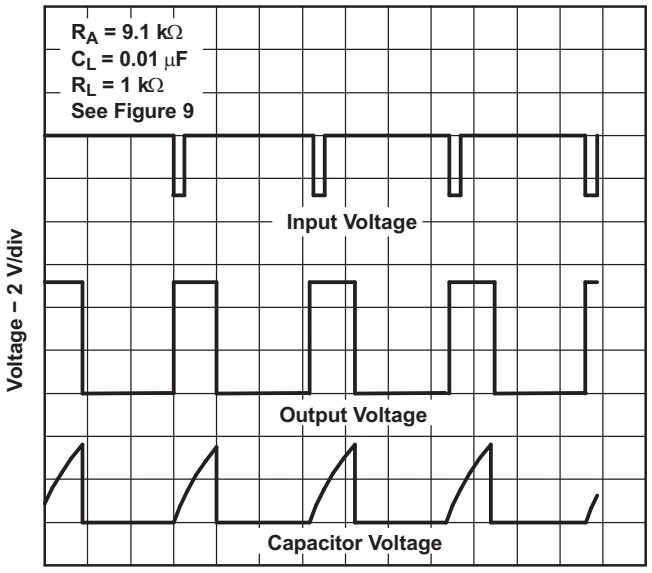


Figure 4. Typical Monostable Waveforms

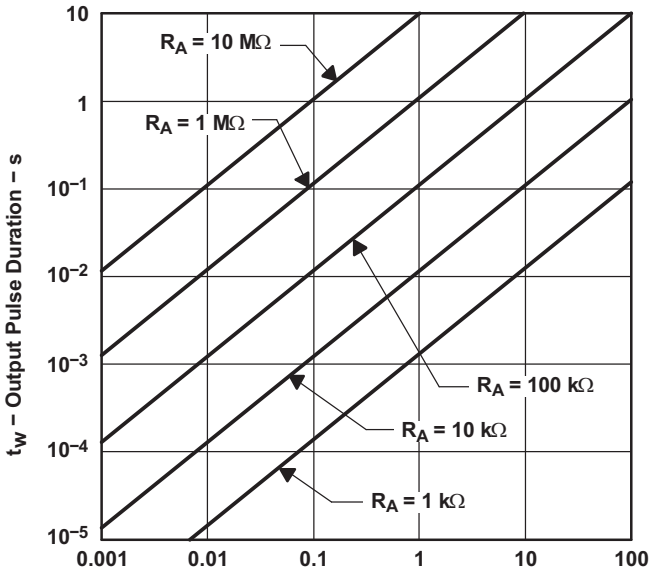


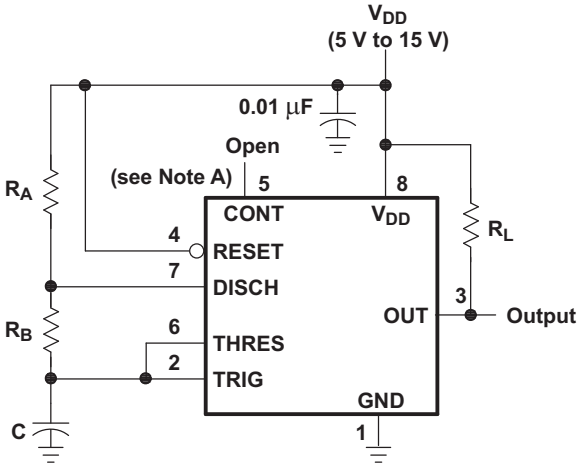
Figure 5. Output Pulse Duration vs Capacitance

8.3.2 A-stable Operation

As shown in Figure 6, adding a second resistor, R_B, to the circuit of and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multi-vibrator. The capacitor C charges through R_A and R_B and then discharges through R_B only. Therefore, the duty cycle is controlled by the values of R_A and R_B.

This astable connection results in capacitor C charging and discharging between the threshold-voltage level (≈ 0.67 × V_{CC}) and the trigger-voltage level (≈ 0.33 × V_{CC}). As in the mono-stable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage.

Feature Description (continued)



NOTE A: Decoupling CONT voltage to ground with a capacitor can improve operation. This should be evaluated for individual applications.

Figure 6. Circuit for A-stable Operation

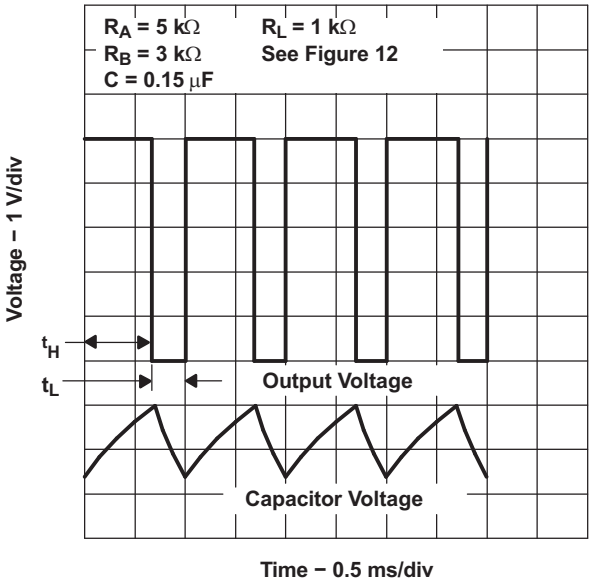


Figure 7. Typical A-stable Waveforms

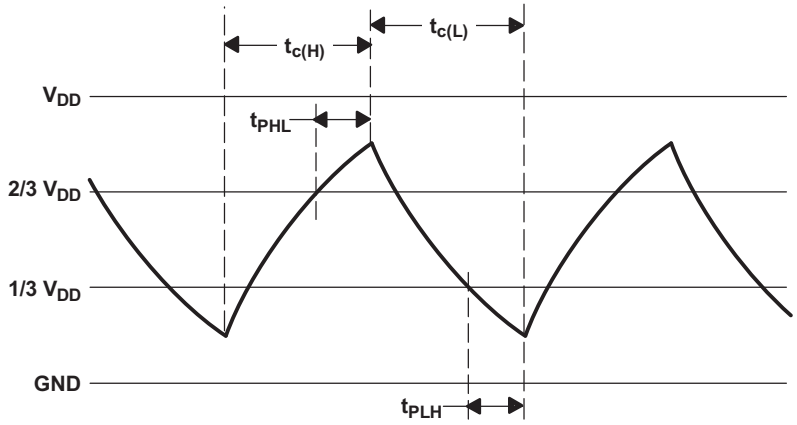


Figure 8. Trigger and Threshold Voltage Waveform

Figure 8 shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L can be calculated as follows:

$$t_H = 0.693(R_A + R_B)C \quad (1)$$

$$t_L = 0.693(R_B)C \quad (2)$$

Other useful relationships are shown below:

$$\text{period} = t_H + t_L = 0.693(R_A + 2R_B)C \quad (3)$$

$$\text{frequency} \approx \frac{1.44}{(R_A + 2R_B)C} \quad (4)$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B} \quad (5)$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B} \quad (6)$$

$$\text{Low-to-high ratio} = \frac{t_L}{t_H} = \frac{R_B}{R_A + R_B} \quad (7)$$

Feature Description (continued)

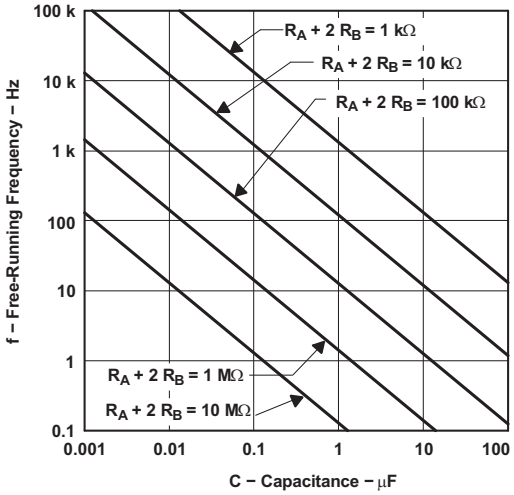


Figure 9. Free-Running Frequency

8.3.3 Frequency Divider

By adjusting the length of the timing cycle, the basic circuit of Figure 11 can be made to operate as a frequency divider. Figure 10 shows a divide-by-three circuit that makes use of the fact that re-triggering cannot occur during the timing cycle.

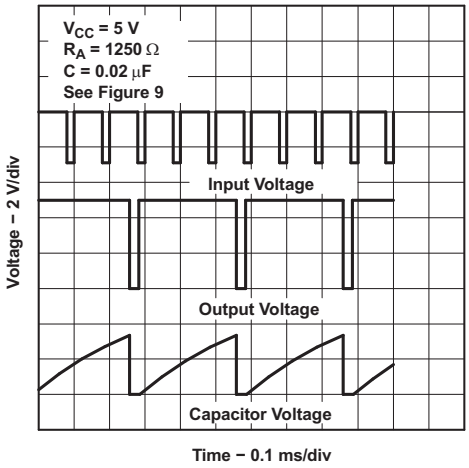


Figure 10. Divide-by-Three Circuit Waveforms

8.4 Device Functional Modes

Table 1 shows the device functional modes.

Table 1. Function Table

RESET	TRIGGER VOLTAGE(1)	THRESHOLD VOLTAGE(1)	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	<1/3 V_{CC}	Irrelevant	High	Off
High	>1/3 V_{CC}	>2/3 V_{CC}	Low	On
High	>1/3 V_{CC}	<2/3 V_{CC}	As previously established	

(1) Voltage levels shown are nominal.

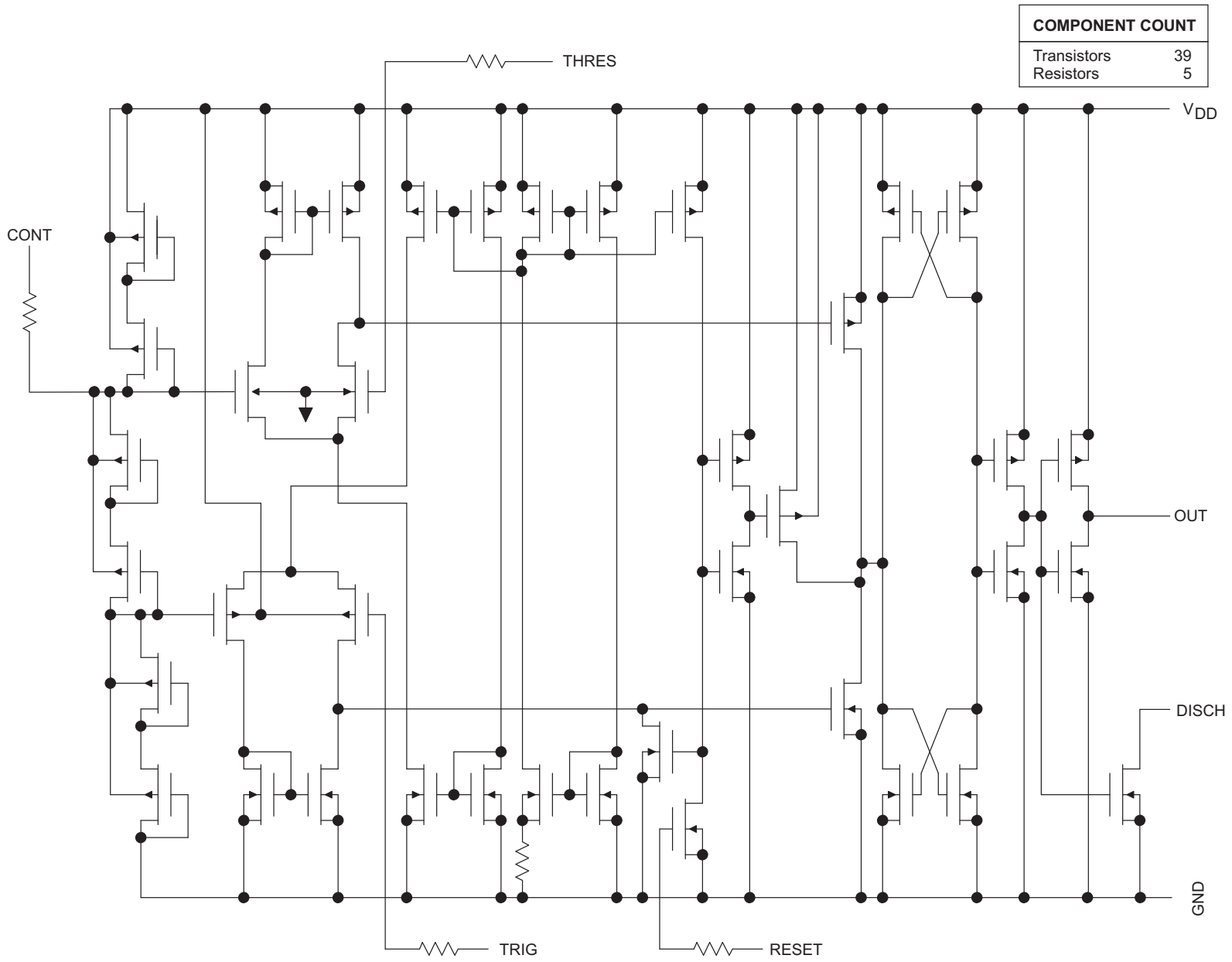


Figure 11. Equivalent Schematic

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLC555-Q1 timer device uses resistor and capacitor charging delay to provide a programmable time delay or operating frequency. The following section presents a simplified discussion of the design process.

9.2 Typical Applications

9.2.1 Missing-Pulse Detector

The circuit shown in Figure 12 can be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is re-triggered continuously by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as shown in Figure 13.

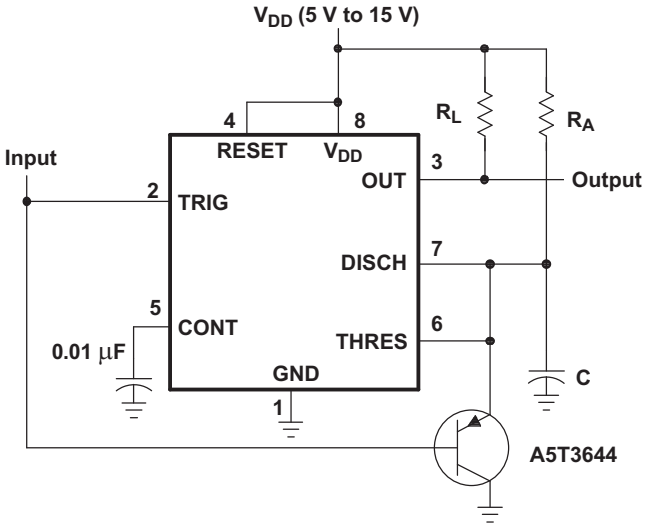


Figure 12. Circuit for Missing-Pulse Detector

9.2.1.1 Design Requirements

Input fault (missing pulses) must be input high. Input stuck low will not be detected because timing capacitor (C) remains discharged.

9.2.1.2 Detailed Design Procedure

Choose R_A and C so that $R_A \times C >$ [maximum normal input high time]. R_L improves V_{OH}, but it is not required for TTL compatibility.

Typical Applications (continued)

9.2.1.3 Application Curve

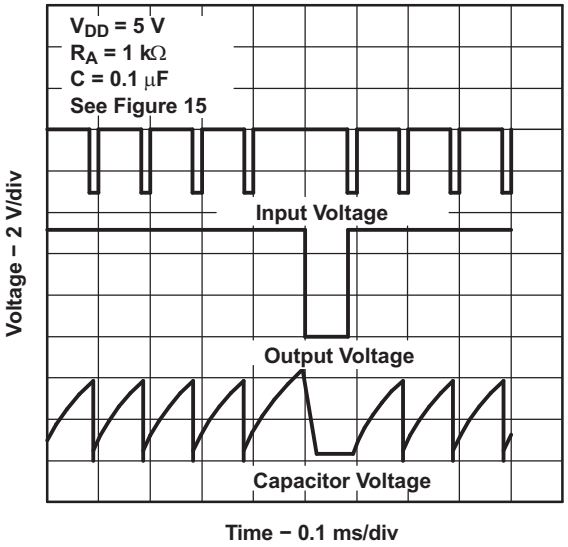
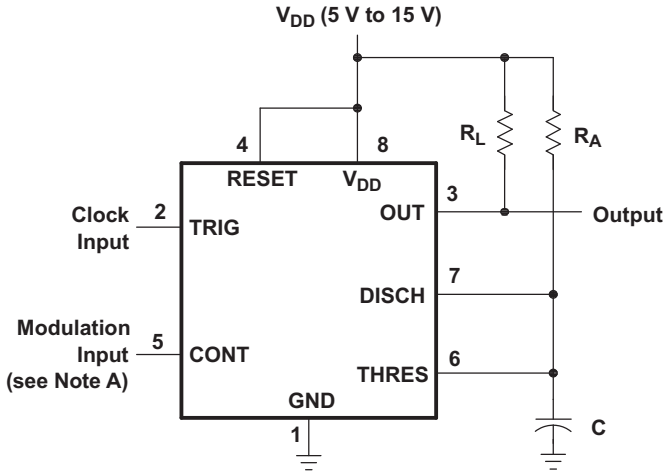


Figure 13. Completed Timing Waveforms for Missing-Pulse Detector

9.2.2 Pulse-Width Modulation

The operation of the timer can be modified by modulating the internal threshold and trigger voltages, which is accomplished by applying an external voltage (or current) to CONT. Figure 14 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. Figure 15 shows the resulting output pulse-width modulation. While a sine-wave modulation signal is shown, any wave shape could be used.



NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 14. Circuit for Pulse-Width Modulation

Typical Applications (continued)

9.2.2.1 Design Requirements

Clock input must have V_{OL} and V_{OH} levels that are less than and greater than 1/3 VDD. Modulation input can vary from ground to VDD. The application must be tolerant of a nonlinear transfer function; the relationship between modulation input and pulse width is not linear because the capacitor charge is based RC on an negative exponential curve.

9.2.2.2 Detailed Design Procedure

Choose R_A and C so that $R_A \times C = 1/4$ [clock input period]. R_L improves V_{OH}, but it is not required for TTL compatibility.

9.2.2.3 Application Curve

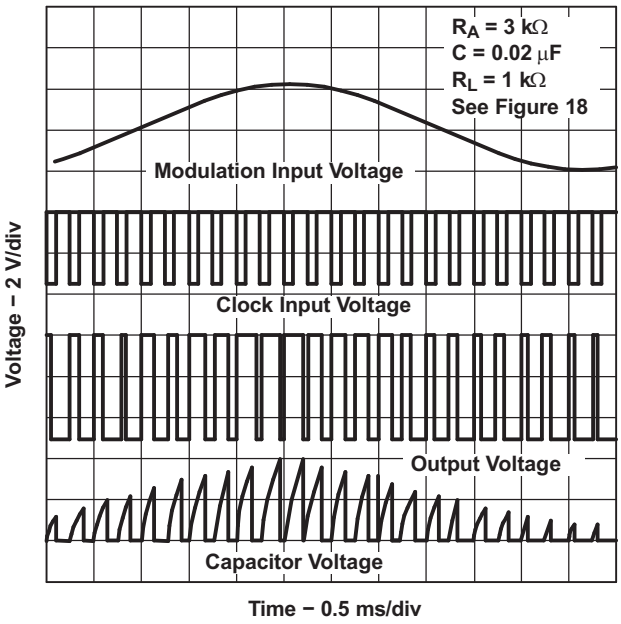
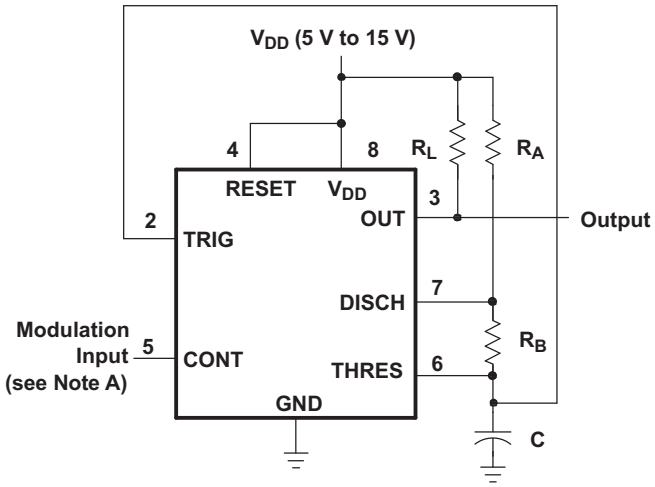


Figure 15. Pulse-Width-Modulation Waveforms

9.2.3 Pulse-Position Modulation

As shown in Figure 16, any of these timers can be used as a pulse-position modulator. This application modulates the threshold voltage and, thereby, the time delay, of a free-running oscillator. Figure 17 shows a triangular-wave modulation signal for such a circuit; however, any wave shape could be used.

Typical Applications (continued)



NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 16. Circuit for Pulse-Position Modulation

9.2.3.1 Design Requirements

Both DC and AC coupled modulation input will change the upper and lower voltage thresholds for the timing capacitor. Both frequency and duty cycle will vary with the modulation voltage.

9.2.3.2 Detailed Design Procedure

The nominal output frequency and duty cycle can be determined using formulas in A-stable Operation section. R_L improves V_{OH}, but it is not required for TTL compatibility.

9.2.3.3 Application Curve

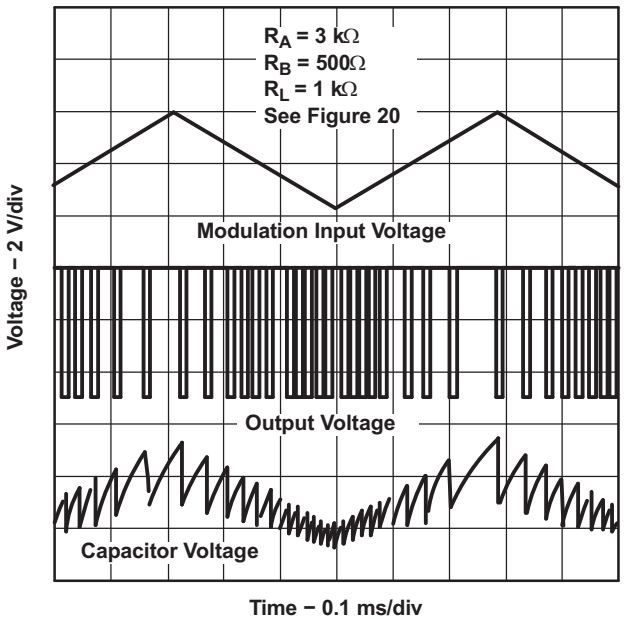
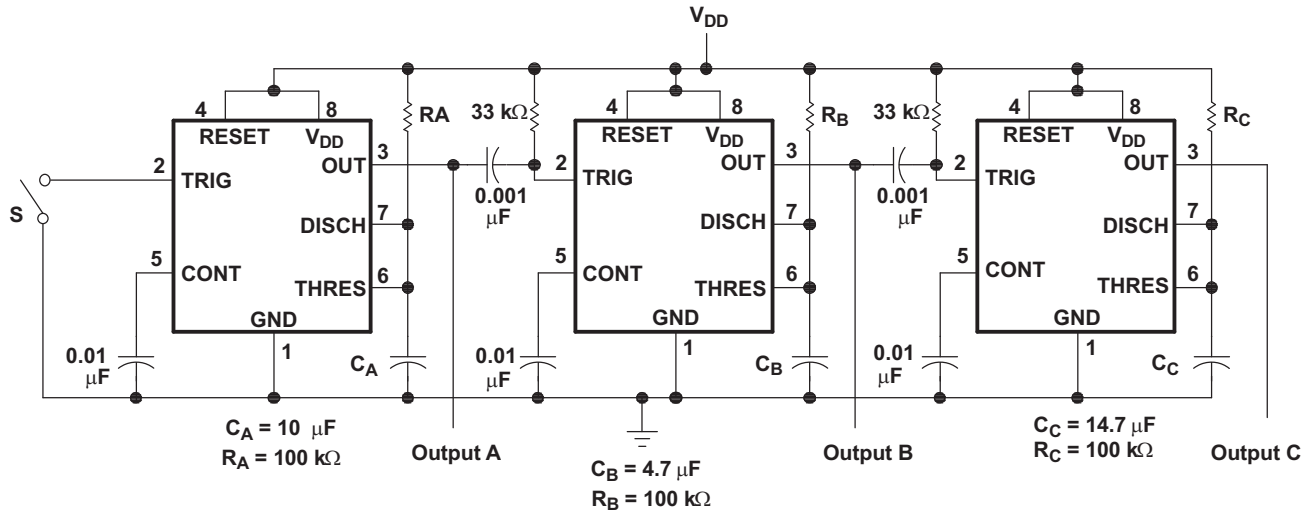


Figure 17. Pulse-Position-Modulation Waveforms

Typical Applications (continued)

9.2.4 Sequential Timer

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications, such as test equipment, require activation of test signals in sequence. These timing circuits can be connected to provide such sequential control. The timers can be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. Figure 18 shows a sequencer circuit with possible applications in many systems, and Figure 19 shows the output waveforms.



NOTE A: S closes momentarily at t = 0.

Figure 18. Sequential Timer Circuit

9.2.4.1 Design Requirements

The sequential timer application chains together multiple mono-stable timers. The joining components are the 33-kΩ resistors and 0.001-µF capacitors. The output high to low edge passes a 10-µs start pulse to the next monostable.

9.2.4.2 Detailed Design Procedure

The timing resistors and capacitors can be chosen using this formula. $t_w = 1.1 \times R \times C$.

Typical Applications (continued)

9.2.4.3 Application Curve

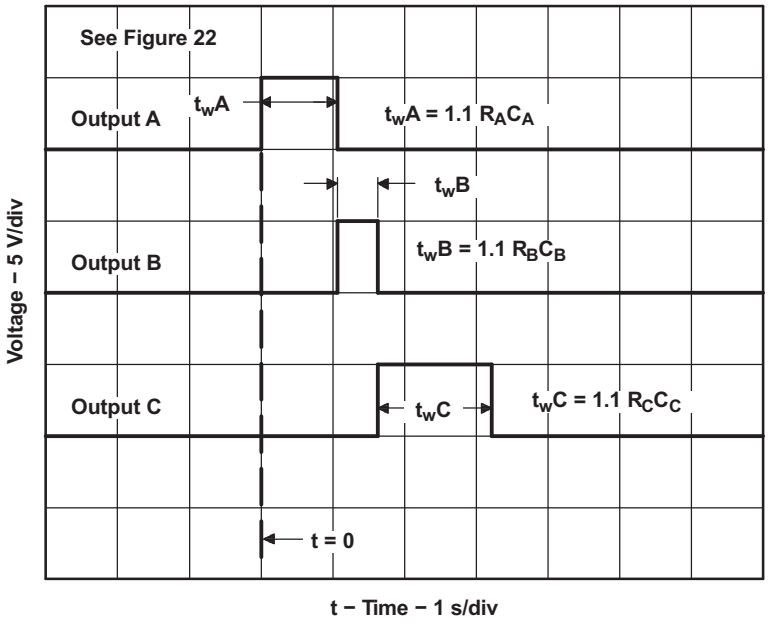


Figure 19. Sequential Timer Waveforms

10 Power Supply Recommendations

The TLC555-Q1 requires a voltage supply within 2 V to 15 V. Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1 µF in parallel with 1-µF electrolytic. Place the bypass capacitors as close as possible to the TLC555-Q1 and minimize the trace length.

11 Layout

11.1 Layout Guidelines

Standard PCB rules apply to routing the TLC555-Q1. The 0.1 µF in parallel with a 1-µF electrolytic capacitor should be as close as possible to the TLC555-Q1. The capacitor used for the time delay should also be placed as close to the discharge pin. A ground plane on the bottom layer can be used to provide better noise immunity and signal integrity.

11.2 Layout Example

Figure 20 is the basic layout for various applications.

- C1 – based on time delay calculations
- C2 – 0.01-µF bypass capacitor for control voltage pin
- C3 – 0.1-µF bypass ceramic capacitor
- C4 – 1-µF electrolytic bypass capacitor
- R1 – based on time delay calculations

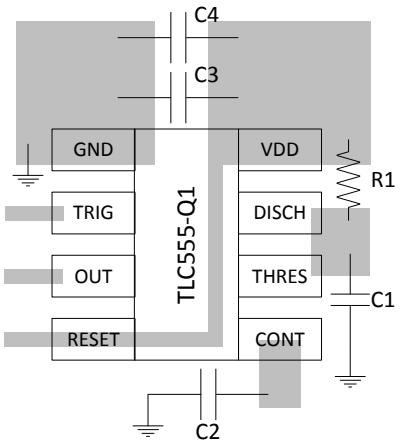


Figure 20. Recommended Layout

12 Device and Documentation Support

12.1 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

LinCMOS, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC555QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL555Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

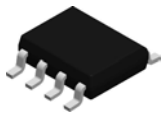
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLC555-Q1 :

- Catalog: TLC555
- Military: TLC555M

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

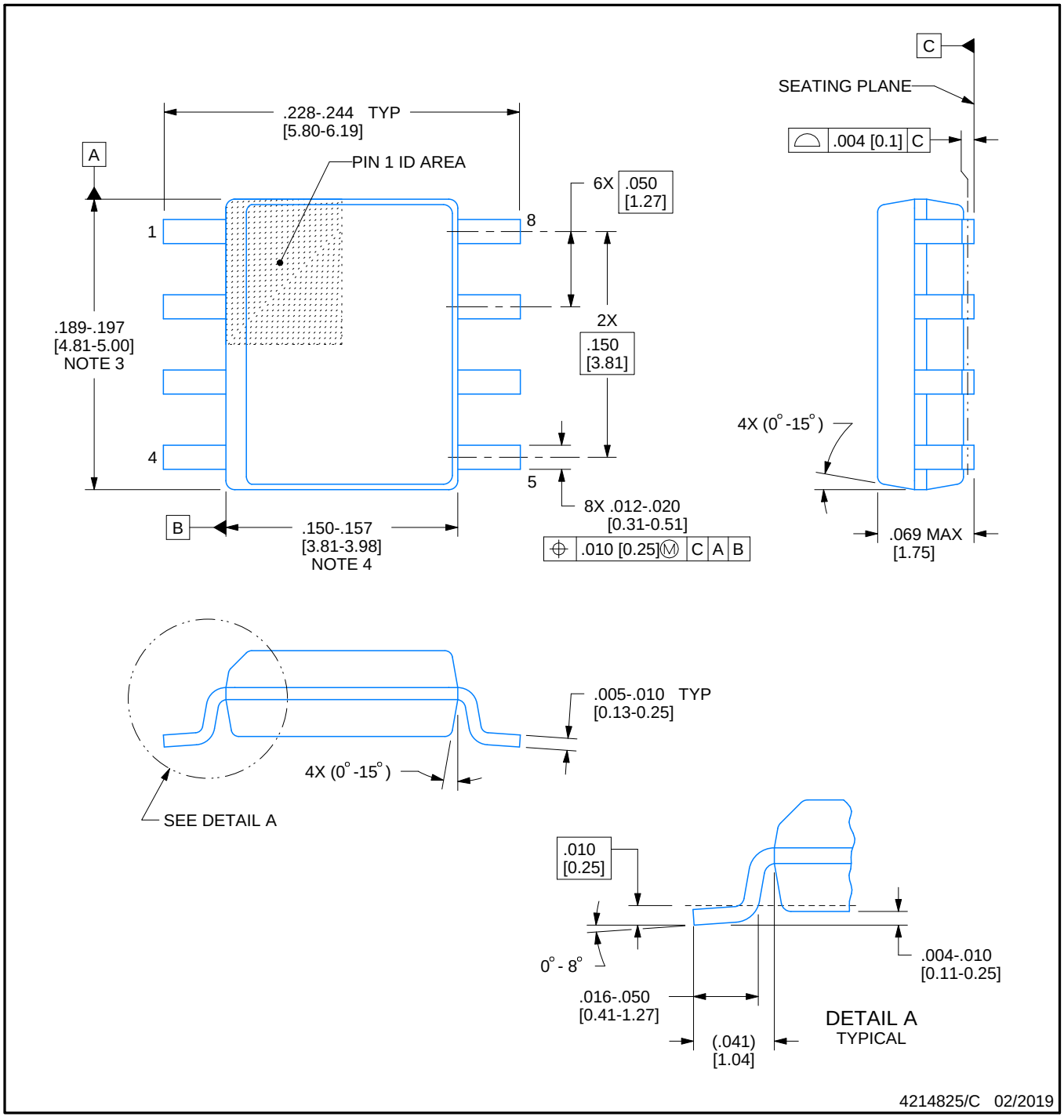


PACKAGE OUTLINE

D0008A

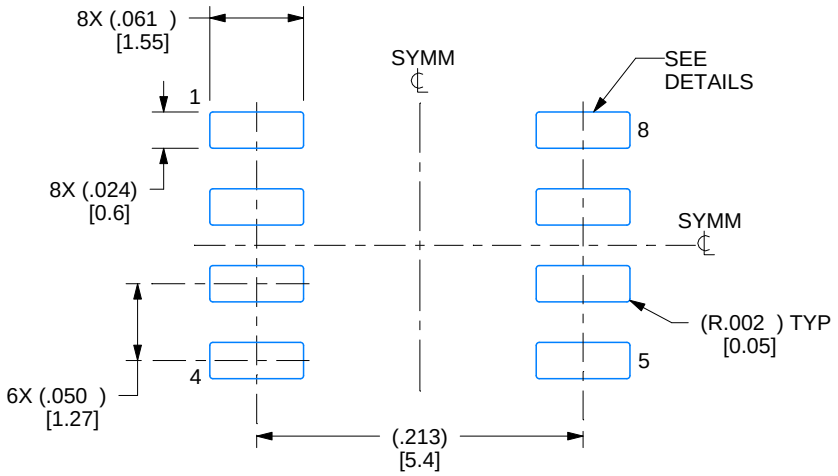
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

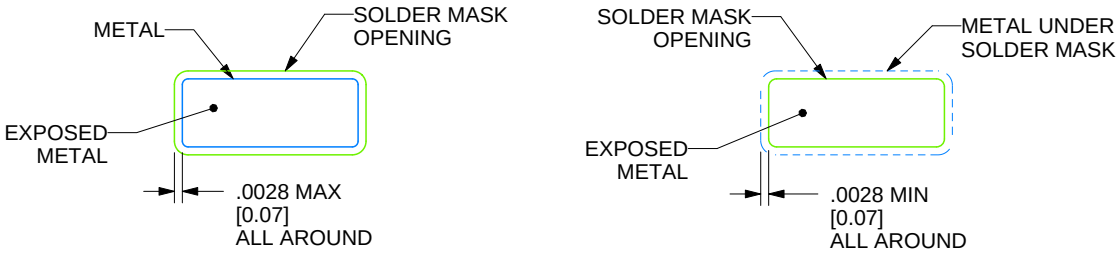


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

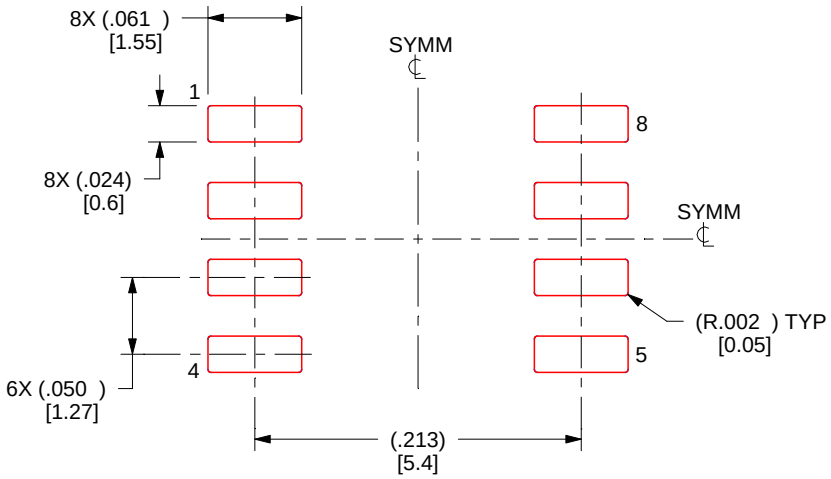
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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