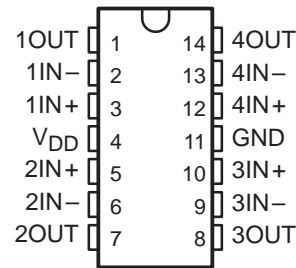


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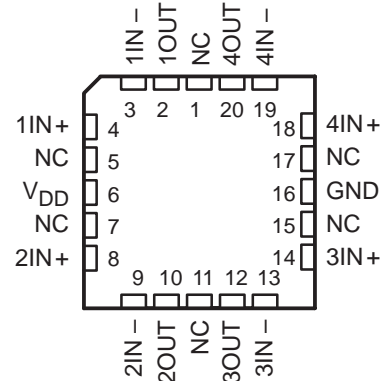
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- **Trimmed Offset Voltage:**
TLC27L9 . . . 900 μV Max at 25°C,
 $V_{\text{DD}} = 5 \text{ V}$
- **Input Offset Voltage Drift . . . Typically**
0.1 $\mu\text{V}/\text{Month}$, Including the First 30 Days
- **Wide Range of Supply Voltages Over**
Specified Temperature Range:
0°C to 70°C . . . 3 V to 16 V
–40°C to 85°C . . . 4 V to 16 V
–55°C to 125°C . . . 4 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range**
Extends Below the Negative Rail (C-Suffix,
I-Suffix Types)
- **Ultra-Low Power . . . Typically 195 μW**
at 25°C, $V_{\text{DD}} = 5 \text{ V}$
- **Output Voltage Range includes Negative**
Rail
- **High Input Impedance . . . $10^{12} \Omega$ Typ**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also**
Available in Tape and Reel
- **Designed-In Latch-Up Immunity**

**D, J, N, OR PW PACKAGE
(TOP VIEW)**



**FK PACKAGE
(TOP VIEW)**



NC – No internal connection

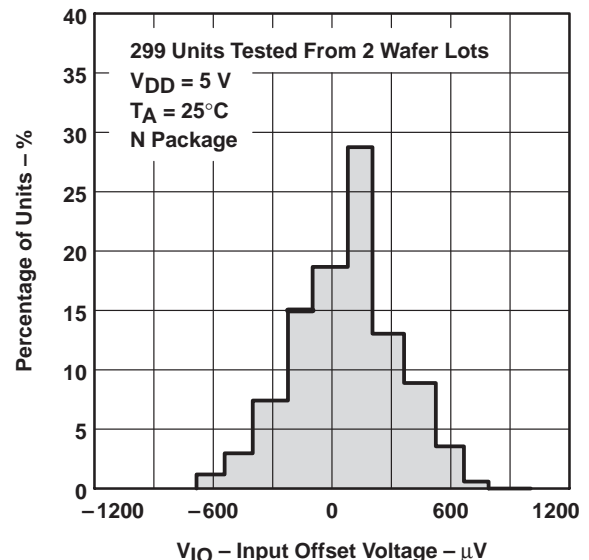
description

The TLC27L4 and TLC27L9 quad operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, extremely low power, and high gain.

These devices use Texas instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and low-power consumption make these cost-effective devices ideal for high-gain, low-frequency, low-power applications. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27L4 (10 mV) to the high-precision TLC27L9 (900 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

**DISTRIBUTION OF TLC27L9
INPUT OFFSET VOLTAGE**



LinCMOS is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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description (continued)

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC27L4 and TLC27L9. The devices also exhibit low voltage single-supply operation and ultra-low power consumption, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip-carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up.

The TLC27L4 and TLC27L9 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices, as exposure to ESD may result in the degradation of the device parametric performance.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation from –55°C to 125°C.

AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES					CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP (PW)	
0°C to 70°C	900 μV	TLC27L9CD	—	—	TLC27L9CN	—	—
	2 mV	TLC27L4BCD	—	—	TLC27L4BCN	—	—
	5 mV	TLC27L4ACD	—	—	TLC27L4ACN	—	—
	10 mV	TLC27L4CD	—	—	TLC27L4CN	TLC27L4CPW	TLC27L4Y
–40°C to 85°C	900 μV	TLC27L9ID	—	—	TLC27L9IN	—	—
	2 mV	TLC27L4BID	—	—	TLC27L4BIN	—	—
	5 mV	TLC27L4AID	—	—	TLC27L4AIN	—	—
	10 mV	TLC27L4ID	—	—	TLC27L4IN	—	—
–55°C to 125°C	900 μV	TLC27L9MD	TLC27L9MFK	TLC27L9MJ	TLC27L9MN	—	—
	10 mV	TLC27L4MD	TLC27L4MFK	TLC27L4MJ	TLC27L4MN	—	—

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC27L9CDR).

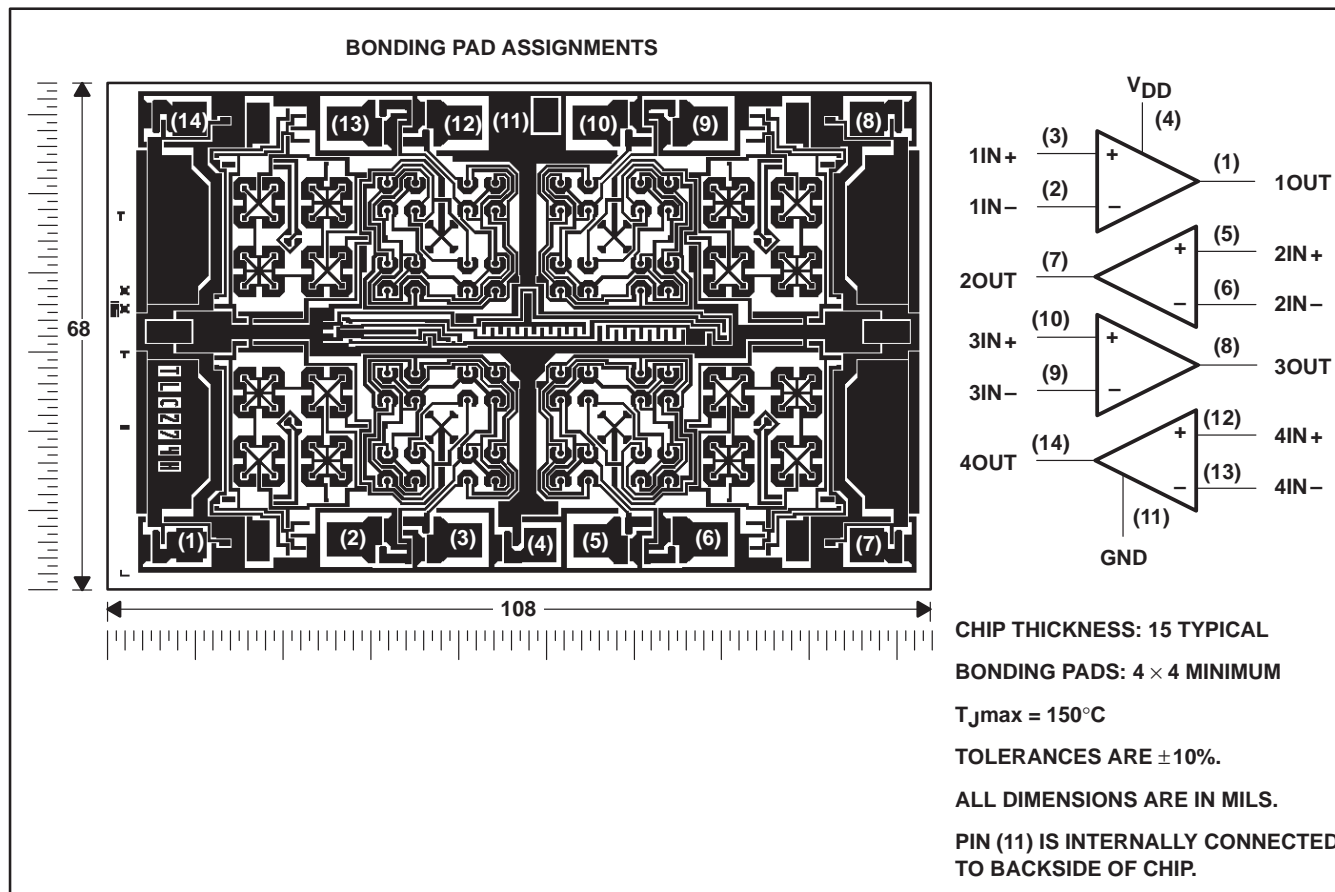


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TLC27L4Y chip information

These chips, when properly assembled, display characteristics similar to the TLC27L4C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A †	TLC27L4C TLC27L4AC TLC27L4BC TLC27L9C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L4C	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$,	$V_{IC} = 0$, $R_L = 1\text{ M}\Omega$	25°C	1.1	10	mV
					Full range		12	
		TLC27L4AC	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$,	$V_{IC} = 0$, $R_L = 1\text{ M}\Omega$	25°C	0.9	5	
					Full range		6.5	
	TLC27L4BC	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$,	$V_{IC} = 0$, $R_L = 1\text{ M}\Omega$	25°C	240	2000	μV	
				Full range		3000		
	TLC27L9C	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$,	$V_{IC} = 0$, $R_L = 1\text{ M}\Omega$	25°C	200	900		
				Full range		1500		
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C	1.1		$\mu\text{V}/^\circ\text{C}$	
I_{IO}	Input offset current (see Note 4)	$V_O = 2.5\text{ V}$,	$V_{IC} = 2.5\text{ V}$	25°C	0.1		pA	
				70°C	7	300		
I_{IB}	Input bias current (see Note 4)	$V_O = 2.5\text{ V}$,	$V_{IC} = 2.5\text{ V}$	25°C	0.6		pA	
				70°C	40	600		
V_{ICR}	Common mode input voltage range (see Note 5)			25°C	-0.2 to 4	-0.3 to 4.2	V	
				Full range	-0.2 to 3.5		V	
V_{OH}	High-level output voltage	$V_{ID} = 100\text{ mV}$,	$R_L = 1\text{ M}\Omega$	25°C	3.2	4.1	V	
				0°C	3	4.1		
				70°C	3	4.2		
V_{OL}	Low-level output voltage	$V_{ID} = -100\text{ mV}$,	$I_{OL} = 0$	25°C	0	50	mV	
				0°C	0	50		
				70°C	0	50		
A_{VD}	Large-signal differential voltage amplification	$V_O = 2.5\text{ V to }2\text{ V}$,	$R_L = 1\text{ M}\Omega$	25°C	50	520	V/mV	
				0°C	50	680		
				70°C	50	380		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$		25°C	65	94	dB	
				0°C	60	95		
				70°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 5\text{ V to }10\text{ V}$,	$V_O = 1.4\text{ V}$	25°C	70	97	dB	
				0°C	60	97		
				70°C	60	98		
I_{DD}	Supply current (four amplifiers)	$V_O = 2.5\text{ V}$, No load	$V_{IC} = 2.5\text{ V}$,	25°C	40	68	μA	
				0°C	48	84		
				70°C	31	56		

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.



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electrical characteristics at specified free-air temperature, $V_{DD} = 10\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A †	TLC27L4C TLC27L4AC TLC27L4BC TLC27L9C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L4C	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$,	$V_{IC} = 0$, $R_L = 1\text{ M}\Omega$	25°C	1.1	10	mV
					Full range		12	
		TLC27L4AC	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$,	$V_{IC} = 0$, $R_L = 1\text{ M}\Omega$	25°C	0.9	5	mV
					Full range		6.5	
		TLC27L4BC	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$,	$V_{IC} = 0$, $R_L = 1\text{ M}\Omega$	25°C	260	2000	μV
					Full range		3000	
		TLC27L9C	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$,	$V_{IC} = 0$, $R_L = 1\text{ M}\Omega$	25°C	210	1200	μV
					Full range		1900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C	1		$\mu\text{V}/^\circ\text{C}$	
I_{IO}	Input offset current (see Note 4)	$V_O = 5\text{ V}$,	$V_{IC} = 5\text{ V}$	25°C	0.1		pA	
				70°C	7	300		
I_{IB}	Input bias current (see Note 4)	$V_O = 5\text{ V}$,	$V_{IC} = 5\text{ V}$	25°C	0.7		pA	
				70°C	50	600		
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	-0.2 to 9	-0.3 to 9.2	V	
				Full range	-0.2 to 8.5		V	
V_{OH}	High-level output voltage	$V_{ID} = 100\text{ mV}$,	$R_L = 1\text{ M}\Omega$	25°C	8	8.9	V	
				0°C	7.8	8.9		
				70°C	7.8	8.9		
V_{OL}	Low-level output voltage	$V_{ID} = -100\text{ mV}$,	$I_{OL} = 0$	25°C	0	50	mV	
				0°C	0	50		
				70°C	0	50		
A_{VD}	Large-signal differential voltage amplification	$V_O = 1\text{ V to }6\text{ V}$,	$R_L = 1\text{ M}\Omega$	25°C	50	870	V/mV	
				0°C	50	1020		
				70°C	50	660		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$		25°C	65	97	dB	
				0°C	60	97		
				70°C	60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 5\text{ V to }10\text{ V}$,	$V_O = 1.4\text{ V}$	25°C	70	97	dB	
				0°C	60	97		
				70°C	60	98		
I_{DD}	Supply current (four amplifiers)	$V_O = 5\text{ V}$, No load	$V_{IC} = 5\text{ V}$,	25°C	57	92	μA	
				0°C	72	132		
				70°C	44	80		

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.



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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A †	TLC27L4I TLC27L4AI TLC27L4BI TLC27L9I			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L4I	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$,	$V_{IC} = 0$, $R_L = 1\text{ M}\Omega$	25°C	1.1 10		mV
					Full range	13		
		TLC27L4AI	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$,	$V_{IC} = 0$, $R_L = 1\text{ M}\Omega$	25°C	0.9 5		
					Full range	7		
	TLC27L4BI	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$,	$V_{IC} = 0$, $R_L = 1\text{ M}\Omega$	25°C	240	2000	μV	
				Full range	3500			
	TLC27L9I	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$,	$V_{IC} = 0$, $R_L = 1\text{ M}\Omega$	25°C	200	900		
				Full range	2000			
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C	1.1		$\mu\text{V}/^\circ\text{C}$	
I_{IO}	Input offset current (see Note 4)	$V_O = 2.5\text{ V}$,	$V_{IC} = 2.5\text{ V}$	25°C	0.1		pA	
				85°C	24	1000		
I_{IB}	Input bias current (see Note 4)	$V_O = 2.5\text{ V}$,	$V_{IC} = 2.5\text{ V}$	25°C	0.6		pA	
				85°C	200	2000		
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	-0.2 to 4	-0.3 to 4.2	V	
				Full range	-0.2 to 3.5		V	
V_{OH}	High-level output voltage	$V_{ID} = 100\text{ mV}$,	$R_L = 1\text{ M}\Omega$	25°C	3.2	4.1	V	
				-40°C	3	4.1		
				85°C	3	4.2		
V_{OL}	Low-level output voltage	$V_{ID} = -100\text{ mV}$,	$I_{OL} = 0$	25°C	0	50	mV	
				-40°C	0	50		
				85°C	0	50		
A_{VD}	Large-signal differential voltage amplification	$V_O = 0.25\text{ V to }2\text{ V}$,	$R_L = 1\text{ M}\Omega$	25°C	50	480	V/mV	
				-40°C	50	900		
				85°C	50	330		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$		25°C	65	94	dB	
				-40°C	60	95		
				85°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 5\text{ V to }10\text{ V}$,	$V_O = 1.4\text{ V}$	25°C	70	97	dB	
				-40°C	60	97		
				85°C	60	98		
I_{DD}	Supply current (four amplifiers)	$V_O = 2.5\text{ V}$, No load	$V_{IC} = 2.5\text{ V}$,	25°C	39	68	μA	
				-40°C	62	108		
				85°C	29	52		

† Full range is -40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.



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electrical characteristics at specified free-air temperature, $V_{DD} = 10\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A †	TLC27L4I TLC27L4AI TLC27L4BI TLC27L9I			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L4I	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$,	$V_{IC} = 0$, $R_L = 1\text{ M}\Omega$	25°C	1.1	10	mV
					Full range		13	
	TLC27L4AI	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$,	$V_{IC} = 0$, $R_L = 1\text{ M}\Omega$	25°C	0.9	5	mV	
				Full range		7		
	TLC27L4BI	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$,	$V_{IC} = 0$, $R_L = 1\text{ M}\Omega$	25°C	260	2000	μV	
				Full range		3500		
	TLC27L9I	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$,	$V_{IC} = 0$, $R_L = 1\text{ M}\Omega$	25°C	210	1200	μV	
				Full range		2900		
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C	1		$\mu\text{V}/^\circ\text{C}$	
I_{IO}	Input offset current (see Note 4)	$V_O = 5\text{ V}$,	$V_{IC} = 5\text{ V}$	25°C	0.1		pA	
				85°C	26	1000		
I_{IB}	Input bias current (see Note 4)	$V_O = 5\text{ V}$,	$V_{IC} = .5\text{ V}$	25°C	0.7		pA	
				85°C	220	2000		
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	-0.2 to 9	-0.3 to 9.2	V	
				Full range	-0.2 to 8.5		V	
V_{OH}	High-level output voltage	$V_{ID} = 100\text{ mV}$,	$R_L = 1\text{ M}\Omega$	25°C	8	8.9	V	
				-40°C	7.8	8.9		
				85°C	7.8	8.9		
V_{OL}	Low-level output voltage	$V_{ID} = -100\text{ mV}$,	$I_{OL} = 0$	25°C	0	50	mV	
				-40°C	0	50		
				85°C	0	50		
A_{VD}	Large-signal differential voltage amplification	$V_O = 1\text{ V to }6\text{ V}$,	$R_L = 1\text{ M}\Omega$	25°C	50	800	V/mV	
				-40°C	50	1550		
				85°C	50	585		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$		25°C	65	97	dB	
				-40°C	60	97		
				85°C	60	98		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 5\text{ V to }10\text{ V}$,	$V_O = 1.4\text{ V}$	25°C	70	97	dB	
				-40°C	60	97		
				85°C	60	98		
I_{DD}	Supply current (four amplifiers)	$V_O = 5\text{ V}$, No load	$V_{IC} = 5\text{ V}$,	25°C	57	92	μA	
				-40°C	98	172		
				85°C	40	72		

† Full range is -40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.



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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A †	TLC27L4M TLC27L9M			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$,	$V_{IC} = 0$, $R_L = 1\text{ M}\Omega$	25°C	1.1	10	mV
				Full range		12	
	TLC27L9M	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$,	$V_{IC} = 0$, $R_L = 1\text{ M}\Omega$	25°C	200	900	μV
				Full range		3750	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 125°C	1.4		$\mu\text{V}/^\circ\text{C}$	
I_{IO}	Input offset current (see Note 4)	$V_O = 2.5\text{ V}$,	$V_{IC} = 2.5\text{ V}$	25°C	0.1		pA
				125°C	1.4	15	nA
I_{IB}	Input bias current (see Note 4)	$V_O = 2.5\text{ V}$,	$V_{IC} = 2.5\text{ V}$	25°C	0.6		pA
				125°C	9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	-0.2 to 4	-0.3 to 4.2	V
				Full range	-0.2 to 3.5		V
V_{OH}	High-level output voltage	$V_{ID} = 100\text{ mV}$,	$R_L = 1\text{ M}\Omega$	25°C	3.2	4.1	V
				-55°C	3	4.1	
				125°C	3	4.2	
V_{OL}	Low-level output voltage	$V_{ID} = -100\text{ mV}$,	$I_{OL} = 0$	25°C	0	50	mV
				-55°C	0	50	
				125°C	0	50	
A_{VD}	Large-signal differential voltage amplification	$V_O = 0.25\text{ V to }2\text{ V}$,	$R_L = 1\text{ M}\Omega$	25°C	50	480	V/mV
				-55°C	25	950	
				125°C	25	200	
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$		25°C	65	94	dB
				-55°C	60	95	
				125°C	60	85	
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 5\text{ V to }10\text{ V}$,	$V_O = 1.4\text{ V}$	25°C	70	97	dB
				-55°C	60	97	
				125°C	60	98	
I_{DD}	Supply current (four amplifiers)	$V_O = 2.5\text{ V}$, No load	$V_{IC} = 2.5\text{ V}$,	25°C	39	68	μA
				-55°C	69	120	
				125°C	27	48	

† Full range is -55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.



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electrical characteristics at specified free-air temperature, $V_{DD} = 10\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A †	TLC27L4M TLC27L9M			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC27L4M	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$	$V_{IC} = 0$, $R_L = 1\text{ M}\Omega$	25°C	1.1	10	mV
					Full range		12	
		TLC27L9M	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$	$V_{IC} = 0$, $R_L = 1\text{ M}\Omega$	25°C	210	1200	μV
					Full range		4300	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C	1.4		$\mu\text{V}/^\circ\text{C}$	
I_{IO}	Input offset current (see Note 4)	$V_O = 5\text{ V}$	$V_{IC} = 5\text{ V}$	25°C	0.1		pA	
				125°C	1.8	15	nA	
I_{IB}	Input bias current (see Note 4)	$V_O = 5\text{ V}$	$V_{IC} = 5\text{ V}$	25°C	0.7		pA	
				125°C	10	35	nA	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	0 to 9	-0.3 to 9.2	V	
				Full range	0 to 8.5		V	
V_{OH}	High-level output voltage	$V_{ID} = 100\text{ mV}$	$R_L = 1\text{ M}\Omega$	25°C	8	8.9	V	
				-55°C	7.8	8.8		
				125°C	7.8	9		
V_{OL}	Low-level output voltage	$V_{ID} = -100\text{ mV}$	$I_{OL} = 0$	25°C	0	50	mV	
				-55°C	0	50		
				125°C	0	50		
A_{VD}	Large-signal differential voltage amplification	$V_O = 1\text{ V to }6\text{ V}$	$R_L = 1\text{ M}\Omega$	25°C	50	800	V/mV	
				-55°C	25	1750		
				125°C	25	380		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$		25°C	65	97	dB	
				-55°C	60	97		
				125°C	60	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 5\text{ V to }10\text{ V}$	$V_O = 1.4\text{ V}$	25°C	70	97	dB	
				-55°C	60	97		
				125°C	60	98		
I_{DD}	Supply current (four amplifiers)	$V_O = 5\text{ V}$, No load	$V_{IC} = 5\text{ V}$	25°C	57	92	μA	
				-55°C	111	192		
				125°C	35	60		

† Full range is -55°C to 125°C.

NOTES: 4. The typical values of input bias current and Input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.



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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TLC27L4Y			UNIT
		MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 0$, $R_L = 1\text{ M}\Omega$		1.1	10	mV
α_{VIO} Average temperature coefficient of input offset voltage	$T_A = 25^\circ\text{C}$ to 70°C		1.1		$\mu\text{V}/^\circ\text{C}$
I_{IO} Input offset current (see Note 4)	$V_O = 2.5\text{ V}$, $V_{IC} = 2.5\text{ V}$		0.1		pA
I_{IB} Input bias current (see Note 4)	$V_O = 2.5\text{ V}$, $V_{IC} = 2.5\text{ V}$		0.6		pA
V_{ICR} Common-mode input voltage range (see Note 5)		-0.2 to 4	-0.3 to 4.2		V
V_{OH} High-level output voltage	$V_{ID} = 100\text{ mV}$, $R_L = 1\text{ M}\Omega$		3.2	4.1	V
V_{OL} Low-level output voltage	$V_{ID} = -100\text{ mV}$, $I_{OL} = 0$		0	50	mV
A_{VD} Large-signal differential voltage amplification	$V_O = 0.25\text{ V}$ to 2 V , $R_L = 1\text{ M}\Omega$		50	520	V/mV
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$		65	94	dB
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 5\text{ V}$ to 10 V , $V_O = 1.4\text{ V}$		70	97	dB
I_{DD} Supply current (four amplifiers)	$V_O = 2.5\text{ V}$, No load $V_{IC} = 2.5\text{ V}$		40	68	μA

electrical characteristics at specified free-air temperature, $V_{DD} = 10\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TLC27L4Y			UNIT
		MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_O = 1.4\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 0$, $R_L = 1\text{ M}\Omega$		1.1	10	mV
α_{VIO} Average temperature coefficient of input offset voltage	$T_A = 25^\circ\text{C}$ to 70°C		1		$\mu\text{V}/^\circ\text{C}$
I_{IO} Input offset current (see Note 4)	$V_O = 5\text{ V}$, $V_{IC} = 5\text{ V}$		0.1		pA
I_{IB} Input bias current (see Note 4)	$V_O = 5\text{ V}$, $V_{IC} = 5\text{ V}$		0.7		pA
V_{ICR} Common-mode input voltage range (see Note 5)		-0.2 to 9	-0.3 to 9.2		V
V_{OH} High-level output voltage	$V_{ID} = 100\text{ mV}$, $R_L = 1\text{ M}\Omega$		8	8.9	V
V_{OL} Low-level output voltage	$V_{ID} = -100\text{ mV}$, $I_{OL} = 0$		0	50	mV
A_{VD} Large-signal differential voltage amplification	$V_O = 1\text{ V}$ to 6 V , $R_L = 1\text{ M}\Omega$		50	870	V/mV
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$		65	97	dB
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 5\text{ V}$ to 10 V , $V_O = 1.4\text{ V}$		70	97	dB
I_{DD} Supply current (four amplifiers)	$V_O = 5\text{ V}$, No load $V_{IC} = 5\text{ V}$		57	92	μA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.



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operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A	TLC27L4C TLC27L4AC TLC27L4BC TLC27L9C			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 1\text{ M}\Omega$, $C_L = 20\text{ pF}$, See Figure 1	$V_{I\text{PP}} = 1\text{ V}$	25°C	0.03		V/ μs
			0°C	0.04		
			70°C	0.03		
		$V_{I\text{PP}} = 2.5\text{ V}$	25°C	0.03		
			0°C	0.03		
			70°C	0.02		
V_n Equivalent input noise voltage	$f = 1\text{ kHz}$, See Figure 2	$R_S = 20\ \Omega$, 25°C	70		nV/ $\sqrt{\text{Hz}}$	
B_{OM} Maximum output-swing bandwidth	$V_O = V_{\text{OH}}$, $R_L = 1\text{ M}\Omega$, See Figure 1	$C_L = 20\text{ pF}$, See Figure 1	25°C	5		kHz
			0°C	6		
			70°C	4.5		
B_1 Unity-gain bandwidth	$V_I = 10\text{ mV}$, See Figure 3	$C_L = 20\text{ pF}$, See Figure 3	25°C	85		kHz
			0°C	100		
			70°C	65		
ϕ_m Phase margin	$V_I = 10\text{ mV}$, $C_L = 20\text{ pF}$, See Figure 3	$f = B_1$, See Figure 3	25°C	34°		
			0°C	36°		
			70°C	30°		

operating characteristics at specified free-air temperature, $V_{DD} = 10\text{ V}$

PARAMETER	TEST CONDITIONS	T_A	TLC27L4C TLC27L4AC TLC27L4BC TLC27L9C			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 1\text{ M}\Omega$, $C_L = 20\text{ pF}$, See Figure 1	$V_{I\text{PP}} = 1\text{ V}$	25°C	0.05		V/ μs
			0°C	0.05		
			70°C	0.04		
		$V_{I\text{PP}} = 5.5\text{ V}$	25°C	0.04		
			0°C	0.05		
			70°C	0.04		
V_n Equivalent input noise voltage	$f = 1\text{ kHz}$, See Figure 2	$R_S = 20\ \Omega$, 25°C	70		nV/ $\sqrt{\text{Hz}}$	
B_{OM} Maximum output-swing bandwidth	$V_O = V_{\text{OH}}$, $R_L = 1\text{ M}\Omega$, See Figure 1	$C_L = 20\text{ pF}$, See Figure 1	25°C	1		kHz
			0°C	1.3		
			70°C	0.9		
B_1 Unity-gain bandwidth	$V_I = 10\text{ mV}$, See Figure 3	$C_L = 20\text{ pF}$, See Figure 3	25°C	110		kHz
			0°C	125		
			70°C	90		
ϕ_m Phase margin	$V_I = 10\text{ mV}$, $C_L = 20\text{ pF}$, See Figure 3	$f = B_1$, See Figure 3	25°C	38°		
			0°C	40°		
			70°C	34°		



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operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS		T_A	TLC27L4I TLC27L4AI TLC27L4BI TLC27L9I			UNIT
				MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 1\text{ M}\Omega$, $C_L = 20\text{ pF}$, See Figure 1	$V_{I\text{PP}} = 1\text{ V}$	25°C	0.03		V/ μs	
			-40°C	0.04			
			85°C	0.03			
		$V_{I\text{PP}} = 2.5\text{ V}$	25°C	0.03			
			-40°C	0.04			
			85°C	0.02			
V_n Equivalent input noise voltage	$f = 1\text{ Hz}$, See Figure 2	$R_S = 20\ \Omega$,	25°C	70		nV/ $\sqrt{\text{Hz}}$	
B_{OM} Maximum output-swing bandwidth	$V_O = V_{\text{OH}}$, $R_L = 1\text{ M}\Omega$, See Figure 1	$C_L = 20\text{ pF}$, See Figure 1	25°C	5		kHz	
			-40°C	7			
			85°C	4			
B_1 Unity-gain bandwidth	$V_I = 10\text{ mV}$, See Figure 3	$C_L = 20\text{ pF}$,	25°C	85		kHz	
			-40°C	130			
			85°C	55			
ϕ_m Phase margin	$V_I = 10\text{ mV}$, $C_L = 20\text{ pF}$,	$f = B_1$, See Figure 3	25°C	34°			
			-40°C	38°			
			85°C	28°			

operating characteristics at specified free-air temperature, $V_{DD} = 10\text{ V}$

PARAMETER	TEST CONDITIONS		T_A	TLC27L4I TLC27L4AI TLC27L4BI TLC27L9I			UNIT
				MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 1\text{ M}\Omega$, $C_L = 20\text{ pF}$, See Figure 1	$V_{I\text{PP}} = 1\text{ V}$	25°C	0.05		V/ μs	
			-40°C	0.06			
			85°C	0.03			
		$V_{I\text{PP}} = 2.5\text{ V}$	25°C	0.04			
			-40°C	0.05			
			85°C	0.03			
V_n Equivalent input noise voltage	$f = 1\text{ Hz}$, See Figure 2	$R_S = 20\ \Omega$,	25°C	70		nV/ $\sqrt{\text{Hz}}$	
B_{OM} Maximum output-swing bandwidth	$V_O = V_{\text{OH}}$, $R_L = 1\text{ M}\Omega$, See Figure 1	$C_L = 20\text{ pF}$, See Figure 1	25°C	1		kHz	
			-40°C	1.4			
			85°C	0.8			
B_1 Unity-gain bandwidth	$V_I = 10\text{ mV}$, See Figure 3	$C_L = 20\text{ pF}$,	25°C	110		kHz	
			-40°C	155			
			85°C	80			
ϕ_m Phase margin	$V_I = 10\text{ mV}$, $C_L = 20\text{ pF}$,	$f = B_1$, See Figure 3	25°C	38°			
			-40°C	42°			
			85°C	32°			



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operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A	TLC27L4M TLC27L9M			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 1\text{ M}\Omega$, $C_L = 20\text{ pF}$, See Figure 1	$V_{I\text{PP}} = 1\text{ V}$	25°C	0.03		V/ μs
			-55°C	0.04		
			125°C	0.02		
		$V_{I\text{PP}} = 2.5\text{ V}$	25°C	0.03		
			-55°C	0.04		
			125°C	0.02		
V_n Equivalent input noise voltage	$f = 1\text{ kHz}$, See Figure 2	$R_S = 20\ \Omega$, 25°C	70		nV/ $\sqrt{\text{Hz}}$	
B_{OM} Maximum output-swing bandwidth	$V_O = V_{\text{OH}}$, $R_L = 1\text{ M}\Omega$, $C_L = 20\text{ pF}$, See Figure 1	25°C	5		kHz	
		-55°C	8			
		125°C	3			
B_1 Unity-gain bandwidth	$V_I = 10\text{ mV}$, See Figure 3	$C_L = 20\text{ pF}$, 25°C	85		kHz	
			-55°C	140		
			125°C	45		
ϕ_m Phase margin	$V_I = 10\text{ mV}$, $C_L = 20\text{ pF}$, $f = B_1$, See Figure 3	25°C	34°			
		-55°C	39°			
		125°C	25°			

operating characteristics at specified free-air temperature, $V_{DD} = 10\text{ V}$

PARAMETER	TEST CONDITIONS	T_A	TLC27L4M TLC27L9M			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 1\text{ M}\Omega$, $C_L = 20\text{ pF}$, See Figure 1	$V_{I\text{PP}} = 1\text{ V}$	25°C	0.05		V/ μs
			-55°C	0.06		
			125°C	0.03		
		$V_{I\text{PP}} = 5.5\text{ V}$	25°C	0.04		
			-55°C	0.06		
			125°C	0.03		
V_n Equivalent input noise voltage	$f = 1\text{ kHz}$, See Figure 2	$R_S = 20\ \Omega$, 25°C	70		nV/ $\sqrt{\text{Hz}}$	
B_{OM} Maximum output-swing bandwidth	$V_O = V_{\text{OH}}$, $R_L = 1\text{ M}\Omega$, $C_L = 20\text{ pF}$, See Figure 1	25°C	1		kHz	
		-55°C	1.5			
		125°C	0.7			
B_1 Unity-gain bandwidth	$V_I = 10\text{ mV}$, See Figure 3	$C_L = 20\text{ pF}$, 25°C	110		kHz	
			-55°C	165		
			125°C	70		
ϕ_m Phase margin	$V_I = 10\text{ mV}$, $C_L = 20\text{ pF}$, $f = B_1$, See Figure 3	25°C	38°			
		-55°C	43°			
		125°C	29°			



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operating characteristics, $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TLC27L4Y			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	$R_L = 1\text{ M}\Omega$, $C_L = 20\text{ pF}$, See Figure 1	$V_{I\text{PP}} = 1\text{ V}$	0.03			$\text{V}/\mu\text{s}$
			$V_{I\text{PP}} = 2.5\text{ V}$	0.03			
V_n	Equivalent input noise voltage	$f = 1\text{ kHz}$, See Figure 2	$R_S = 20\ \Omega$,	70			$\text{nV}/\sqrt{\text{Hz}}$
B _{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 1\text{ M}\Omega$, See Figure 1	$C_L = 20\text{ pF}$, See Figure 1	5			kHz
B ₁	Unity-gain bandwidth	$V_I = 10\text{ mV}$, See Figure 3	$C_L = 20\text{ pF}$,	85			kHz
ϕ_m	Phase margin	$V_I = 10\text{ mV}$, $C_L = 20\text{ pF}$,	$f = B_1$, See Figure 3	34°			

operating characteristics, $V_{DD} = 10\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TLC27L4Y			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	$R_L = 1\text{ M}\Omega$, $C_L = 20\text{ pF}$, See Figure 1	$V_{I\text{PP}} = 1\text{ V}$	0.05			$\text{V}/\mu\text{s}$
			$V_{I\text{PP}} = 5.5\text{ V}$	0.04			
V_n	Equivalent input noise voltage	$f = 1\text{ kHz}$, See Figure 2	$R_S = 20\ \Omega$,	70			$\text{nV}/\sqrt{\text{Hz}}$
B _{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 1\text{ M}\Omega$, See Figure 1	$C_L = 20\text{ pF}$, See Figure 1	1			kHz
B ₁	Unity-gain bandwidth	$V_I = 10\text{ mV}$, See Figure 3	$C_L = 20\text{ pF}$,	110			kHz
ϕ_m	Phase margin	$V_I = 10\text{ mV}$, $C_L = 20\text{ pF}$,	$f = B_1$, See Figure 3	38°			



PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC27L4 and TLC27L9 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.

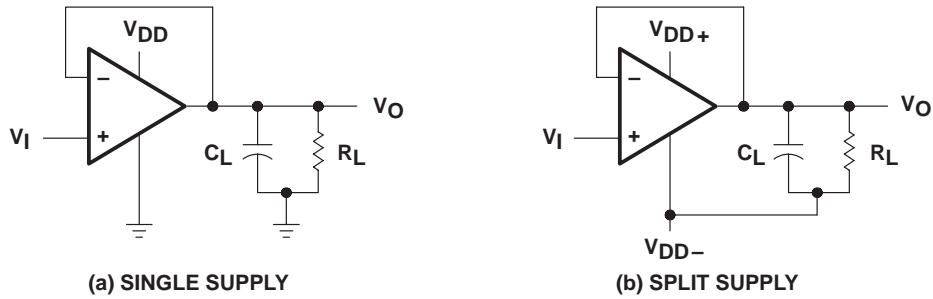


Figure 1. Unity-Gain Amplifier

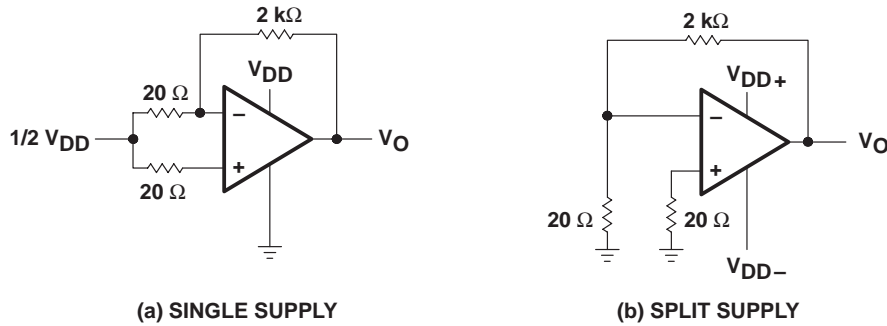


Figure 2. Noise-Test Circuit

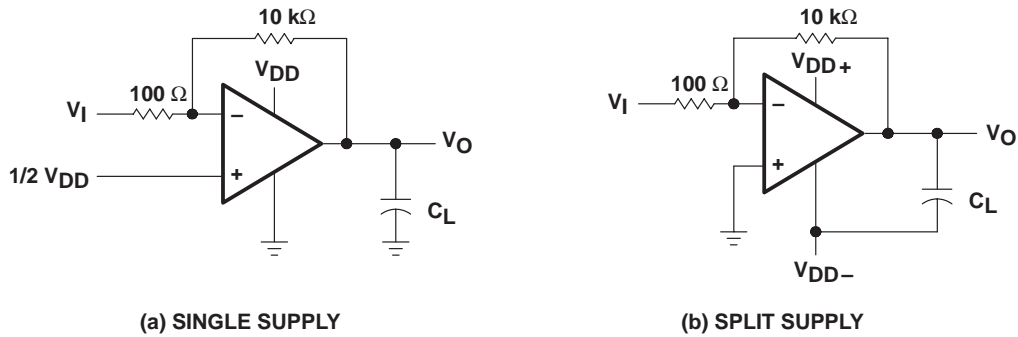


Figure 3. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC27L4 and TLC27L9 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs are shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution: many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

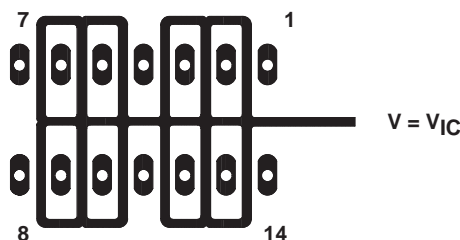


Figure 4. Isolation Metal Around Device Inputs (J and N packages)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

PARAMETER MEASUREMENT INFORMATION

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



Figure 5. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

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TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6, 7
α_{VIO}	Temperature coefficient	Distribution	8, 9
V_{OH}	High-level output voltage	vs High-level output current	10, 11
		vs Supply voltage	12
		vs Free-air temperature	13
V_{OL}	Low-level output voltage	vs Common-mode input voltage	14, 15
		vs Differential input voltage	16
		vs Free-air temperature	17
		vs Low-level output current	18, 19
A_{VD}	Differential voltage amplification	vs Supply voltage	20
		vs Free-air temperature	21
		vs Frequency	32, 33
I_{IB}/I_{IO}	Input bias and input offset current	vs Free-air temperature	22
V_{IC}	Common-mode input voltage	vs Supply voltage	23
I_{DD}	Supply current	vs Supply voltage	24
		vs Free-air temperature	25
SR	Slew rate	vs Supply voltage	26
		vs Free-air temperature	27
	Normalized slew rate	vs Free-air temperature	28
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	29
B_1	Unity-gain bandwidth	vs Free-air temperature	30
		vs Supply voltage	31
ϕ_m	Phase margin	vs Supply voltage	34
		vs Free-air temperature	35
		vs Capacitive loads	36
V_n	Equivalent input noise voltage	vs Frequency	37
ϕ	Phase shift	vs Frequency	32, 33



TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC27L4
 INPUT OFFSET VOLTAGE

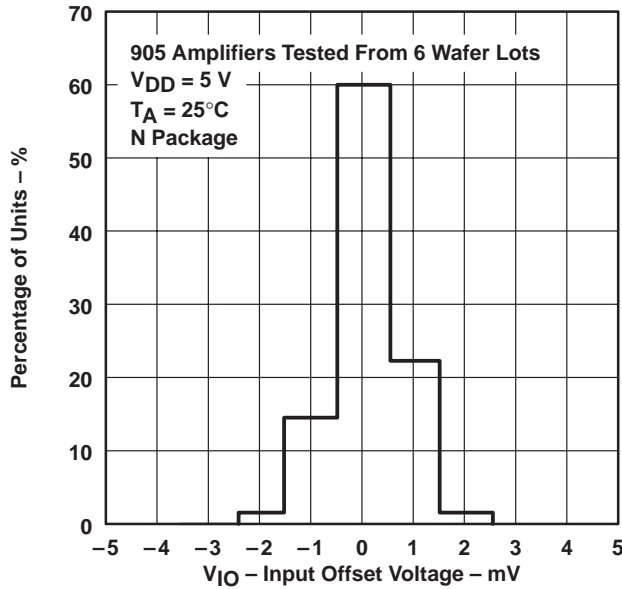


Figure 6

DISTRIBUTION OF TLC27L4
 INPUT OFFSET VOLTAGE

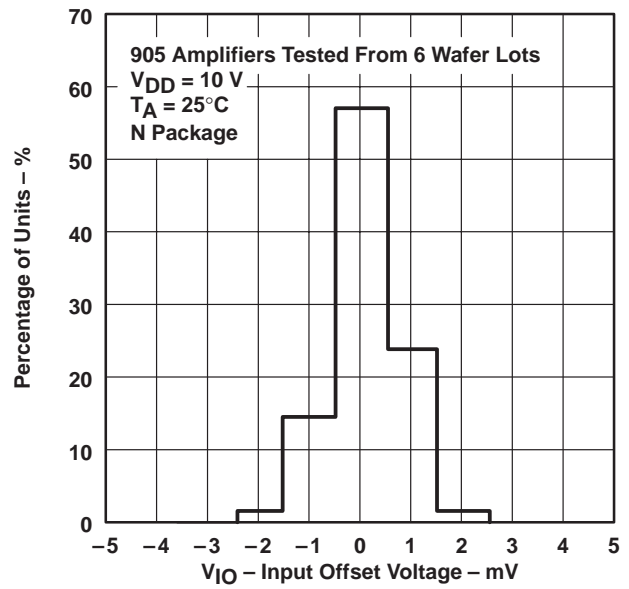


Figure 7

DISTRIBUTION OF TLC27L4 AND TLC27L9
 INPUT OFFSET VOLTAGE
 TEMPERATURE COEFFICIENT

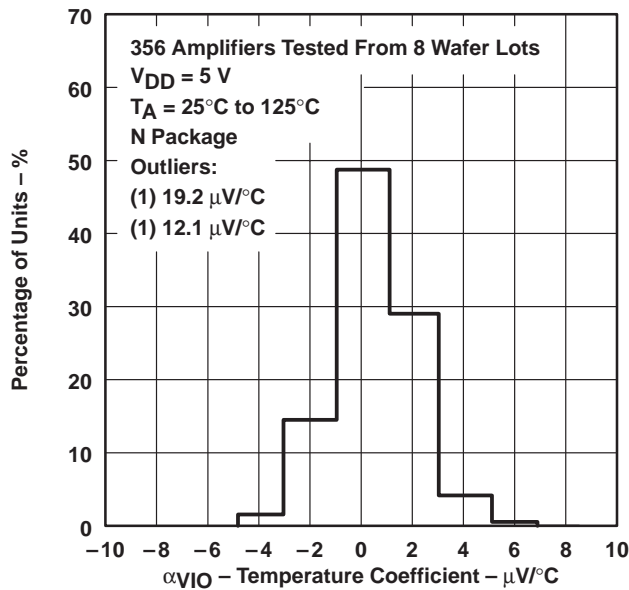


Figure 8

DISTRIBUTION OF TLC27L4 AND TLC27L9
 INPUT OFFSET VOLTAGE
 TEMPERATURE COEFFICIENT

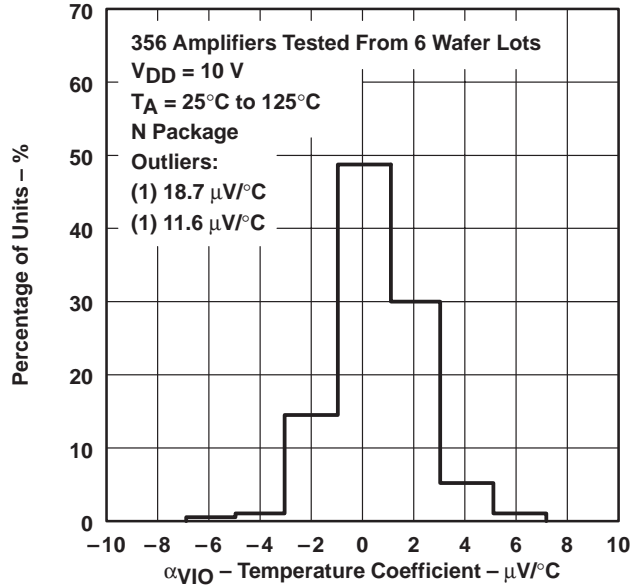


Figure 9

TYPICAL CHARACTERISTICS†

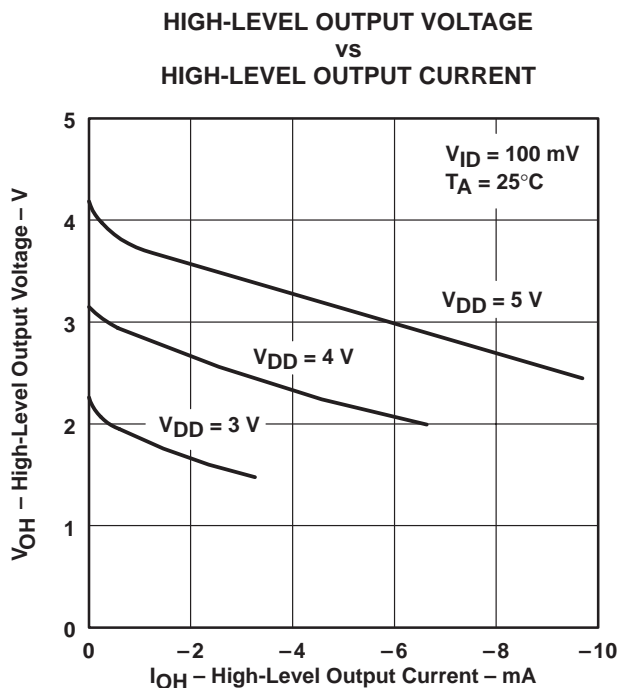


Figure 10

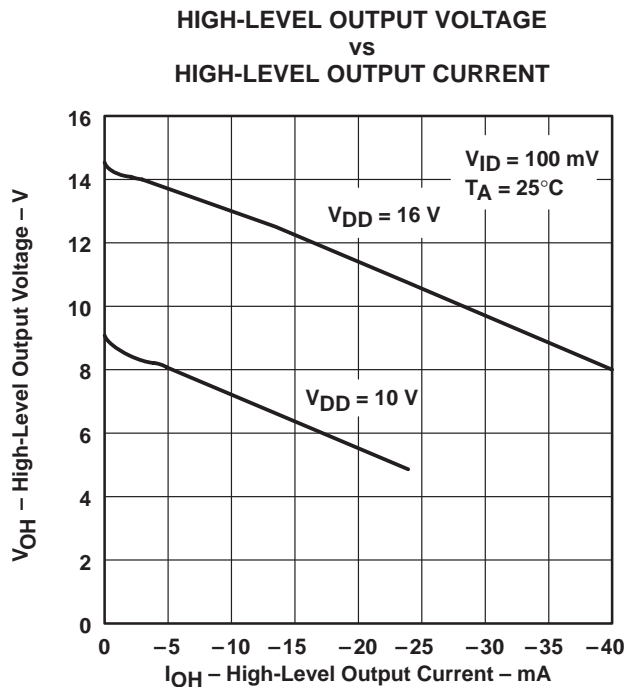


Figure 11

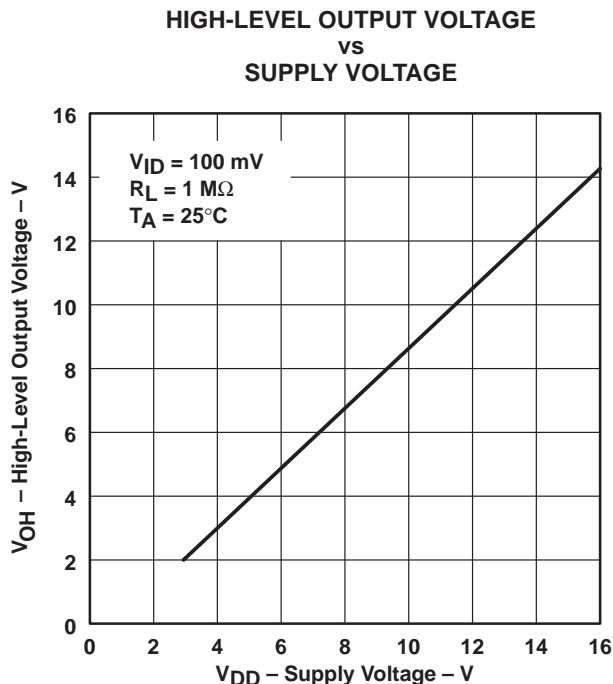


Figure 12

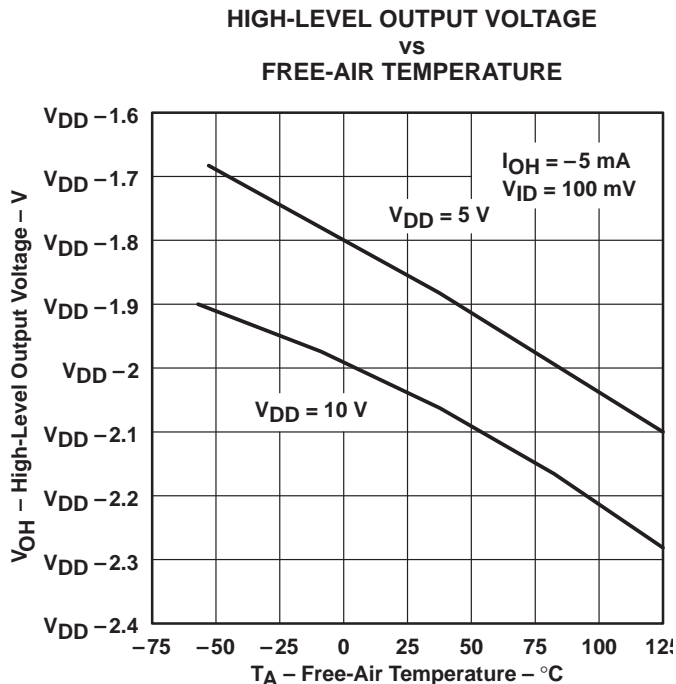


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
 vs
 COMMON-MODE INPUT VOLTAGE

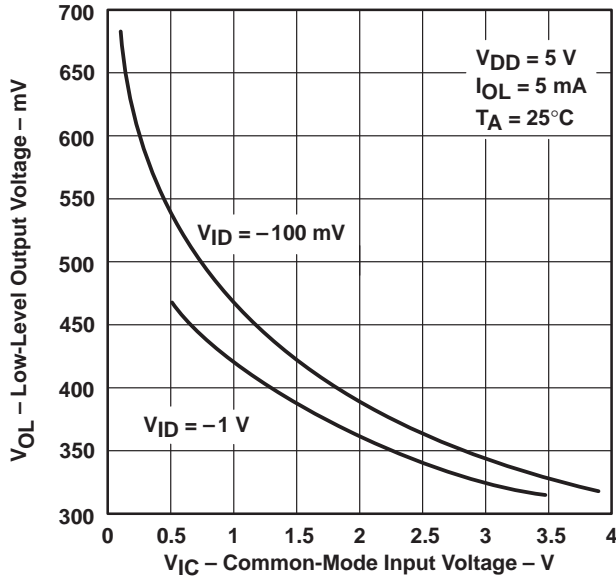


Figure 14

LOW-LEVEL OUTPUT VOLTAGE
 vs
 COMMON-MODE INPUT VOLTAGE

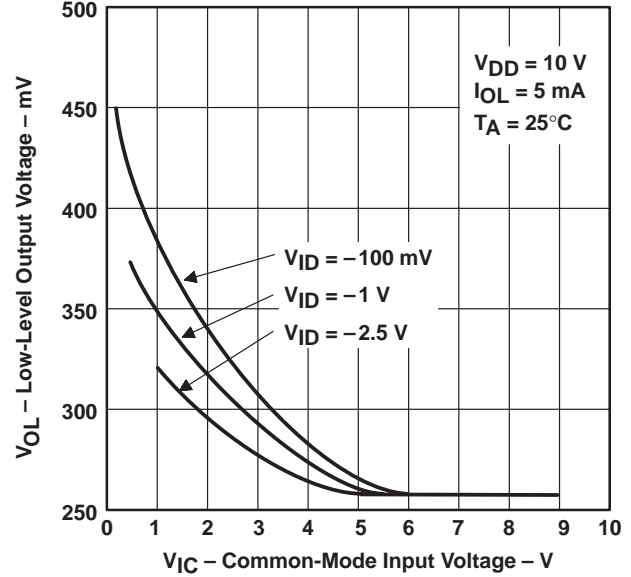


Figure 15

LOW-LEVEL OUTPUT VOLTAGE
 vs
 DIFFERENTIAL INPUT VOLTAGE

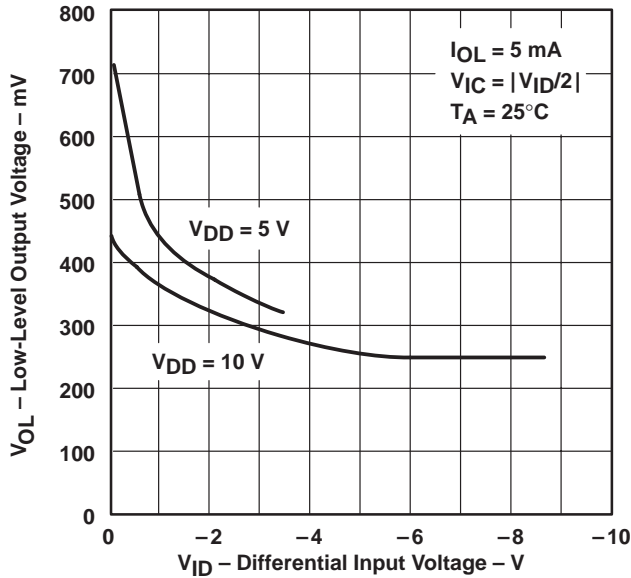


Figure 16

LOW-LEVEL OUTPUT VOLTAGE
 vs
 FREE-AIR TEMPERATURE

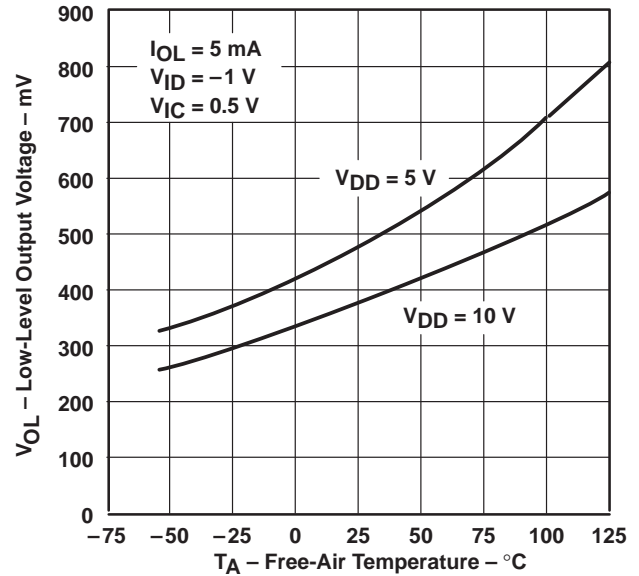


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
 vs
 LOW-LEVEL OUTPUT CURRENT

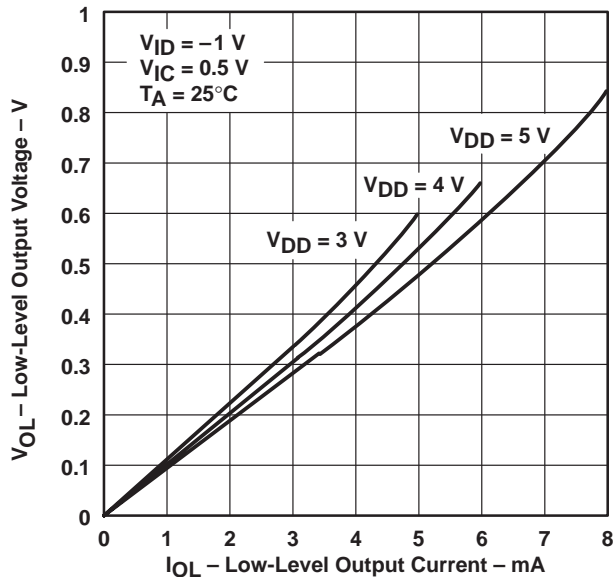


Figure 18

LOW-LEVEL OUTPUT VOLTAGE
 vs
 LOW-LEVEL OUTPUT CURRENT

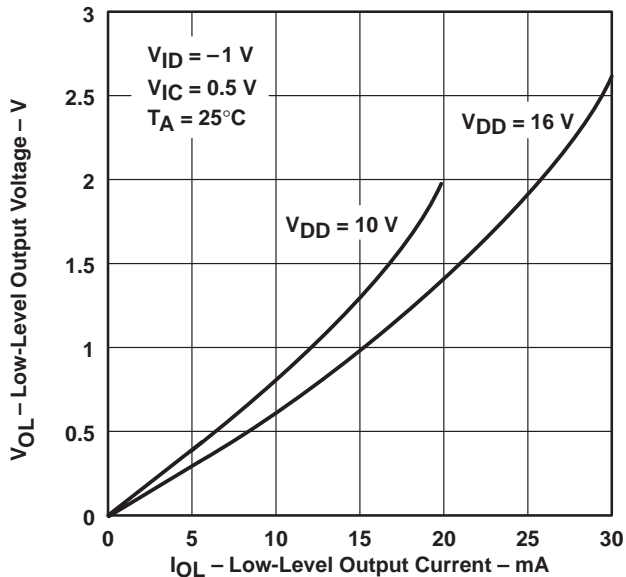


Figure 19

LARGE-SIGNAL
 DIFFERENTIAL VOLTAGE AMPLIFICATION
 vs
 SUPPLY VOLTAGE

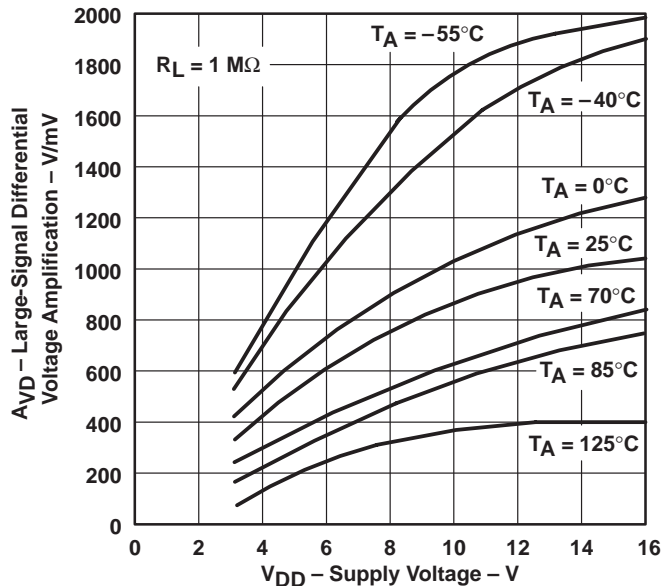


Figure 20

LARGE-SIGNAL
 DIFFERENTIAL VOLTAGE AMPLIFICATION
 vs
 FREE-AIR TEMPERATURE

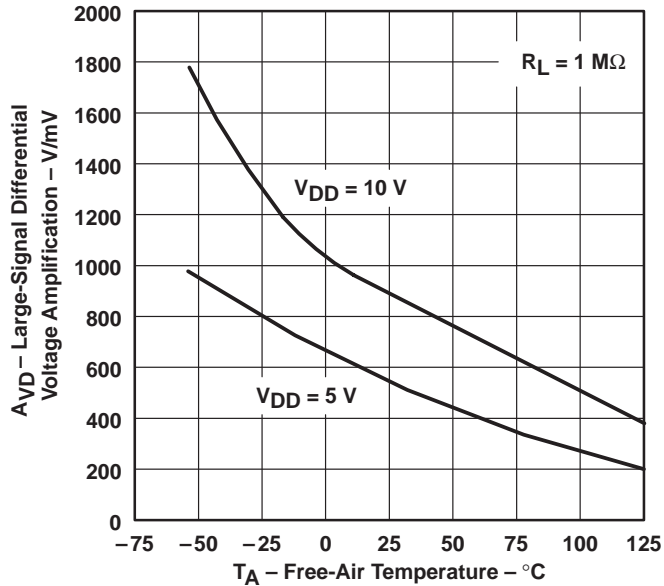
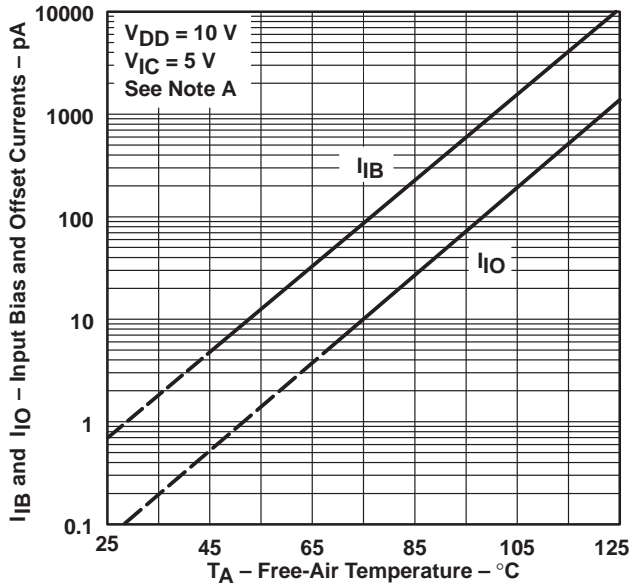


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
 vs
 FREE-AIR TEMPERATURE



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 22

COMMON-MODE
 INPUT VOLTAGE POSITIVE LIMIT
 vs
 SUPPLY VOLTAGE

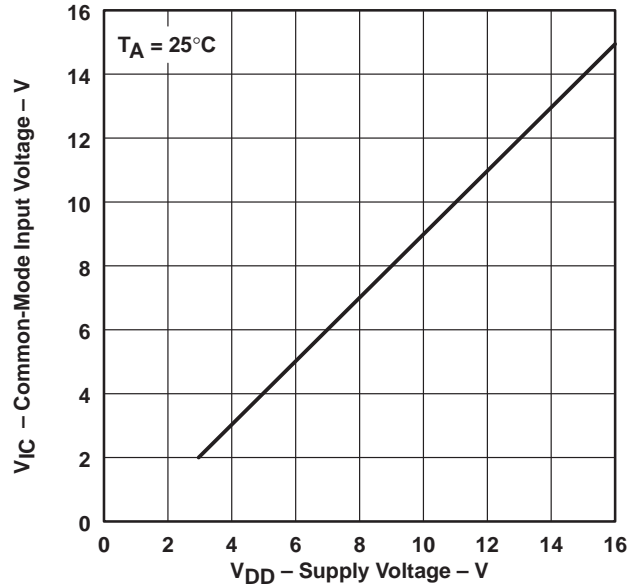


Figure 23

SUPPLY CURRENT
 vs
 SUPPLY VOLTAGE

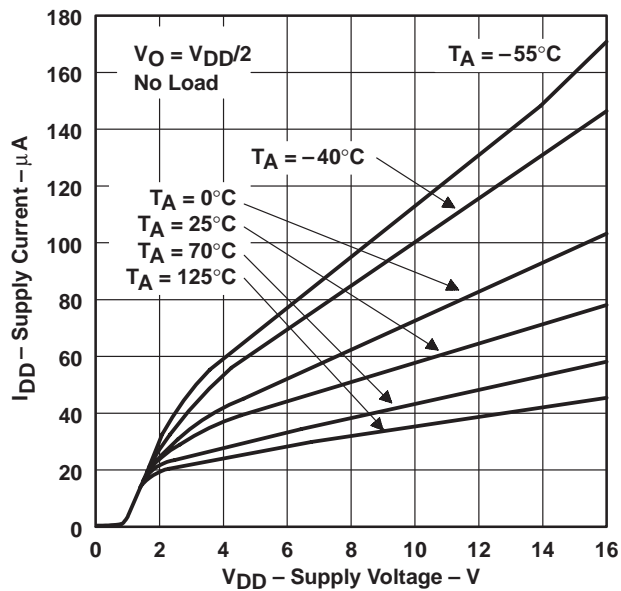


Figure 24

SUPPLY CURRENT
 vs
 FREE-AIR TEMPERATURE

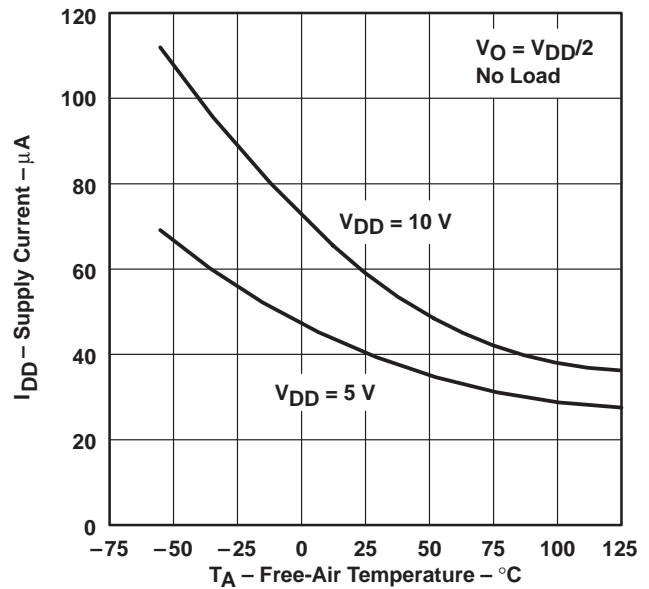


Figure 25

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

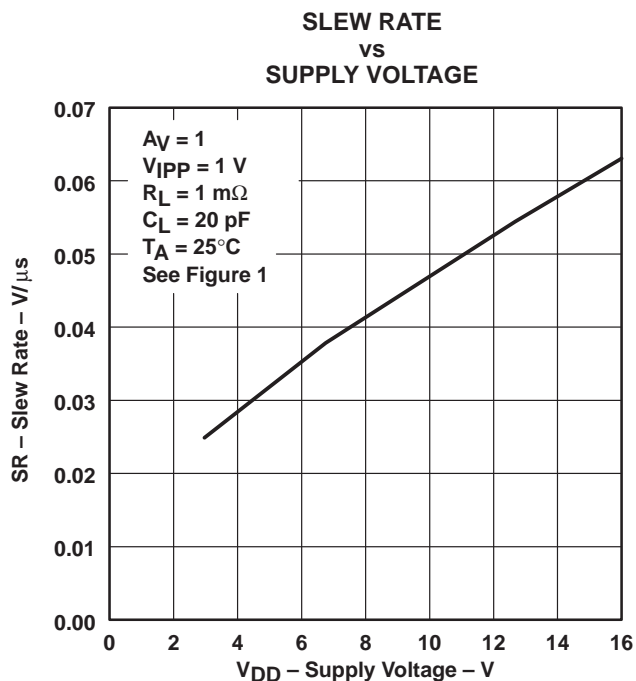


Figure 26

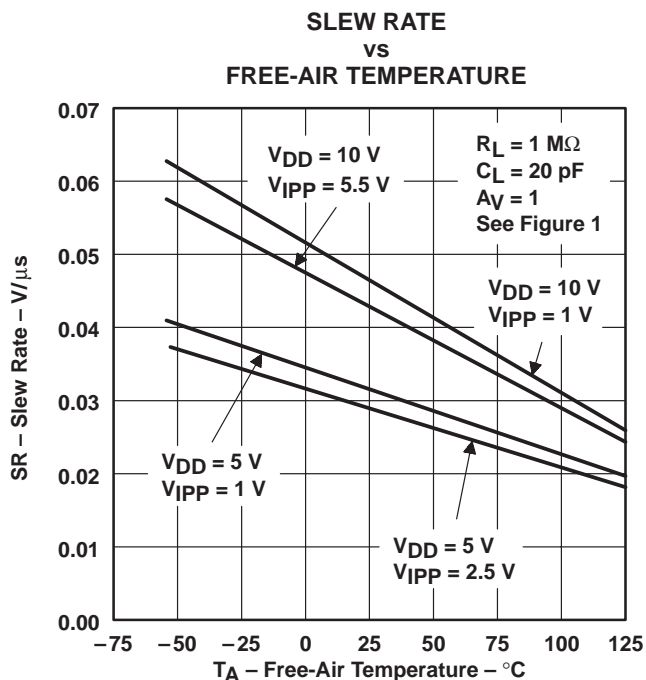


Figure 27

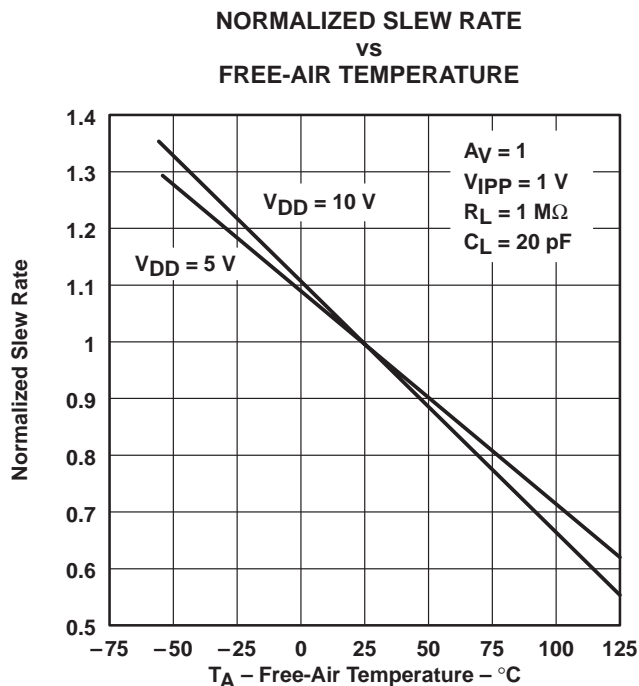


Figure 28

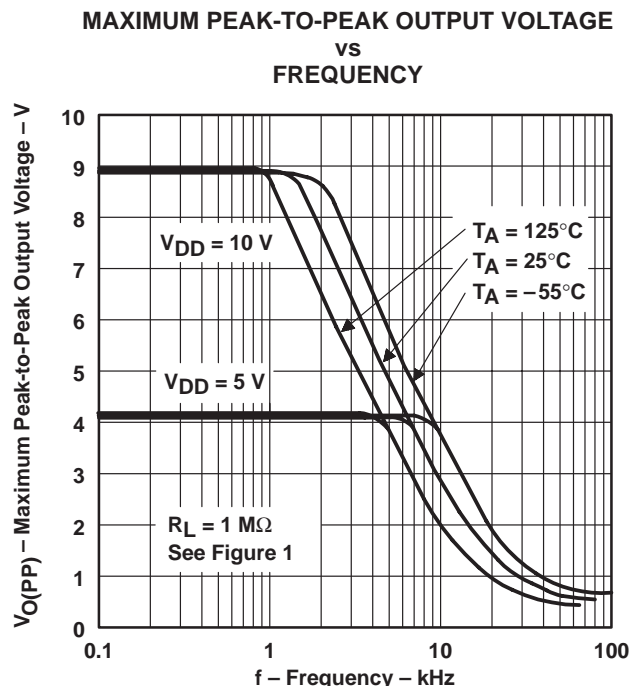


Figure 29

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

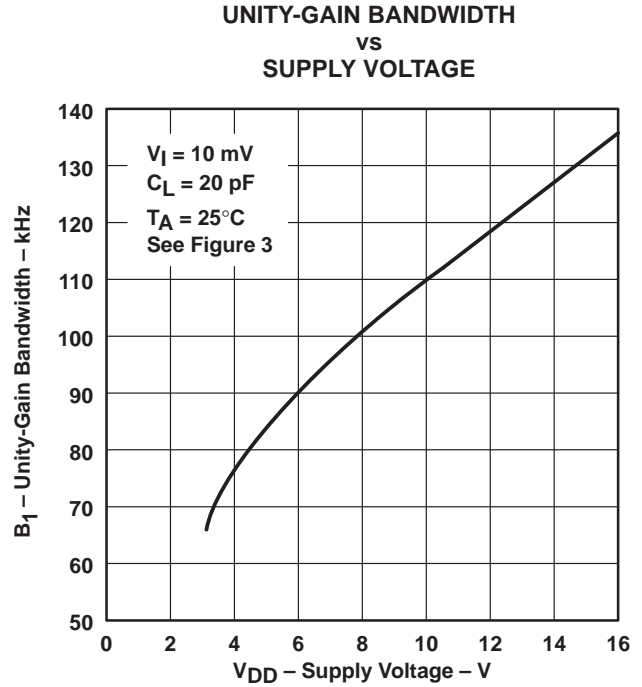
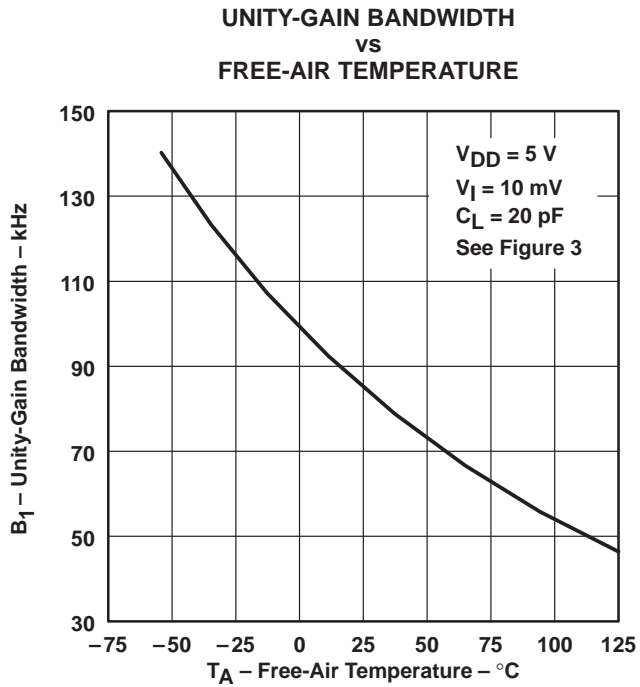


Figure 30

Figure 31

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE
 AMPLIFICATION AND PHASE SHIFT
 vs
 FREQUENCY**

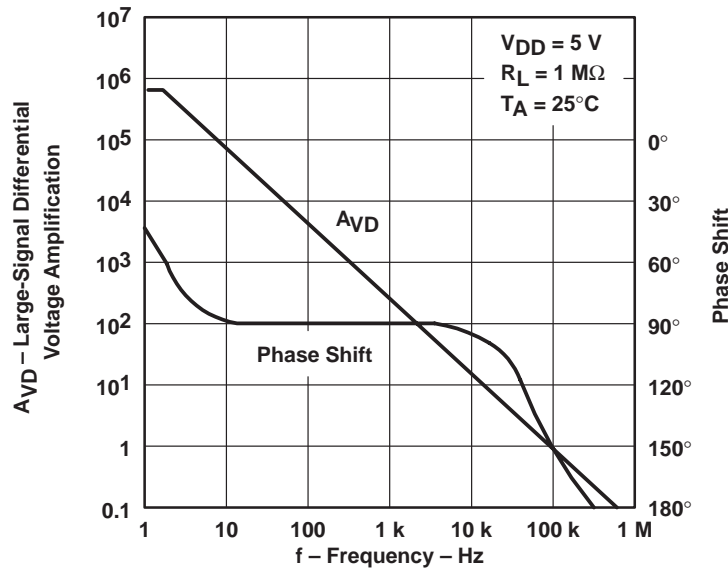


Figure 32

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
 AMPLIFICATION AND PHASE SHIFT
 VS
 FREQUENCY

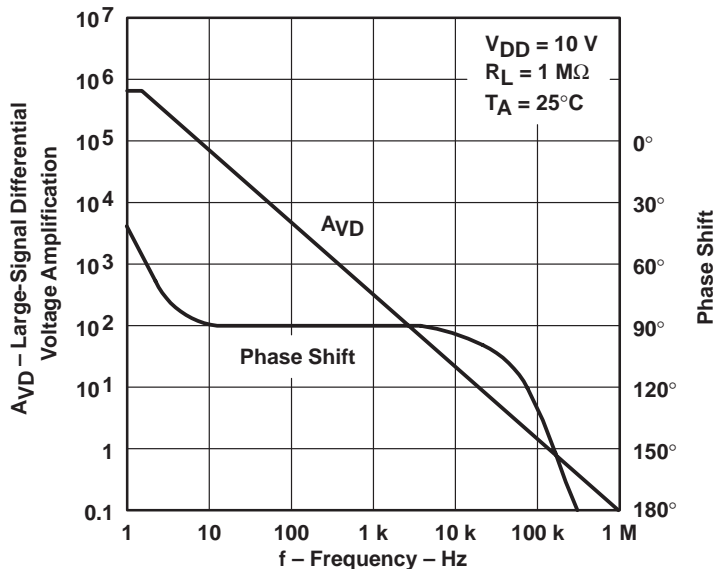


Figure 33

PHASE MARGIN
 VS
 SUPPLY VOLTAGE

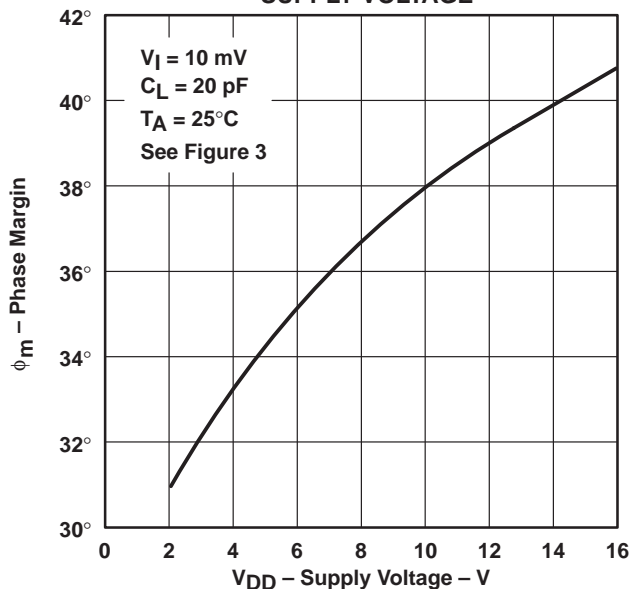


Figure 34

PHASE MARGIN
 VS
 FREE-AIR TEMPERATURE

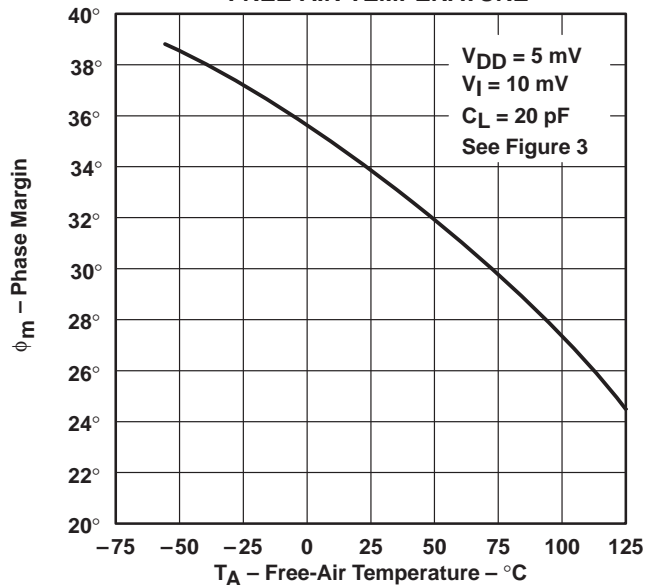


Figure 35

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

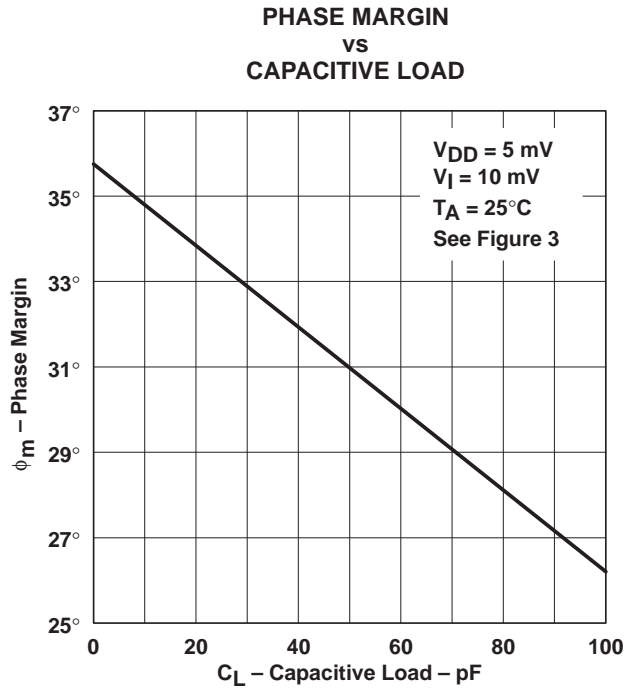


Figure 36

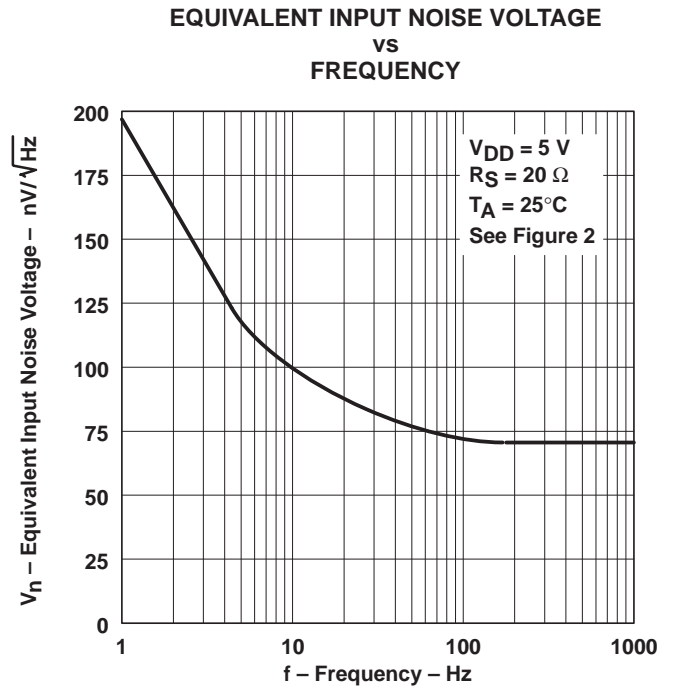


Figure 37

APPLICATION INFORMATION

single-supply operation

While the TLC27L4 and TLC27L9 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC27L4 and TLC27L9 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27L4 and TLC27L9 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.

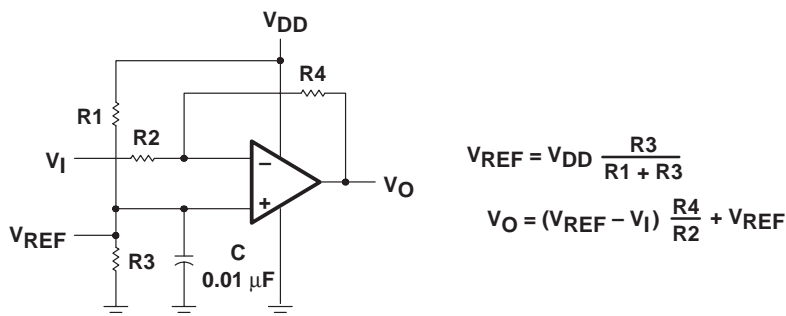


Figure 38. Inverting Amplifier With Voltage Reference

APPLICATION INFORMATION

single-supply operation (continued)

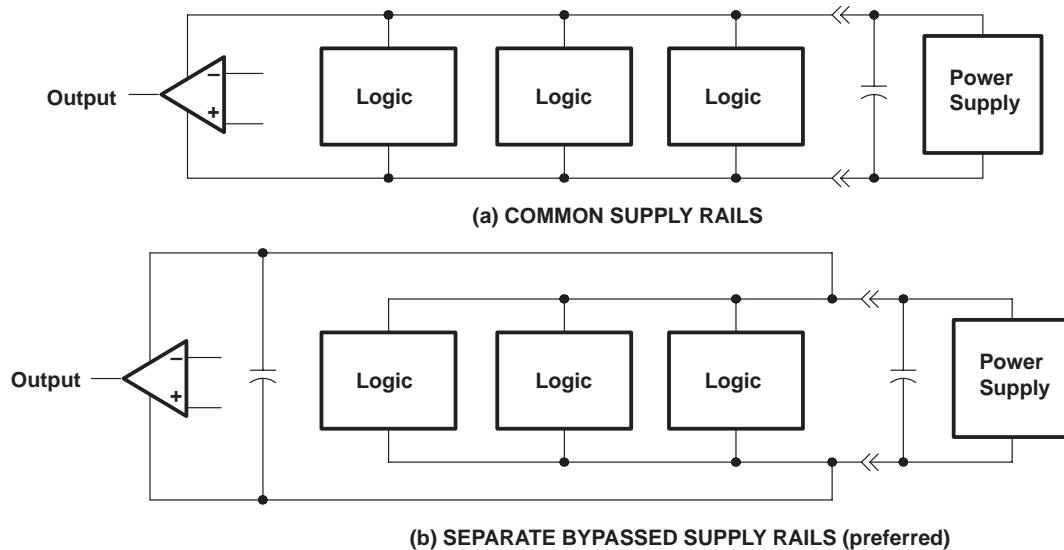


Figure 39. Common Versus Separate Supply Rails

input characteristics

The TLC27L4 and TLC27L9 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1\text{ V}$ at $T_A = 25^\circ\text{C}$ and at $V_{DD} - 1.5\text{ V}$ at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLC27L4 and TLC27L9 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically $0.1\ \mu\text{V}/\text{month}$, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27L4 and TLC27L9 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27L4 and TLC27L9 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than $50\ \text{k}\Omega$, since bipolar devices exhibit greater noise currents.

APPLICATION INFORMATION

noise performance (continued)

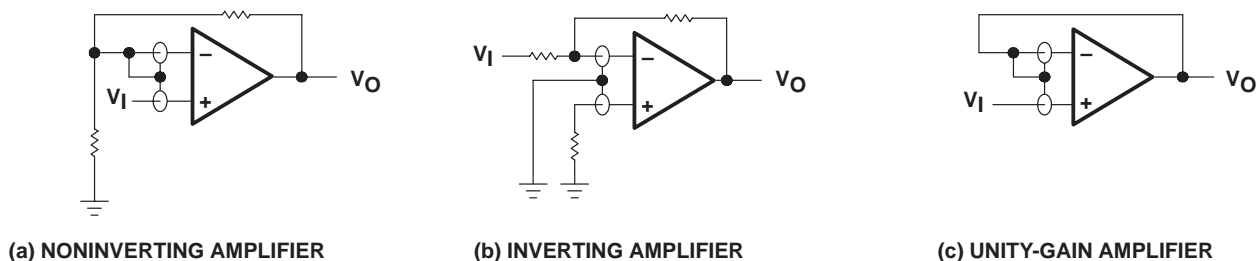


Figure 40. Guard-Ring Schemes

output characteristics

The output stage of the TLC27L4 and TLC27L9 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC27L4 and TLC27L9 were measured using a 20-pF load. The devices drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance alleviates the problem.

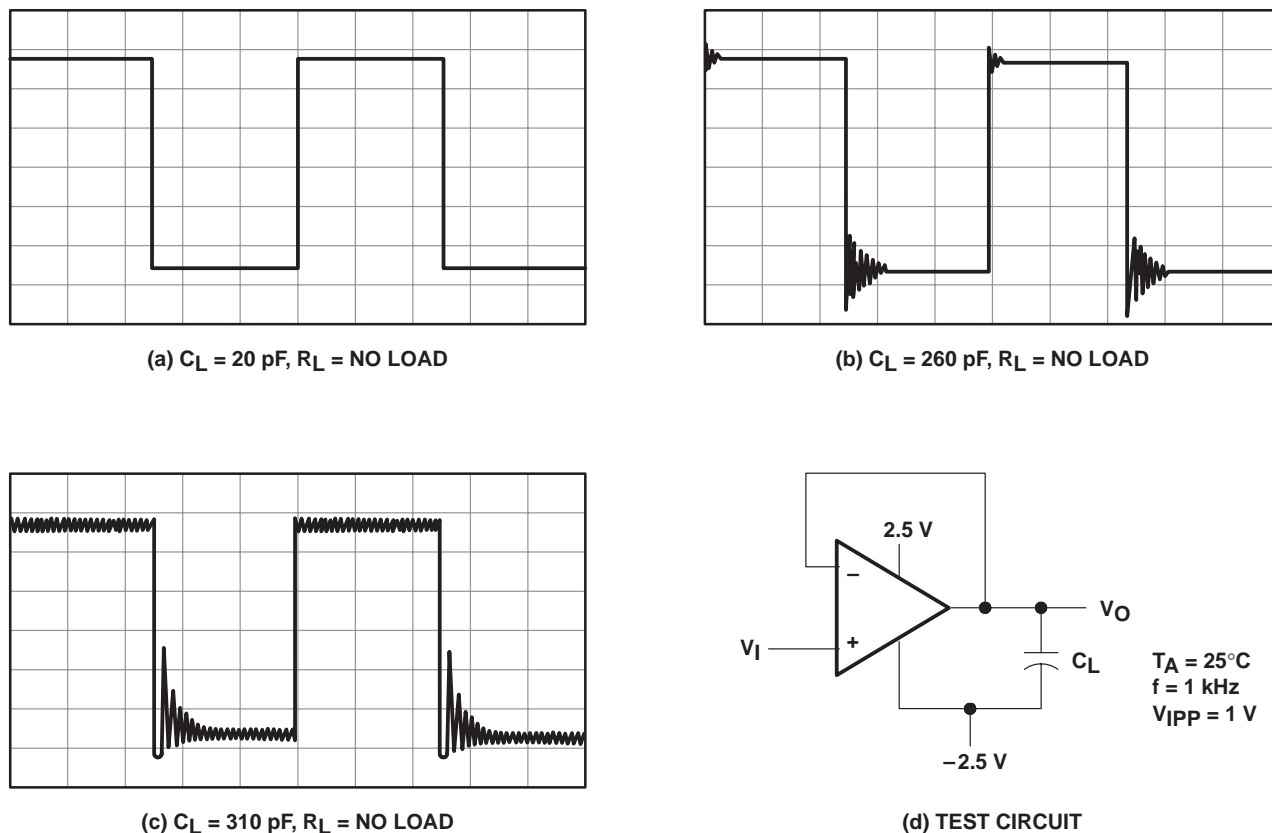


Figure 41. Effect of Capacitive Loads and Test Circuit

APPLICATION INFORMATION

output characteristics (continued)

Although the TLC27L4 and TLC27L9 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω , depending on how hard the operational amplifier input is driven. With very low values of R_P , a voltage offset from 0 V at the output occurs. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

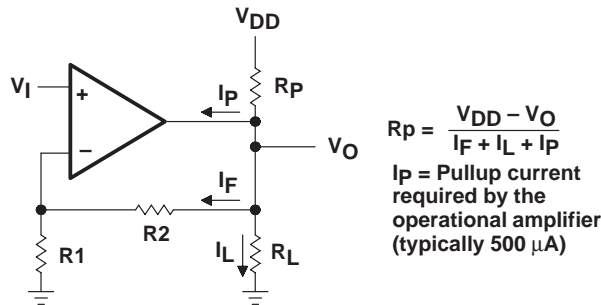


Figure 42. Resistive Pullup to Increase V_{OH}

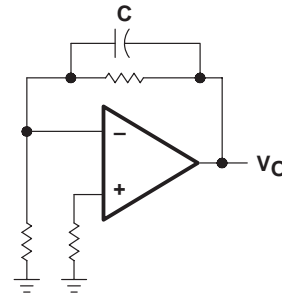


Figure 43. Compensation for Input Capacitance

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

The TLC27L4 and TLC27L9 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices, as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC27L4 and TLC27L9 inputs and outputs were designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

APPLICATION INFORMATION

latch-up (continued)

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

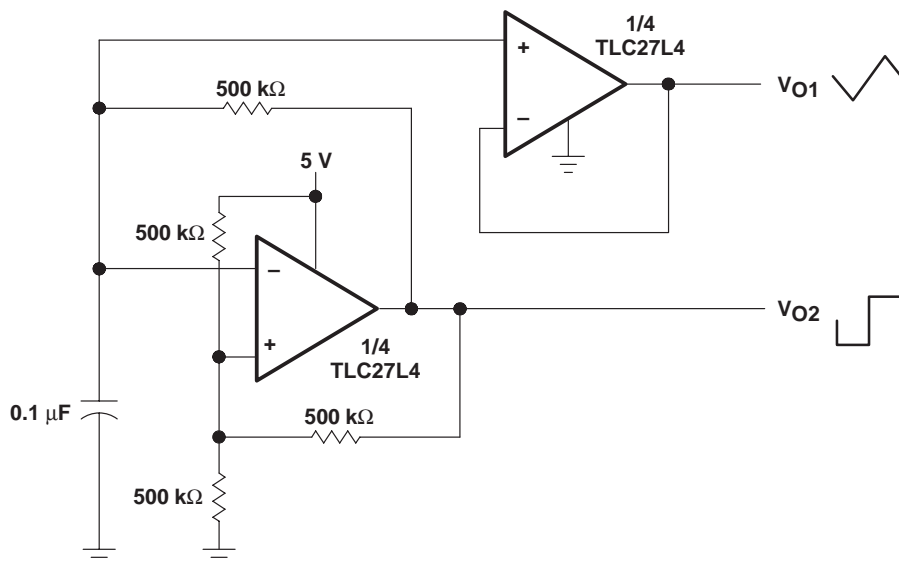
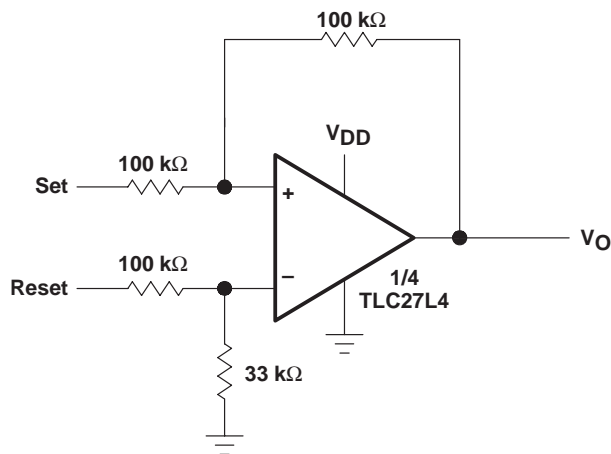


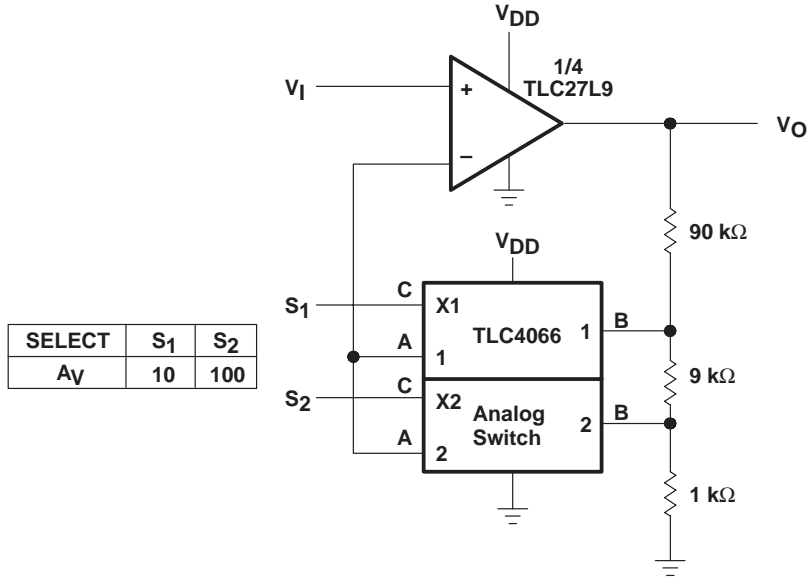
Figure 44. Multivibrator



NOTE: V_{DD} = 5 V to 16 V

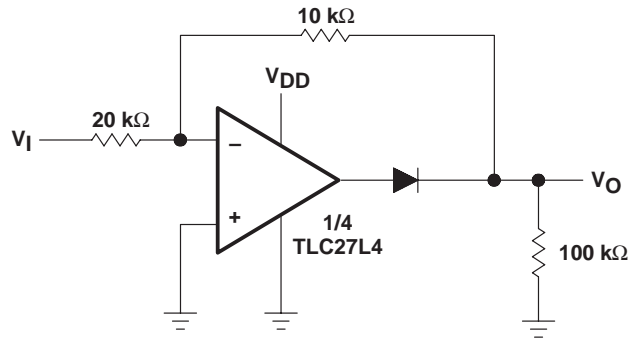
Figure 45. Set/Reset Flip-Flop

APPLICATION INFORMATION



NOTE: V_{DD} = 5 V to 12 V

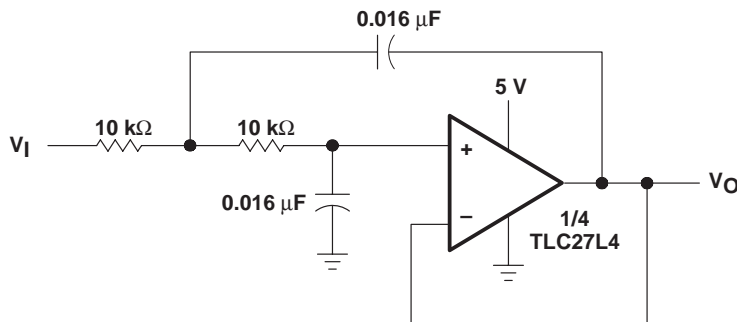
Figure 46. Amplifier With Digital Gain Selection



NOTE: V_{DD} = 5 V to 16 V

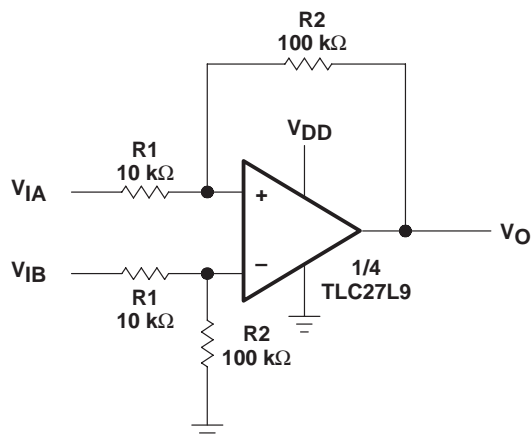
Figure 47. Full-Wave Rectifier

APPLICATION INFORMATION



NOTE: Normalized to $F_C = 1 \text{ kHz}$ and $R_L = 10 \text{ k}\Omega$

Figure 48. Two-Pole Low-Pass Butterworth Filter



NOTE: $V_{DD} = 5 \text{ V to } 16 \text{ V}$

$$V_O = \frac{R_2}{R_1}(V_{IB} - V_{IA})$$

Figure 49. Difference Amplifier

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC27L4ACDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L4AC	Samples
TLC27L4AIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L4AI	Samples
TLC27L4AIN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TLC27L4AIN	Samples
TLC27L4BCDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L4BC	Samples
TLC27L4BIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L4BI	Samples
TLC27L4BIDRG4	ACTIVE	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 85		Samples
TLC27L4CDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC27L4C	Samples
TLC27L4CN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC27L4CN	Samples
TLC27L4CNS	ACTIVE	SO	NS	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC27L4	Samples
TLC27L4CNSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC27L4	Samples
TLC27L4CPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27L4C	Samples
TLC27L4CPWRG4	LIFEBUY	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	P27L4C	
TLC27L4IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC27L4I	Samples
TLC27L4IN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TLC27L4IN	Samples
TLC27L4INE4	ACTIVE	PDIP	N	14	25	TBD	Call TI	Call TI	-40 to 85		Samples
TLC27L4IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	P27L4I	Samples
TLC27L9CDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC27L9C	Samples
TLC27L9CN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC27L9CN	Samples
TLC27L9CNSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC27L9	Samples
TLC27L9IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC27L9I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC27L9IN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TLC27L9IN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

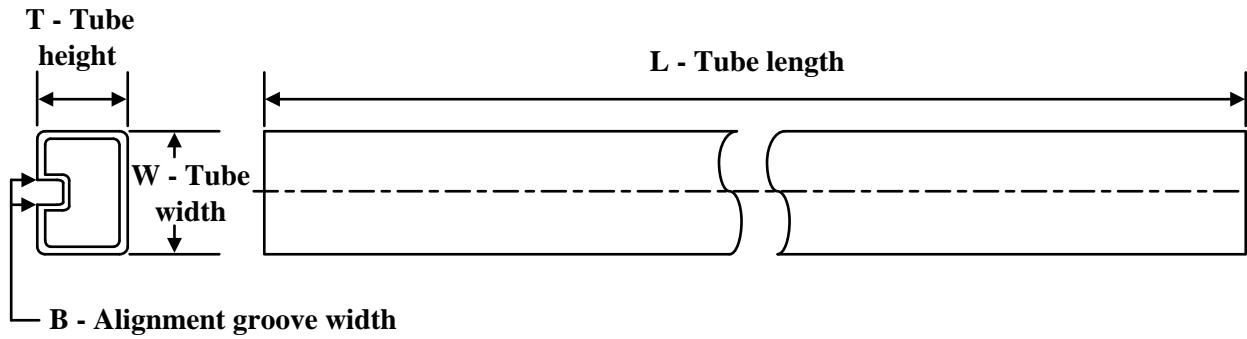

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC27L4ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC27L4ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC27L4AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC27L4BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC27L4BIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC27L4CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC27L4CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC27L4CNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TLC27L4CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC27L4IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC27L4IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC27L9CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC27L9CNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TLC27L9IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC27L4ACDR	SOIC	D	14	2500	350.0	350.0	43.0
TLC27L4ACDR	SOIC	D	14	2500	340.5	336.1	32.0
TLC27L4AIDR	SOIC	D	14	2500	356.0	356.0	35.0
TLC27L4BCDR	SOIC	D	14	2500	367.0	367.0	38.0
TLC27L4BIDR	SOIC	D	14	2500	356.0	356.0	35.0
TLC27L4CDR	SOIC	D	14	2500	367.0	367.0	38.0
TLC27L4CDR	SOIC	D	14	2500	333.2	345.9	28.6
TLC27L4CNSR	SO	NS	14	2000	356.0	356.0	35.0
TLC27L4CPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TLC27L4IDR	SOIC	D	14	2500	367.0	367.0	38.0
TLC27L4IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TLC27L9CDR	SOIC	D	14	2500	350.0	350.0	43.0
TLC27L9CNSR	SO	NS	14	2000	356.0	356.0	35.0
TLC27L9IDR	SOIC	D	14	2500	350.0	350.0	43.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLC27L4AIN	N	PDIP	14	25	506	13.97	11230	4.32
TLC27L4CN	N	PDIP	14	25	506	13.97	11230	4.32
TLC27L4CNS	NS	SOP	14	50	530	10.5	4000	4.1
TLC27L4IN	N	PDIP	14	25	506	13.97	11230	4.32
TLC27L9CN	N	PDIP	14	25	506	13.97	11230	4.32
TLC27L9IN	N	PDIP	14	25	506	13.97	11230	4.32

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