



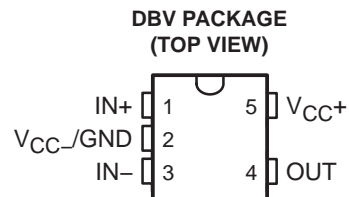
THE DATASHEET OF TL3431DBVR



TL343 SINGLE LOW-POWER OPERATIONAL AMPLIFIER

SLOS250G – JUNE 1999 – REVISED JANUARY 2005

- Wide Range of Supply Voltages, Single Supply 3 V to 30 V, or Dual Supplies
- Class AB Output Stage
- True Differential-Input Stage
- Low Input Bias Current
- Internal Frequency Compensation
- Short-Circuit Protection



description/ordering information

The TL343 is a single operational amplifier similar in performance to the μ A741, but with several distinct advantages. It is designed to operate from a single supply over a range of voltages from 3 V to 30 V. Operation from split supplies also is possible, provided the difference between the two supplies is 3 V to 30 V. The common-mode input range includes the negative supply. Output range is from the negative supply to $V_{CC} - 1.5$ V.

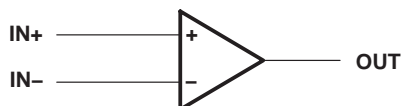
ORDERING INFORMATION

T_A	$V_{IO\text{MAX}}$ AT 25°C	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
–40°C to 125°C	10 mV	SOT-23-5 (DBV)	Reel of 3000	TL343IDBVR
			Reel of 250	TL343IDBVT
				T4I_

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ The actual top-side marking has one additional character that designates the assembly/test site.

symbol



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

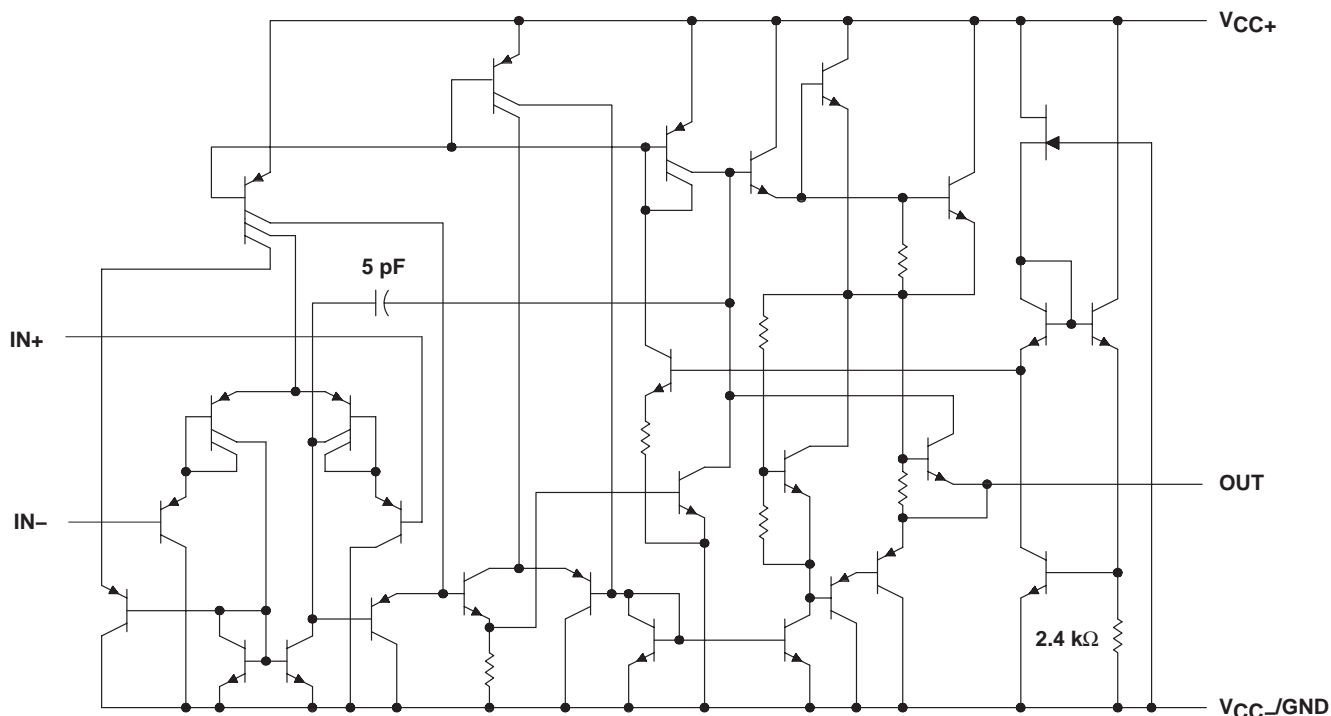
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TL343 SINGLE LOW-POWER OPERATIONAL AMPLIFIER

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schematic



NOTE A: Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	MAX	UNIT
Supply voltage (see Note 1)	V _{CC+}	18
	V _{CC-}	-18
Supply voltage, V _{CC+} with respect to V _{CC-}	36	V
Differential input voltage (see Note 2)	±36	V
Input voltage (see Notes 1 and 3)	±18	V
Package thermal impedance, θ_{JA} (see Notes 4 and 5)	206	°C/W
Operating virtual junction temperature, T _J	150	°C
Storage temperature range, T _{stg}	-65 to 150	°C

- NOTES:
1. These voltage values are with respect to the midpoint between V_{CC+} and V_{CC-}.
 2. Differential voltages are at IN+ with respect to IN-.
 3. Neither input must ever be more positive than V_{CC+} or more negative than V_{CC-}.
 4. Maximum power dissipation is a function of T_{J(max)}, θ_{JA} , and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A) / \theta_{JA}$. Selecting the maximum of 150°C can affect reliability.
 5. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Single-supply voltage	3	30	V
V_{CC+}	Dual-supply voltage	1.5	15	V
V_{CC-}		-1.5	-15	
T_A	Operating free-air temperature	-40	125	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER	TEST CONDITION [†]	MIN	TYP	MAX	UNIT		
V_{IO}	Input offset voltage	See Note 6	25°C	2	10	mV	
			Full range		12		
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage	See Note 6	Full range	10		$\mu\text{V}/^\circ\text{C}$	
I_{IO}	Input offset current	See Note 6	25°C	30	50	nA	
			Full range		200		
$\alpha_{I_{IO}}$	Temperature coefficient of input offset current	See Note 6	Full range	50		$\text{pA}/^\circ\text{C}$	
I_{IB}	Input bias current	See Note 6	25°C	-200	-500	nA	
			Full range		-800		
V_{ICR}	Common-mode input voltage range [‡]		25°C	V_{CC-} to 13	V_{CC-} to 13.5	V	
V_{OM}	Peak output-voltage swing	$R_L = 10\text{ k}\Omega$	25°C	± 12	± 13.5	V	
			25°C	± 10	± 13		
			Full range	± 10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10\text{ V}$, $R_L = 2\text{ k}\Omega$	25°C	20	200	V/mV	
			Full range	15			
B_{OM}	Maximum-output-swing bandwidth	$V_{OPP} = 20\text{ V}$, THD $\leq 5\%$,	25°C	9		kHz	
		$A_{VD} = 1$, $R_L = 2\text{ k}\Omega$					
B_1	Unity-gain bandwidth	$V_O = 50\text{ mV}$, $R_L = 10\text{ k}\Omega$	25°C	1		MHz	
ϕ_m	Phase margin	$C_L = 200\text{ pF}$, $R_L = 2\text{ k}\Omega$	25°C	44		Deg	
r_i	Input resistance	$f = 20\text{ Hz}$	25°C	0.3	1	$\text{M}\Omega$	
r_o	Output resistance	$f = 20\text{ Hz}$	25°C	75		Ω	
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}(\text{min})$	25°C	70	90	dB	
k_{SVS}	Supply-voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC\pm} = \pm 2.5$ to $\pm 15\text{ V}$	25°C	30	150	$\mu\text{V}/\text{V}$	
I_{OS}	Short-circuit output current [§]		25°C	± 10	± 30	± 55	mA
I_{CC}	Total supply current	No load, See Note 6	25°C	0.7	2.8	mA	

[†] All characteristics are measured under open-loop conditions, with zero common-mode voltage, unless otherwise specified. Full range for T_A is -40°C to 125°C .

[‡] The V_{ICR} limits are linked directly, volt-for-volt, to supply voltage; the positive limit is 2 V less than V_{CC+} .

[§] Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

NOTE 6: V_{IO} , I_{IO} , I_{IB} , and I_{CC} are defined at $V_O = 0$.



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electrical characteristics, $V_{CC+} = 3\text{ V}$ and 5 V , $V_{CC-} = 0\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITION†	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage	$V_O = 1.5\text{ V}$ and 2.5 V		2	10	mV
I_{IO} Input offset current	$V_O = 1.5\text{ V}$ and 2.5 V		30	50	nA
I_{IB} Input bias current	$V_O = 1.5\text{ V}$ and 2.5 V		-200	-500	nA
V_{OM} Peak output voltage swing‡	$R_L = 10\text{ k}\Omega$	3.3	3.5		V
A_{VD} Large-signal differential voltage amplification	$V_O = 1.7\text{ V}$ to 3.3 V , $R_L = 2\text{ k}\Omega$	20	200		V/mV
k_{SVS} Supply-voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC\pm}$)	$V_{CC\pm} = \pm 2.5\text{ V}$ to $\pm 15\text{ V}$			150	$\mu\text{V}/\text{V}$
I_{CC} Supply current	$V_O = 1.5\text{ V}$ and 2.5 V , No load		0.7	1.75	mA

† All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified.

‡ Output swings essentially to ground.

operating characteristics, $V_{CC\pm} = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, $A_{VD} = 1$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	UNIT
SR Slew rate at unity gain	$V_I = \pm 10\text{ V}$, $C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$, See Figure 1	1	$\text{V}/\mu\text{s}$
t_r Rise time	$\Delta V_O = 50\text{ mV}$, $C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$, See Figure 1	0.35	μs
t_f Fall time	$\Delta V_O = 50\text{ mV}$, $C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$, See Figure 1	0.35	μs
Overshoot factor	$\Delta V_O = 50\text{ mV}$, $C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$, See Figure 1	20%	
Crossover distortion	$V_{I(PP)} = 30\text{ mV}$, $V_{OPP} = 2\text{ V}$, $f = 10\text{ kHz}$	1%	

PARAMETER MEASUREMENT INFORMATION

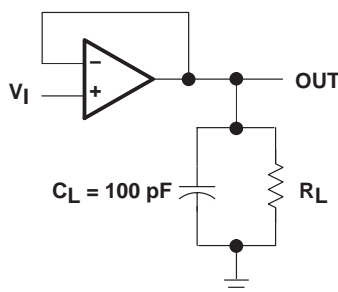


Figure 1. Unity-Gain Amplifier

TYPICAL CHARACTERISTICS†

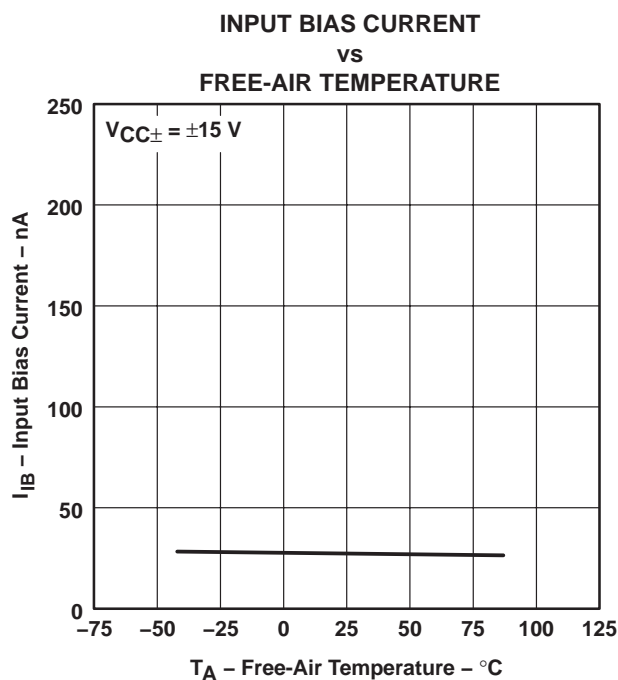


Figure 2

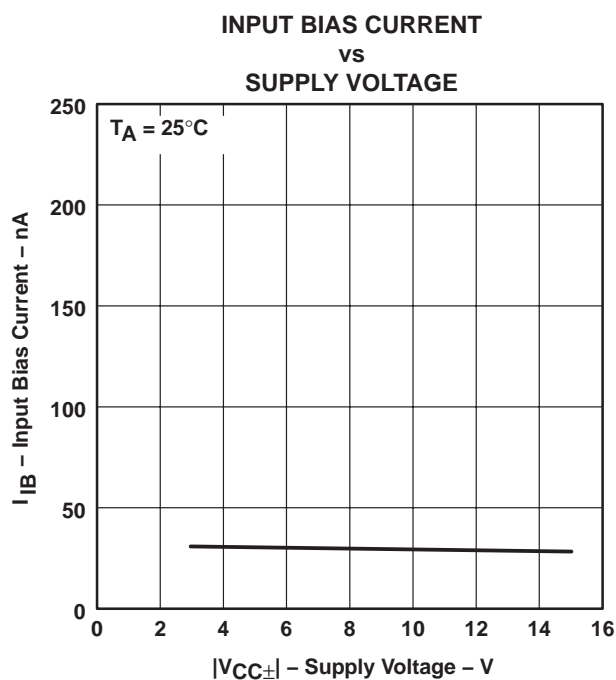


Figure 3

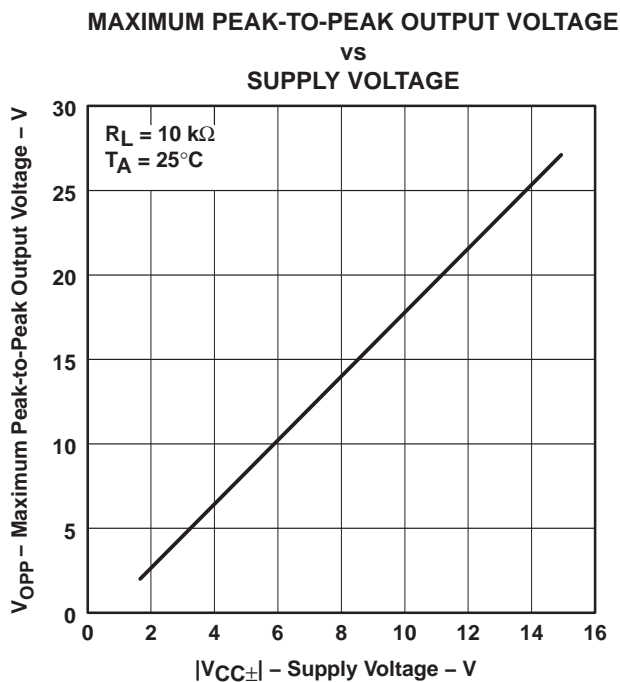


Figure 4

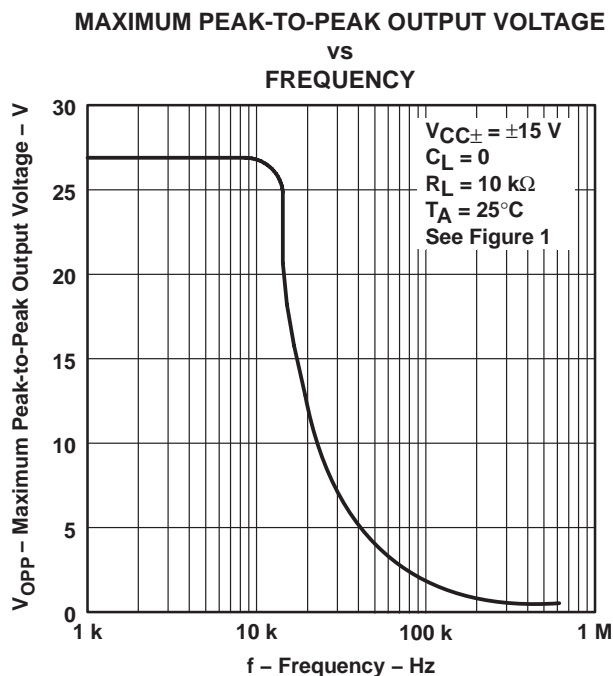


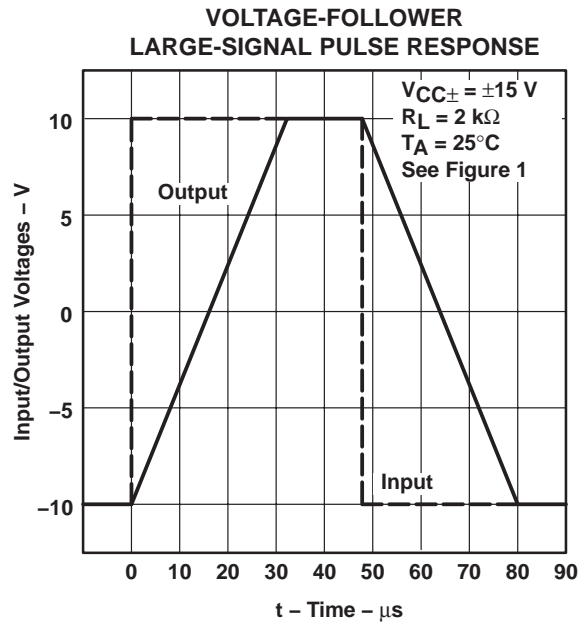
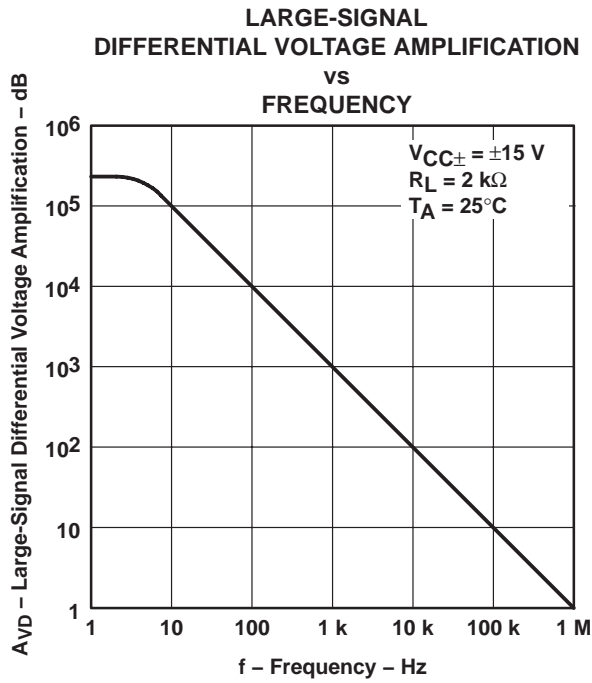
Figure 5

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

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TYPICAL CHARACTERISTICS†



† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL3431DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 125	(T4IG, T4IL, T4IS)	Samples
TL3431DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 125	(T4IG, T4IL, T4IU)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL343IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TL343IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TL343IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL343IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TL343IDBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
TL343IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

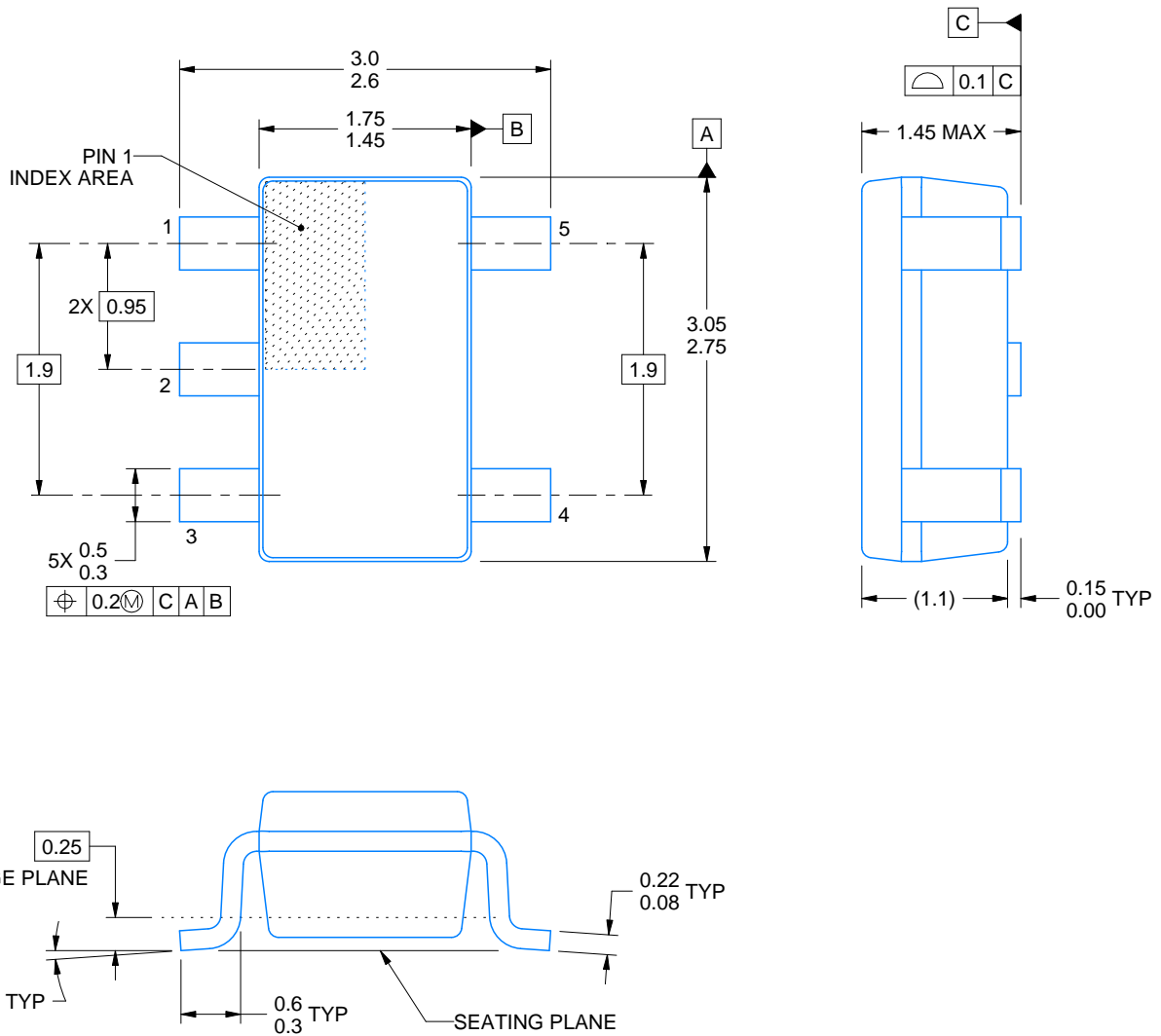
DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/D 11/2018

NOTES:

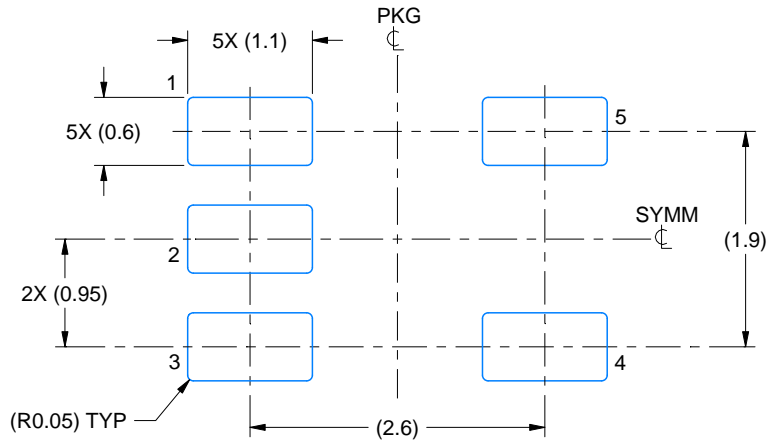
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

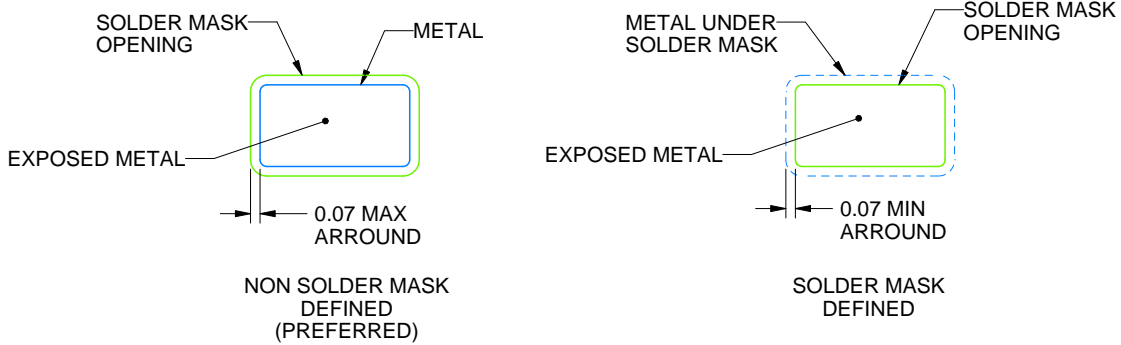
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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