



**THE DATASHEET OF  
TL33072AD**

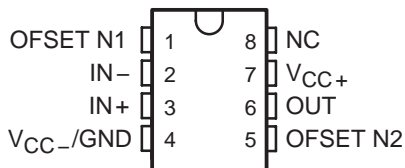


# TL3x071, TL3x071A, TL3x072, TL3x072A, TL3x074, TL3x074A HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

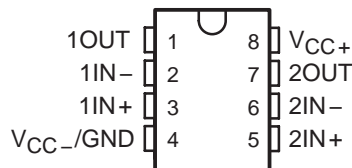
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- Wide Gain-Bandwidth Product . . . 4.5 MHz
- High Slew Rate . . . 13 V/ $\mu$ s
- Fast Settling Time . . . 1.1  $\mu$ s to 0.1%
- Wide-Range Single-Supply Operation  
4 V to 44 V
- Wide Input Common-Mode Range Includes  
Ground ( $V_{CC-}$ )
- Low Total Harmonic Distortion . . . 0.02%
- Low Input Offset Voltage . . . 3 mV Max  
(A Suffix)
- Large Output Voltage Swing  
–14.7 V to 14 V (With  $\pm$ 15-V Supplies)
- Large Capacitance Drive Capability  
10,000 pF
- Excellent Phase Margin . . . 60°
- Excellent Gain Margin . . . 12 dB
- Output Short-Circuit Protection

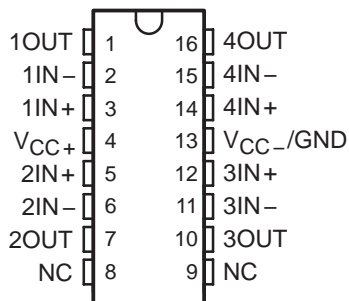
D OR P PACKAGE  
(SINGLE, TOP VIEW)



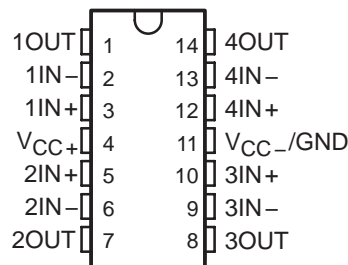
D OR P PACKAGE  
(DUAL, TOP VIEW)



DW PACKAGE  
(QUAD, TOP VIEW)



N PACKAGE  
(QUAD, TOP VIEW)



NC – No internal connection

## AVAILABLE OPTIONS

T <sub>A</sub>	COMPLEXITY	PACKAGE			
		PLASTIC DIP		SMALL OUTLINE	
		STANDARD GRADE	PRIME GRADE	STANDARD GRADE	PRIME GRADE
0°C to 70°C	Single Dual Quad	TL34071P TL34072P TL34074N	TL34071AP TL34072AP TL34074AN	TL34071D TL34072D TL34074DW	TL34071AD TL34072AD TL34074ADW
–40°C to 105°C	Single Dual Quad	TL33071P TL33072P TL33074N	TL33071AP TL33072AP TL33074AN	TL33071D TL33072D TL33074DW	TL33071AD TL33072AD TL33074ADW
–55°C to 125°C	Single Dual Quad	TL35071P TL35072P TL35074N	TL35071AP TL35072AP TL35074AN	TL35071D TL35072D TL35074DW	TL35071AD TL35072AD TL35074ADW

D and DW packages are available taped and reeled. Add R suffix to device type (e.g., TL34071ADR).



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# TL3x071, TL3x071A, TL3x072, TL3x072A, TL3x074, TL3x074A HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

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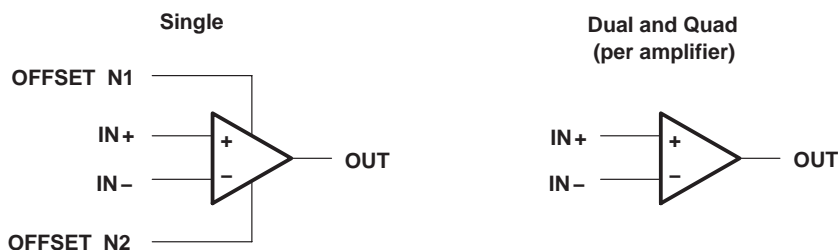
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## description

Quality, low cost, bipolar fabrication with innovative design concepts are employed for the TL33071/2/4, TL34071/2/4, and TL35071/2/4 series of monolithic operational amplifiers. This series of operational amplifiers offers 4.5 MHz of gain bandwidth product, 13 V/ $\mu$ s slew rate, and fast settling time without the use of JFET device technology. Although this series can be operated from split supplies, it is particularly suited for single-supply operation since the common-mode input voltage range includes ground potential ( $V_{CC-}$ ). With a Darlington transistor input stage, this series exhibits high input resistance, low input offset voltage, and high gain. The all-npn output stage, characterized by no dead-band crossover distortion and large output voltage swing, provides high-capacitance drive capability, excellent phase and gain margins, low open-loop high-frequency output impedance, and symmetrical source/sink ac frequency response.

The TL34071/2/4 devices are available in standard or prime performance (A-suffix) grades and are specified over the commercial (0°C to 70°C) temperature range. The TL33071/2/4 devices are available in standard or prime performance (A-suffix) grades and are specified over industrial/vehicular (-40°C to 105°C) temperature range. The TL35071/2/4 devices are available in standard or prime performance (A-suffix) grades and are specified over the military (-55°C to 125°C) temperature range. These low-cost amplifiers are available in single, dual, and quad configurations and are pin compatible with the MC33071/2/4, MC34071/2/4, and MC35071/2/4 series of amplifiers. Packaging options include standard plastic DIP and SO packages.

## symbol



# TL3x071, TL3x071A, TL3x072, TL3x072A, TL3x074, TL3x074A HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC+}$ (see Note 1)	22 V
Supply voltage, $V_{CC-}$	–22 V
Differential input voltage, $V_{ID}$ (see Note 2)	±44 V
Input voltage, $V_I$ (any input)	$V_{CC\pm}$
Input current, $I_I$ (each input)	±1 mA
Output current, $I_O$	±80 mA
Total current into $V_{CC+}$	80 mA
Total current out of $V_{CC-}$	80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$ : TL3307x	–40°C to 105°C
TL3407x	0°C to 70°C
TL3507x	–55°C to 125°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds: D, DW, N, or P package	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between  $V_{CC+}$  and  $V_{CC-}$ .
  2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows if input is brought below  $V_{CC-} - 0.3$  V.
  3. The output can be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$	$T_A = 105^\circ\text{C}$	$T_A = 125^\circ\text{C}$
	POWER RATING		POWER RATING	POWER RATING	POWER RATING
D	725 mW	5.8 mW/°C	464 mW	261 mW	145 mW
DW	1025 mW	8.2 mW/°C	656 mW	369 mW	205 mW
N	1150 mW	9.2 mW/°C	736 mW	414 mW	230 mW
P	1000 mW	8.0 mW/°C	640 mW	360 mW	200 mW

## recommended operating conditions

		TL3307x		TL3407x		TL3507x		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±2	±22	±2	±22	±2	±22	V
Common-mode input voltage, $V_{IC}$	$V_{CC} = 5$ V	0	2.7	0	2.9	0	2.7	V
	$V_{CC\pm} = \pm 15$ V	–15	12.7	–15	12.9	–15	12.7	
Operating free-air temperature, $T_A$		–40	105	0	70	–55	125	°C



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electrical characteristics at specified free-air temperature,  $V_{CC\pm} = \pm 15\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A$ †	TL3x07xA			TL3x07x			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IO}$ Input offset voltage	$V_{CC} = 5\text{ V}$	25°C	0.5	3		1.5	5	mV	
		25°C	0.5	3		1.0	5		
$\alpha V_{IO}$ Temperature coefficient of input offset voltage	$V_{IC} = 0,$ $V_O = 0,$ $R_S = 50\ \Omega$	Full range				7			$\mu\text{V}/^\circ\text{C}$
			$V_{CC} = \pm 15\text{ V}$	Full range	10			10	
$I_{IO}$ Input offset current	$V_{CC} = \pm 15\text{ V}$	25°C	7	100		7	100	nA	
		Full range				250			
$I_{IB}$ Input bias current	$V_{CC} = 5\text{ V}$	25°C	-0.8	-2		-0.8	-2	$\mu\text{A}$	
		Full range				-2.3			
	$V_{CC} = \pm 15\text{ V}$	25°C	-0.7	-1.5		-0.7	-1.5		
		Full range				-1.8			
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	-15 to 13.2			-15 to 13.2		V	
		Full range	-15 to 12.8			-15 to 12.8			
$V_{OH}$ High-level output voltage	$V_{CC+} = 5\text{ V}, V_{CC-} = 0,$ $R_L = 2\text{ k}\Omega$	25°C	3.7	4		3.7	4	V	
	$R_L = 10\text{ k}\Omega$	25°C	13.6	14		13.6	14		
	$R_L = 2\text{ k}\Omega$	Full range	13.4			13.4			
$V_{OL}$ Low-level output voltage	$V_{CC+} = 5\text{ V}, V_{CC-} = 0,$ $R_L = 2\text{ k}\Omega$	25°C	0.1	0.3		0.1	0.3	V	
	$R_L = 10\text{ k}\Omega$	25°C	-14.7	-14.3		-14.7	-14.3		
	$R_L = 2\text{ k}\Omega$	Full range	-13.5			-13.5			
$AVD$ Large-signal differential voltage amplification	$V_O = \pm 10\text{ V}, R_L = 2\text{ k}\Omega$	25°C	50	100		25	100	V/mV	
		Full range	25			20			
$I_{OS}$ Short-circuit output current	Source: $V_{ID} = 1\text{ V}, V_O = 0$	25°C	-10	-30		-10	-30	mA	
	Sink: $V_{ID} = -1\text{ V}, V_O = 0$		20	30		20	30		
$CMRR$ Common-mode rejection ratio	$V_{IC} = V_{ICRmin},$ $R_S = 50\ \Omega$	25°C	80	97		70	97	dB	
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC\pm} = \pm 13.5\text{ V}$ to $\pm 16.5\text{ V}, R_S = 100\ \Omega$	25°C	80	97		70	97	dB	
$I_{CC}$ Supply current (per channel)	$V_O = 0,$ No Load	25°C	3.5	4.5		3.5	4.5	mA	
		Full range	4.7			4.7			
	$V_{CC+} = 5\text{ V}, V_{CC-} = 0,$ $V_O = 0,$ No Load	25°C	3.4	4.4		3.4	4.4		
		Full range	4.6			4.6			

† Full range is 0°C to 70°C for the TL3407x devices, and -40°C to 105°C for the TL3307x devices, and -55°C to 125°C for the TL3507x devices.  
‡ All typical values are at  $T_A = 25^\circ\text{C}$ .



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operating characteristics,  $V_{CC\pm} = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TL3x07xA			TL3x07x			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_I = -10\text{ V to }10\text{ V}$ , $R_L = 2\text{ k}\Omega$	$A_V = 1$	8	10		8	10	V/ $\mu\text{s}$	
SR-	Negative slew rate		$A_V = -1$		13			13		
$t_s$	Settling time	$A_{VD} = -1$ , 10-V step	$T_o = 0.1\%$		1.1			1.1	$\mu\text{s}$	
			$T_o = 0.01\%$		2.2			2.2		
$V_n$	Equivalent input noise voltage	$f = 1\text{ kHz}$ , $R_S = 100\ \Omega$		32			32	nV/ $\sqrt{\text{Hz}}$		
$I_n$	Equivalent input noise current	$f = 1\text{ kHz}$		0.22			0.22	pA/ $\sqrt{\text{Hz}}$		
THD	Total harmonic distortion	$V_O = 2\text{ V to }20\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $A_{VD} = 10$ , $f = 10\text{ kHz}$		0.02			0.02	%		
GBW	Gain-bandwidth product	$f = 100\text{ kHz}$	3.5	4.5		3.5	4.5	MHz		
BW	Power bandwidth	$R_L = 2\text{ k}\Omega$ , $V_{O(PP)} = 20\text{ V}$ , $A_{VD} = 1$ , THD = 5.0%		200			200	kHz		
$\phi_m$	Phase margin	$R_L = 2\text{ k}\Omega$ , $C_L = 0$		60°			60°			
		$R_L = 2\text{ k}\Omega$ , $C_L = 300\text{ pF}$		40°			40°			
	Gain margin	$R_L = 2\text{ k}\Omega$ , $C_L = 0$		12			12	dB		
		$R_L = 2\text{ k}\Omega$ , $C_L = 300\text{ pF}$		4			4			
$r_i$	Differential input resistance	$V_{IC} = 0$		150			150	M $\Omega$		
$C_i$	Input capacitance	$V_{IC} = 0$		2.5			2.5	pF		
	Channel separation	$f = 10\text{ kHz}$		120			120	dB		
$z_o$	Open-loop output impedance	$f = 1\text{ MHz}$		30			30	$\Omega$		



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL35072P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		TL35072P	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

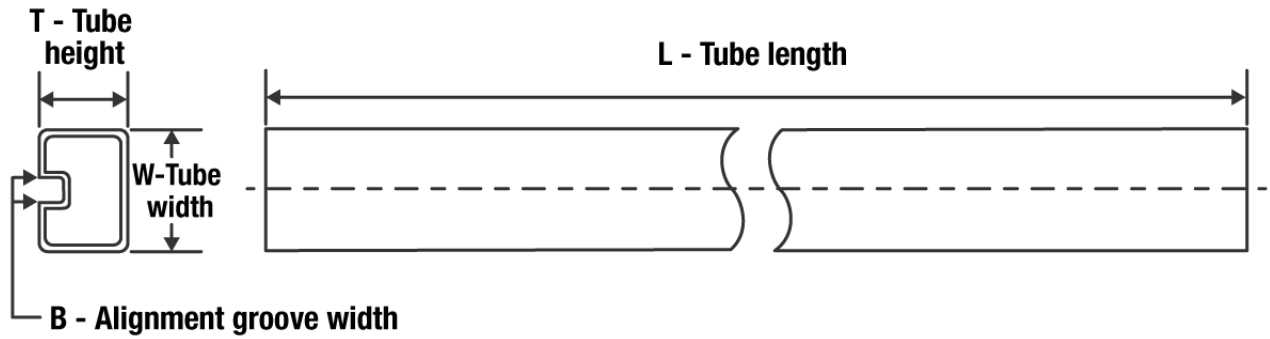
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TL35072P	P	PDIP	8	50	506	13.97	11230	4.32

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