THE DATASHEET OF

TL16C2550PFB

1.8-V to 5-V DUAL UART WITH 16-BYTE FIFOS

Check for Samples: TL16C2550

FEATURES

- **Programmable Auto-RTS and Auto-CTS**
- **In Auto-CTS Mode, CTS Controls Transmitter**
- **In Auto-RTS Mode, RCV FIFO Contents, and Threshold Control RTS**
- **Serial and Modem Control Outputs Drive a RJ11 Cable Directly When Equipment Is on the Same Power Drop**
- **Capable of Running With All Existing TL16C450 Software**
- **After Reset, All Registers Are Identical to the TL16C450 Register Set**
- **Up to 24-MHz Clock Rate for up to 1.5-Mbaud Operation With VCC = 5 V**
- **Up to 20-MHz Clock Rate for up to 1.25-Mbaud Operation With VCC = 3.3 V**
- **Up to 16-MHz Clock Rate for up to 1-Mbaud Operation With VCC = 2.5 V**
- **Up to 10-MHz Clock Rate for up to 625-kbaud Operation With VCC = 1.8 V**
- **In the TL16C450 Mode, Hold and Shift Registers Eliminate the Need for Precise Synchronization Between the CPU and Serial Data**
- **Programmable Baud Rate Generator Allows Division of Any Input Reference Clock by 1 to (2 16 -1) and Generates an Internal 16 × Clock**
- **Standard Asynchronous Communication Bits (Start, Stop, and Parity) Added to or Deleted From the Serial Data Stream**
- **5-V, 3.3-V, 2.5-V, and 1.8-V Operation**
- **Independent Receiver Clock Input**
- **Transmit, Receive, Line Status, and Data Set Interrupts Independently Controlled**
- **Fully Programmable Serial Interface Characteristics:**
  - **5-, 6-, 7-, or 8-Bit Characters**
  - **Even-, Odd-, or No-Parity Bit Generation and Detection**
  - **1-, 1 1/2-, or 2-Stop Bit Generation**
  - **Baud Generation (DC to 1 Mbit/s)**
- **False-Start Bit Detection**
- **Complete Status Reporting Capabilities**
- **3-State Output TTL Drive Capabilities for Bidirectional Data Bus and Control Bus**
- **Line Break Generation and Detection Internal Diagnostic Capabilities:**
  - **Loopback Controls for Communications Link Fault Isolation**
  - **Break, Parity, Overrun, and Framing Error Simulation**
- **Fully Prioritized Interrupt System Controls**
- **Modem Control Functions (CTS, RTS, DSR, DTR, RI, and DCD)**
- **Available in 48-Pin TQFP (PFB) Package, 32-Pin QFN (RHB), or 44-Pin PLCC (FN) Package**
- **Pin Compatible with TL16C752B (48-Pin Package PFB)**

APPLICATIONS

- **Point-of-Sale Terminals**
- **Gaming Terminals**
- **Portable Applications**
- **Router Control**
- **Cellular Data**
- **Factory Automation**

DESCRIPTION

The TL16C2550 is a dual universal asynchronous receiver and transmitter (UART). It incorporates the functionality of two TL16C550D UARTs, each UART having its own register set and FIFOs. The two UARTs share only the data bus interface and clock source, otherwise they operate independently. Another name for the uart function is Asynchronous Communications Element (ACE), and these terms will be used interchangeably. The bulk of this document describes the behavior of each ACE, with the understanding that two such devices are incorporated into the TL16C2550.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

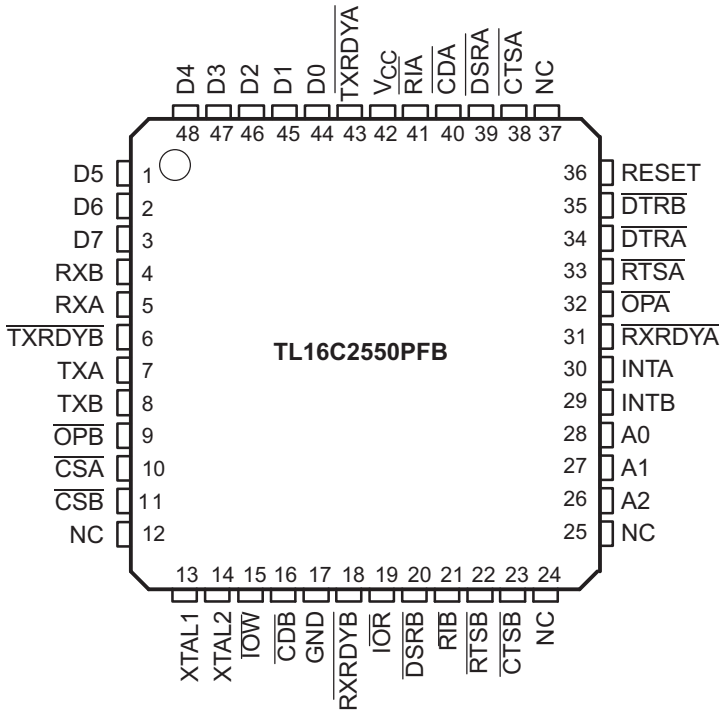
Each ACE is a speed and voltage range upgrade of the TL16C550C, which in turn is a functional upgrade of the TL16C450. Functionally equivalent to the TL16C450 on power up or reset (single character or TL16C450 mode), each ACE can be placed in an alternate FIFO mode. This relieves the CPU of excessive software overhead by buffering received and to be transmitted characters. Each receiver and transmitter store up to 16 bytes in their respective FIFOs, with the receive FIFO including three additional bits per byte for error status. In the FIFO mode, a selectable autoflow control feature can significantly reduce software overload and increase system efficiency by automatically controlling serial data flow using handshakes between the $\overline{RTS}$ output and $\overline{CTS}$ input, thus eliminating overruns in the receive FIFO.

Each ACE performs serial-to-parallel conversions on data received from a peripheral device or modem and stores the parallel data in its receive buffer or FIFO, and each ACE performs parallel-to-serial conversions on data sent from its CPU after storing the parallel data in its transmit buffer or FIFO. The CPU can read the status of either ACE at any time. Each ACE includes complete modem control capability and a processor interrupt system that can be tailored to the application.

Each ACE includes a programmable baud rate generator capable of dividing a reference clock with divisors from 1 to 65535, thus producing a 16× internal reference clock for the transmitter and receiver logic. Each ACE accommodates up to a 1.5-Mbaud serial data rate (24-MHz input clock). As a reference point, that speed would generate a 667-ns bit time and a 6.7-µs character time (for 8,N,1 serial data), with the internal clock running at 24 MHz.

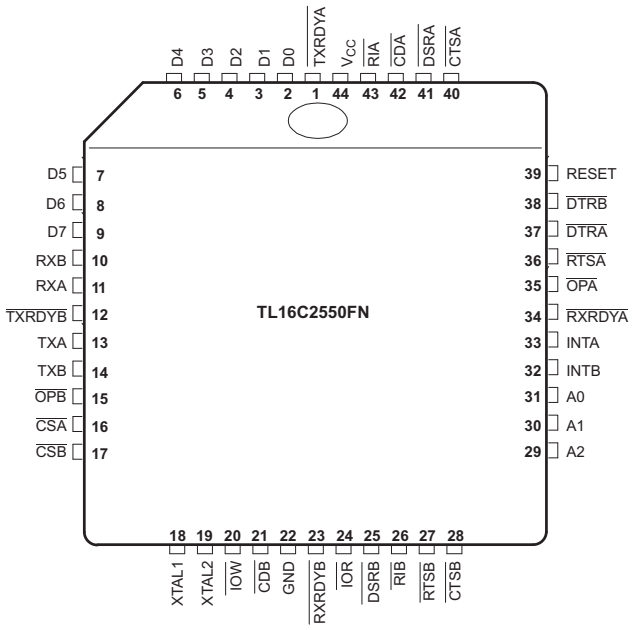
Each ACE has a $\overline{TXRDY}$ and $\overline{RXRDY}$ output that can be used to interface to a DMA controller.

PFB PACKAGE
(TOP VIEW)

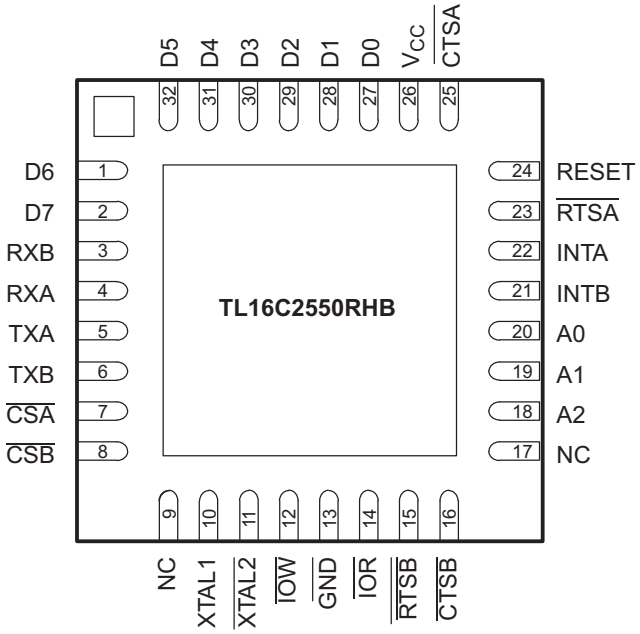


NC - No internal connection

FN PACKAGE
(TOP VIEW)



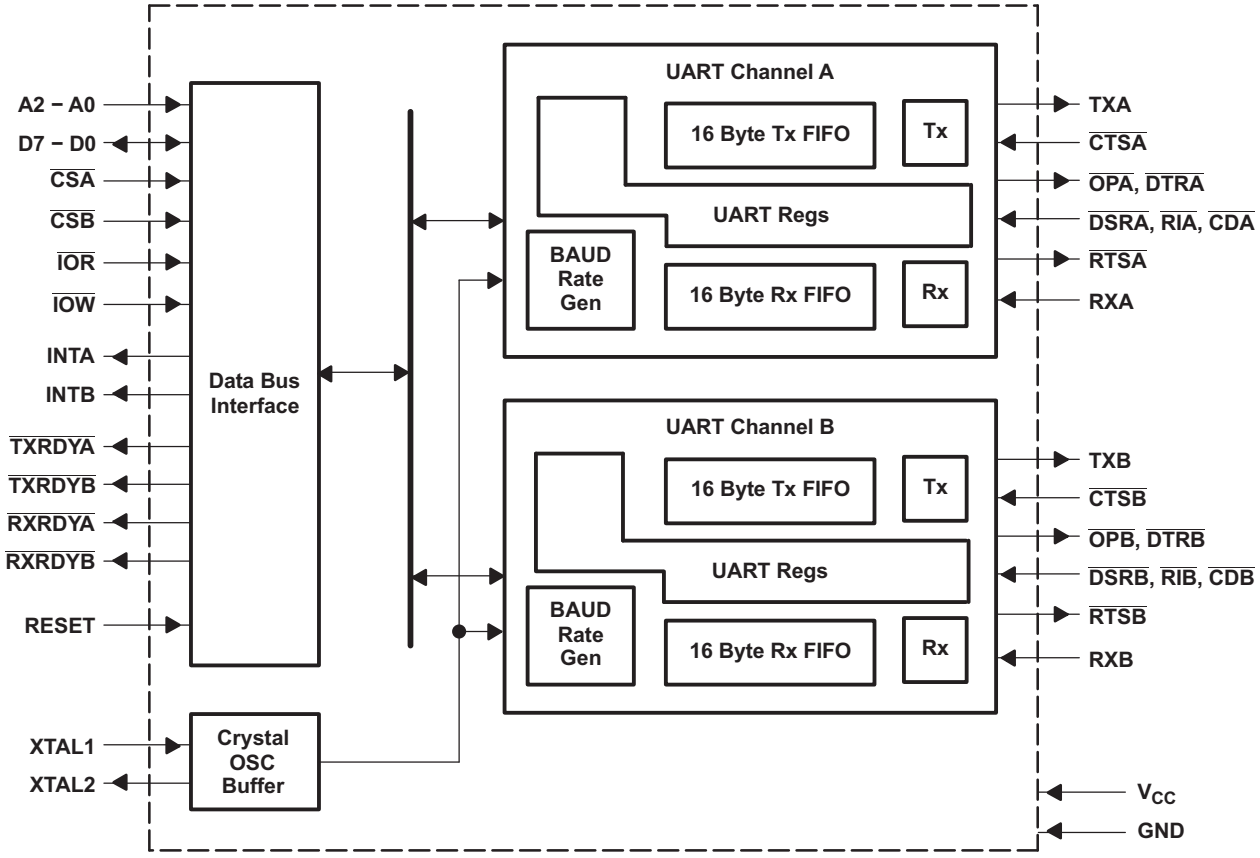
RHB PACKAGE
(TOP VIEW)



NC - No internal connection

The 32-pin RHB package does not provide access to $\overline{\text{DSRA}}$, $\overline{\text{DSRB}}$, $\overline{\text{RIA}}$, $\overline{\text{RIB}}$, $\overline{\text{CDA}}$, $\overline{\text{CDB}}$ inputs, and $\overline{\text{OPA}}$, $\overline{\text{OPB}}$, $\overline{\text{RXRDYA}}$, $\overline{\text{RXRDYB}}$, $\overline{\text{TXRDYA}}$, $\overline{\text{TXRDYB}}$, $\overline{\text{DTRA}}$, $\overline{\text{DTRB}}$ outputs.

TL16C2550 Block Diagram



DEVICE INFORMATION

PIN FUNCTIONS

PIN				I/O	DESCRIPTION
NAME	PFB	FN	RHB		
A0	28	31	20	I	Address 0 select bit. Internal registers address selection
A1	27	30	19	I	Address 1 select bit. Internal registers address selection
A2	26	29	18	I	Address 2 select bit. Internal registers address selection
$\overline{CDA}$, $\overline{CDB}$	40, 16	42, 21	–	I	Carrier detect (active low). These inputs are associated with individual UART channels A and B. A low on these pins indicates that a carrier has been detected by the modem for that channel. The state of these inputs is reflected in the modem status register (MSR).
$\overline{CSA}$, $\overline{CSB}$	10, 11	16, 17	7, 8	I	Chip select A and B (active low). These pins enable data transfers between the user CPU and the TL16C2550 for the channel(s) addressed. Individual UART sections (A, B) are addressed by providing a low on the respective $\overline{CSA}$ and $\overline{CSB}$ pins.
$\overline{CTSA}$, $\overline{CTSB}$	38, 23	40, 28	25, 16	I	Clear to send (active low). These inputs are associated with individual UART channels A and B. A logic low on the CTS pins indicates the modem or data set is ready to accept transmit data from the 2550. Status can be tested by reading MSR bit 4. These pins only affect the transmit and receive operations when auto CTS function is enabled through the enhanced feature register (EFR) bit 7, for hardware flow control operation.

PIN FUNCTIONS (continued)

PIN				I/O	DESCRIPTION
NAME	PFB	FN	RHB		
D0-D4 D5-D7	44 -48 1 -3	2 - 6 7 - 9	27 - 31 32, 1, 2	I/O	Data bus (bidirectional). These pins are the eight bit, 3-state data bus for transferring information to or from the controlling CPU. D0 is the least significant bit and the first data bit in a transmit or receive serial data stream.
$\overline{\text{DSRA}}$, $\overline{\text{DSRB}}$	39, 20	41, 25	–	I	Data set ready (active low). These inputs are associated with individual UART channels A and B. A logic low on these pins indicates the modem or data set is powered on and is ready for data exchange with the UART. The state of these inputs is reflected in the modem status register (MSR).
$\overline{\text{DTRA}}$, $\overline{\text{DTRB}}$	34, 35	37, 38	–	O	Data terminal ready (active low). These outputs are associated with individual UART channels A and B. A logic low on these pins indicates that theTLI16C2550 is powered on and ready. These pins can be controlled through the modem control register. Writing a 1 to MCR bit 0 sets the $\overline{\text{DTR}}$ output to low, enabling the modem. The output of these pins is high after writing a 0 to MCR bit 0, or after a reset.
GND	17	22	13		Signal and power ground.
INTA, INTB	30, 29	33. 32	21. 22	O	Interrupt A and B (active high). These pins provide individual channel interrupts, INT A and B. INT A and B are enabled when MCR bit 3 is set to a logic 1, interrupt sources are enabled in the interrupt enable register (IER). Interrupt conditions include: receiver errors, available receiver buffer data, available transmit buffer space or when a modem status flag is detected. INTA-B are in the high-impedance state after reset.
$\overline{\text{IOR}}$	19	24	14	I	Read input (active low strobe). A high to low transition on $\overline{\text{IOR}}$ will load the contents of an internal register defined by address bits A0-A2 onto the TL16C2550 data bus (D0-D7) for access by an external CPU.
$\overline{\text{IOW}}$	15	20	12	I	Write input (active low strobe). A low to high transition on $\overline{\text{IOW}}$ will transfer the contents of the data bus (D0-D7) from the external CPU to an internal register that is defined by address bits A0-A2 and CSA and CSB
NC	12, 24, 25, 37	–	9 , 17		No internal connection
$\overline{\text{OPA}}$, $\overline{\text{OPB}}$	32, 9	35, 15	–	O	User defined outputs. This function is associated with individual channels A and B. The state of these pins is defined by the user through the software settings of the MCR register, bit 3. INTA-B are set to active mode and $\overline{\text{OP}}$ to a logic 0 when the MCR-3 is set to a logic 1. INTA-B are set to the 3-state mode and $\overline{\text{OP}}$ to a logic 1 when MCR-3 is set to a logic 0. See bit 3, modem control register (MCR bit 3). The output of these two pins is high after reset.
RESET	36	39	24	I	Reset. RESET will reset the internal registers and all the outputs. The UART transmitter output and the receiver input will be disabled during reset time. See TL16C2550 external reset conditions for initialization details. RESET is an active-high input.
$\overline{\text{RIA}}$, $\overline{\text{RIB}}$	41, 21	43 ,26	–	I	Ring indicator (active low). These inputs are associated with individual UART channels A and B. A logic low on these pins indicates the modem has received a ringing signal from the telephone line. A low to high transition on these input pins generates a modem status interrupt, if enabled. The state of these inputs is reflected in the modem status register (MSR)

PIN FUNCTIONS (continued)

PIN				I/O	DESCRIPTION
NAME	PFB	FN	RHB		
$\overline{RTSA}$, $\overline{RTSB}$	33, 22	36, 27	23, 15	O	Request to send (active low). These outputs are associated with individual UART channels A and B. A low on the $\overline{RTS}$ pin indicates the transmitter has data ready and waiting to send. Writing a 1 in the modem control register (MCR bit 1) sets these pins to low, indicating data is available. After a reset, these pins are set to high. These pins only affects the transmit and receive operation when auto $\overline{RTS}$ function is enabled through the enhanced feature register (EFR) bit 6, for hardware flow control operation.
RXA, RXB	5, 4	11, 10	4, 3	I	Receive data input. These inputs are associated with individual serial channel data to the 2550. During the local loopback mode, these RX input pins are disabled and TX data is internally connected to the UART RX input internally.
$\overline{RXRDYA}$, $\overline{RXRDYB}$	31, 18	34, 23	–	O	Receive ready (active low). $\overline{RXRDY}$ A and B goes low when the trigger level has been reached or a timeout interrupt occurs. They go high when the RX FIFO is empty or there is an error in RX FIFO.
TXA, TXB	7, 8	13, 14	5 , 6	O	Transmit data. These outputs are associated with individual serial transmit channel data from the 2550. During the local loopback mode, the TX input pin is disabled and TX data is internally connected to the UART RX input.
$\overline{TXRDYA}$, $\overline{TXRDYB}$	43, 6	1, 12	–	O	Transmit ready (active low). $\overline{TXRDY}$ A and B go low when there are at least a trigger level numbers of spaces available. They go high when the TX buffer is full.
V_{CC}	42	44	26	I	Power supply inputs.
XTAL1	13	18	10	I	Crystal or external clock input. XTAL1 functions as a crystal input or as an external clock input. A crystal can be connected between XTAL1 and XTAL2 to form an internal oscillator circuit (see Figure 14). Alternatively, an external clock can be connected to XTAL1 to provide custom data rates.
XTAL2	14	19	11	O	Output of the crystal oscillator or buffered clock. See also XTAL1. XTAL2 is used as a crystal oscillator output or buffered a clock output.

DETAILED DESCRIPTION

Autoflow Control (see Figure 1)

Autoflow control is comprised of auto-$\overline{\text{CTS}}$ and auto-$\overline{\text{RTS}}$. With auto-$\overline{\text{CTS}}$, the $\overline{\text{CTS}}$ input must be active before the transmitter FIFO can emit data. With auto-RTS, RTS becomes active when the receiver needs more data and notifies the sending serial device. When $\overline{\text{RTS}}$ is connected to $\overline{\text{CTS}}$, data transmission does not occur unless the receiver FIFO has space for the data; thus, overrun errors are eliminated using ACE1 and ACE2 from a TLC16C2550 with the autoflow control enabled. If not, overrun errors occur when the transmit data rate exceeds the receiver FIFO read latency.

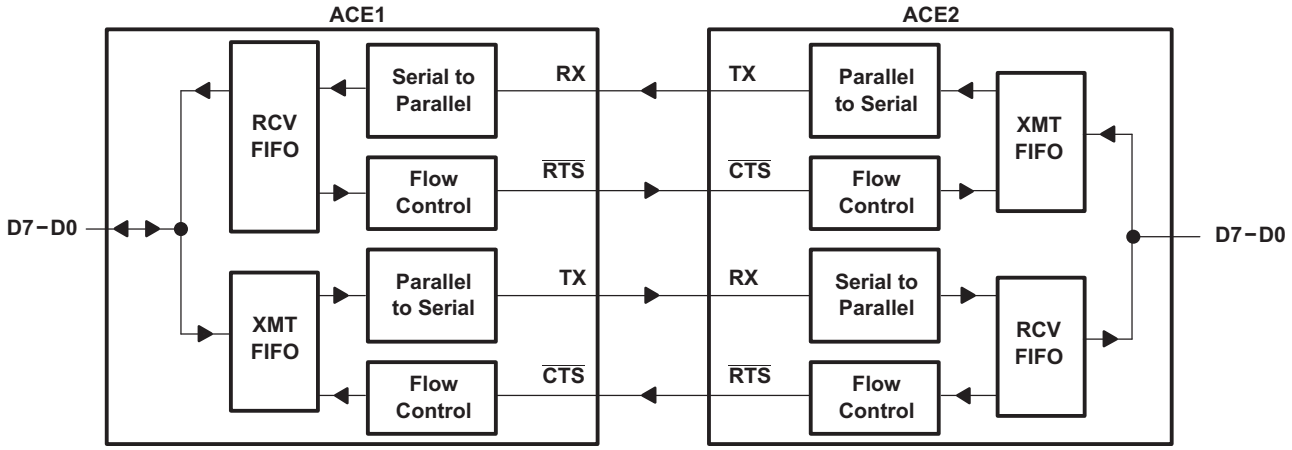


Figure 1. Autoflow Control (Auto-$\overline{\text{RTS}}$ and Auto-$\overline{\text{CTS}}$) Example

Auto-$\overline{\text{CTS}}$ (See Figure 2)

The transmitter circuitry checks $\overline{\text{CTS}}$ before sending the next data byte. When $\overline{\text{CTS}}$ is active, it sends the next byte. To stop the transmitter from sending the following byte, $\overline{\text{CTS}}$ must be released before the middle of the last stop bit that is currently being sent (see Figure 1). The auto-CTS function reduces interrupts to the host system. When flow control is enabled, $\overline{\text{CTS}}$ level changes do not trigger host interrupts because the device automatically controls its own transmitter. Without auto-$\overline{\text{CTS}}$, the transmitter sends any data present in the transmit FIFO and a receiver overrun error may result.

Auto-$\overline{\text{RTS}}$ (See Figure 3 and Figure 4)

Auto-$\overline{\text{RTS}}$ data flow control originates in the receiver timing and control block (see functional block diagram) and is linked to the programmed receiver FIFO trigger level. When the receiver FIFO level reaches a trigger level of 1, 4, or 8 (see Figure 2), $\overline{\text{RTS}}$ is deasserted. With trigger levels of 1, 4, and 8, the sending ACE may send an additional byte after the trigger level is reached (assuming the sending ACE has another byte to send) because it may not recognize the deassertion of $\overline{\text{RTS}}$ until after it has begun sending the additional byte. $\overline{\text{RTS}}$ is automatically reasserted once the RCV FIFO is emptied by reading the receiver buffer register.

When the trigger level is 14 (see Figure 3), $\overline{\text{RTS}}$ is deasserted after the first data bit of the 16th character is present on the RX line. $\overline{\text{RTS}}$ is reasserted when the RCV FIFO has at least one available byte space.

Enabling Autoflow Control and Auto-$\overline{\text{CTS}}$

Autoflow control is enabled by setting modem control register bits 5 (autoflow enable or AFE) and 1 (RTS) to a 1. Autoflow incorporates both auto-$\overline{\text{RTS}}$ and auto-$\overline{\text{CTS}}$. When only auto-$\overline{\text{CTS}}$ is desired, bit 1 in the modem control register should be cleared (this assumes that a control signal is driving $\overline{\text{CTS}}$).

Auto-$\overline{CTS}$ and Auto-$\overline{RTS}$ Functional Timing

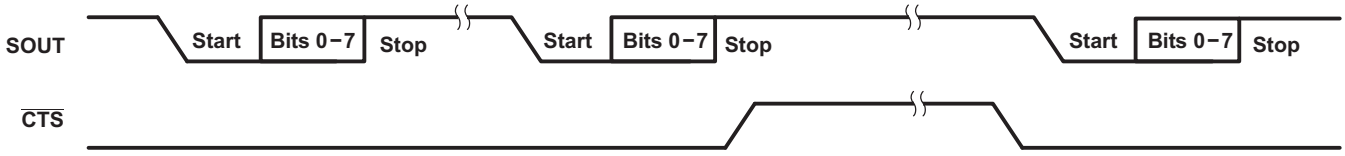


Figure 2. $\overline{CTS}$ Functional Timing Waveforms

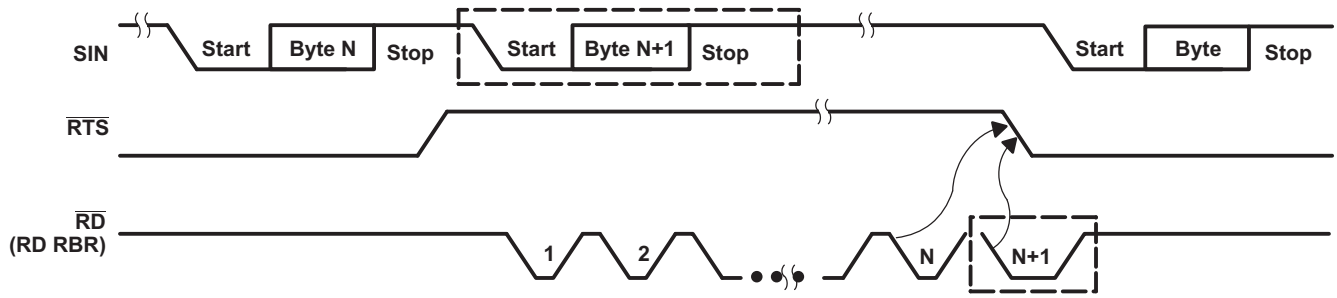


Figure 3. $\overline{RTS}$ Functional Timing Waveforms, RCV FIFO Trigger Level = 1, 4, or 8 Bytes

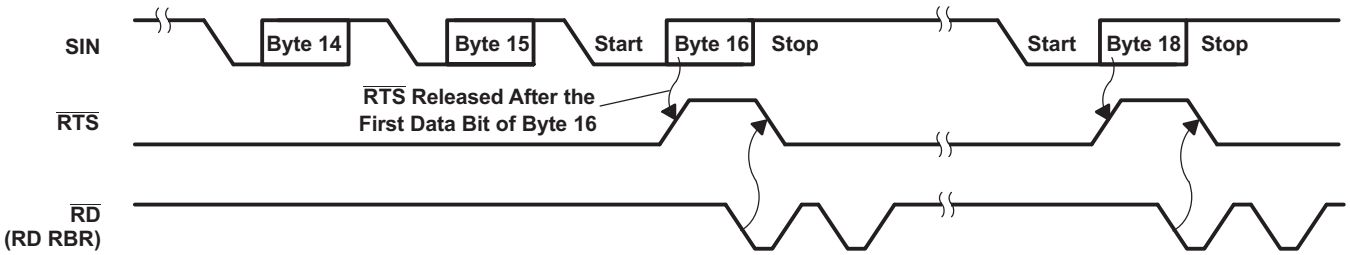
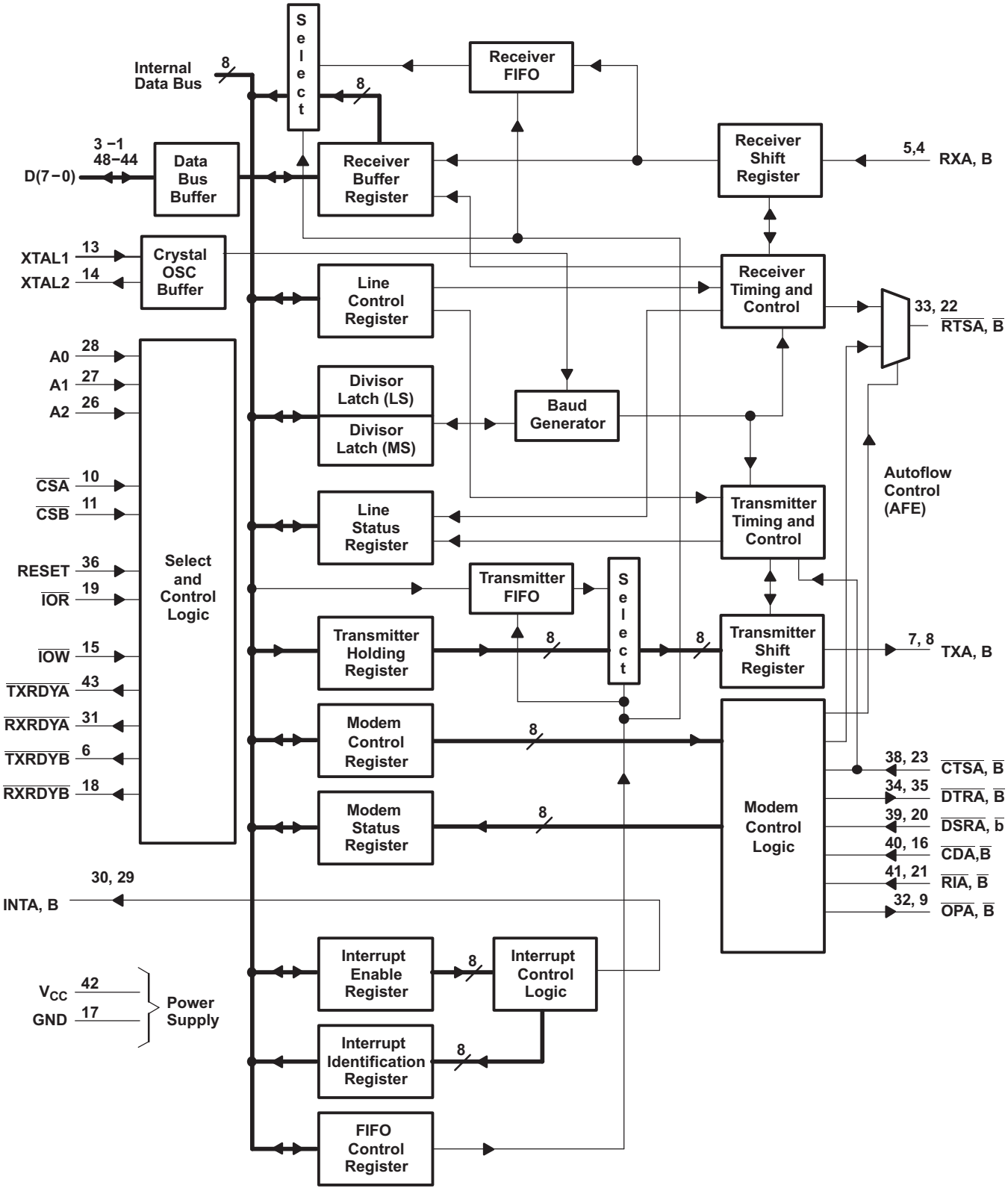


Figure 4. $\overline{RTS}$ Functional Timing Waveforms, RCV FIFO Trigger Level = 14 Bytes



A. Pin numbers shows are for 48-pin TQFP PFB package.

Figure 5. Functional Block Diagram

ORDERING INFORMATION

T_A	PACKAGE		ORDERABLE PART NAME	TOP-SIDE MARKING
–40°C to 85°C	TQFP - PFB	Reel of 1000	TL16C2550IPFBRQ1	TL2550RQ

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		UNIT
V_{CC}	Supply voltage range, (2)	–0.5 V to 7 V
V_I	Input voltage range at any input	–0.5 V to 7 V
V_O	Output voltage range	–0.5 V to 7 V
T_A	Operating free-air temperature, TL16C2550	0°C to 70°C
T_A	Operating free-air temperature, TL16C2550I	–40°C to 85°C
T_{stg}	Storage temperature range	–65°C to 150°C
ESD	Human Body Model (HBM)	2000 V
	Charged Device Model (CDM)	1000 V
	Machine Model (MM)	150 V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
1.8 V ±10%					
V_{CC}	Supply voltage	1.62	1.8	1.98	V
V_I	Input voltage	0		V_{CC}	V
V_{IH}	High-level input voltage	1.4		1.98	V
V_{IL}	Low-level input voltage	–0.3		0.4	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current (all outputs)			0.5	mA
I_{OL}	Low-level output current (all outputs)			1	mA
	Oscillator/clock speed			10	MHz
2.5 V ±10%					
V_{CC}	Supply voltage	2.25	2.5	2.75	V
V_I	Input voltage	0		V_{CC}	V
V_{IH}	High-level input voltage	1.8		2.75	V
V_{IL}	Low-level input voltage	–0.3		0.6	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current (all outputs)			1	mA
I_{OL}	Low-level output current (all outputs)			2	mA
	Oscillator/clock speed			16	MHz

RECOMMENDED OPERATING CONDITIONS (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
3.3 V ±10%						
V_{CC}	Supply voltage		3	2.5	2.75	V
V_I	Input voltage		0		V_{CC}	V
V_{IH}	High-level input voltage		$0.7V_{CC}$			V
V_{IL}	Low-level input voltage				$0.3V_{CC}$	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current (all outputs)				1.8	mA
I_{OL}	Low-level output current (all outputs)				3.2	mA
	Oscillator/clock speed				20	MHz
5 V ±10%						
V_{CC}	Supply voltage		4.5	5	5.5	V
V_I	Input voltage		0		V_{CC}	V
V_{IH}	High-level input voltage	All except XTAL1, XTAL2	2			V
		XTAL1, XTAL2	$0.7V_{CC}$			
V_{IL}	Low-level input voltage	All except XTAL1, XTAL2			0.8	V
		XTAL1, XTAL2			$0.3V_{CC}$	
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current (all outputs)				4	mA
I_{OL}	Low-level output current (all outputs)				4	mA
	Oscillator/clock speed				24	MHz

ELECTRICAL CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
1.8 V NOMINAL						
V_{OH}	High-level output voltage(1)	I_{OH} = –0.5 mA	1.3			V
V_{OL}	Low-level output voltage(2)	I_{OL} = 1 mA			0.5	V
I_I	Input current(3)	V_{CC} = 1.98 V, V_{SS} = 0, V_I = 0 to 1.98 V, All other terminals floating			10	µA
I_{OZ}	High-impedance-state output current(3)	V_{CC} = 1.98 V, V_{SS} = 0, V_I = 0 to 1.98 V, Chip slected in write mode or chip deselcted			±20	µA
I_{CC}	Supply current(3)	V_{CC} = 1.98 V, T_A = 0°C, RXA, RXB, DSRA, DSRB, CDA, CDB, CTSA, CTSB, RIA, and RIB at 1.4 V, All other inputs at 0.4 V, XTAL1 at 10 MHz, No load on outputs			1.5	mA
$C_{i(CLK)}$	Clock input impedance(3)	V_{CC} = 0, V_{SS} = 0, f = 1 MHz, T_A = 25°C, All other terminals grounded		15	20	pF
$C_{O(CLK)}$	Clock output impedance(3)			20	30	pF
C_I	Input impedance(3)			6	10	pF
C_O	Output impedance(3)			10	20	pF

(1) All typical values are at V_{CC} = 1.8 V and T_A = 25°C.
(2) These parameters apply for all outputs except XTAL2.
(3) Not production tested.

ELECTRICAL CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
2.5 V NOMINAL						
V_{OH}	High-level output voltage(2) (3)	I_{OH} = –1 mA	1.8			V
V_{OL}	Low-level output voltage(2) (3)	I_{OL} = 2 mA			0.5	V
I_I	Input current	V_{CC} = 5.5 V, V_{SS} = 0, V_I = 0 to 2.75 V, All other terminals floating			10	µA
I_{OZ}	High-impedance-state output current	V_{CC} = 2.75 V, V_{SS} = 0, V_I = 0 to 2.75 V, Chip slected in write mode or chip deselcted			±20	µA
I_{CC}	Supply current(3)	V_{CC} = 2.75 V, T_A = 0°C, RXA, RXB, DSRA, DSRB, CDA, CDB, CTSA, CTSB, RIA, and RIB at 1.8 V, All other inputs at 0.6 V, XTAL1 at 16 MHz, No load on outputs			2.5	mA
$C_{i(CLK)}$	Clock input impedance(3)	V_{CC} = 0, V_{SS} = 0, f = 1 MHz, T_A = 25°C, All other terminals grounded		15	20	pF
$C_{O(CLK)}$	Clock output impedance(3)			20	30	pF
C_I	Input impedance(3)			6	10	pF
C_O	Output impedance(3)			10	20	pF

(1) All typical values are at V_{CC} = 2.5 V and T_A = 25°C.
(2) These parameters apply for all outputs except XTAL2.
(3) Not production tested.

ELECTRICAL CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
3.3 V NOMINAL						
V_{OH}	High-level output voltage(2)	I_{OH} = –1.8 mA	2.4			V
V_{OL}	Low-level output voltage(2)	I_{OL} = 3.2 mA			0.5	V
I_I	Input current	V_{CC} = 3.6 V, V_{SS} = 0, V_I = 0 to 3.6 V, All other terminals floating			10	µA
I_{OZ}	High-impedance-state output current	V_{CC} = 3.6 V, V_{SS} = 0, V_I = 0 to 3.6 V, Chip slected in write mode or chip deselcted			±20	µA
I_{CC}	Supply current(3)	V_{CC} = 3.6 V, T_A = 0°C, RXA, RXB, DSRA, DSRB, CDA, CDB, CTSA, CTSB, RIA, and RIB at 2 V, All other inputs at 0.8 V, XTAL1 at 20 MHz, No load on outputs			4	mA
$C_{i(CLK)}$	Clock input impedance(3)	V_{CC} = 0, V_{SS} = 0, f = 1 MHz, T_A = 25°C, All other terminals grounded		15	20	pF
$C_{O(CLK)}$	Clock output impedance(3)			20	30	pF
C_I	Input impedance(3)			6	10	pF
C_O	Output impedance(3)			10	20	pF

(1) All typical values are at V_{CC} = 3.3 V and T_A = 25°C.
(2) These parameters apply for all outputs except XTAL2.
(3) Not production tested.

ELECTRICAL CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
5 V NOMINAL						
V_{OH}	High-level output voltage(2)	I_{OH} = –4 mA	4			V
V_{OL}	Low-level output voltage(2)	I_{OL} = 4 mA			0.4	V
I_I	Input current	V_{CC} = 5.5 V, V_{SS} = 0, V_I = 0 to 5.5 V, All other terminals floating			10	µA
I_{OZ}	High-impedance-state output current	V_{CC} = 5.5 V, V_{SS} = 0, V_I = 0 to 5.5 V, Chip slected in write mode or chip deselcted			±20	µA
I_{CC}	Supply current	V_{CC} = 5.5 V, T_A = 0°C, RXA, RXB, DSRA, DSRB, CDA, CDB, CTSA, CTSB, RIA, and RIB at 2 V, All other inputs at 0.8 V, XTAL1 at 24 MHz, No load on outputs			7.5	mA
$C_{i(CLK)}$	Clock input impedance(3)	V_{CC} = 0, V_{SS} = 0, f = 1 MHz, T_A = 25°C, All other terminals grounded		15	20	pF
$C_{O(CLK)}$	Clock output impedance(3)			20	30	pF
C_I	Input impedance(3)			6	10	pF
C_O	Output impedance(3)			10	20	pF

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) These parameters apply for all outputs except XTAL2.
(3) Not production tested.

TIMING REQUIREMENTS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	1.8 V		2.5 V		3.3 V		5 V		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{w8}	Pulse duration, RESET	t_{RESET}			1		1		1		1		µs
t_{w1}	Pulse duration, clock high	t_{XH}	10		40		25		20		18		ns
t_{w2}	Pulse duration, clock low	t_{XL}	10		115		80		62		57		ns
t_{cR}	Cycle time, read (t_{w7} + t_{d8} + t_{h7})	RC	12		115		80		62		57		ns
t_{cW}	Cycle time, write (t_{w6} + t_{d5} + t_{h4})	WC	11		115		80		62		57		ns
t_{w6}	Pulse duration, $\overline{IOW}$	t_{IOW}	11		80		55		45		40		ns
t_{w7}	Pulse duration, $\overline{IOR}$	t_{IOR}	12		80		55		45		40		ns
t_{SU3}	Setup time, data valid before $\overline{IOW}$↑	t_{DS}	11		25		20		15		15		ns
t_{h3}	Hold time, CS valid after $\overline{IOW}$↑	t_{WCS}	11		0		0		0		0		ns
t_{h4}	Hold time, address valid after $\overline{IOW}$↑	t_{WA}	11		20		15		10		10		ns
t_{h5}	Hold time, data valid after $\overline{IOW}$↑	t_{DH}	11		15		10		5		5		ns
t_{h6}	Hold time, chip select valid after $\overline{IOR}$↑	t_{RCS}	12		0		0		0		0		ns
t_{h7}	Hold time, address valid after $\overline{IOR}$↑	t_{RA}	12		20		15		10		10		ns
t_{d4}	Delay time, CS valid before $\overline{IOW}$↓	t_{CSW}	11		0		0		0		0		ns
t_{d5}	Delay time, address valid before $\overline{IOW}$↓	t_{AW}	11		15		10		7		7		ns
t_{d7}	Delay time, CS valid to $\overline{IOR}$↓	t_{CSR}	12		0		0		0		0		ns
t_{d8}	Delay time, address valid to $\overline{IOR}$↓	t_{AR}	12		15		10		7		7		ns
t_{d10}	Delay time, $\overline{IOR}$↓ to data valid	t_{RVD}	12	C_L = 30 pF		55		35		25		20	ns
t_{d11}	Delay time, $\overline{IOR}$↓ to floating data	t_{HZ}	12	C_L = 30 pF		40		30		20		20	ns

RECEIVER SWITCHING CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	LIMITS								UNIT
					1.8 V		2.5 V		3.3 V		5 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{d12}	Delay time, RCLK to sample	t_{SCD}	13			20		15		10		10	ns
t_{d13}	Delay time, stop to set INT or read RBR to LSI interrupt or stop to $\overline{RXRDY}$↓	t_{SINT}	13, 14, 15, 16, 17			1		1		1	1		RCLK cycle
t_{d14}	Delay time, read RBR/LSR to reset INT	t_{RINT}	13, 14, 15, 16, 17	C_L = 30 pF		100		90		80		70	ns
t_{d26}	Delay time, RCV threshold byte to $\overline{RTS}$↑		23	C_L = 30 pF								2	baudout cycles
t_{d27}	Delay time, read of last byte in receive FIFO to $\overline{RTS}$↓		23	C_L = 30 pF								2	baudout cycles
t_{d28}	Delay time, first data bit of 16th character to $\overline{RTS}$↑		24	C_L = 30 pF								2	baudout cycles
t_{d29}	Delay time, RBRRD low to $\overline{RTS}$↓		24	C_L = 30 pF								2	baudout cycles

(1) In the FIFO mode, the read cycle (RC) = 1 baudclock (min) between reads of the receive FIFO and the status registers (interrupt identification register or line status register)
(2) Not production tested.

TRANSMITTER SWITCHING CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	LIMITS								UNIT
					1.8 V		2.5 V		3.3 V		5 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{d15}	Delay time, initial write to transmit start	t_{IRS}	18		8	24	8	24	8	24	8	24	baudout cycles
t_{d16}	Delay time, start to INT	t_{STI}	18		8	10	8	10	8	10		10	baudout cycles
t_{d17}	Delay time, $\overline{IOW}$ (WR THR) to reset INT	t_{HR}	18	C_L = 30 pF		70		60		50	8	50	ns
t_{d18}	Delay time, initial write to INT (THRE(3))	t_{SI}	18		16	34	16	34	16	34	16	34	baudout cycles
t_{d19}	Delay time, read $\overline{IOR}$↑ to reset INT (THRE(3))	t_{IR}	18	C_L = 30 pF		70		50		35		35	ns
t_{d20}	Delay time, write to $\overline{TXRDY}$ inactive	t_{WXI}	19, 20	C_L = 30 pF		60		45		35		35	ns
t_{d21}	Delay time, start to $\overline{TXRDY}$ active	t_{SXA}	19, 20	C_L = 30 pF		9		9		9		9	baudout cycles
t_{SU4}	Setup time, $\overline{CTS}$↑ before midpoint of stop bit		22		30		20		10		10		ns
t_{d25}	Delay time, $\overline{CTS}$ low to TX↓		22	C_L = 30 pF		24		24		24		24	baudout cycles

(1) In the FIFO mode, the read cycle (RC) = 1 baudclock (min) between reads of the receive FIFO and the status registers (interrupt identification register or line status register)
(2) Not production tested.
(3) THRE = Transmitter Holding Register Empty; IIR = Interrupt Identification Register.

MODEM CONTROL SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	LIMITS								UNIT(2)
					1.8 V		2.5 V		3.3 V		5 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{d22}	Delay time, WR MCR to output	t_{MDO}	21	C_L = 30 pF		90		70		60		50	ns
t_{d23}	Delay time, modem interrupt to set INT	t_{SIM}	21	C_L = 30 pF		60		50		40		35	ns
t_{d24}	Delay time, RD MSR to reset INT	t_{RIM}	21	C_L = 30 pF		80		60		50		40	ns

(1) Not production tested.
(2) A baudout cycle is equal to the period of the input clock divided by the programmed divider in DLL, DLM.

TYPICAL CHARACTERISTICS

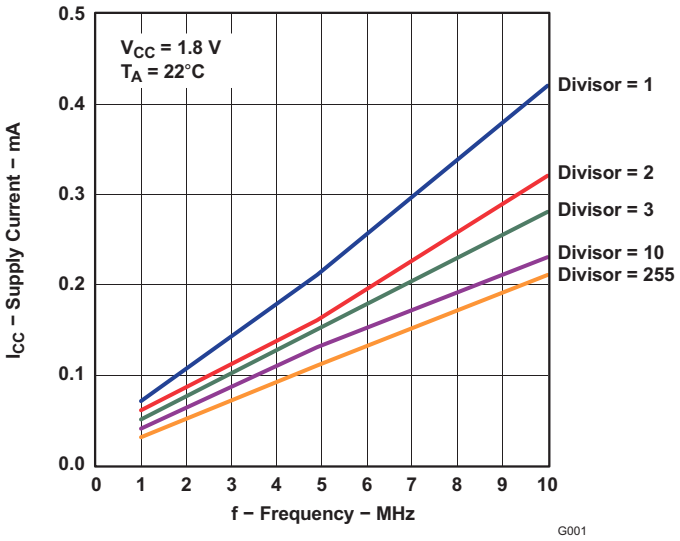


Figure 6.

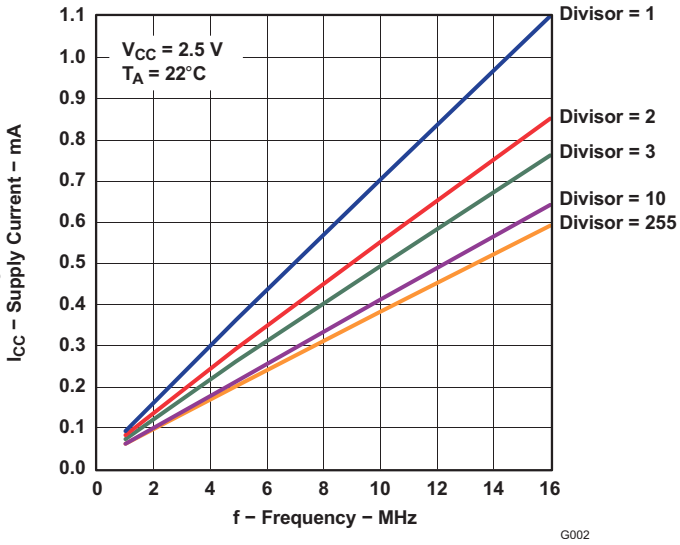


Figure 7.

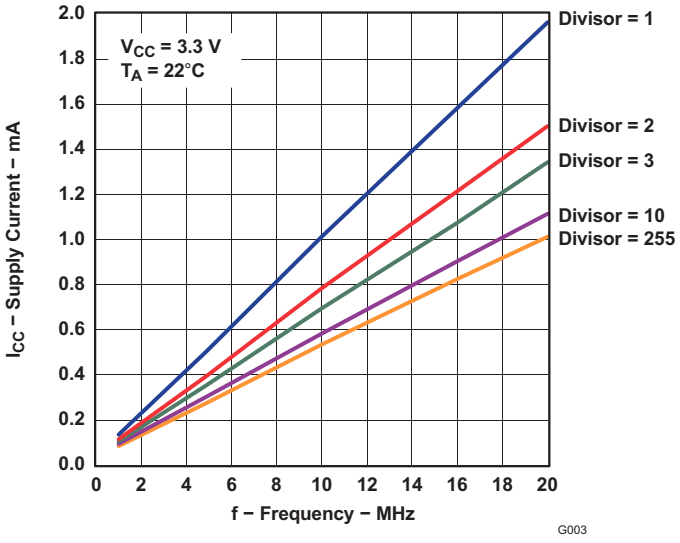


Figure 8.

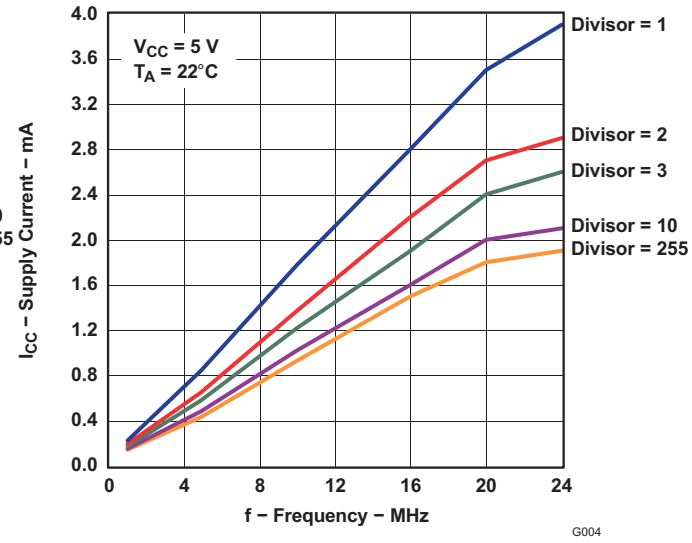


Figure 9.

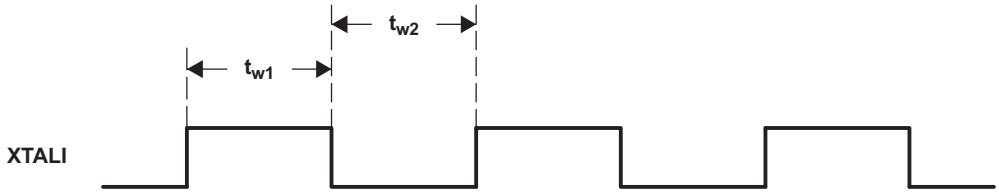


Figure 10. Clock Input

TYPICAL CHARACTERISTICS (continued)

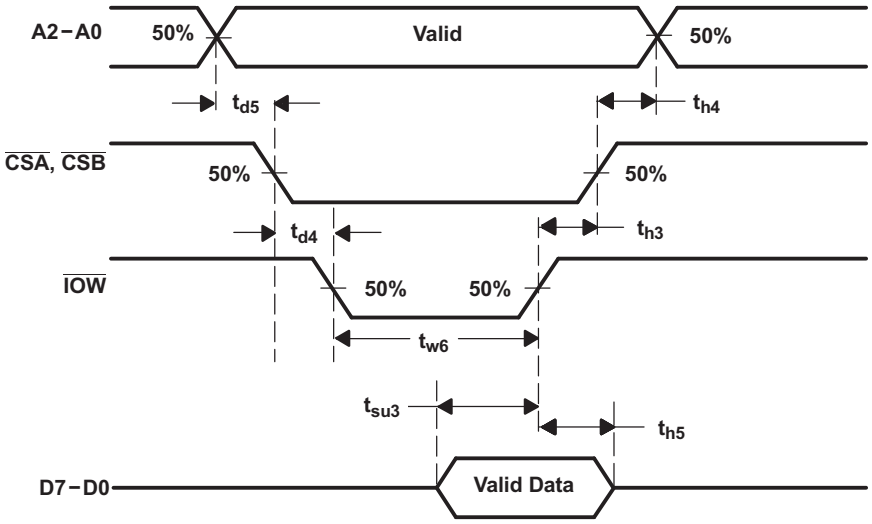


Figure 11. Write Cycle Timing Waveforms

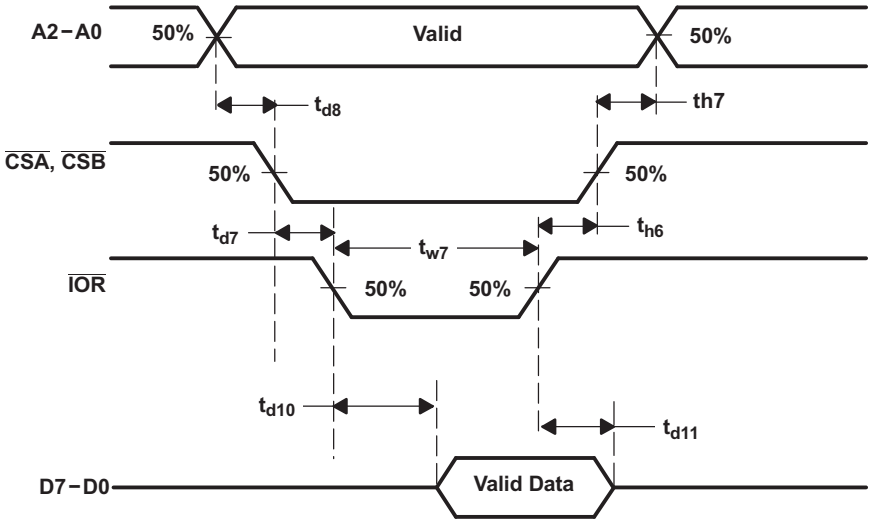


Figure 12. Read Cycle Timing Waveforms

TYPICAL CHARACTERISTICS (continued)

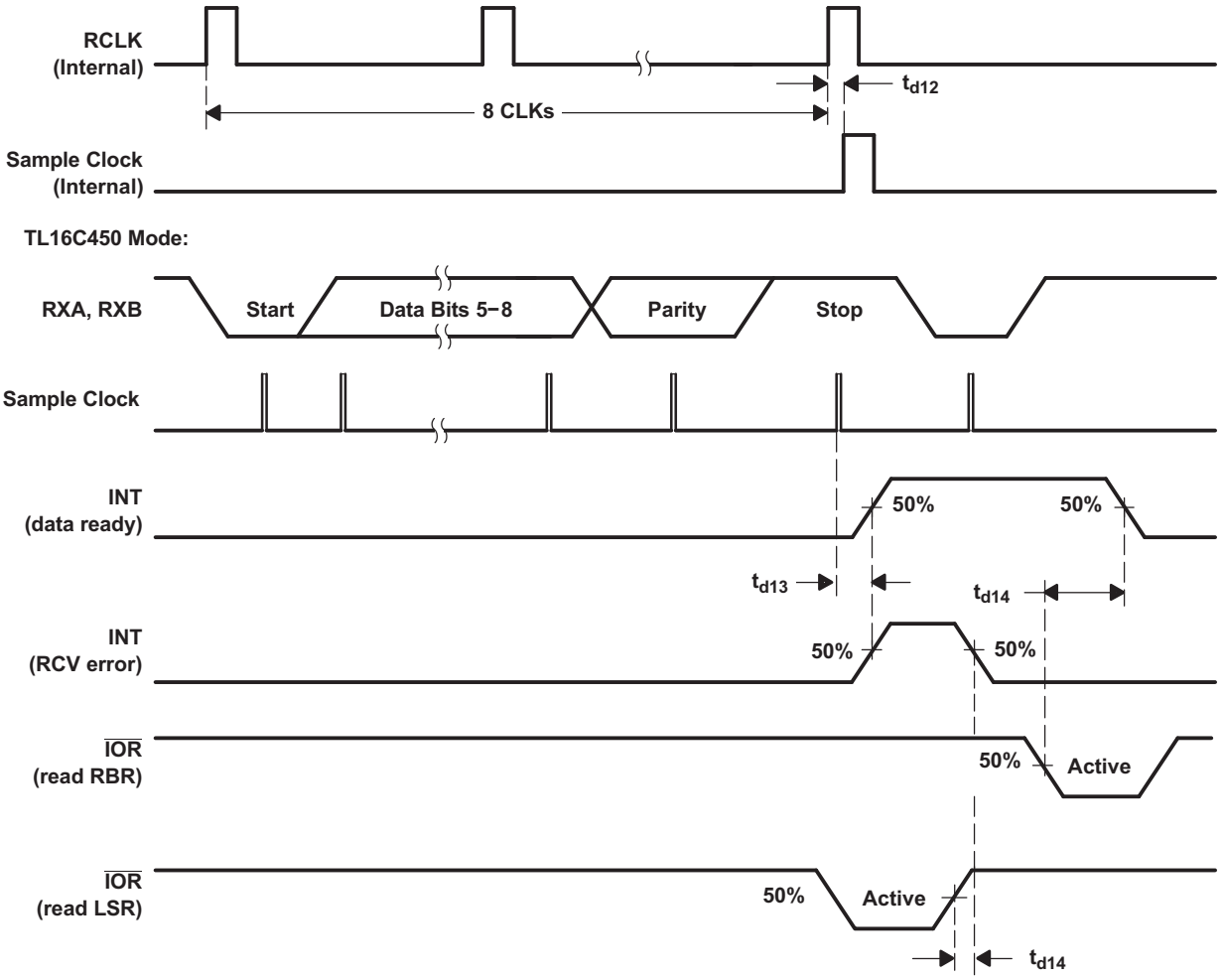


Figure 13. Receiver Timing Waveforms

TYPICAL CHARACTERISTICS (continued)

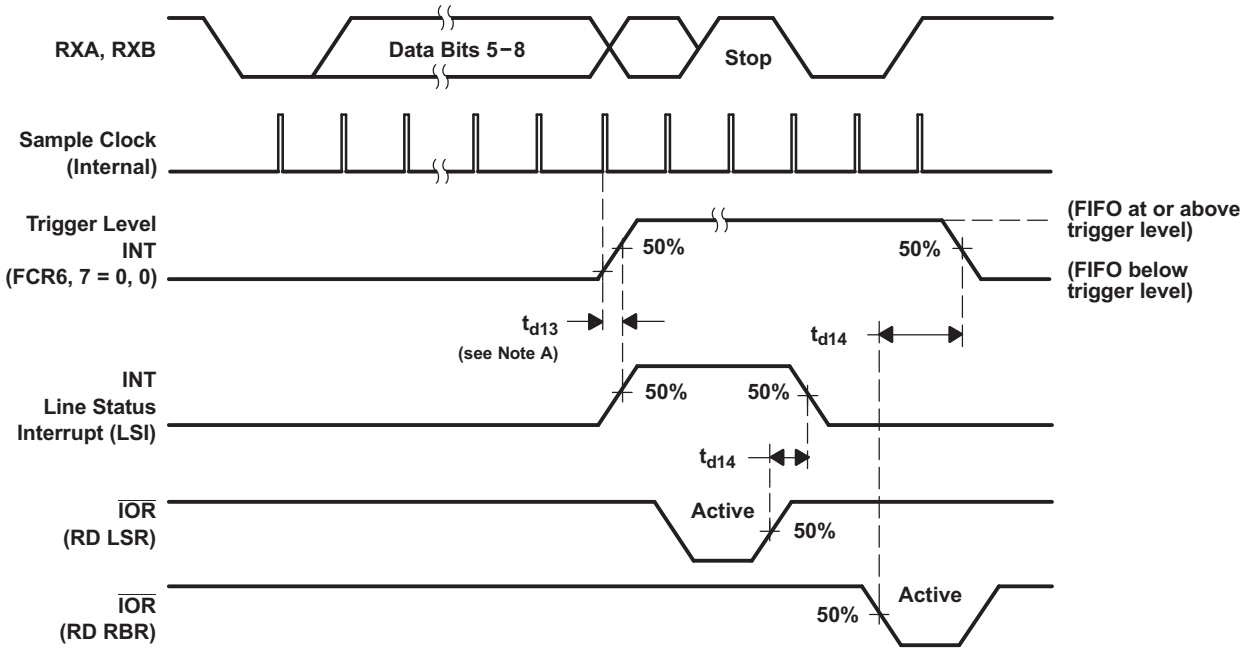


Figure 14. Receive First Byte (Sets DR Bit) Waveforms

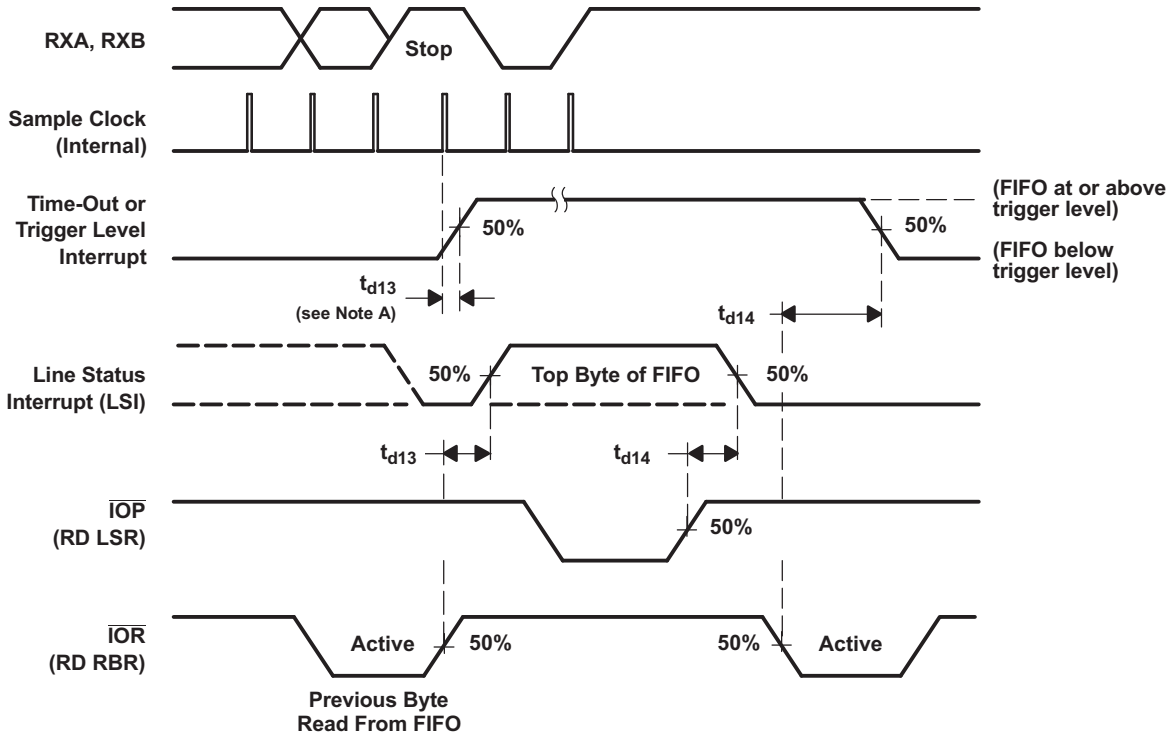


Figure 15. Receive FIFO Bytes Other than the First Byte (DR Internal BIt already set) Waveforms

TYPICAL CHARACTERISTICS (continued)

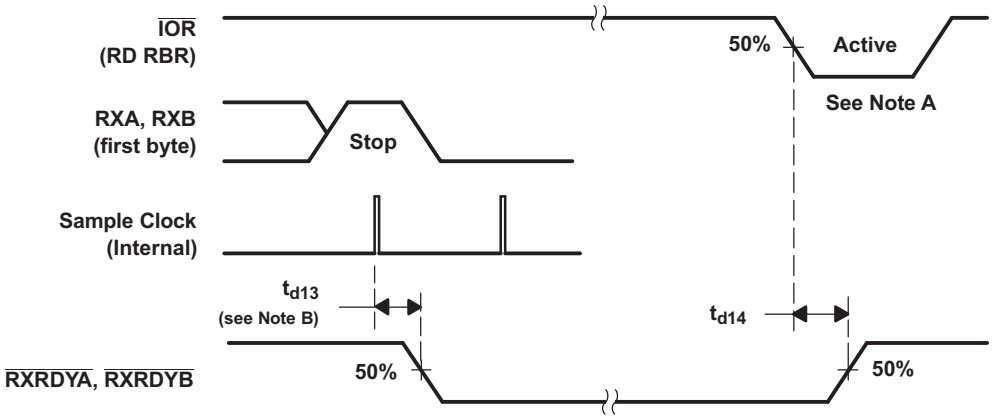


Figure 16. Receiver Ready ($\overline{\text{RXRDY}}$) Waveforms, FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (Mode 0)

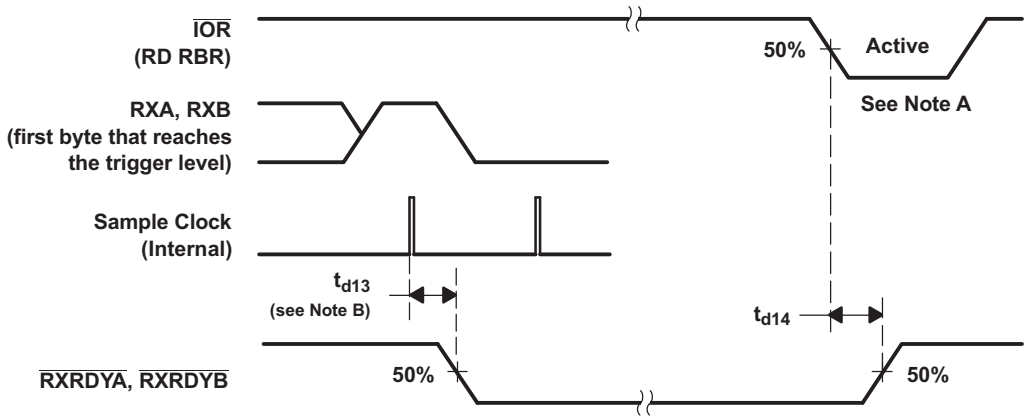


Figure 17. Receiver Ready ($\overline{\text{RXRDY}}$) Waveforms, FCR0 = 0 and FCR3 = 1 (Mode 1)

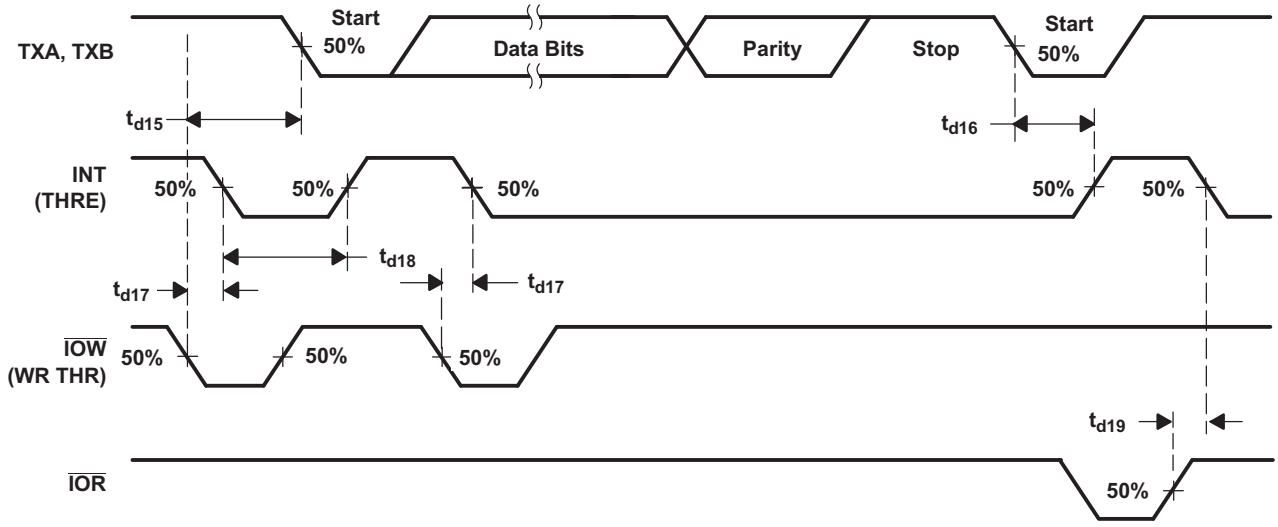


Figure 18. Transmitter Timing Waveforms

TYPICAL CHARACTERISTICS (continued)

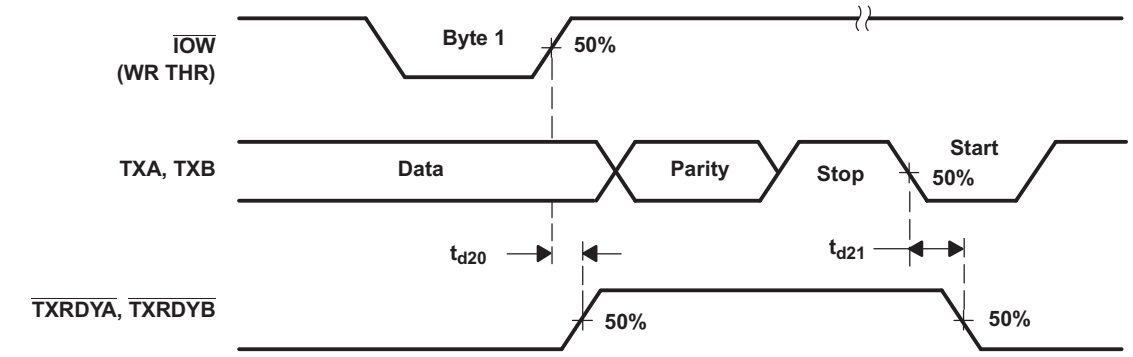


Figure 19. Tranceiver Ready (TXRDY) Waveforms, FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (Mode 0)

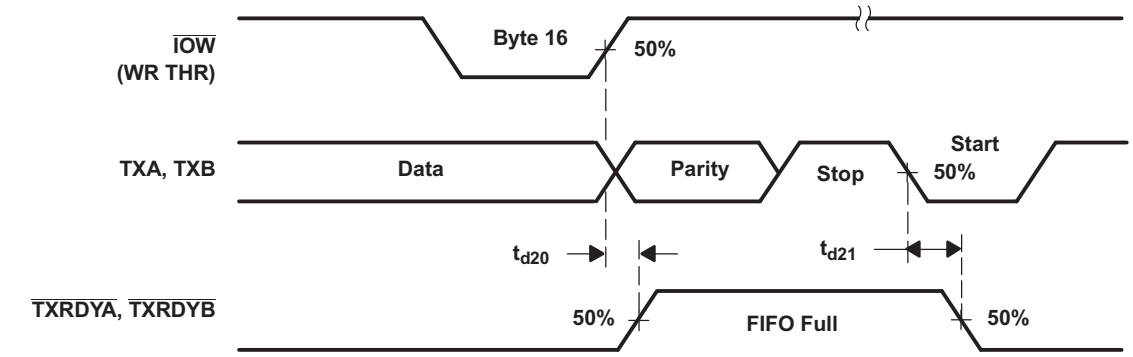


Figure 20. Tranceiver Ready (TXRDY) Waveforms, FCR0 = 0 and FCR3 = 1 (Mode 1)

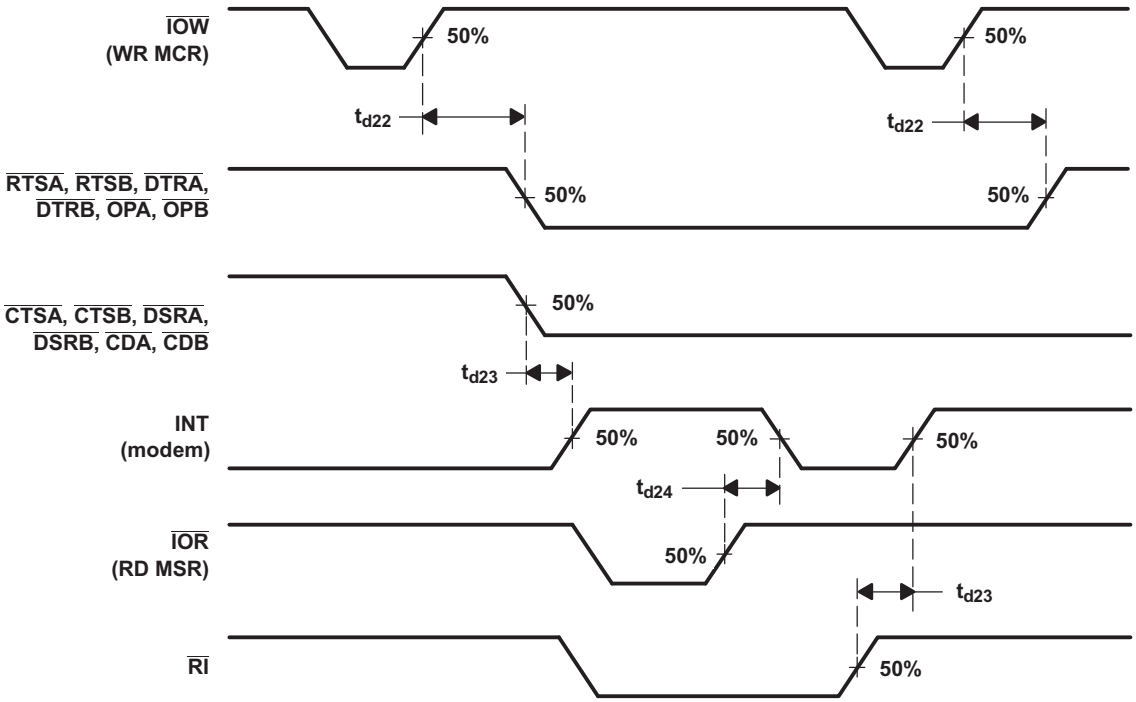


Figure 21. Modem Control Timing Waveforms

TYPICAL CHARACTERISTICS (continued)

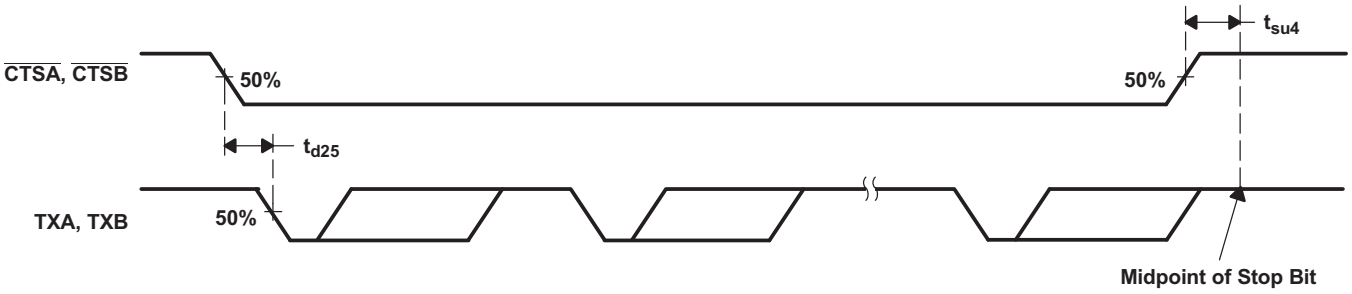


Figure 22. $\overline{\text{CTS}}$ and TX Autoflow Control Timing (Start and Stop) Waveforms

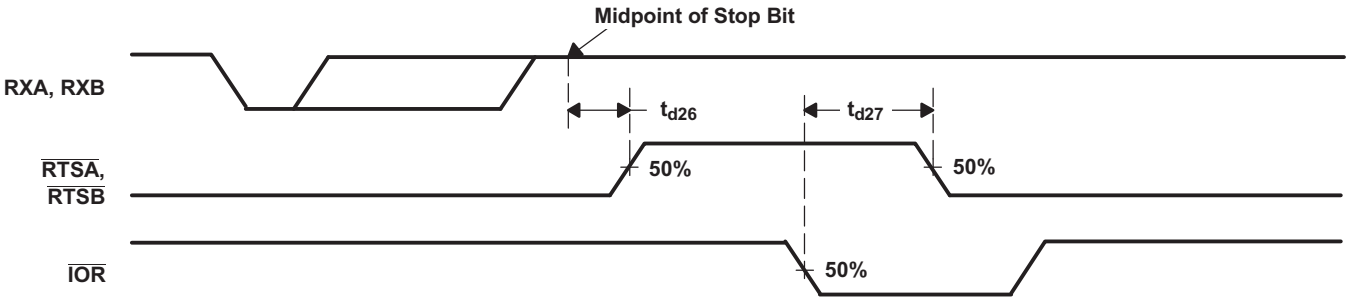


Figure 23. Auto-$\overline{\text{RTS}}$ Timing for RCV Threshold of 1, 4, or 8 Waveforms

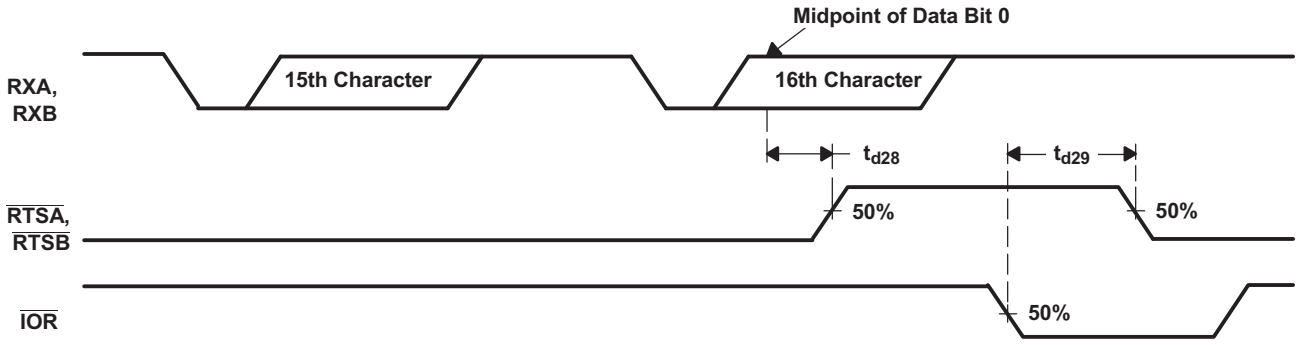


Figure 24. Auto-$\overline{\text{RTS}}$ Timing for RCV Threshold of 14 Waveforms

APPLICATION INFORMATION

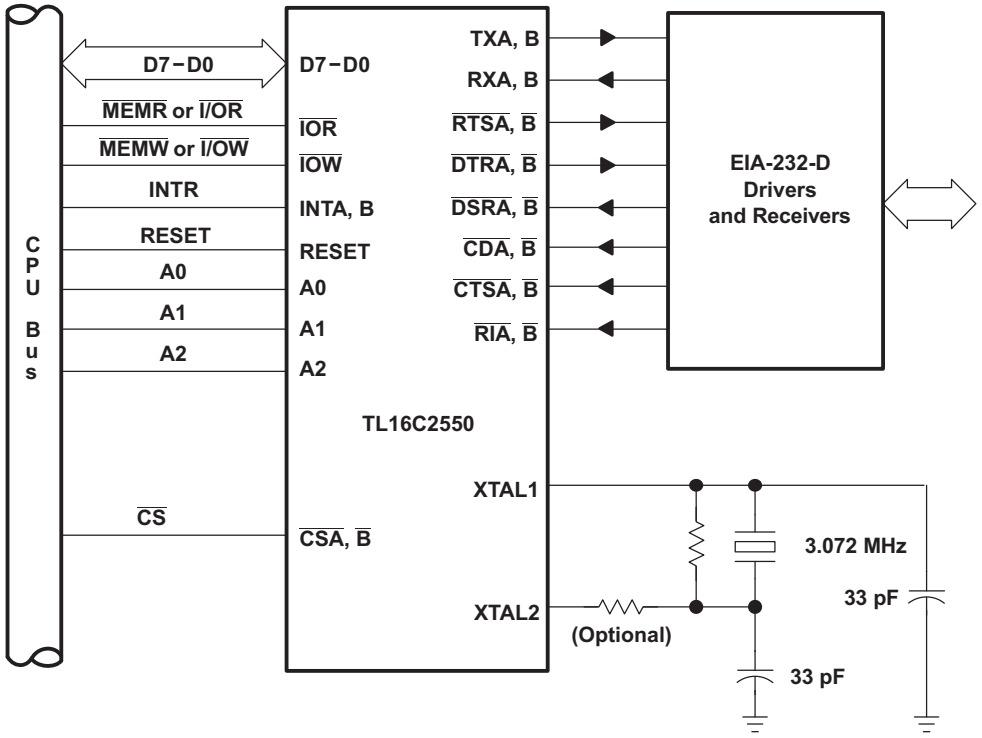


Figure 25. Basic TL16C2550 Configuration

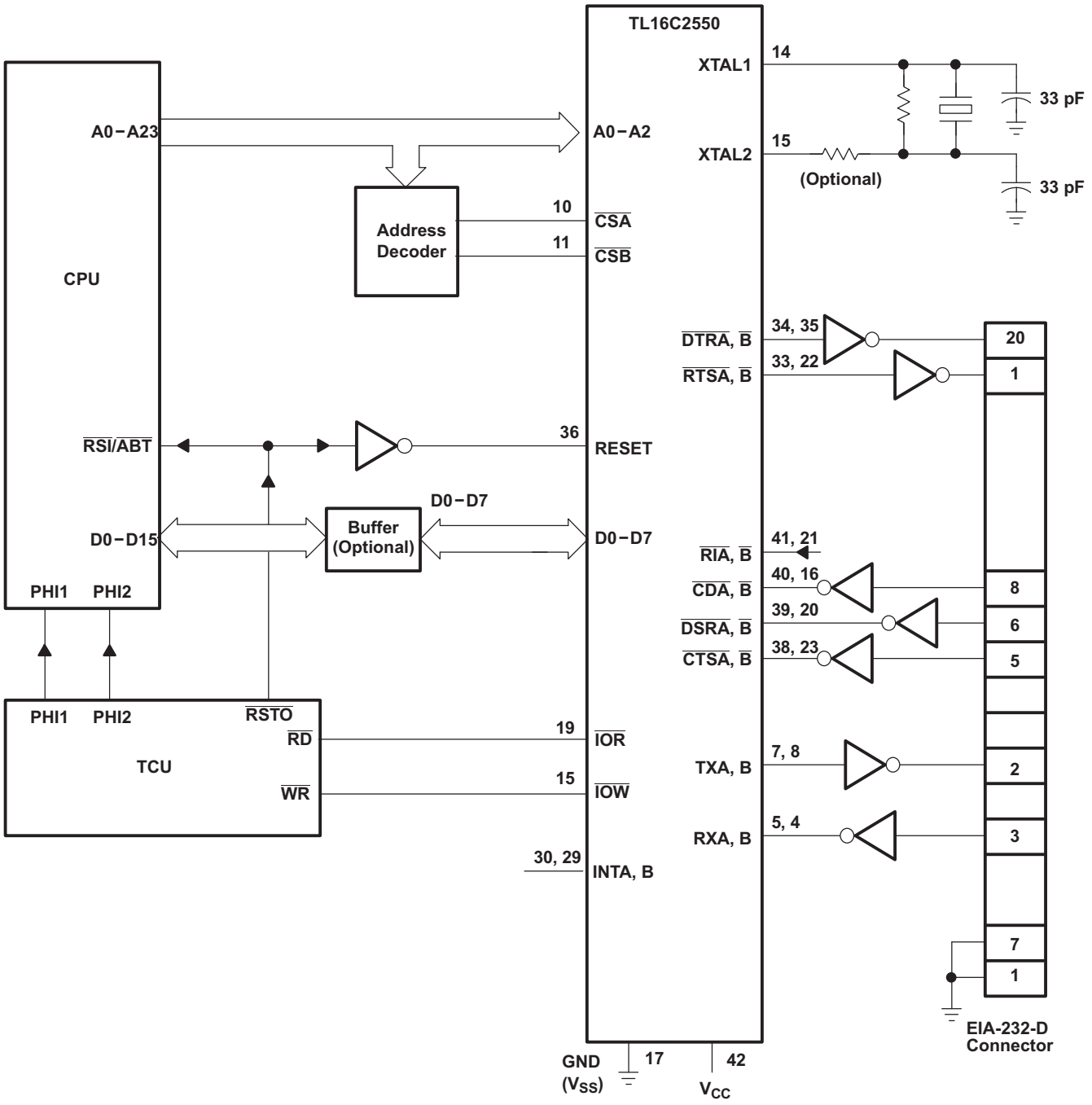


Figure 26. Typical TL16C2550 Connection

PRINCIPLES OF OPERATION

REGISTER SELECTION

Table 1. Register Selection

DLAB (1)	A2	A1	A0	REGISTER
0	L	L	L	Receiver buffer (read), transmitter holding register (write)
0	L	L	H	Interrupt enable register
X	L	H	L	Interrupt identification register (read only)
X	L	H	L	FIFO control register (write)
X	L	H	H	Line control register
X	H	L	L	Modem control register
X	H	L	H	Line status register
X	H	H	L	Modem status register
X	H	H	H	Scratch register
1	L	L	L	Divisor latch (LSB)
1	L	L	H	Divisor latch (MSB)

(1) The divisor latch access bit (DLAB) is the most significant bit of the line control register. The DLAB signal is controlled by writing to this bit location (see Table 2).

Table 2. ACE Reset Functions

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt enable register	Master reset	All bits cleared (0–3 forced and 4–7 permanent)
Interrupt identification register	Master reset	Bit 0 is set, bits 1, 2, 3, 6, and 7 are cleared, and bits 4–5 are permanently cleared
FIFO control register	Master reset	All bits cleared
Line control register	Master reset	All bits cleared
Modem control register	Master reset	All bits cleared (6 -7 permanent)
Line status register	Master reset	Bits 5 and 6 are set; all other bits are cleared
Modem status register	Master reset	Bits 0–3 are cleared; bits 4–7 are input signals
TX	Master reset	High
INT	Master reset, MCR3	Output buffer tristated
Interrupt condition (receiver error flag)	Read LSR/MR	Low
Interrupt condition (received data available)	Read RBR/MR	Low
Interrupt condition (transmitter holding register empty)	Read IIR/write THR/MR	Low
Interrupt condition (modem status changes)	Read MSR/MR	Low
OP	Master reset	High
RTS	Master reset	High
DTR	Master reset	High
Scratch register	Master reset	No effect
Divisor latch (LSB and MSB) registers	Master reset	No effect
Receiver buffer register	Master reset	No effect
Transmitter holding register	Master reset	No effect
RCVR FIFO	MR/FCR1 – FCR0/DFCR0	All bits cleared
XMIT FIFO	MR/FCR2 – FCR0/DFCR0	All bits cleared

Accessible Registers

The system programmer, using the CPU, has access to and control over any of the ACE registers that are summarized in Table 2. These registers control ACE operations, receive data, and transmit data. Descriptions of these registers follow Table 3.

Table 3. Summary of Accessible Registers

BIT NO.	REGISTER ADDRESS											
	DLAB = 0										DLAB = 1	
	0	0	1	2	2	3	4	5	6	7	0	1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident Register (Read Only)	FIFO Control Register (WriteOnly)	Line Control Register	Modem Control Register	Line Status Register	Modem Status Register	Scratch Register	Divisor Latch (LSB)	Divisor Latch (MSB)
	RBR	THR	IER	IIR	FCR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0(1)	Data Bit 0	Enable Received Data Available Interrupt (ERBI)	0 if Interrupt Pending	FIFO Enable	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (ΔCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit 1	Receiver FIFO Reset	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (ΔDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit 2	Transmitter FIFO Reset	Number of Stop Bits (STB)	OUT1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable Modem Status Interrupt (EDSSI)	Interrupt ID Bit 3(2)	DMA Mode Select	Parity Enable (PEN)	OUT2, OPcontrol, INT Enable	Framing Error (FE)	Delta Data Carrier Detect (ΔDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	Autoflow Control Enable (AFE)	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled(2)	Receiver Trigger (LSB)	Break Control	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled(2)	Receiver Trigger (MSB)	Divisor Latch Access Bit (DLAB)	0	Error in RCVR FIFO(2)	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

(1) Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
(2) These bits are always 0 in the TL16C450 mode.

FIFO Control Register (FCR)

The FCR is a write-only register at the same location as the IIR, which is a read-only register. The FCR enables and clears the FIFOs, sets the receiver FIFO trigger level, and selects the type of DMA signalling.

- Bit 0: This bit, when set, enables the transmitter and receiver FIFOs. Bit 0 must be set when other FCR bits are written to or they are not programmed. Changing this bit clears the FIFOs.
- Bit 1: This bit, when set, clears all bytes in the receiver FIFO and clears its counter. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.
- Bit 2: This bit, when set, clears all bytes in the transmit FIFO and clears its counter. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.
- Bit 3: When FCR0 is set, setting FCR3 causes $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ to change from level 0 to level 1.
- Bits 4 and 5: These two bits are reserved for future use.
- Bits 6 and 7: These two bits set the trigger level for the receiver FIFO interrupt (see Table 4).

Table 4. Receiver FIFO Trigger Level

BIT 7	BIT 6	RECEIVER FIFO TRIGGER LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

FIFO Interrupt Mode Operation

When the receiver FIFO and receiver interrupts are enabled (FCR0 = 1, IER0 = 1, IER2 = 1), a receiver interrupt occurs as follows:

1. The received data available interrupt is issued to the microprocessor when the FIFO has reached its programmed trigger level. It is cleared when the FIFO drops below its programmed trigger level.
2. The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt, it is cleared when the FIFO drops below the trigger level.
3. The receiver line status interrupt (IIR = 06) has higher priority than the received data available (IIR = 04) interrupt.
4. The data ready bit (LSR0) is set when a character is transferred from the shift register to the receiver FIFO. It is cleared when the FIFO is empty.

When the receiver FIFO and receiver interrupts are enabled:

1. FIFO time-out interrupt occurs if the following conditions exist:
   (a) At least one character is in the FIFO.
   (b) The most recent serial character was received more than four continuous character times ago (if two stop bits are programmed, the second one is included in this time delay).
   (c) The most recent microprocessor read of the FIFO has occurred more than four continuous character times before. This causes a maximum character received command to interrupt an issued delay of 160 ms at a 300-baud rate with a 12-bit character.
2. Character times are calculated by using the RCLK input for a clock signal (makes the delay proportional to the baud rate).
3. When a time-out interrupt has occurred, it is cleared and the timer is cleared when the microprocessor reads one character from the receiver FIFO.
4. When a time-out interrupt has not occurred, the time-out timer is cleared after a new character is received or after the microprocessor reads the receiver FIFO.

When the transmitter FIFO and THRE interrupt are enabled (FCR0 = 1, IER1 = 1), transmit interrupts occur as follows:

1. The transmitter holding register empty interrupt [IIR (3 -0) = 2] occurs when the transmit FIFO is empty. It is cleared [IIR (3 -0) = 1] when the THR is written to (1 to 16 characters may be written to the transmit FIFO while servicing this interrupt) or the IIR is read.
2. The transmitter holding register empty interrupt is delayed one character time minus the last stop bit time when there have not been at least two bytes in the transmitter FIFO at the same time since the last time that the FIFO was empty. The first transmitter interrupt after changing FCR0 is immediate if it is enabled.

FIFO Polled Mode Operation

With FCR0 = 1 (transmitter and receiver FIFOs enabled), clearing IER0, IER1, IER2, IER3, or all four to 0 puts the ACE in the FIFO polled mode of operation. Because the receiver and transmitter are controlled separately, either one or both can be in the polled mode of operation.

In this mode, the user program checks receiver and transmitter status using the LSR. As stated previously:

- LSR0 is set as long as one byte is in the receiver FIFO.
- LSR1 -LSR 4 specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode; the IIR is not affected since IER2 = 0.
- LSR5 indicates when the THR is empty.
- LSR6 indicates that both the THR and TSR are empty.
- LSR7 indicates whether any errors are in the receiver FIFO.

  There is no trigger level reached or time-out condition indicated in the FIFO polled mode. However, the receiver and transmitter FIFOs are still fully capable of holding characters.

Interrupt Enable Register (IER)

The IER enables each of the five types of interrupts (see Table 5) and enables INTRPT in response to an interrupt generation. The IER can also disable the interrupt system by clearing bits 0 through 3. The contents of this register are summarized in Table 3 and are described in the following bullets.

- Bit 0: When set, this bit enables the received data available interrupt.
- Bit 1: When set, this bit enables the THRE interrupt.
- Bit 2: When set, this bit enables the receiver line status interrupt.
- Bit 3: When set, this bit enables the modem status interrupt.
- Bits 4 through 7: These bits are not used (always cleared).

Interrupt Identification Register (IIR)

The ACE has an on-chip interrupt generation and prioritization capability that permits a flexible interface with the most popular microprocessors.

The ACE provides four prioritized levels of interrupts:

- Priority 1 -Receiver line status (highest priority)
- Priority 2 -Receiver data ready or receiver character time-out
- Priority 3 -Transmitter holding register empty
  - Priority 4 -Modem status (lowest priority)
  - When an interrupt is generated, the IIR indicates that an interrupt is pending and encodes the type of interrupt in its three least significant bits (bits 0, 1, and 2). The contents of this register are summarized in Table 3 and described in Table 5. Detail on each bit is as follows:
- Bit 0: This bit is used either in a hardwire prioritized or polled interrupt system. When bit 0 is cleared, an interrupt is pending. If bit 0 is set, no interrupt is pending.
- Bits 1 and 2: These two bits identify the highest priority interrupt pending as indicated in Table 3.
- Bit 3: This bit is always cleared in TL16C450 mode. In FIFO mode, bit 3 is set with bit 2 to indicate that a time-out interrupt is pending.
- Bits 4 and 5: These two bits are not used (always cleared).
- Bits 6 and 7: These bits are always cleared in TL16C450 mode. They are set when bit 0 of the FIFO control register is set.

Table 5. Interrupt Control Functions

INTERRUPT IDENTIFICATION REGISTER				PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET METHOD
BIT 3	BIT 2	BIT 1	BIT 0				
0	0	0	1	None	None	None	None
0	1	1	0	1	Receiver line status	Overrun error, parity error, framing error, or break interrupt	Read the line status register
0	1	0	0	2	Received data available	Receiver data available in the TL16C450 mode or trigger level reached in the FIFO mode	Read the receiver buffer register
1	1	0	0	2	Character time-out indication	No characters have been removed from or input to the receiver FIFO during the last four character times, and there is at least one character in it during this time	Read the receiver buffer register
0	0	1	0	3	Transmitter holding register empty	Transmitter holding register empty	Read the interrupt identification register (if source of interrupt) or writing into the transmitter holding register
0	0	0	0	4	Modem status	Clear to send, data set ready, ring indicator, or data carrier detect	Read the modem status register

Line Control Register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the LCR. In addition, the programmer is able to retrieve, inspect, and modify the contents of the LCR; this eliminates the need for separate storage of the line characteristics in system memory. The contents of this register are summarized in Table 3 and described in the following bulleted list.

- Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. These bits are encoded as shown in Table 6.

Table 6. Serial Character Word Length

BIT 1	BIT 0	WORD LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

- Bit 2: This bit specifies either one, one and one-half, or two stop bits in each transmitted character. When bit 2 is cleared, one stop bit is generated in the data. When bit 2 is set, the number of stop bits generated is dependent on the word length selected with bits 0 and 1. The receiver clocks only the first stop bit regardless of the number of stop bits selected. The number of stop bits generated in relation to word length and bit 2 are shown in Table 7.

Table 7. Number of Stop Bits Generated

BIT 2	Word Length Selectedby Bits 1 and 2	Number of Stop Bits Generated
0	Any word length	1
1	5 bits	1 1/2
1	6 bits	2
1	7 bits	2
1	8 bits	2

- Bit 3: This bit is the parity enable bit. When bit 3 is set, a parity bit is generated in transmitted data between the last data word bit and the first stop bit. In received data, if bit 3 is set, parity is checked. When bit 3 is cleared, no parity is generated or checked.
- Bit 4: This bit is the even parity select bit. When parity is enabled (bit 3 is set) and bit 4 is set, even parity (an even number of logic 1s in the data and parity bits) is selected. When parity is enabled and bit 4 is cleared, odd parity (an odd number of logic 1s) is selected.
- Bit 5: This bit is the stick parity bit. When bits 3, 4, and 5 are set, the parity bit is transmitted and checked as cleared. When bits 3 and 5 are set and bit 4 is cleared, the parity bit is transmitted and checked as set. If bit 5 is cleared, stick parity is disabled.
- Bit 6: This bit is the break control bit. Bit 6 is set to force a break condition; i.e., a condition where TX is forced to the spacing (cleared) state. When bit 6 is cleared, the break condition is disabled and has no effect on the transmitter logic; it only effects TX.
- Bit 7: This bit is the divisor latch access bit (DLAB). Bit 7 must be set to access the divisor latches of the baud generator during a read or write. Bit 7 must be cleared during a read or write to access the receiver buffer, the THR, or the IER.

NOTE

The line status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment.

The LSR provides information to the CPU concerning the status of data transfers. The contents of this register are summarized in Table 3 and described in the following bulleted list.

- Bit 0: This bit is the data ready (DR) indicator for the receiver. DR is set whenever a complete incoming character has been received and transferred into the RBR or the FIFO. DR is cleared by reading all of the data in the RBR or the FIFO.

NOTE

Bits 1 through 4 are the error conditions that produce a receiver line status interrupt.

- Bit 1: This bit is the overrun error (OE) indicator. When OE is set, it indicates that before the character in the RBR was read, it was overwritten by the next character transferred into the register. OE is cleared every time the CPU reads the contents of the LSR. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error occurs only after the FIFO is full, and the next character has been completely received in the shift register. An overrun error is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but it is not transferred to the FIFO.
- Bit 2: This bit is the parity error (PE) indicator. When PE is set, it indicates that the parity of the received data character does not match the parity selected in the LCR (bit 4). PE is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO.
- Bit 3: This bit is the framing error (FE) indicator. When FE is set, it indicates that the received character did not have a valid (set) stop bit. FE is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. The ACE tries to resynchronize after a framing error. To accomplish this, it is assumed that the framing error is due to the next start bit. The ACE samples this start bit twice and then accepts the input data.
- Bit 4: This bit is the break interrupt (BI) indicator. When BI is set, it indicates that the received data input was held low for longer than a full-word transmission time. A full-word transmission time is defined as the total time to transmit the start, data, parity, and stop bits. BI is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. When a break occurs, only one 0 character is loaded into the FIFO. The next character transfer is enabled after RX goes to the marking state for at least two RCLK samples and then receives the next valid start bit.
- Bit 5: This bit is the THRE indicator. THRE is set when the THR is empty, indicating that the ACE is ready to accept a new character. If the THRE interrupt is enabled when THRE is set, an interrupt is generated. THRE is set when the contents of the THR are transferred to the TSR. THRE is cleared concurrent with the loading of the THR by the CPU. In the FIFO mode, THRE is set when the transmit FIFO is empty; it is cleared when

at least one byte is written to the transmit FIFO.

- Bit 6: This bit is the transmitter empty (TEMT) indicator. TEMT bit is set when the THR and the TSR are both empty. When either the THR or the TSR contains a data character, TEMT is cleared. In the FIFO mode, TEMT is set when the transmitter FIFO and shift register are both empty.
- Bit 7: In the TL16C450 mode, this bit is always cleared. In the FIFO mode, LSR7 is set when there is at least one parity, framing, or break error in the FIFO. It is cleared when the microprocessor reads the LSR and there are no subsequent errors in the FIFO.

Modem Control Register (MCR)

The MCR is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modem. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit (DTR) controls the DTR output.
- Bit 1: This bit (RTS) controls the RTS output.
- Bit 2: This bit (OUT1) is reserved for output and can also be used for loopback mode.
- Bit 3: This bit (OUT2) controls the high-impedance state output buffer for the INT signal and the OP output. When low, the INT signal is in a high-impedance state and OP is high. When high, the INT signal is enabled and OP is low.
- Bit 4: This bit (LOOP) provides a local loop back feature for diagnostic testing of the ACE. When LOOP is set, the following occurs:
  - The transmitter TX is set high.
  - The receiver RX is disconnected.
  - The output of the TSR is looped back into the receiver shift register input.
  - The four modem control inputs (CTS, DSR, CD, and RI) are disconnected.
  - The four modem control outputs (DTR, RTS, OUT1, and OUT2) are internally connected to the four modem control inputs.
  - The four modem control outputs are forced to the inactive (high) levels.
- Bit 5: This bit (AFE) is the autoflow control enable. When set, the autoflow control as described in the detailed description is enabled. In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify the transmit and receive data paths to the ACE. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but the modem control interrupt's sources are now the lower four bits of the MCR instead of the four modem control inputs. All interrupts are still controlled by the IER.

  The ACE flow can be configured by programming bits 1 and 5 of the MCR as shown in Table 8.

Table 8. ACE Flow Configuration

MCR BIT 5 (AFE)	MCR BIT 1 (RTS)	ACE FLOW CONFIGURATION
1	1	Auto-$\overline{\text{RTS}}$ and auto-$\overline{\text{CTS}}$ enabled (autoflow control enabled)
1	0	Auto-$\overline{\text{CTS}}$ only enabled
0	X	Auto-$\overline{\text{RTS}}$ and auto-$\overline{\text{CTS}}$ disabled

Modem Status Register (MSR)

The MSR is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the CPU. Additionally, four bits of this register provide change information; when a control input from the modem changes state, the appropriate bit is set. All four bits are cleared when the CPU reads the MSR. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit is the change in clear-to-send (ΔCTS) indicator. ΔCTS indicates that the $\overline{CTS}$ input has changed state since the last time it was read by the CPU. When ΔCTS is set (autoflow control is not enabled and the modem status interrupt is enabled), a modem status interrupt is generated. When autoflow control is enabled (ΔCTS is cleared), no interrupt is generated.
- Bit 1: This bit is the change in data set ready (ΔDSR) indicator. ΔDSR indicates that the $\overline{DSR}$ input has changed state since the last time it was read by the CPU. When ΔDSR is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 2: This bit is the trailing edge of the ring indicator (TERI) detector. TERI indicates that the $\overline{RI}$ input to the chip has changed from a low to a high level. When TERI is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 3: This bit is the change in data carrier detect (ΔDCD) indicator. ΔDCD indicates that the DCD input to the chip has changed state since the last time it was read by the CPU. When ΔDCD is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 4: This bit is the complement of the clear-to-send ($\overline{CTS}$) input. When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 1 (RTS).
- Bit 5: This bit is the complement of the data set ready ($\overline{DSR}$) input. When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 0 (DTR).
- Bit 6: This bit is the complement of the ring indicator ($\overline{RI}$) input. When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 2 (OUT1).
- Bit 7: This bit is the complement of the data carrier detect ($\overline{DCD}$) input. When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 3 (OUT2).

Programmable Baud Generator

The ACE contains a programmable baud generator that takes a clock input in the range between dc and 16 MHz and divides it by a divisor in the range between 1 and (216 -1). The output frequency of the baud generator is sixteen times (16 ×) the baud rate. The formula for the divisor is:

divisor = XIN frequency input P (desired baud rate × 16)

Two 8-bit registers, called divisor latches, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the ACE in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load.

Table 9 and Table 10 illustrate the use of the baud generator with crystal frequencies of 1.8432 MHz and 3.072 MHz respectively. For baud rates of 38.4 kbits/s and below, the error obtained is small. The accuracy of the selected baud rate is dependent on the selected crystal frequency (see Figure 27 for examples of typical clock circuits).

Table 9. Baud Rates Using a 1.8432-MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19200	6	
38400	3	
56000	2	2.86

Table 10. Baud Rates Using a 3.072-MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	
75	2560	
110	1745	0.026
134.5	1428	0.034
150	1280	
300	640	
600	320	
1200	160	
1800	107	0.312
2000	96	
2400	80	
3600	53	0.628
4800	40	
7200	27	1.23
9600	20	
19200	10	
38400	5	

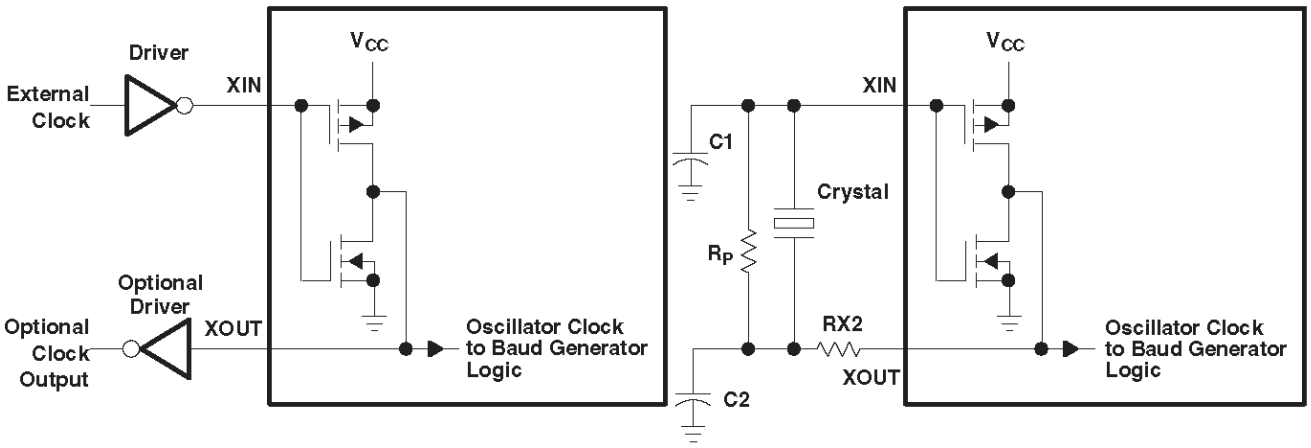


Figure 27. Typical Clock Circuits

Table 11. Typical Crystal Oscillator Network

Crystal	R_P	RX2 (Optional)	C1	C2
3.072 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF
1.8432 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF
16 MHz	1 MΩ	0 kΩ	33 pF	33 pF

Receiver Buffer Register (RBR)

The ACE receiver section consists of a receiver shift register (RSR) and a RBR. The RBR is actually a 16-byte FIFO. Timing is derived from the input clock divided by the programmed devisor. Receiver section control is a function of the ACE line control register.

The ACE RSR receives serial data from RX. The RSR then concatenates the data and moves it into the RBR FIFO. In the TL16C450 mode, when a character is placed in the RBR and the received data available interrupt is enabled (IER0 = 1), an interrupt is generated. This interrupt is cleared when the data is read out of the RBR. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

Scratch Register

The scratch register is an 8-bit register that is intended for the programmer's use as a scratchpad in the sense that it temporarily holds the programmer's data without affecting any other ACE operation.

Transmitter Holding Register (THR)

The ACE transmitter section consists of a THR and a transmitter shift register (TSR). The THR is actually a 16-byte FIFO. Timing is derived from the input clock divided by the programmed devisor. Transmitter section control is a function of the ACE line control register.

The ACE THR receives data off the internal data bus and when the shift register is idle, moves it into the TSR. The TSR serializes the data and outputs it at TX. In the TL16C450 mode, if the THR is empty and the transmitter holding register empty (THRE) interrupt is enabled (IER1 = 1), an interrupt is generated. This interrupt is cleared when a character is loaded into the register. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

Table 12. Typical Package Thermal Resistance Data

PACKAGE		
48-Pin TQFP PFB	θ_{JA} = 50.1°C/W	θ_{JC} = 21.1°C/W
32-Pin TQFP RHB	θ_{JA} = xx°C/W	θ_{JC} = xx°C/W
44-Pin PLCC FN	θ_{JA} = 46.2°C/W	θ_{JC} = 22°C/W

Table 13. Typical Package Weight

PACKAGE	WEIGHT IN GRAMS
48-Pin TQFP PFB	0.2
32-Pin TQFP RHB	0.15
44-Pin PLCC FN	0.5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL16C2550IPFB	ACTIVE	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2550IPFB	Samples
TL16C2550IPFBG4	ACTIVE	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2550IPFB	Samples
TL16C2550IPFBR	ACTIVE	TQFP	PFB	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2550IPFB	Samples
TL16C2550IRHB	ACTIVE	VQFN	RHB	32	73	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2550I	Samples
TL16C2550IRHBG4	ACTIVE	VQFN	RHB	32	73	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2550I	Samples
TL16C2550IRHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2550I	Samples
TL16C2550PFB	ACTIVE	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	2550PFB PG_1.1	Samples
TL16C2550PFBG4	ACTIVE	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	2550PFB PG_1.1	Samples
TL16C2550PFBR	ACTIVE	TQFP	PFB	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	2550PFB PG_1.1	Samples
TL16C2550RHB	ACTIVE	VQFN	RHB	32	73	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	2550 RHB	Samples
TL16C2550RHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	2550 RHB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TL16C2550 :

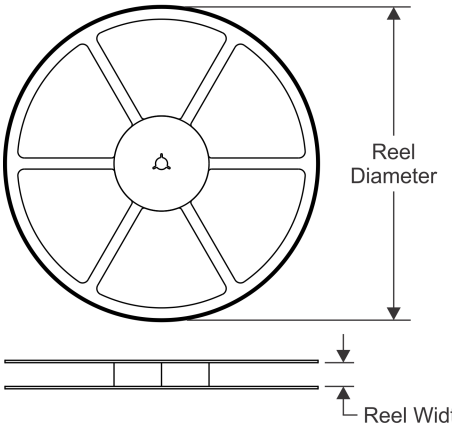
- Automotive: TL16C2550-Q1

NOTE: Qualified Version Definitions:

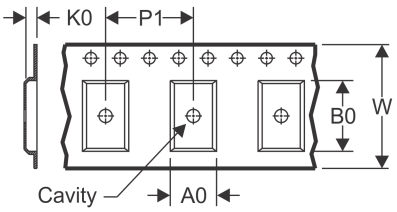
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

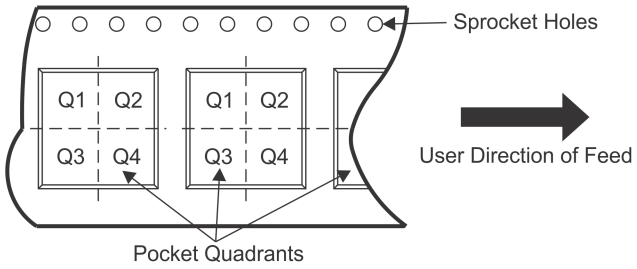


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

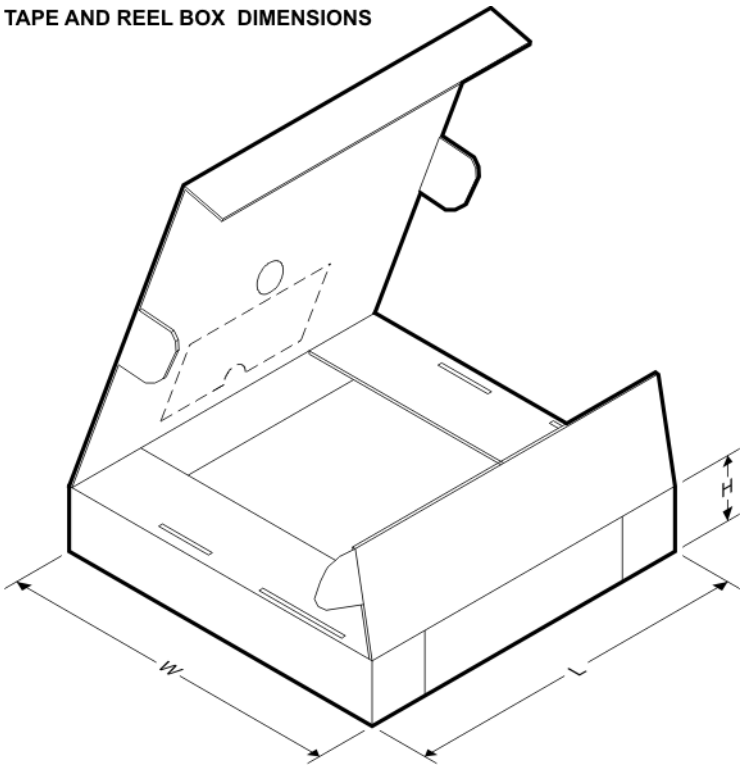
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL16C2550IPFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
TL16C2550IRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TL16C2550PFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
TL16C2550RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL16C2550IPFBR	TQFP	PFB	48	1000	350.0	350.0	43.0
TL16C2550IRHBR	VQFN	RHB	32	3000	350.0	350.0	43.0
TL16C2550PFBR	TQFP	PFB	48	1000	350.0	350.0	43.0
TL16C2550RHBR	VQFN	RHB	32	3000	350.0	350.0	43.0

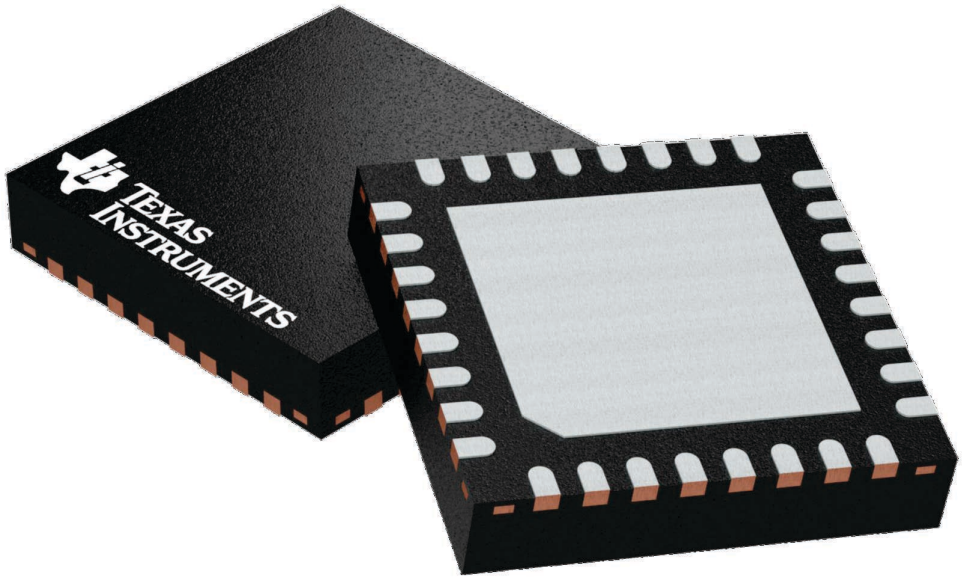
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

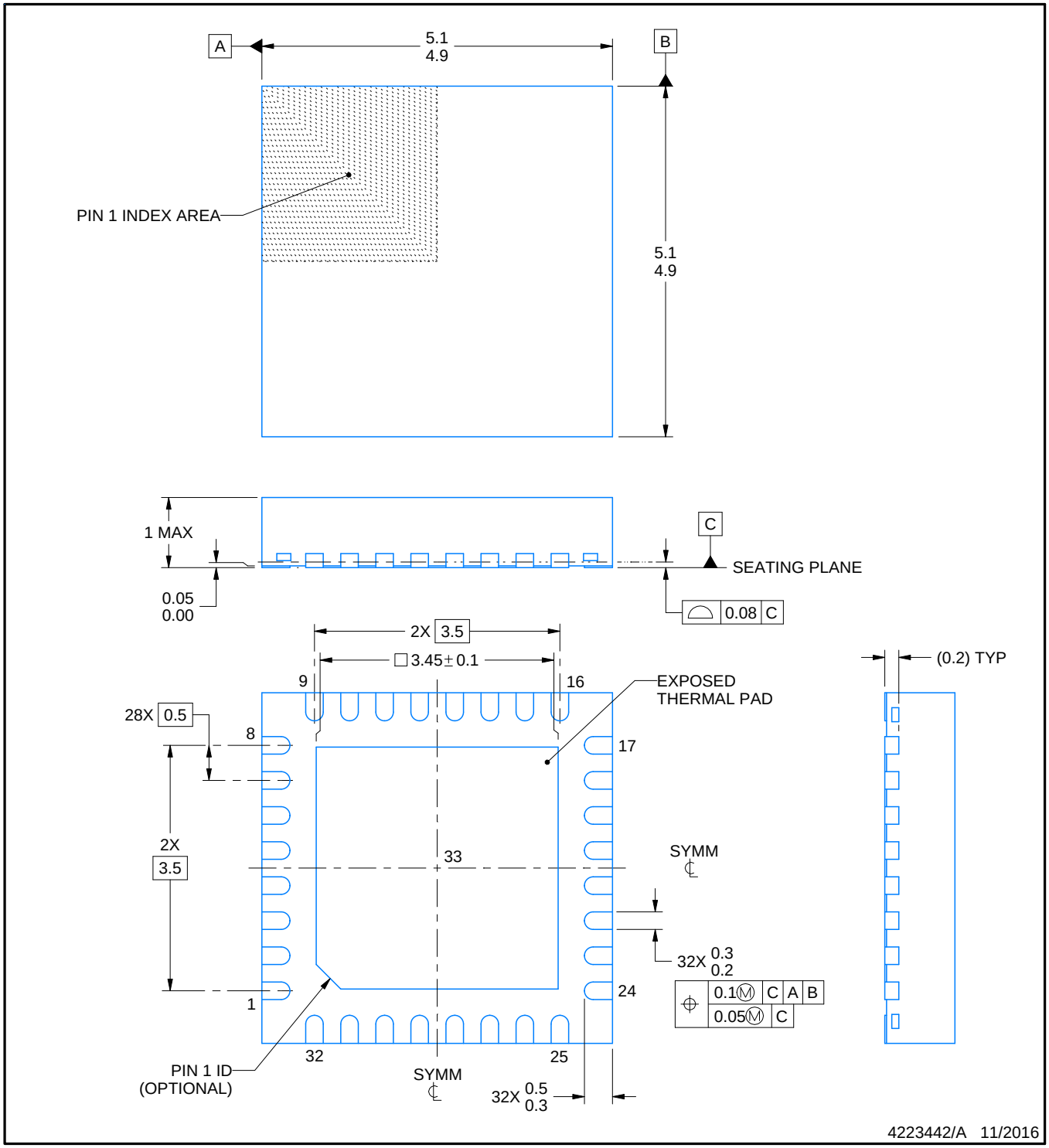
4224745/A

RHB0032E

PACKAGE OUTLINE

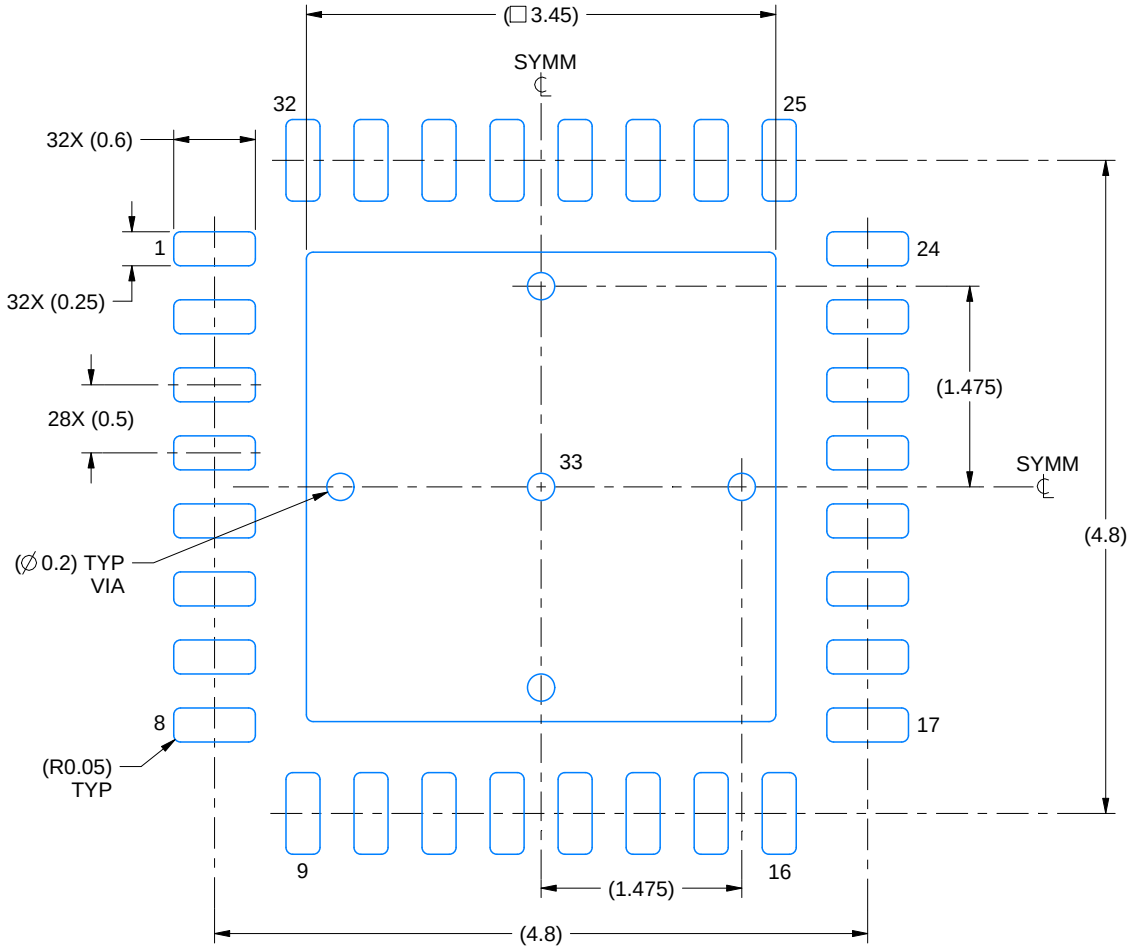
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

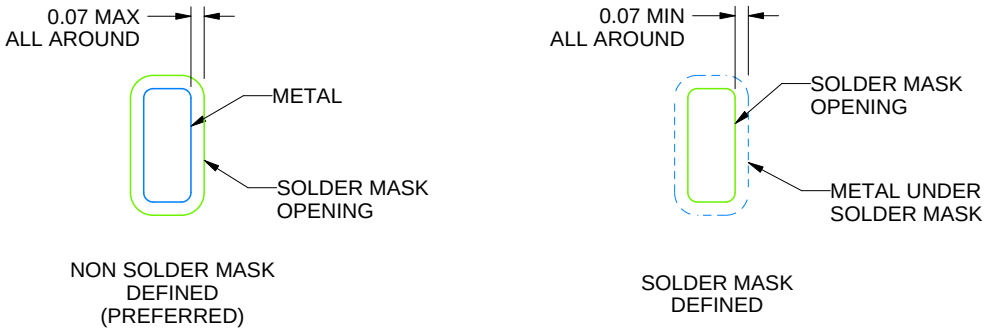


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

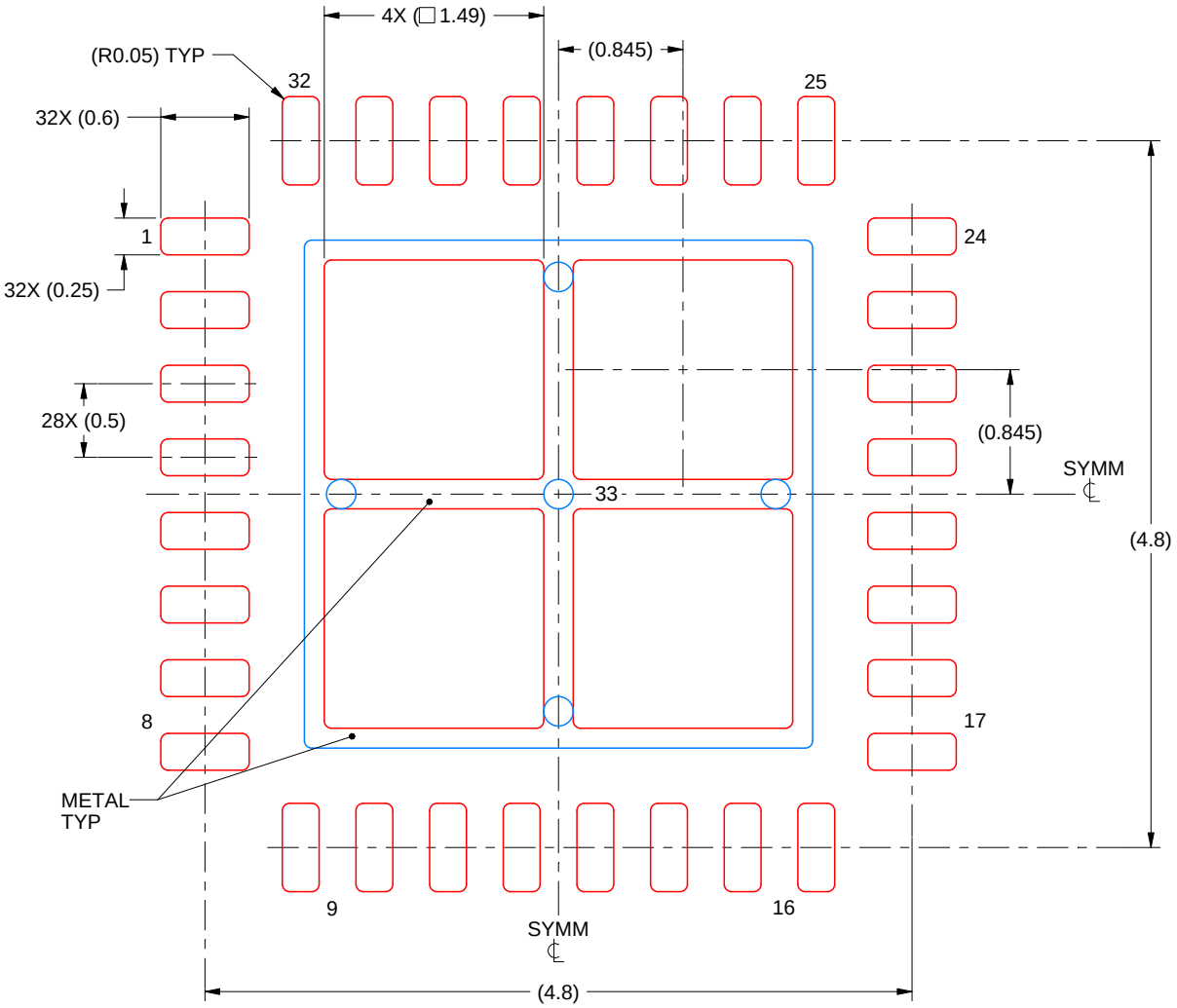


SOLDER MASK DETAILS

4223442/A 11/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

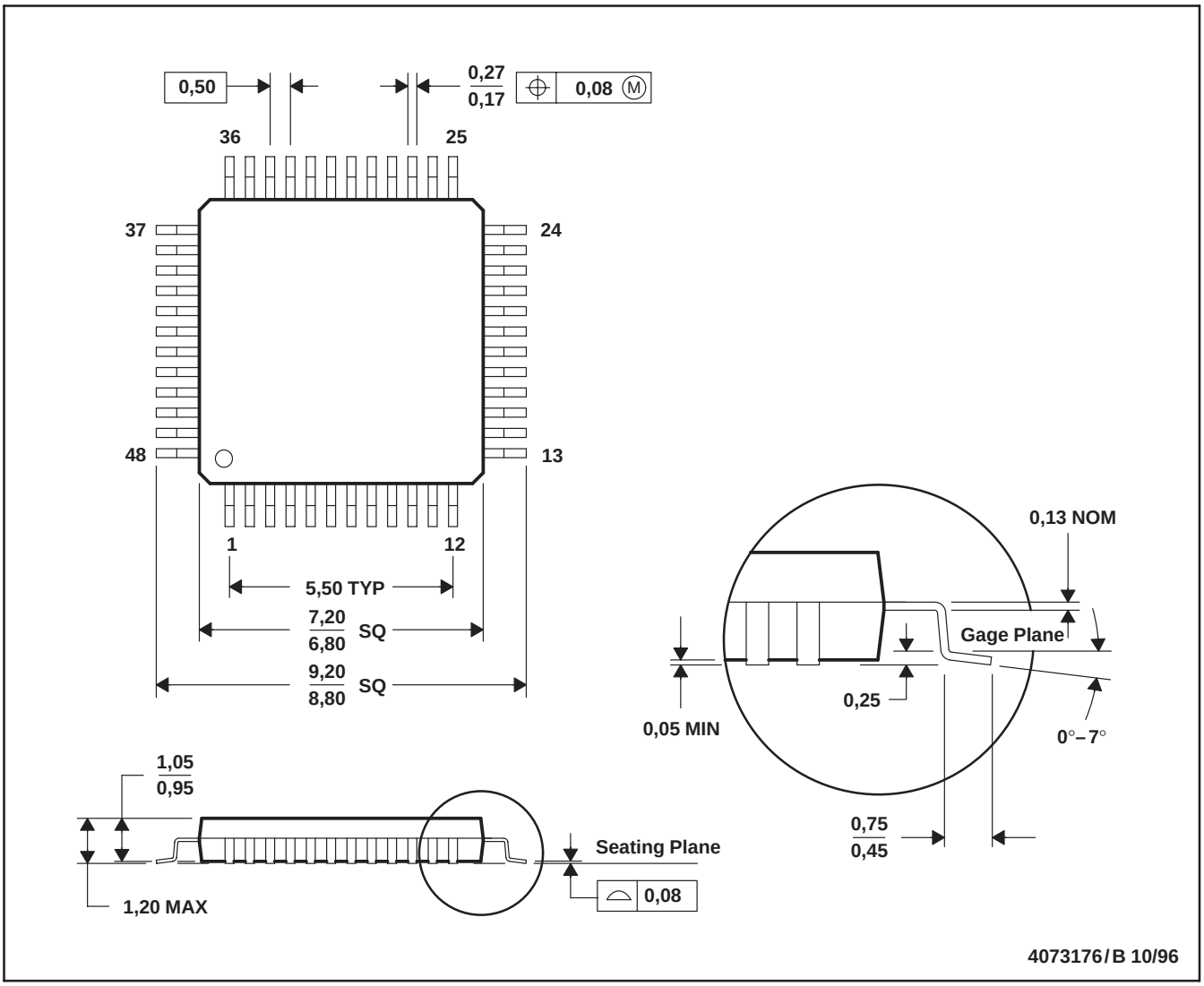
4223442/A 11/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

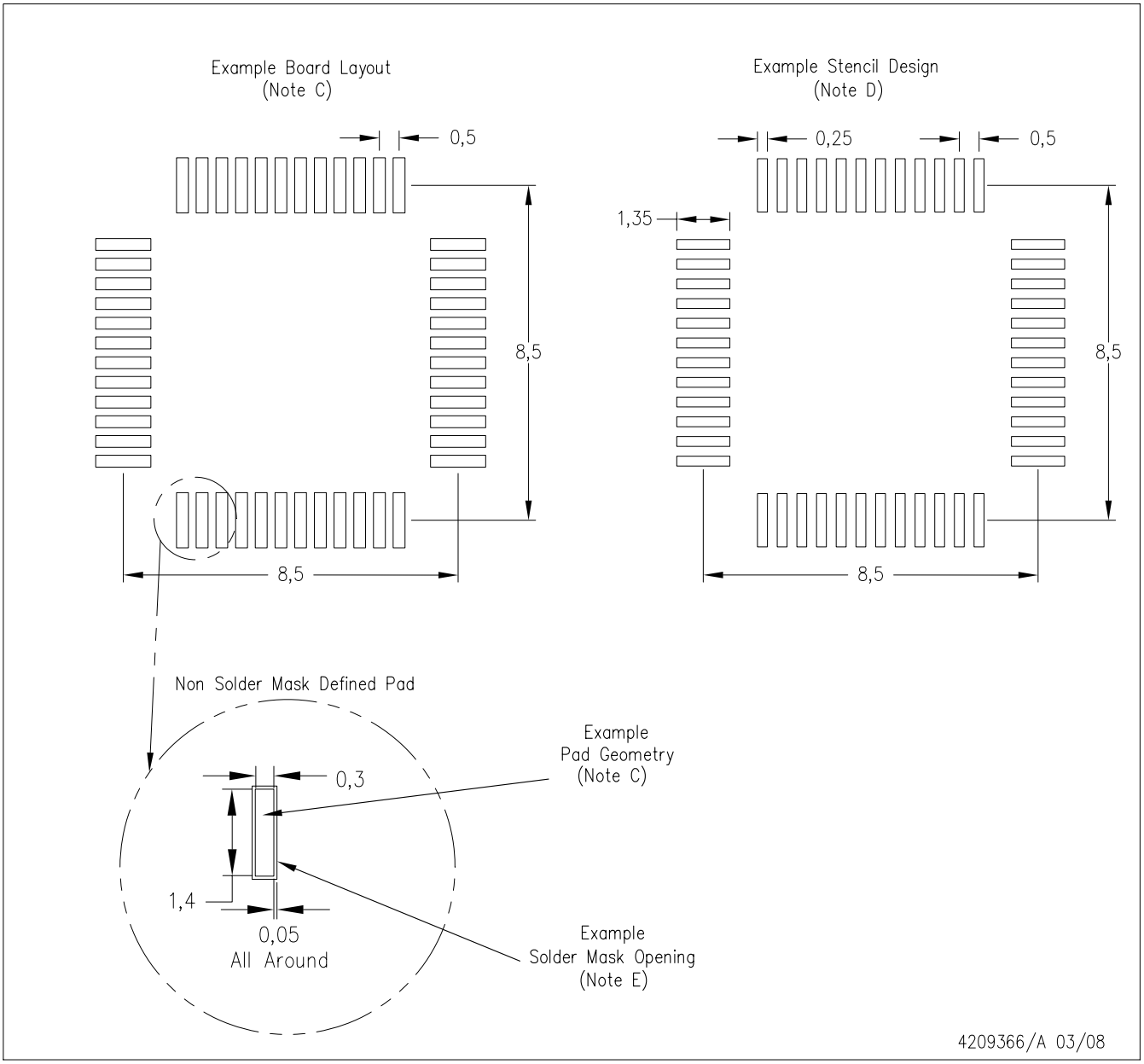
MTQF019A – JANUARY 1995 – REVISED JANUARY 1998

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PFB (S–PQFP–G48)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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