THE DATASHEET OF

TISP61089BDR-S

DUAL FORWARD-CONDUCTING P-GATE THYRISTORS PROGRAMMABLE OVERVOLTAGE PROTECTORS

TISP61089B High Voltage Ringing SLIC Protector

Dual Voltage-Programmable Protectors
- **Supports Battery Voltages Down to -155 V**
- **Low 5 mA max. Gate Triggering Current**
- **High 150 mA min. Holding Current**

Rated for LSSGR '1089 Conditions

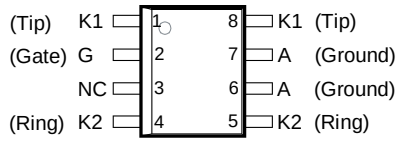
Impulse Waveshape	'1089 Test		I_{TSP} A
	Section	Test #	
2/10	4.5.7 4.5.8	4 1	120
10/360	4.5.7	2, 5	30
10/1000	4.5.7	1, 3	30

60 Hz Power Fault Times	'1089 Test		I_{TSM} A
	Section	Test #	
0.5	4.5.12	9	6.5
1	4.5.12	3, 4, 8	4.6
2	4.5.12	7	3.4
5	4.5.12 4.5.13	5 2, 3	2.3
30	4.5.12	6	1.3
900	4.5.12 4.5.13 4.5.15/16	1,2 1, 4, 5	0.73

2/10 Overshoot Voltage Specified

Element	I_{TM} = 100 A, di/dt = 80 A/µs V
Diode	10
SCR	12

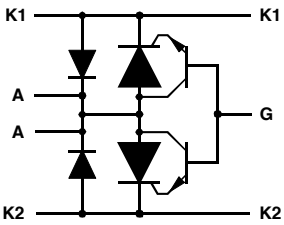
D Package (Top View)



MD6XANB

NC - No internal connection
Terminal typical application names shown in parenthesis

Device Symbol



Terminals K1, K2 and A correspond to the alternative line designators of T, R and G or A, B and C. The negative protection voltage is controlled by the voltage, V_{GG}, applied to the G terminal. SD6XAEB

Additional Information

Click these links for more information:

PRODUCT SELECTOR | TECHNICAL LIBRARY | INVENTORY | SAMPLES | CONTACT

Agency Recognition

Description	
UL	File Number: E215609

.....UL Recognized Component

Rated for ITU-T K.20, K.21 and K.45

Waveshape		I_{TSP} A
Voltage	Current	
10/700	5/310	40

How To Order

Device	Package	Carrier	Order As
TISP61089B	D (8-pin Small-Outline)	Embossed Tape Reeled	TISP61089BDR-S

Description

The TISP61089B is a dual forward-conducting buffered p-gate thyristor (SCR) overvoltage protector. It is designed to protect monolithic SLICs (Subscriber Line Interface Circuits) against overvoltages on the telephone line caused by lightning, a.c. power contact and induction. The TISP61089B limits voltages that exceed the SLIC supply rail voltage. The TISP61089B parameters are specified to allow equipment compliance with Bellcore GR-1089-CORE, Issue 2 and ITU-T recommendations K.20, K.21 and K.45.

WARNING Cancer and Reproductive Harm
www.P65Warnings.ca.gov

OCTOBER 2000 – REVISED JULY 2019
*RoHS Directive 2015/863, Mar 31, 2015 and Annex.
Specifications are subject to change without notice.
Users should verify actual device performance in their specific applications.

Description (Continued)

The SLIC line driver section is typically powered from 0 V (ground) and a negative voltage in the region of -20 V to -150 V. The protector gate is connected to this negative supply. This references the protection (clipping) voltage to the negative supply voltage. The protection voltage will then track the negative supply voltage and the overvoltage stress on the SLIC is minimized.

Positive overvoltages are clipped to ground by diode forward conduction. Negative overvoltages are initially clipped close to the SLIC negative supply rail value. If sufficient current is available from the overvoltage, then the protector SCR will switch into a low voltage on-state condition. As the overvoltage subsides, the high holding current of TISP61089B SCR helps prevent d.c. latchup.

The TISP61089B is intended to be used with a series combination of a 40 Ω or higher resistance and a suitable overcurrent protector. Power fault compliance requires the series overcurrent element to open-circuit or become high impedance (see Applications Information). For equipment compliant to ITU-T recommendations K.20 or K.21 or K.45 only, the series resistor value is set by the coordination requirements. For coordination with a 400 V limit GDT, a minimum series resistor value of 10 Ω is recommended.

These monolithic protection devices are fabricated in ion-implanted planar vertical power structures for high reliability and in normal system operation they are virtually transparent. The TISP61089B buffered gate design reduces the loading on the SLIC supply during overvoltages caused by power cross and induction. The TISP61089B is available in a 8-pin plastic small-outline surface mount package.

Absolute Maximum Ratings, -40 °C ≤ T_J ≤ 85 °C (Unless Otherwise Noted)

Rating	Symbol	Value	Unit
Repetitive peak off-state voltage, V_{GK} = 0	V_{DRM}	-170	V
Repetitive peak gate-cathode voltage, V_{KA} = 0	V_{GKRM}	-167	V
Non-repetitive peak on-state pulse current (see Notes 1 and 2)			
10/1000 µs (Telcordia (Bellcore) GR-1089-CORE, Issue 2, February 1999, Section 4)	I_{TSP}	30	A
5/320 µs (ITU-T K.20, K.21& K.45, K.44 open-circuit voltage wave shape 10/700 µs)		40	
10/360 µs (Telcordia (Bellcore) GR-1089-CORE, Issue 2, February 1999, Section 4)		40	
1.2/50 µs (Telcordia (Bellcore) GR-1089-CORE, Issue 2, February 1999, Section 4)		100	
2/10 µs (Telcordia (Bellcore) GR-1089-CORE, Issue 2, February 1999, Section 4) T_J = 25 °C		120 170	
Non-repetitive peak on-state current, 60 Hz (see Notes 1, 2 and 3)			
0.5 s	I_{TSM}	6.5	A
1 s		4.6	
2 s		3.4	
5 s		2.3	
30 s		1.3	
900 s		0.73	
Non-repetitive peak gate current, 1/2 µs pulse, cathodes commoned (see Notes 1 and 2)	I_{GSM}	+40	A
Operating free-air temperature range	T_A	-40 to +85	°C
Junction temperature	T_J	-40 to +150	°C
Storage temperature range	T_{stg}	-40 to +150	°C

NOTES: 1. Initially, the protector must be in thermal equilibrium with -40 °C ≤ T_J ≤ 85 °C. The surge may be repeated after the device returns to its initial conditions.
2. The rated current values may be applied either to the Ring to Ground or to the Tip to Ground terminal pairs. Additionally, both terminal pairs may have their rated current values applied simultaneously (in this case the Ground terminal current will be twice the rated current value of an individual terminal pair). Above 85 °C, derate linearly to zero at 150 °C lead temperature.
3. Values for V_{GG} = -100 V. For values at other voltages see Figure 2.

Recommended Operating Conditions

Component		Min	Typ	Max	Unit
C_G	TISP61089B gate decoupling capacitor	100	220		nF
R_S	TISP61089B series resistor for GR-1089-CORE first-level surge survival	25			Ω
	TISP61089B series resistor for GR-1089-CORE first-level and second-level surge survival	40			Ω
	TISP61089B series resistor for GR-1089-CORE intra-building port surge survival	8			Ω
	TISP61089B series resistor for K.20, K.21 and K.45 coordination with a 400 V primary protector	10			Ω

Electrical Characteristics, T_J = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
I_D	Off-state current	$V_D = V_{DRM}$, V_{GK} = 0	T_J = 25 °C			-5	μA
			T_J = 85 °C			-50	μA
$V_{(BO)}$	Breakover voltage	2/10 μs, I_{TM} = -100 A, di/dt = -80 A/μs, R_S = 50 Ω, V_{GG} = -100 V				-112	V
$V_{GK(BO)}$	Gate-cathode impulse breakover voltage	2/10 μs, I_{TM} = -100 A, di/dt = -80 A/μs, R_S = 50 Ω, V_{GG} = -100 V, (see Note 4)				12	V
V_F	Forward voltage	I_F = 5 A, t_w = 200 μs				3	V
V_{FRM}	Peak forward recovery voltage	2/10 μs, I_F = 100 A, di/dt = 80 A/μs, R_S = 50 Ω, (see Note 4)				10	V
I_H	Holding current	I_T = -1 A, di/dt = 1A/ms, V_{GG} = -100 V		-150			mA
I_{GKS}	Gate reverse current	$V_{GG} = V_{GK} = V_{GKRM}$, V_{KA} = 0	T_J = 25 °C			-5	μA
			T_J = 85 °C			-50	μA
I_{GT}	Gate trigger current	I_T = -3 A, $t_{p(g)} \geq$ 20 μs, V_{GG} = -100 V				5	mA
V_{GT}	Gate-cathode trigger voltage	I_T = -3 A, $t_{p(g)} \geq$ 20 μs, V_{GG} = -100 V				2.5	V
C_{KA}	Cathode-anode off-state capacitance	f = 1 MHz, V_d = 1 V, I_G = 0, (see Note 5)	V_D = -3 V			100	pF
			V_D = -48 V			50	pF

NOTES: 4. The diode forward recovery and the thyristor gate impulse breakover (overshoot) are not strongly dependent of the gate supply voltage value (V_{GG}).

5. These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The unmeasured device terminals are a.c. connected to the guard terminal of the bridge.

Thermal Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
$R_{\theta JA}$	Junction to free air thermal resistance	T_A = 25 °C, EIA/JESD51-3 PCB, EIA/JESD51-2 environment, P_{TOT} = 1.7 W			120	°C/W

Parameter Measurement Information

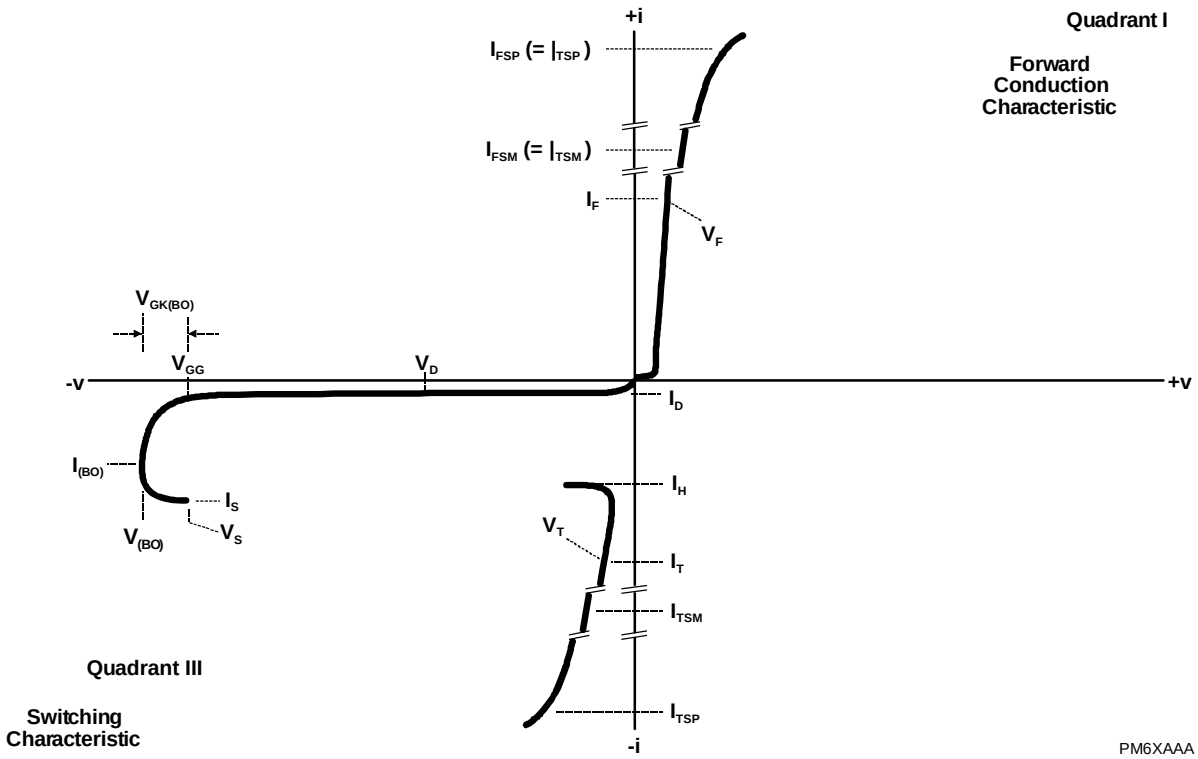


Figure 1. Voltage-Current Characteristic
Unless Otherwise Noted, All Voltages are Referenced to the Anode

Thermal Information

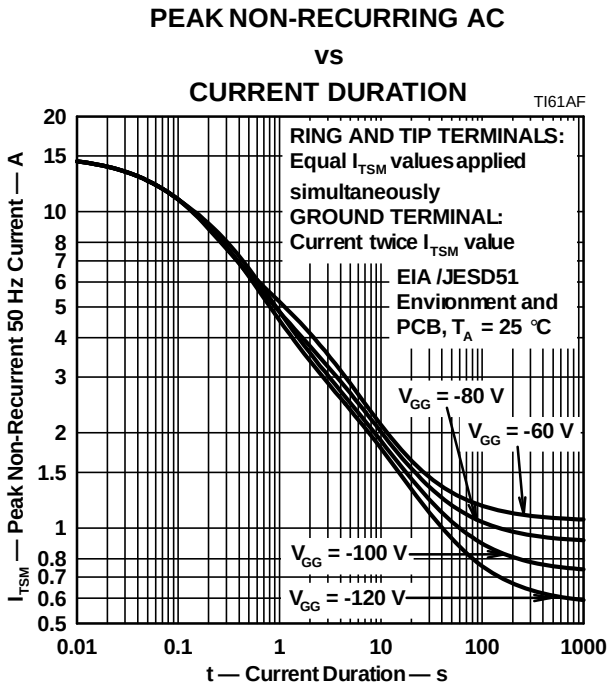


Figure 2. Non-Repetitive Peak On-State Current against Duration

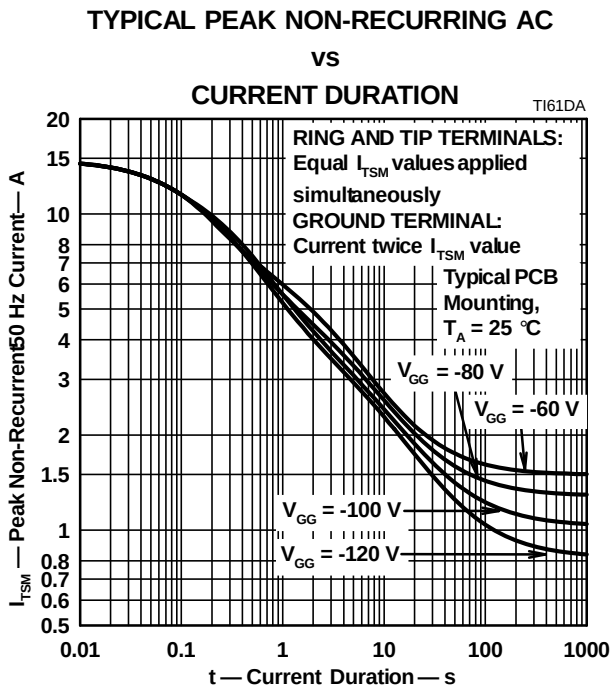


Figure 3. Typical Non-Repetitive Peak On-state Current against Duration

APPLICATIONS INFORMATION

Operation of Ringing SLICs using Multiple Negative Voltage Supply Rails

Figure 4 shows a typical powering arrangement for a multi-supply rail SLIC. V_{BATL} is a lower (smaller) voltage supply than V_{BATH}. With supply switch S1 in the position shown, the line driver amplifiers are powered between 0 V and V_{BATL}. This mode minimizes the power consumption for short loop transmission. For long loops and to generate ringing, the driver voltage is increased by operating S1 to connect V_{BATH}. These conditions are shown in Figure 5.

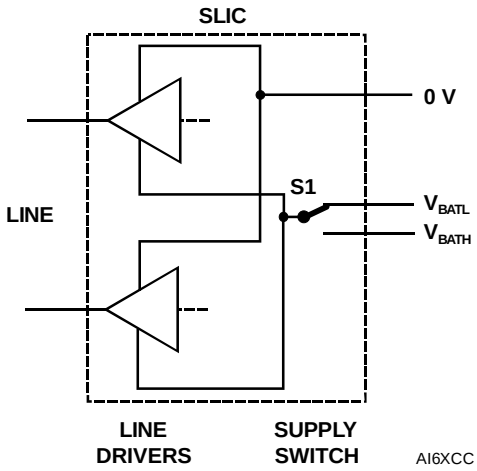


Figure 4. SLIC with Voltage Supply Switching

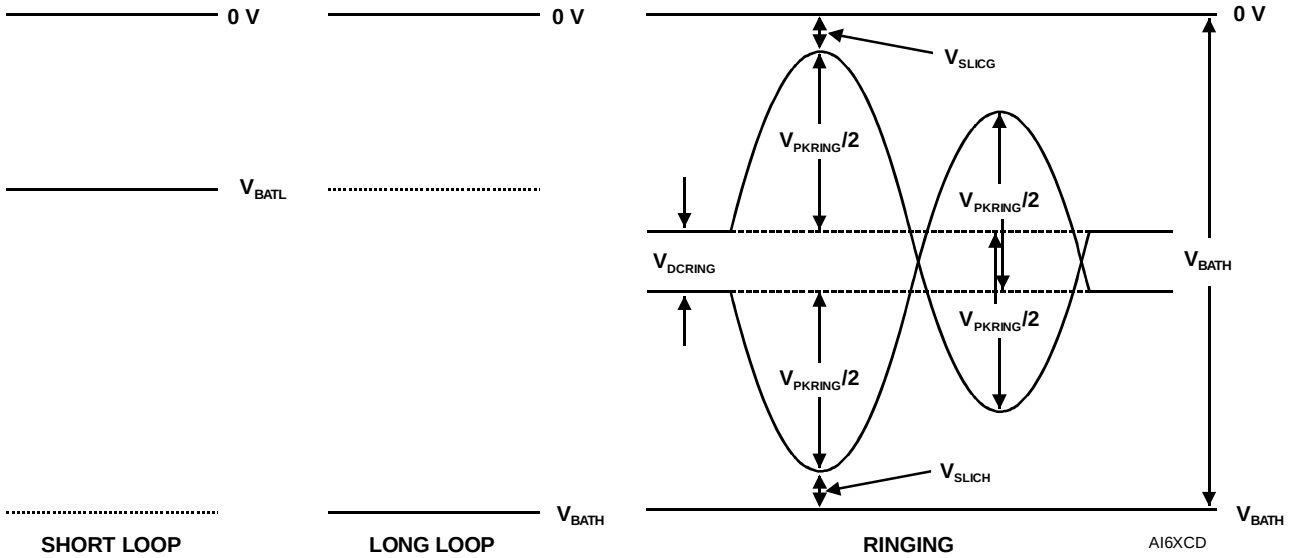


Figure 5. Driver Supply Voltage Levels

Conventional ringing is typically unbalanced ground or battery backed. To minimize the supply voltage required, most multi-rail SLICs use balanced ringing as shown in Figure 5. The ringing has d.c., V_{DCRING}, and a.c., V_{PKRING}, components. A 70 V r.m.s. a.c. sinusoidal ring signal has a peak value, V_{PKRING}, of 99 V. If the d.c. component was 20 V, then the total voltage swing needed would be 99 + 20 = 119 V. There are internal losses in the SLIC from ground, V_{SLICG}, and the negative supply, V_{SLICH}. The sum of these two losses generally amounts to a total of 10 V. This makes a total, V_{BATH}, supply rail value of 119 + 10 = 129 V.

In some cases a trapezoidal a.c. ring signal is used. This would have a peak to r.m.s ratio (crest factor) of about 1.25, increasing the r.m.s. a.c. ring level by 13 %. The d.c. ring voltage may be lowered for short loop applications.

SLIC Parameter Values

The table below shows some details of HV SLICs using multiple negative supply rails.

Manufacturer	INFINEON‡		LEGERITY™‡						Unit
SLIC Series	SLIC-P‡		ISLIC™‡						
SLIC #	PEB 4266		79R241		79R101		79R100		
Data Sheet Issue	14/02/2001		-/08/2000		-/07/2000		-/07/2000		
Short Circuit Current	110		150		150		150		mA
V_{BATH} max.	-155		-104		-104		-104		V
V_{BATL} max.	-150		-104		V_{BATH}		V_{BATH}		V
AC Ringing for:	85		45†		50†		55†		V rms
Crest Factor	1.4		1.4		1.4		1.25		
V_{BATH}	-70		-90		-99		-99		V
V_{BATR}	-150		-36		-24		-24		V
R or T Power Max. < 10 ms	10								W
R or T Overshoot < 10 ms	TBD	TBD	-5	5	-10	5	-10	5	V
R or T Overshoot < 1 ms	-10	+10							V
R or T Overshoot < 1 μs	-10	+30	-10	10	-15	8	-15	8	V
R or T Overshoot < 250 ns			-15	15	-20	12	-20	12	V
Line Feed Resistance	20 + 30		50		50		50		Ω

† Assumes -20 V battery voltage during ringing.
‡ Legerity, the Legerity logo and ISLIC are the trademarks of Legerity, Inc. (formerly AMD's Communication Products Division). Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.

From the table, the maximum supply voltage, V_{BATH}, is -155 V. In terms of minimum voltage overshoot limits, -10 V and +8 V are needed for 1 μs and -15 V, +12 V are needed for 250 ns. To maintain these voltage limits over the temperature range, 25 °C values of -12 V, +10 V are needed for 250 ns.

It is important to define the protector overshoot under the actual circuit current conditions. For example, if the series line feed resistor was 40 Ω, R1 in Figure 12, and Telcordia GR-1089-CORE 2/10 and 10/1000 first-level impulses were applied, the peak protector currents would be 56 A and 20 A. At the second-level, the 2/10 impulse current would be 100 A. Therefore, the protector voltage overshoot should be guaranteed to not exceed the SLIC voltage ratings at 100 A, 2/10 and 20 A, 10/1000. In practice, as the 2/10 waveshape has the highest current (100 A) and fastest di/dt (80 A/μs) the overshoot level testing can restricted to the be 2/10 waveshape.

Using the table values for maximum battery voltage and minimum overshoot gives a protection device requirement of -170 V and +12 V from the output to ground. There needs to be temperature guard banding for the change in protector characteristics with temperature. To cover down to -40 °C, the 25 °C protector minimum values become -185 V (V_{DRM}) on the cathode and -182 V (V_{GKS}) on the gate.

Gated Protectors

This section covers four topics. First, it is explained why gated protectors are needed. Second, the voltage limiting action of the protector is described. Third, how the withstand voltages of the TISP61089B junctions are set. Fourth, an example application circuit is described.

Purpose of Gated Protectors

Fixed voltage thyristor overvoltage protectors have been used since the early 1980s to protect monolithic SLICs (Subscriber Line Interface Circuits) against overvoltages on the telephone line caused by lightning, a.c. power contact and induction. As the SLIC was usually powered from a fixed voltage negative supply rail, the limiting voltage of the protector could also be a fixed value. The TISP1072F3 is a typical example of a fixed voltage SLIC protector.

Gated Protectors (Continued)

SLICs have become more sophisticated. To minimize power consumption, some designs automatically adjust the driver supply voltage to a value that is just sufficient to drive the required line current. For short lines, the supply voltage would be set low, but for long lines, a higher supply voltage would be generated to drive sufficient line current. The optimum protection for this type of SLIC would be given by a protection voltage which tracks the SLIC supply voltage. This can be achieved by connecting the protection thyristor gate to the SLIC V_{BATH} supply, Figure 6. This gated (programmable) protection arrangement minimizes the voltage stress on the SLIC, no matter what value of supply voltage.

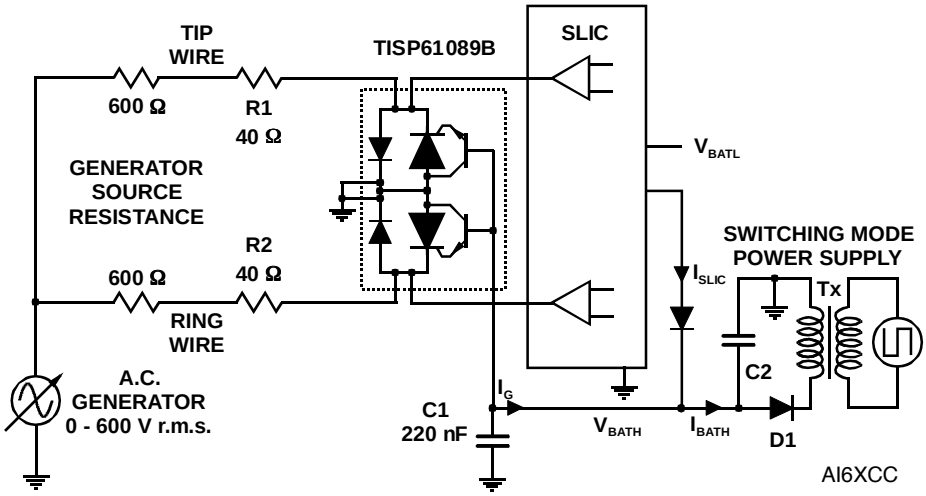


Figure 6. TISP61089B Buffered Gate Protector ('1089 Section 4.5.12 Testing)

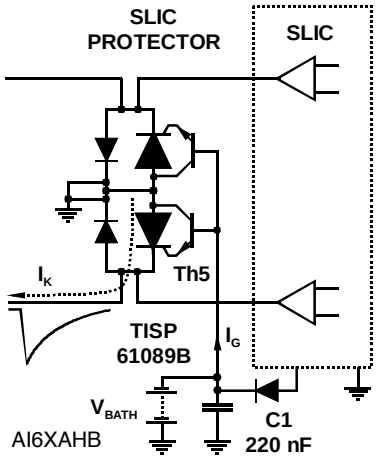


Figure 7. Negative Overvoltage Condition

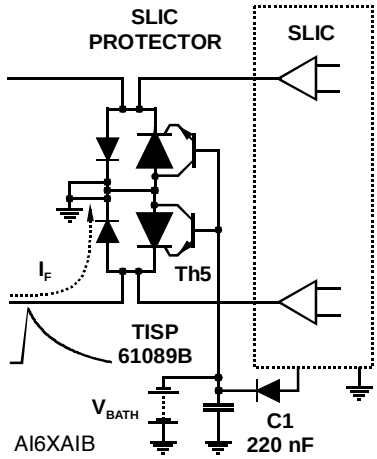


Figure 8. Positive Overvoltage Condition

Operation of Gated Protectors

Figure 7 and Figure 8 show how the TISP61089B limits negative and positive overvoltages. Positive overvoltages (Figure 8) are clipped by the antiparallel diode of Th5 and the resulting current is diverted to ground. Negative overvoltages (Figure 7) are initially clipped close to the SLIC negative supply rail value (V_{BATH}). If sufficient current is available from the overvoltage, then Th5 will switch into a low voltage on-state condition. As the overvoltage subsides the high holding current of Th5 prevents d.c. latchup. The protection voltage will be the sum of the gate supply (V_{BATH}) and the peak gate-cathode voltage ($V_{GK(BO)}$). The protection voltage will be increased if there is a long connection between the gate decoupling capacitor, C1, and the gate terminal. During the initial rise of a fast impulse, the gate current (I_G) is the same as the cathode current (I_K). Rates of 80 A/μs can cause inductive voltages of 0.8 V in 2.5 cm of printed wiring track. To minimize this inductive

Gated Protectors (Continued)

voltage increase of protection voltage, the length of the capacitor to gate terminal tracking should be minimized. Inductive voltages in the protector cathode wiring will also increase the protection voltage. These voltages can be minimized by routing the SLIC connection through the protector as shown in Figure 6.

Figure 9, which has a 10 A/μs rate of impulse current rise, shows a positive gate charge (Q_{GS}) of about 0.1 μC. With the 0.1 μF gate decoupling capacitor used, the increase in gate supply is about 1 V (= Q_{GS}/C1). This change is just visible on the -72 V gate voltage, V_{BATH}. But, the voltage increase does not directly add to the protection voltage as the supply voltage change reaches a maximum at 0.4 μs, when the gate current reverses polarity, and the protection voltage peaks earlier at 0.3 μs. In Figure 9, the peak clamping voltage ($V_{(BO)}$) is -77.5 V, an increase of 5.5 V on the nominal gate supply voltage. This 5.5 V increase is the sum of the supply rail increase at that time, (0.5 V), and the protection circuit's cathode diode to supply rail breakover voltage (5 V). In practice, use of the recommended 220 nF gate decoupling capacitor would give a supply rail increase of about 0.3 V and a $V_{(BO)}$ value of about -77.3 V.

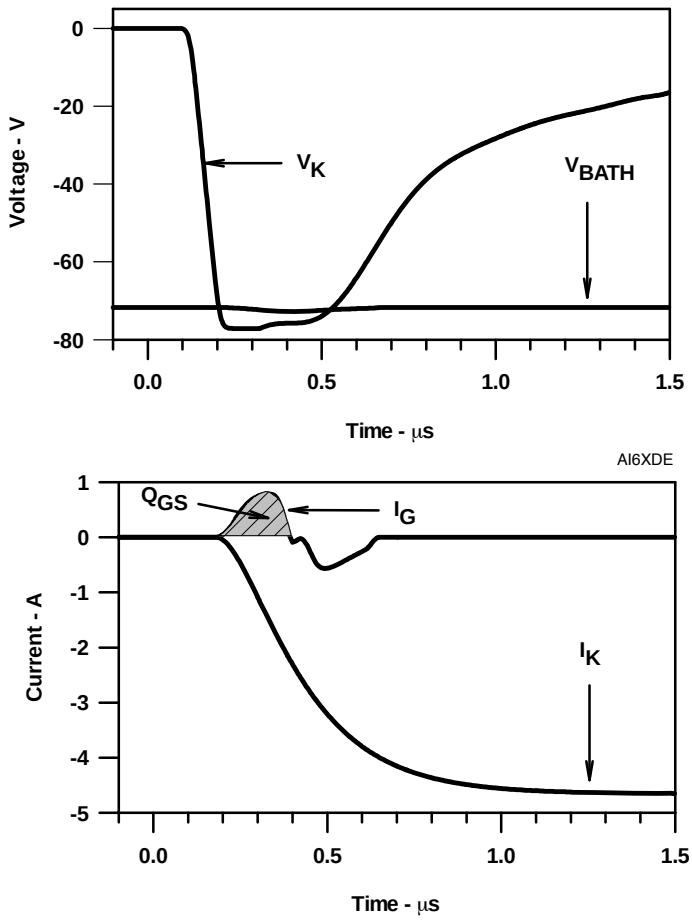


Figure 9. Protector Fast Impulse Clamping and Switching Waveforms

Voltage Stress Levels on the TISP61089B

Figure 10 shows the protector electrodes. The package terminal designated gate, G, is the transistor base, B, electrode connection and so is marked as B (G). The following junctions are subject to voltage stress: Transistor EB and CB, SCR AK (off state) and the antiparallel diode (reverse blocking). This clause covers the necessary testing to ensure the junctions are good.

Testing transistor CB and EB: The maximum voltage stress level for the TISP61089B is V_{BATH} with the addition of the short term antiparallel diode voltage overshoot, V_{FRM}. The current flowing out of the G terminal is measured at V_{BATH} plus V_{FRM}. The SCR K terminal is shorted to the common (0 V) for this test (see Figure 10). The measured current, I_{GKS}, is the sum of the junction currents I_{CB} and I_{EB}.

Gated Protectors (Continued)

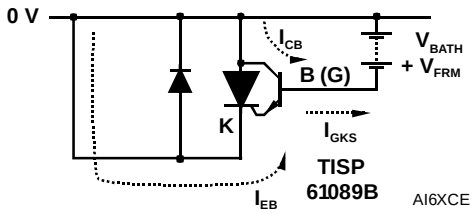
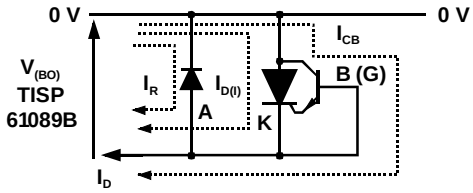


Figure 10. Transistor CB and EB Verification

Testing transistor CB, SCR AK off state and diode reverse blocking: The highest AK voltage occurs during the overshoot period of the protector. To make sure that the SCR and diode blocking junctions do not break down during this period, a d.c. test for off-state current, I_D, can be applied at the overshoot voltage value. To avoid transistor CB current amplification by the transistor gain, the transistor base-emitter is shorted during this test (see Figure 11).



$I_{D(I)}$ is the internal SCR value of I_D

Figure 11. Off-State Current Verification

Summary: Two tests are needed to verify the protector junctions. Maximum current values for I_{GKS} and I_D are required at the specified applied voltage conditions.

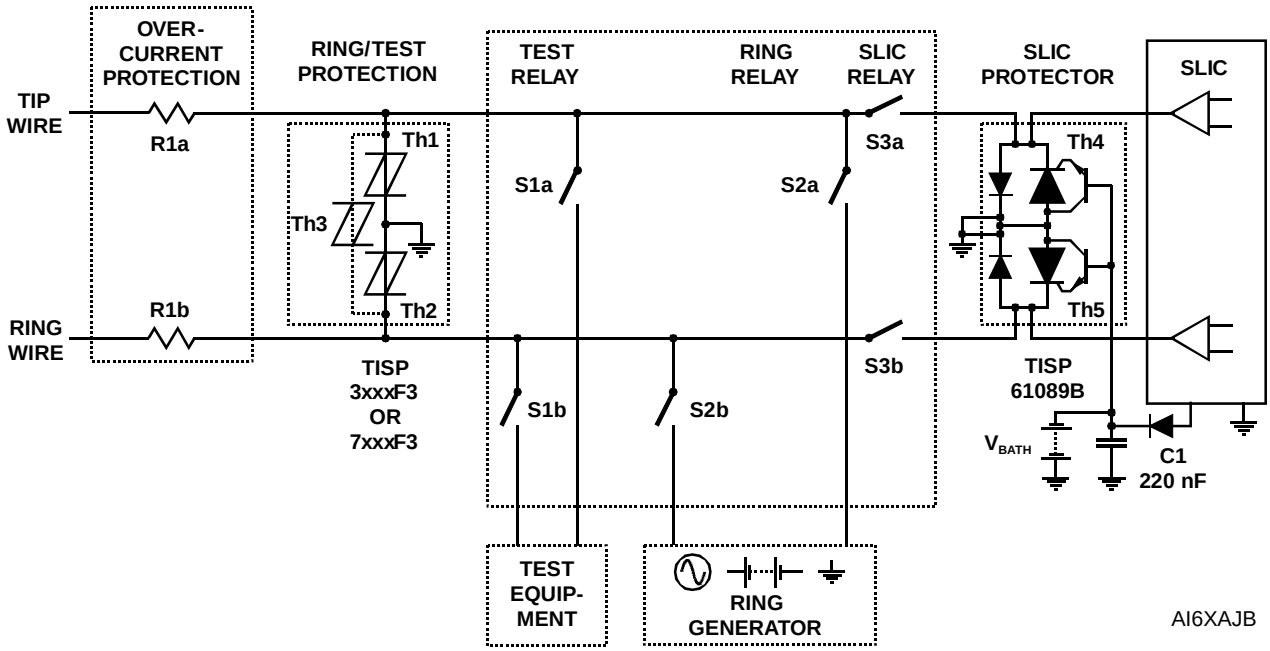


Figure 12. Typical Application Circuit

Application Circuit

Figure 12 shows a typical TISP61089B SLIC card protection circuit. The incoming line conductors, Ring (R) and Tip (T), connect to the relay matrix via the series overcurrent protection. Fusible resistors, fuses and positive temperature coefficient (PTC) resistors can be used for overcurrent protection. Resistors will reduce the prospective current from the surge generator for both the TISP61089B and the ring/test protector. The TISP7xxxF3 protector has the same protection voltage for any terminal pair. This protector is used when the ring generator configuration may be ground or battery-backed. For dedicated ground-backed ringing generators, the TISP3xxxF3 gives better protection as its inter-conductor protection voltage is twice the conductor to ground value.

Relay contacts 3a and 3b connect the line conductors to the SLIC via the TISP61089B protector. The protector gate reference voltage comes from the SLIC negative supply (V_{BATH}). A 220 nF gate capacitor sources the high gate current pulses caused by fast rising impulses.

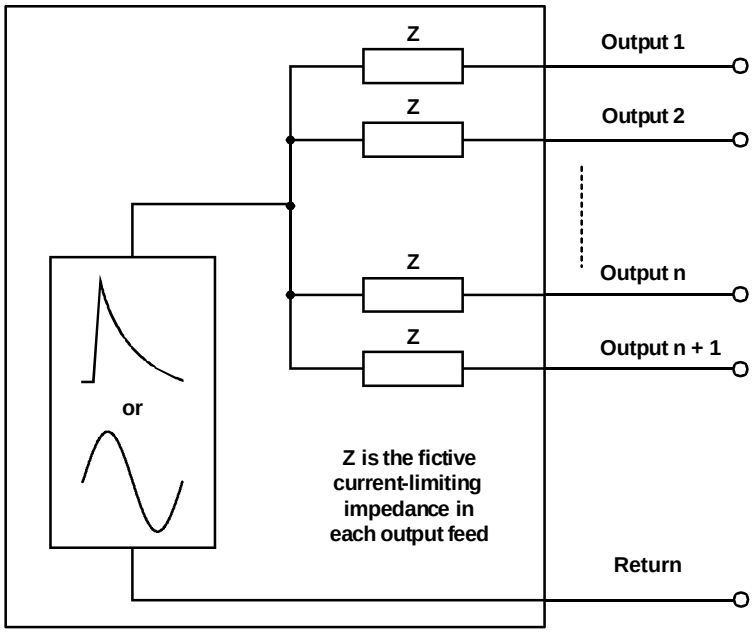
LSSGR 1089

GR-1089-CORE, “1089”, covers electromagnetic compatibility and electrical safety generic criteria for US network telecommunication equipment. It is a module in Volume 3 of LSSGR (LATA (Local Access Transport Area) Switching Systems Generic Requirements, FR-NWT-000064). In ‘1089, surge and power fault immunity tests are done at two levels. After first-level testing, the equipment shall not be damaged and shall continue to operate correctly. Under second-level testing, the equipment shall not become a safety hazard. The equipment is permitted to fail as a result of second-level testing. When the equipment is to be located on customer premises, second-level testing includes a wiring simulator test, which requires the equipment to reduce the power fault current below certain values.

The following clauses reference the ‘1089 section and calculate the protector stress levels. The TISP61089B needs a 40 Ω series resistor to survive second-level surge testing. To survive first-level testing and possibly fail under second-level testing allows lower resistor value of 25 Ω to be used. Tabulated current values are given for both 40 Ω and 25 Ω series resistor values.

‘1089 Section 4.5.5 - Test Generators

The generic form of test generator is shown in Figure 13. It emphasises that multiple outputs must be independent, i.e. the loading condition of one output must not affect the waveforms of the other outputs. It is a requirement that the open-circuit voltage and short circuit current waveforms be recorded for each generator output used for testing. The fictive impedance of a generator output is defined as the peak open-circuit voltage divided by the peak short-circuit current. Specified impulse waveshapes are maximum rise and minimum decay times. Thus, the 10/1000 waveshape should be interpreted as <10/>1000 and not the usually defined nominal values which have a tolerance.



Generic Lightning or AC Test Generator

Figure 13. ‘1089 Test Generators

‘1089 Section 4.5.5 - Test Generators (Continued)

The exception to these two conditions of independence and limit waveshape values is the alternative IEEE C.62.41, 1.2/50-8/20 combination wave generator which may be used for testing in ‘1089 Sections 4.5.7, 4.5.8 and 4.5.9. Here, the quoted waveshape values are nominal with defined tolerance. The open-circuit voltage waveshape is 1.2 μs±0.36 μs front time and 50 μs±10 μs duration. The short-circuit current waveshape is 8 μs+1.0 μs, -2.5 μs front time and 20 μs+8 μs, -4 μs duration. The generator fictive source impedance (peak open-circuit voltage divided by peak short-circuit current) is 2.0 Ω±0.25 Ω.

To get the same peak short-circuit currents as the 2/10 generator, for the same peak open-circuit voltage setting, ‘1089 specifies that the 1.2/50-8/20 generator be used with external resistors for current limiting and sharing. When working into a finite resistive load, the delivered 1.2/50-8/20 generator current waveshape moves towards the 1.2/50 voltage waveshape. Thus, although the 1.2/50-8/20 delivered peak current is similar to the 2/10 generator, the much longer current duration means that a much higher stress is imposed on the equipment protection circuit. This can cause fuses to operate which are perfectly satisfactory on the normal 2/10 generator. Testing with the 1.2/50-8/20 generator gives higher stress levels than the 2/10 generator and, because it is seldom used, will not be covered in this analysis.

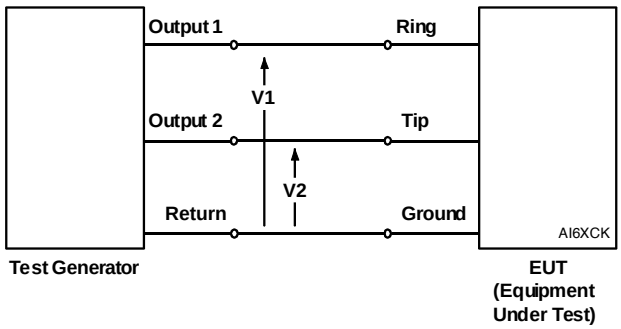


Figure 14. Longitudinal (also Called Common Mode) Testing

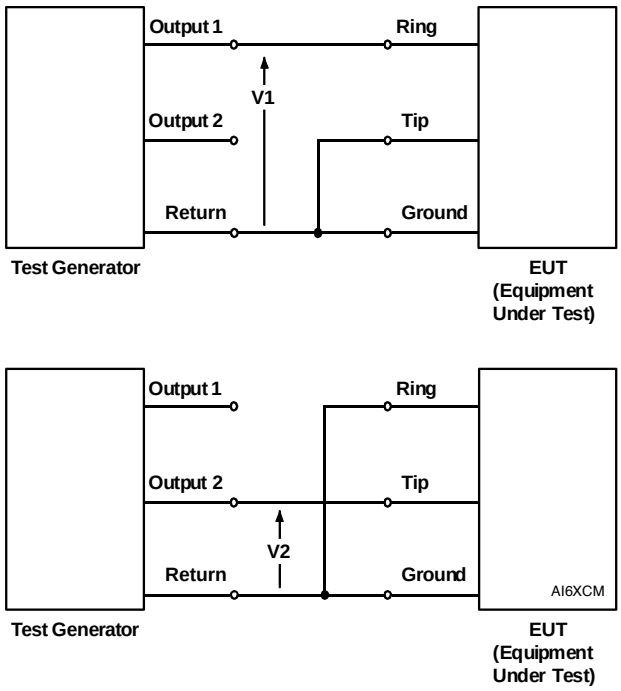


Figure 15. Transverse (also Called Differential or Metallic) Testing

'1089 Section 4.5.6 - Test Connections

The telecommunications port R and T terminals may be tested simultaneously or individually. Figure 14 shows connection for simultaneous (longitudinal) testing. Figure 15 shows the two connections necessary to individually test the R and T terminals during transverse testing.

The values of protector current are calculated by dividing the open-circuit generator voltage by the total circuit resistance. The total circuit resistance is the sum of the generator fictive source resistance and the TISP61089B series resistor value. The starting point of this analysis is to calculate the minimum circuit resistance for a test by dividing the generator open-circuit voltage by the TISP61089B rating. Subtracting the generator fictive resistance from the minimum circuit resistance gives the lowest value of series resistance that can be used. This is repeated for all test connections. As the series resistance must be a fixed value, the value used has to be the highest value calculated from all the considered test connections. Where both 10/1000 and 2/10 waveshape testing occurs, the 10/1000 test connection gives the highest value of minimum series resistance. Unless otherwise stated, the analysis assumes a -40 °C to +85 °C temperature range.

'1089 Section 4.5.7 - First-Level Lightning Surge Testing

Table 1 shows the tests for this section. The peak TISP61089B current, I_{TM}, is calculated by dividing the generator open voltage by the sum of the generator fictive source and the line feed, R_S, resistance values. Columns 9 and 10 show the resultant currents for R_S values of 25 Ω and 40 Ω. The TISP61089B rated current values at the various waveshapes are higher than those listed in Table 1. Used with the specified values of R_S, the TISP61089B will survive these tests.

Table 1. First-Level Surge Currents

Surge #	Waveshape	Open-circuit Voltage V	Short-circuit Current A	No of Tests	Test Connections	Primary Fitted	Generator Fictive Source Resistance Ω	TISP61089B I_{TM} A	
								R_S = 25 Ω	R_S = 40 Ω
1	10/1000	600	100	+25, -25	Transverse & Longitudinal	No	6	19 & 2x19	13 & 2x13
2	10/360	1000	100	+25, -25	Transverse & Longitudinal	No	10	29 & 2x29	20 & 2x20
3	10/1000	1000	100	+25, -25	Transverse & Longitudinal	No	10	29 & 2x29	20 & 2x20
4	2/10	2500	500	+10, -10	Longitudinal	No	5	2x83	2x56
5	10/360	1000	25	+5, -5	Longitudinal	No	40	2x15	2x13

NOTES: 1. Surge 3 may be used instead of Surge 1 and Surge 2.
2. Surge 5 is applied to multiple line pairs up to a maximum of 12.
3. If the equipment contains a voltage-limiting secondary protector, each test is repeated at a voltage just below the threshold of limiting.

'1089 Section 4.5.8 - Second-Level Lightning Surge Testing

Table 2 shows the 2/10 test used for this section. Columns 9 and 10 show the resultant currents for R_S values of 25 Ω and 40 Ω. Used with an R_S of 40 Ω, the TISP61089B with survive this test. The 25 Ω value of R_S is only intended to give first-level (Section 4.5.7) survival. Under second-level conditions, the peak current will be 2x143 A, which may result in failure of the 2x120 A rated TISP61089B. However, if the testing is done at or near 25 °C, the TISP61089B will survive with an R_S value of 25 Ω as the 2/10 rating is 170 A at this temperature.

Table 2. Second-Level Surge Current

Surge #	Waveshape	Open-circuit Voltage V	Short-circuit Current A	No of Tests	Test Connections	Primary Fitted	Generator Fictive Source Resistance Ω	TISP61089B I_{TM} A	
								R_S = 25 Ω	R_S = 40 Ω
1	2/10	5000	500	+1, -1	Longitudinal	No	10	2x143	2x100

NOTE: 1. If the equipment contains a voltage-limiting secondary protector, the test is repeated at a voltage just below the threshold of limiting.

'1089 Section 4.5.9 - Intra-Building Lightning Surge Testing

This test is for network equipment ports that do not serve outside lines. Table 3 shows the 2/10 tests used for this section. Dedicated intra-building ports may use an R_S value of 8 Ω. The 8 Ω value is set by the intra-building second-level a.c. testing of Section 4.5.16. Columns 9, 10 and 11 show the resultant currents for R_S values of 8 Ω, 25 Ω and 40 Ω. The listed currents are lower than the TISP61089B current rating of 2x120 A and the TISP61089B will survive these tests.

Table 3. Intra-building Lightning Surge Currents

Surge #	Waveshape	Open-circuit Voltage V	Short-circuit Current A	No of Tests	Test Connections	Primary Fitted	Generator Fictive Source Resistance Ω	TISP61089B I_{TM} A		
								R_S = 8 Ω	R_S = 25 Ω	R_S = 40 Ω
1	2/10	800	100	+1, -1	Transverse	NA	8	50	24	17
2	2/10	1500	100	+1, -1	Longitudinal	NA	15	2x65	2x38	2x27

NOTE: 1. If the equipment contains a voltage-limiting secondary protector, the test is repeated at a voltage just below the threshold of limiting.

'1089 Section 4.5.11 - Current-Limiting Protector Testing

Equipment that allows unacceptable current to flow during power faults (Figure 16) shall be specified to use an appropriate current-limiting protector. The equipment performance can be determined by testing with a series fuse, which simulates the safe current levels of a telephone cable. If this fuse opens, the equipment allows unacceptable current flow and an external current-limiting protector must be specified. For acceptable currents, the equipment must not allow current flows for times that would operate the simulator. The wiring simulator fuse current-time characteristic shall match the boundary of Figure 16. A Bussmann MDQ-1 $^{6}/_{10}$ fuse is often specified as meeting this requirement, Figure 17.

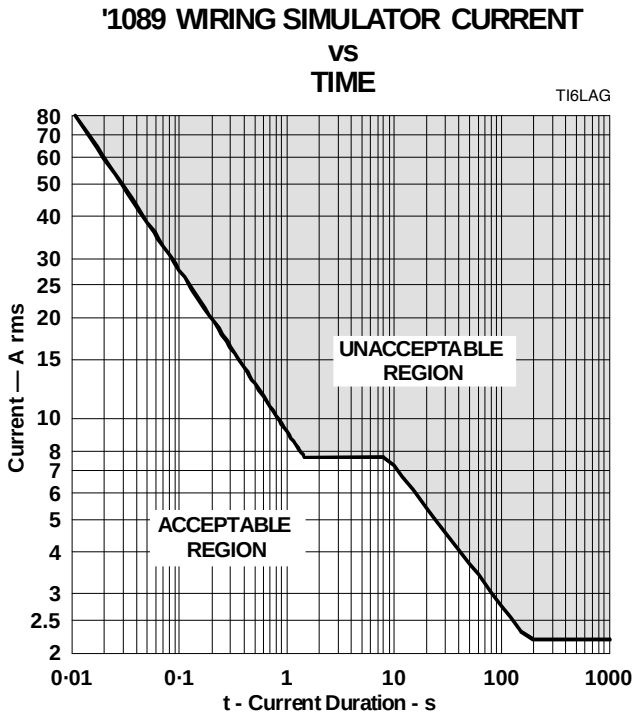


Figure 16. Wiring Simulator Current-Time

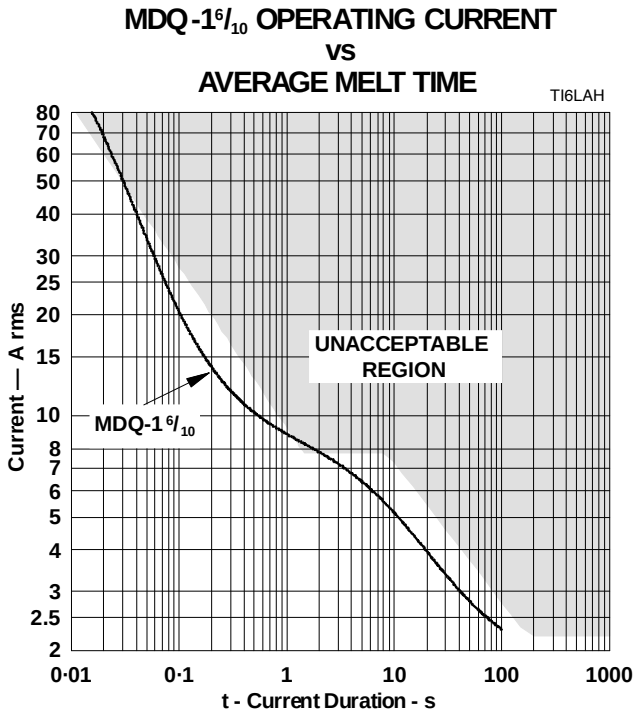


Figure 17. MDQ-1$^{6}/_{10}$ Current-Time

'1089 Section 4.5.11 - Current-Limiting Protector Testing (Continued)

The test generator has a voltage source that can be varied from zero to 600 V rms and an output resistance of 20 Ω to each conductor. Table 4 shows the range of currents conducted by the TISP61089B.

Table 4. Wiring Simulator Testing

AC Duration s	Open-Circuit RMS Voltage V	Short-Circuit RMS Current A	Test Connections	Primary Fitted	Source Resistance Ω	TISP61089B I_{TM} A (peak)	
						R_S = 25 Ω	R_S = 40 Ω
900	0 to 600	0 to 30	Transverse & Longitudinal	No	20	0 to 2x 19	0 to 2x 14

'1089 Section 4.5.12 - First-Level Power Fault Testing

Table 5 shows the nine tests used for this section. The TISP61089B will survive these peak current values as they are lower than the TISP61089B current-time ratings.

Table 5. First-Level Power Fault Currents

Test #	AC Duration s	Open-circuit RMS Voltage V	Short-circuit RMS Current A	No of Tests	Test Connections	Primary Fitted	Source Resistance Ω	TISP61089B I_{TM} A (peak)	
								R_S = 25 Ω	R_S = 40 Ω
1	900	50	0.33	1	Transverse & Longitudinal	No	150	2x0.40	2x0.37
2	900	100	0.17	1	Transverse & Longitudinal	No	600	2x0.23	2x0.22
3	1	200 400 600	0.33 0.67 1.00	60 60 60	Transverse & Longitudinal	No	600	2x0.45 2x0.90 2x1.36	2x0.44 2x0.89 2x1.33
4	1	1000	1	60	Longitudinal	Yes	1000	2x1.38	2x1.30
5	5	600	0.09	60	Differential	No	Capacitive	2x0.12	2x0.12
6	30	600	0.5	1	Transverse & Longitudinal	No	1200	2x0.69	2x0.68
7	2	600	2.2	1	Transverse & Longitudinal	No	273	2x2.85	2x2.71
8	1	600	3.0	1	Transverse & Longitudinal	No	200	2x3.77	2x3.54
9	0.5	1000	5	1	Longitudinal	Yes	200	2x6.28	2x5.89

NOTES: 1. If the equipment contains a voltage-limiting device or a current-limiting device, tests 1, 2 and 3 are repeated at a level just below the thresholds of the limiting devices.
2. Test 5 uses a special circuit with transformer coupled a.c. and capacitive feed.
3. Tests 1 through 5 are requirements and the equipment shall not be damaged after these tests.
4. Tests 6 through 9 are desirable objectives and the equipment can be damaged after these tests.

'1089 Section 4.5.13 - Second-Level Power Fault Testing for Central Office Equipment

Table 6 shows the five tests used for this section. Columns 9 and 10 show the prospective currents for these tests using R_S values of 25 Ω and 40 Ω. The two most stressful tests of this section are test 1 and test 2. As shown in Table 6, the peak currents for these tests are 2x17 A and 2x7.7 A respectively. With the exception of test 5, all the other tests require the series overcurrent protection to operate before the TISP61089B current-time ratings are exceeded. In the case of test 2, with an R_S of 25 Ω, the overcurrent protection must operate within the initial a.c. half cycle to prevent damage.

'1089 Section 4.5.13 - Second-Level Power Fault Testing for Central Office Equipment (Continued)

Table 6. Second-Level Power Fault Currents

Test #	AC Duration s	Open-circuit RMS Voltage V	Short-circuit RMS Current A	No of Tests	Test Connections	Primary Fitted	Source Resistance Ω	TISP61089B I_{TM} A (peak)	
								R_S = 25 Ω	R_S = 40 Ω
1	900	120 277	25	1 1	Transverse & Longitudinal	No	5 11	2x5.7 2x11	2x3.8 2x7.7
2	5	600	60	1	Transverse & Longitudinal	No	10	2x24	2x17
3	5	600	7	1	Transverse & Longitudinal	No	86	2x7.7	2x6.8
4	900	100 to 600	0.37 to 2.2		Transverse & Longitudinal	No	270	2x2.9	2x2.7
5	900	600	0.09	60	Differential	No	Capacitive	2x0.09	2x0.09

NOTES: 1. If the equipment contains a voltage-limiting device or a current-limiting device, these tests are repeated at a level just below the thresholds of the limiting devices.
2. Test 5 uses a special circuit with transformer coupled a.c. and capacitive feed.

'1089 Section 4.5.15 - Second-Level Power Fault Testing for Equipment Located on the Customer Premise

This test, Table 7, is for network equipment located on the customer premises. The purpose is to ensure that the feed wiring does not become a hazard due to excessive current. This testing is similar to the Section 4.5.11 testing. If the equipment is directly wired, the wiring simulator described in Section 4.5.11 is replaced by a one-foot section of 26 AWG wrapped in cheesecloth. The equipment fails if an open circuit occurs or the cheesecloth is damaged.

Table 7 shows the test conditions for this section. Columns 7 and 8 show the prospective currents using R_S values of 25 Ω and 40 Ω. For the TISP61089B to survive, the series overcurrent protection to operate before the TISP61089B current-time ratings are exceeded.

Table 7. Customer Premise Wiring Simulator Testing

AC Duration s	Open-circuit RMS Voltage V	Short-circuit RMS Current A	Test Connections	Primary Fitted	Source Resistance Ω	TISP61089B I_{TM} A (peak)	
						R_S = 25 Ω	R_S = 40 Ω
900	0 to 600	0 to 30	Transverse & Longitudinal	No	20	0 to 2x 19	0 to 2x 14

NOTE: 1. If the equipment interrupts the current before the 600 V rms level is reached, a second piece of equipment is tested. The second piece of equipment shall withstand 600 V rms applied for 900 s without causing a hazard.

'1089 Section 4.5.16 - Second-Level Intra-Building Power Fault Testing for Equipment Located on the Customer Premise

This test, Table 8, is for network equipment ports that do not serve outside lines. For standard plugable premise wiring, the wiring simulator fuse shall be used for testing. Where direct wiring occurs, the simulator shall consist of a length of the wire used wrapped in cheesecloth. The equipment fails if a hazard occurs or a wiring simulator open circuit occurs or the cheesecloth is damaged.

Table 8. Second-Level Power Fault Currents

Test #	AC Duration s	Open-circuit RMS Voltage V	Short-circuit RMS Current A	No of Tests	Test Connections	Primary Fitted	Source Resistance Ω	TISP61089B I_{TM} A (peak)		
								R_S = 8 Ω	R_S = 25 Ω	R_S = 40 Ω
1	900	120	25	1	Transverse & Longitudinal	No	5	2x13	2x5.7	2x3.8

NOTE: 1. If the equipment contains a voltage-limiting device or a current-limiting device, these tests are repeated at a level just below the thresholds of the limiting devices.

‘1089 Section 4.5.16 (Continued)

Dedicated intra-building ports may use an R_S value of 8 Ω. The 8 Ω value limits the initial current to 13 A, which is within the TISP61089B single cycle rating. For the TISP61089B to survive the full 900 s test, the series overcurrent protection to operate before the TISP61089B current-time ratings are exceeded.

Overcurrent and Overvoltage Protection Coordination

To meet ‘1089, the overcurrent protection must be coordinated with the requirements of Sections 4.5.7, 4.5.8, 4.5.9, 4.5.12, 4.5.13, 4.5.15 and the TISP61089B. The overcurrent protection must not fail in the first-level tests of Sections 4.5.7, 4.5.9 and 4.5.12 (tests 1 through 5). Test 6 through 9 of Section 4.5.12 are not requirements. The test current levels and their duration are shown in Figure 18. First-level tests have a high source resistance and the current levels are not strongly dependent on the TISP61089B series resistor value.

Second-level tests have a low source resistance and the current levels are dependent on the TISP61089B R_S resistor value. The two stepped lines at the top of Figure 18 are for the 25 Ω and 40 Ω series resistor cases. The unacceptable current region (Section 4.5.11) is also shown in Figure 18. If current flows for the full second-level test time, the unacceptable current region will be entered. The series overcurrent protector must operate before the unacceptable region is reached.

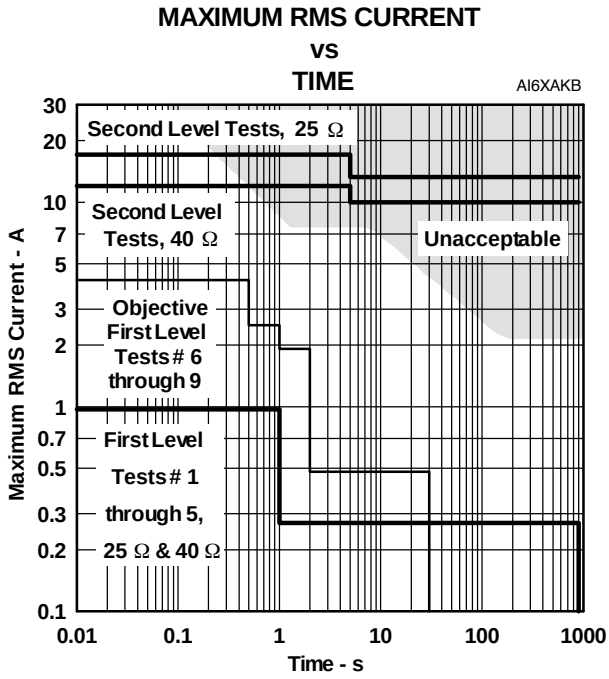


Figure 18. ‘1089 Test Current Levels

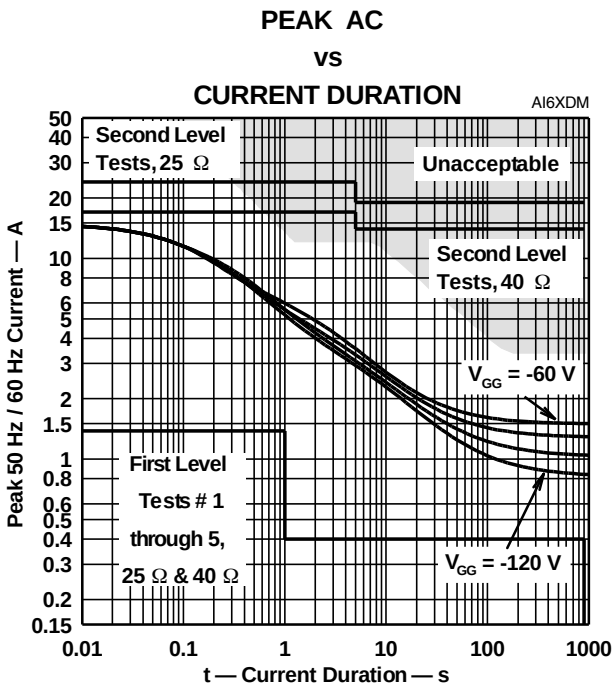


Figure 19. TISP61089B Overlay

Fusible overcurrent protectors cannot operate at first-level current levels. Thus, the permissible low current time-current boundary for fusible overcurrent protectors is formed by the first-level test currents. Automatically resettable overcurrent protectors (e.g. Positive Temperature Coefficient Thermistors) may operate during first-level testing, but normal equipment working must be restored after the test has ended.

At system level, the high current boundary is formed by the unacceptable region. However, component and printed wiring, PW, current limitations will typically lower the high current boundary. Although the series line feed resistance, R_S, limits the maximum available current in second-level testing, after about 0.5 s this limitation will exceed the acceptable current flow values.

These three boundaries, first-level, second-level and unacceptable, are replotted in terms of peak current rather than rms current values in Figure 19. Using a peak current scale allows the TISP61089B longitudinal current rating curves (Figure 3) to be added to Figure 19. Assuming the PW is sized to adequately carry any currents that may flow, the high current boundary for the overcurrent protector is formed by the TISP61089B rated current. Note that the TISP61089B rated current curve also depends on the value of gate supply voltage.

Overcurrent and Overvoltage Protection Coordination (Continued)

The overcurrent protector should not allow current-time durations greater than the TISP61089B current ratings, otherwise the TISP61089B may fail. A satisfactory fusible resistor performance is shown in Figure 20. The line feed resistor (LFR) current-time curve is above the first-level currents and below the TISP61089B rated current for V_{GG} > -100 V. This particular curve is for a Bourns 4B04B-523-400 2 x 40 Ω, 2 % tolerance, 0.5 % matched resistor module. Fusible resistors are also available with integrated thermal fuses or PTC thermistors. Thermal fuses will cause a rapid drop in the operating current after about 10 s. Figure 20 shows the fused LFR curve for a Bourns 4B04B-524-400 2 x 40 Ω, 2 % tolerance, 0.5 % matched resistor module with integrated thermal fuse links. The Bourns 4B04B-524-400 allows the TISP61089B to operate down to its full rated voltage of V_{GG} = -155 V. An LFR with integrated PTC thermistors will give an automatically resettable current limiting function for all but the highest currents.

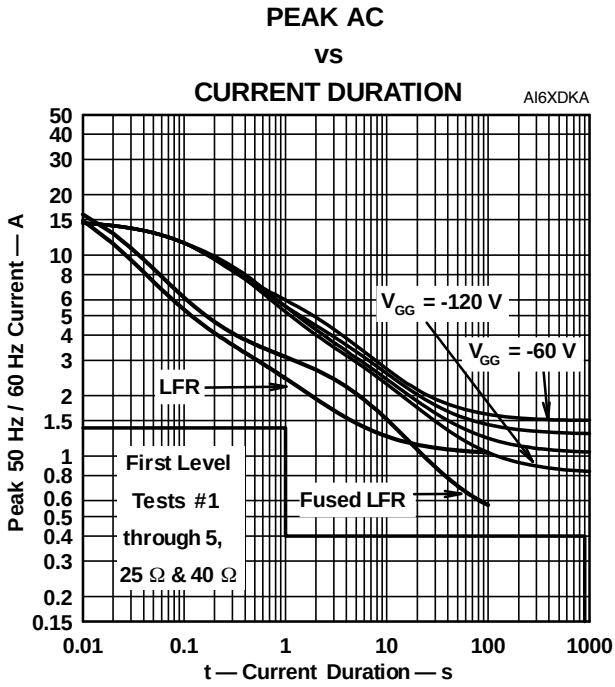


Figure 20. Line Feed Resistor - with and without Thermal Fuse

Ceramic PTC thermistors are available in suitable ohmic values to be used as the series line feed resistor R_S . Figure 21 overlays a typical ceramic PTC thermistor operating characteristic. Some of the first-level tests will cause thermistor operation. Generally, the resistance matching stability of the two PTC thermistors after power fault switching lightning will meet the required line balance performance.

Ceramic PTC thermistors reduce in resistance value under high voltage conditions. Under high current impulse conditions, the resistance can be less than 50 % of the d.c. resistance. This means that more current than expected will flow under high voltage impulse conditions. The manufacturer should be consulted on the 2/10 currents conducted by their product under ‘1089 conditions. To keep the 2/10 current below 120 A, an increase of the PTC thermistor d.c. resistance value to 50 Ω or more may be needed. In controlled temperature environments, where the temperature does not drop below freezing, the TISP61089B 2/10 capability is about 170 A, and this would allow a lower value of resistance.

Generally, polymer PTC thermistors are not available in sufficiently high ohmic values to be used as the only line feed resistance. To meet the required resistance value, an addition (fixed) series resistance can be used. Figure 22 overlays a typical polymer PTC thermistor operating characteristic. Compared to ceramic PTC thermistors, the lower thermal mass of the polymer type will generally give a faster current reduction time than the ceramic type. However, in this case the polymer resistance value is much less than the ceramic value. For the same current level, the dissipation in the polymer thermistor is much less than the ceramic thermistor. As a result, the polymer thermistor is slower to operate than the ceramic one.

The resistance stability of polymer PTC thermistors is not as good as ceramic ones. However, the thermistor resistance change will be diluted by additional series resistance. If an SLIC with adaptive line balance is used, thermistor resistance stability may not be a problem. Polymer PTC thermistors do not have a resistance decrease under high voltage conditions.

Overcurrent and Overvoltage Protection Coordination (Continued)

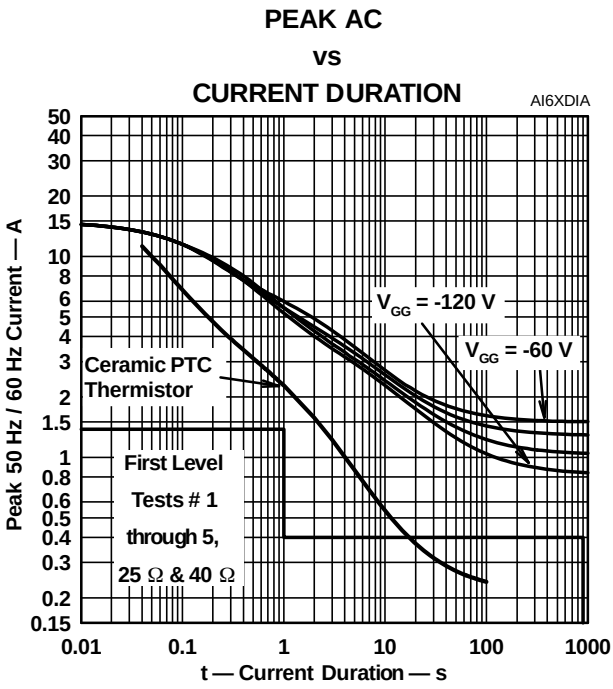


Figure 21. Ceramic PTC Thermistor

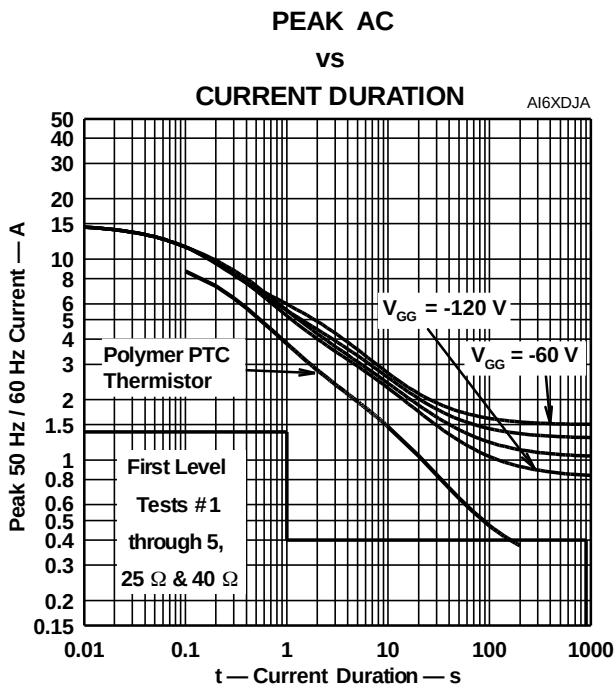


Figure 22. Polymer PTC Thermistor

MECHANICAL DATA

Device Symbolization Code

Devices will be coded as below.

Device	Symbolization Code
TISP61089B	61089B

BOURNS®

Asia-Pacific: Tel: +886-2 2562-4117 • Email: asiacus@bourns.com
EMEA: Tel: +36 88 885 877 • Email: eurocus@bourns.com
The Americas: Tel: +1-951 781-5500 • Email: americus@bourns.com
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