THE DATASHEET OF

TIR1000IPWR

TIR1000x Standalone IrDA™ Encoder and Decoder

1 Features

- Adds Infrared (IR) Port to Universal Asynchronous Receiver Transmitter (UART)
- Compatible With Infrared Data Association (IrDA™) and Hewlett Packard Serial Infrared (HPSIR)
- Provides 1200-bps to 115-kbps Data Rate
- Operates from 2.7 V to 5.5 V
- Provides Simple Interface With UART
- Decodes Negative or Positive Pulses
- Available in Two 8-Terminal Plastic Small Outline Packages (PSOP)
  - PS Package Has Slightly Larger Dimensions Than PW Package

2 Applications

- UART Interfacing
- Infrared Data Communications

3 Description

The TIR1000x serial infrared (SIR) encoder and decoder is a CMOS device that encodes and decodes bit data in conformance with the IrDA specification.

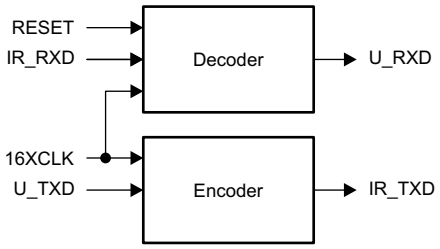
A transceiver device is needed to interface to the photo-sensitive diode (PIN) and the light emitting diode (LED). A UART is needed to interface to the serial data lines.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TIR1000x	TSSOP (8)	3.00 mm × 4.40 mm
	SO (8)	6.20 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



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4 Revision History

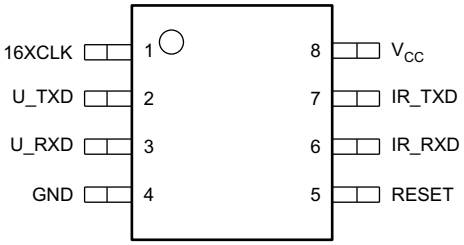
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (July 1999) to Revision G **Page**

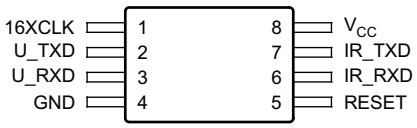
- Added *Applications*, *Pin Configuration and Functions* section, *ESD Ratings* table, *Typical Characteristics* section, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added PS package drawing ... 3
- Changed t_r output rise time FROM: 1.3 ns TO: 23.8 ns in *Switching Characteristics* ... 5
- Changed t_f output fall time FROM: 1.8 ns TO: 9.2 ns in *Switching Characteristics* ... 5

5 Pin Configuration and Functions

PS Package
8-Pin SO
Top View



PW Package
8-Pin TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
16XCLK	1	I	Clock signal. 16XCLK must be set to 16 times the baud rate. The highest baud rate for IrDA is 115.2 kbps for which the clock frequency equals 1.843 MHz (this terminal is tied to the BAUDOUT of a UART).
GND	4	—	Ground
IR_RXD	6	I	Infrared receiver data. IR_RXD is an IrDA-SIR-modulated input from an optoelectronics transceiver whose input pulses should be 3/16 of the baud rate period.
IR_TXD	7	O	Infrared transmitter data. IR_TXD is an IrDA-SIR-modulated output to an optoelectronics transceiver.
RESET	5	I	Active high reset. RESET initializes an IrDA-SIR-decode/encode state machine (this terminal is tied to a UART reset line).
U_RXD	3	O	Receiver data. U_RXD is decoded (demodulated) data from IR_RXD according to the IrDA specification (this terminal is tied to SIN of a UART).
U_TXD	2	I	Transmitter data. U_TXD is encoded (modulated) data and output data as IR_TXD (this terminal is tied to SOUT from a UART).
V_{CC}	8	—	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		–0.5	6	V
V_I	Input voltage at any input		–0.5	V_{CC} + 0.5	V
V_O	Output voltage		–0.5	V_{CC} + 0.5	V
T_A	Operating free-air temperature range	TIR1000		0	°C
		TIR1000I	–40	85	°C
	Case temperature for 10 seconds	SO package		260	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage levels are with respect to GND.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±900	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
LOW VOLTAGE (3-V NOMINAL)						
V_{CC}	Supply voltage		2.7	3	3.3	V
V_{IH}	High-level input voltage		0.7 V_{CC}			V
V_{IL}	Low-level input voltage				0.2 V_{CC}	V
T_A	Operating free-air temperature	TIR1000	0		70	°C
		TIR1000I	–40		85	
STANDARD VOLTAGE (5-V NOMINAL)						
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		0.7 V_{CC}			V
V_{IL}	Low-level input voltage				0.2 V_{CC}	V
T_A	Operating free-air temperature	TIR1000	0		70	°C
		TIR1000I	–40		85	

6.4 Thermal Information

THERMAL METRIC (1)		TIR1000 PS (SO), PW (TSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	179.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	108.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	106.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = – 4 mA	V_{CC} = 5 V	V_{CC} – 0.8			V
		I_{OH} = – 1.8 mA	V_{CC} = 3 V	V_{CC} – 0.55			
V_{OL}	Low-level output voltage	I_{OL} = +4 mA	V_{CC} = 5 V			0.5	V
		I_{OL} = +1.8 mA	V_{CC} = 3 V			0.5	
I_I	II Input current	V_I = 0 to V_{CC}	All other pins floating			±3	µA
I_{CC}	Supply current	V_{CC} = 5.25 V All inputs at 0.2 V No load on outputs	T_A = 25°C 16XCLK at 2 MHz			1	mA
$C_{i(16XCLK)}$	Clock input capacitance				5		pF
$f_{(16XCLK)}$	Clock frequency					2	MHz

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_r	Output rise time	No load		23.8		ns
t_f	Output fall time	No load		9.2		ns

(1) Typical values are at T_A = 25°C.

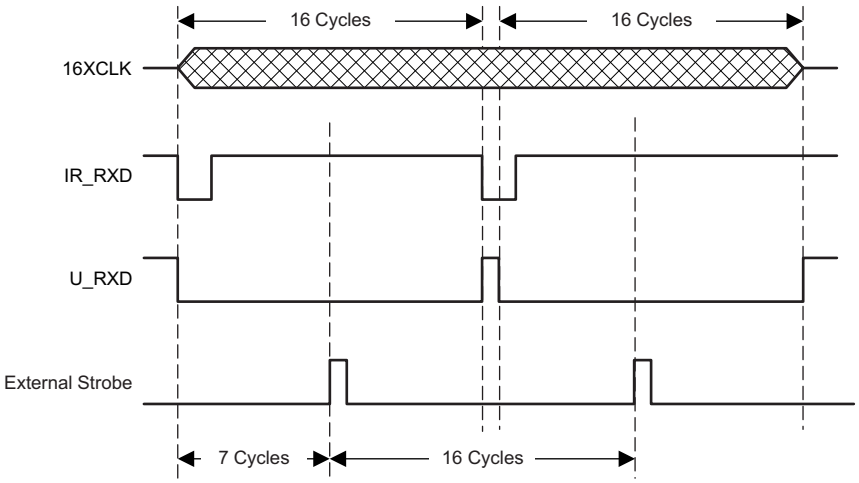


Figure 1. Recommended Strobing For Decoded Data

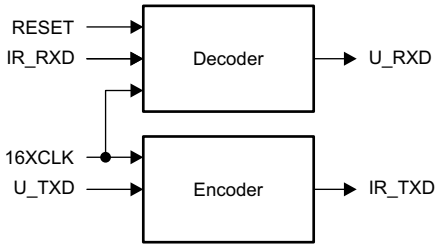
7 Detailed Description

7.1 Overview

TIR1000 serial infrared (SIR) encoder and decoder is a device (CMOS) that encodes and decodes bit data according with the IrDA specifications.

For the correct performance of the TIR1000 device, an optoelectronics device and a UART device are necessary. The TIR1000 device operates as an interface between wireless infrared and UART communication.

7.2 Functional Block Diagram



7.3 Feature Description

The Infrared Data Association (IrDA) defines several protocols for sending and receiving serial infrared data, including the following rates:

- 115.2 kbps
- 0.576 Mbps
- 1.152 Mbps
- 4 Mbps

The low rate of 115.2 kbps was specified first and the others must maintain downward compatibility with it. At the 115.2 kbps rate, the protocol implemented in the hardware is fairly simple. It primarily defines a serial infrared data word to be surrounded by a start bit equal to 0 and a stop bit equal to 1. Individual bits are encoded or decoded the same whether they are start, data, or stop bits.

The TIR1000 and TIR1000I devices evaluate only single bits and follow only the 115.2-kbps protocol. The 115.2-kbps rate is a maximum rate. When both ends of the transfer are set up to a lower but matching speed, the protocol (with the TIR1000 and TIR1000I devices) still works.

The clock used to code or sample the data is 16 times the baud rate, or 1.843 MHz maximum. To code a 1, no pulse is sent or received for 1-bit time period, or 16 clock cycles. To code a 0, one pulse is sent or received within a 1-bit time period, or 16 clock cycles. The pulse must be at least 1.6 µs wide and 3 clock cycles long at 1.843 MHz. At lower baud rates, the pulse can be 1.6 µs wide or as long as 3 clock cycles.

The transmitter output, IR_TXD, is intended to drive an LED circuit to generate an infrared pulse. The LED circuits work on positive pulses. A terminal circuit is expected to create the receiver input, IR_RXD. Most (but not all) PIN circuits have inversion and generate negative pulses from the detected infrared light. Their output is normally high. The TIR1000 and TIR1000I devices can decode either negative or positive pulses on IR_RXD.

7.4 Device Functional Modes

7.4.1 IrDA Encoder Function

Serial data from a UART is encoded to transmit data to the optoelectronics. While the serial data input to this block (U_TXD) is high, the output (IR_TXD) is always low, and the counter used to form a pulse on IR_TXD is continuously cleared. After U_TXD resets to 0, IR_TXD rises on the falling edge of the seventh 16XCLK. On the falling edge of the tenth 16XCLK pulse, IR_TXD falls, creating a 3-clock-wide pulse. While U_TXD stays low, a pulse is transmitted during the seventh to tenth clocks of each 16-clock bit cycle.

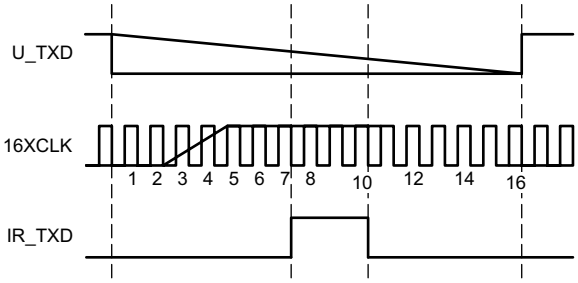


Figure 2. IrDA-SIR Encoding Scheme Detailed Timing Diagram

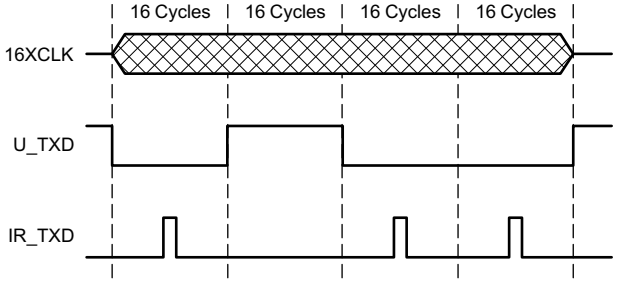


Figure 3. Encoding Scheme Macro View

7.4.2 IrDA Decoder Function

After reset, U_RXD is high and the 4-bit counter is cleared. When a falling edge is detected on IR_RXD, U_RXD falls on the next rising edge of 16XCLK with sufficient setup time. U_RXD stays low for 16 cycles (16XCLK) and then returns to high as required by the IrDA specification. As long as no pulses (falling edges) are detected on IR_RXD, U_RXD remains high.

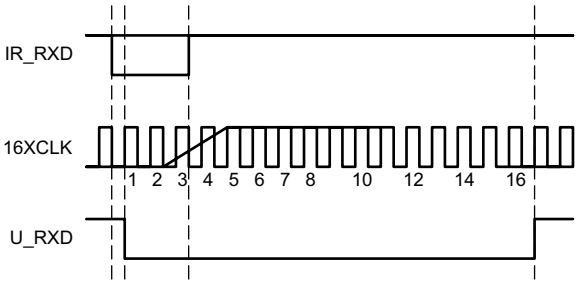


Figure 4. IrDA-SIR Decoding Scheme Detailed Timing Diagram

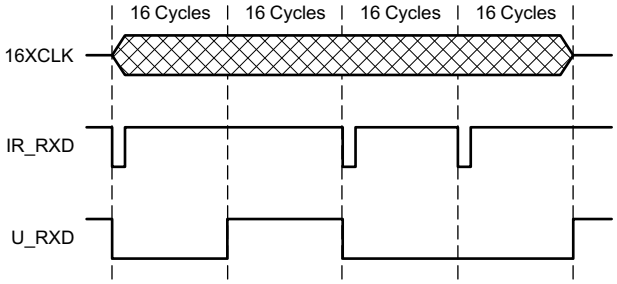


Figure 5. Decoding Scheme Macro View

It is possible for jitter or slight frequency differences to cause the next falling edge on IR_RXD to be missed for one 16XCLK cycle. In that case, a 1-clock-wide pulse appears on U_RXD between consecutive zeroes. It is important for the UART to strobe U_RXD in the middle of the bit time to avoid latching this 1-clock-wide pulse. The TL16C550C UART already strobes incoming serial data at the proper time. Otherwise, note that data is required to be framed by a leading zero and a trailing one. The falling edge of that first zero on U_RXD synchronizes the read strobe. The strobe occurs on the eighth 16XCLK pulse after the U_RXD falling edge and once every 16 cycles thereafter until the stop bit occurs.

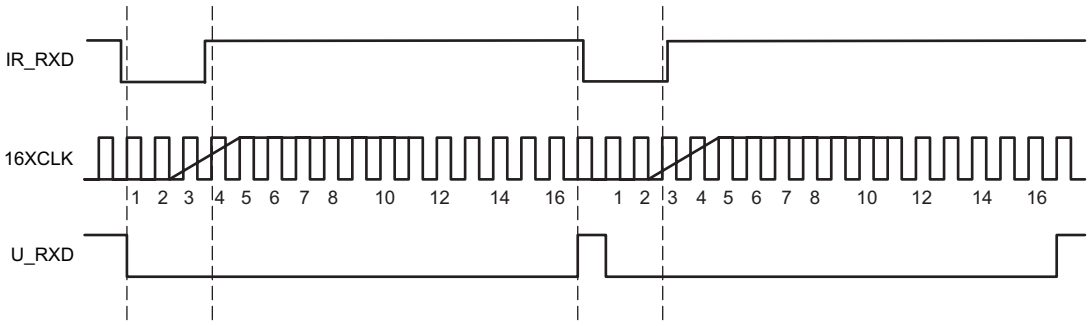


Figure 6. Timing Causing 1-Clock-Wide Pulse Between Consecutive Ones

The TIR1000 and TIR1000I can decode positive pulses on IR_RXD. The timing is different, but the variation is invisible to the UART. The decoder, which works from the falling edge, now recognizes a zero on the trailing edge of the pulse rather than on the leading edge. As long as the pulse width is fairly constant, as defined by the specification, the trailing edges should also be 16 clock cycles apart and data can readily be decoded. The zero appears on U_RXD after the pulse rather than at the start of it.

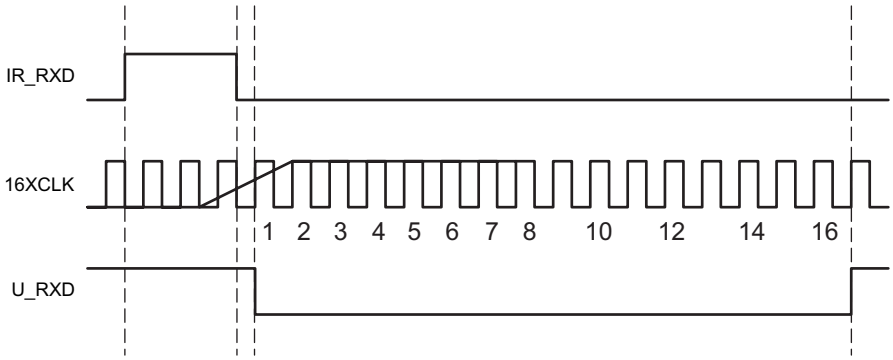


Figure 7. Positive IR_RXD Pulse Decode Detailed View

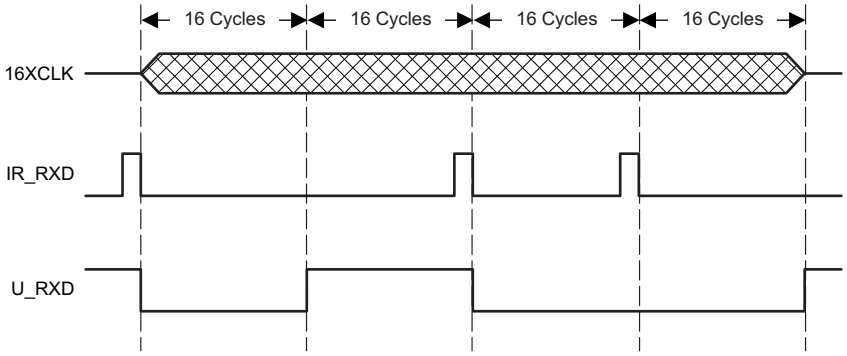


Figure 8. Positive IR_RXD Pulse Decode Macro View

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

IrDA provides several specifications for a complete set of protocols for wireless infrared communications.

8.2 Typical Application

A simple application of the TIR1000 device is developing a system with an optoelectronics device and a UART device (TL16C500C). Hence, the TIR1000 device interfaces between the infrared and serial devices.

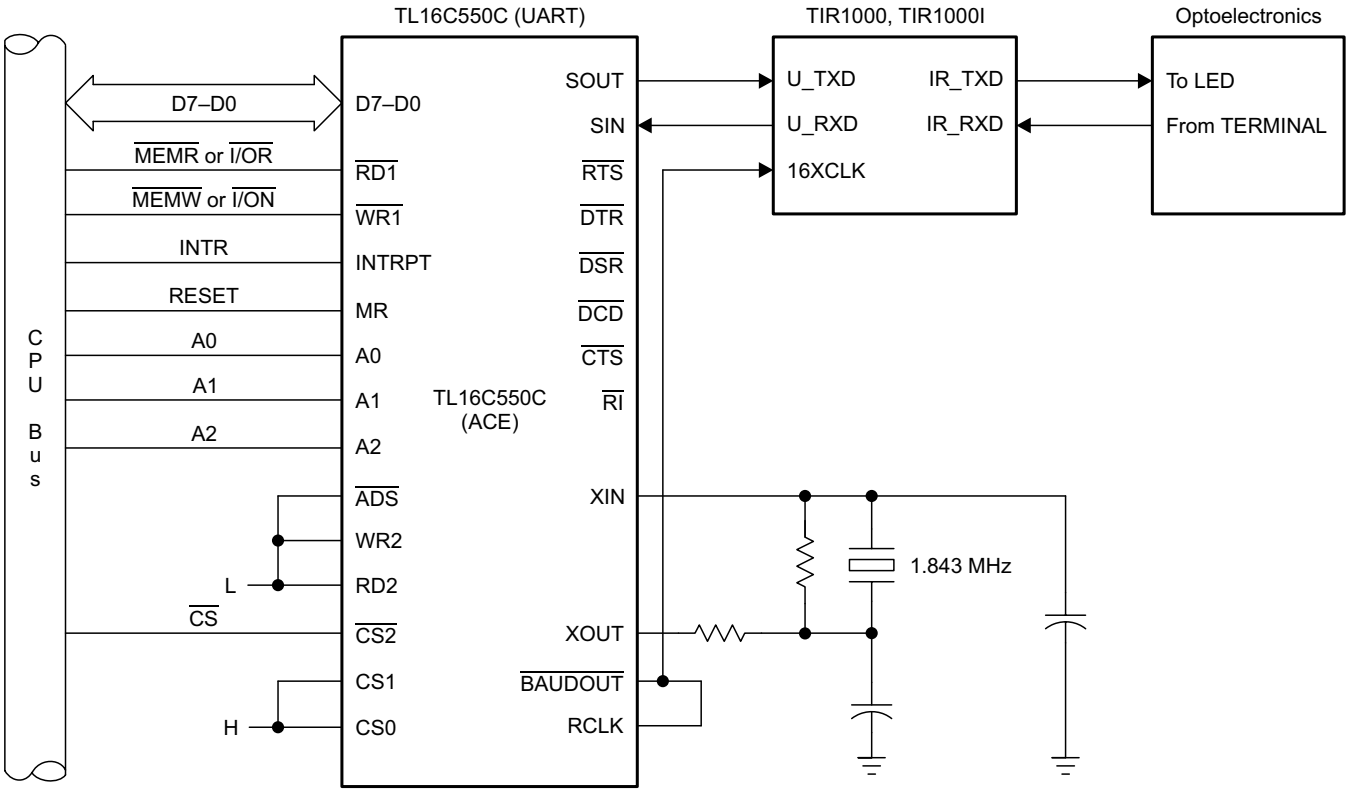


Figure 9. Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

Table 1 lists the design requirements for the typical application.

Table 1. Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Power supply	3 V (low voltage)
1.843-MHz clock source	Crystal
Baud rate	115.2 kbps
TRANSMITTER	
Peak wavelength	850–900 nm
Intensity in angular range	40–500 mW/Sr
Half angle	±15-30°
Pulse Duration at 115.2 kbps	2.23 µs
RECEIVER	
Irradiance in angular range	4–500 mW/cm2
Half angle	±15°
Receiver latency	10 ms

8.2.2 Detailed Design Procedure

The asynchronous communications element (TL16C550C) contains a programmable baud generator that takes a clock input in the range between DC and 16 MHz and divides it by a divisor in the range between 1 and (216 – 1). The output frequency of the baud generator is sixteen times (16×) the baud rate. The formula for the divisor is shown in Equation 1.

divisor = XIN frequency input / (desired baud rate × 16) (1)

For example:

divisor = 1.843 MHz / (115.2 kbps × 16) = 0.9999 (2)

Error (divisor) <1%

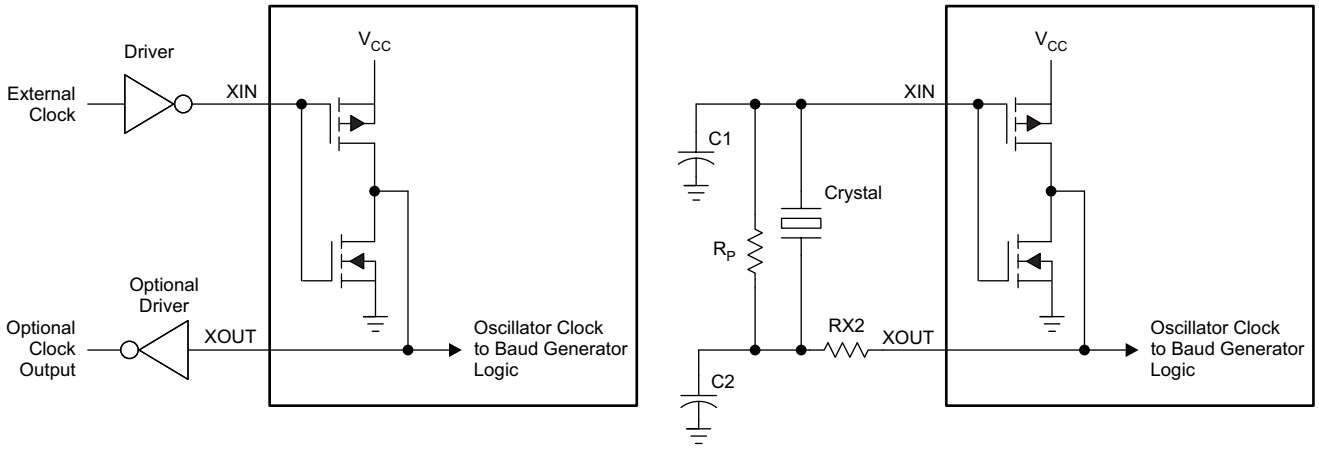


Figure 10. Typical Clock Circuits (Programmable Baud Generator)

Table 2. Typical Crystal Oscillator Network

CRYSTAL	Rp	RX2	C1	C2
1.8432 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF

8.2.3 Application Curves

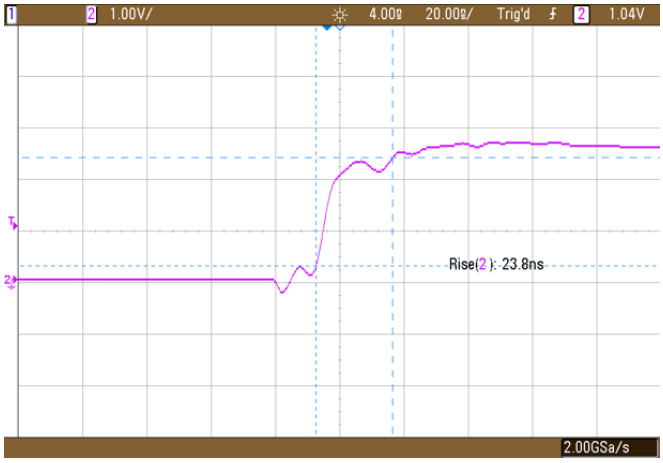


Figure 11. Rise Time of IR_TXD (Data)

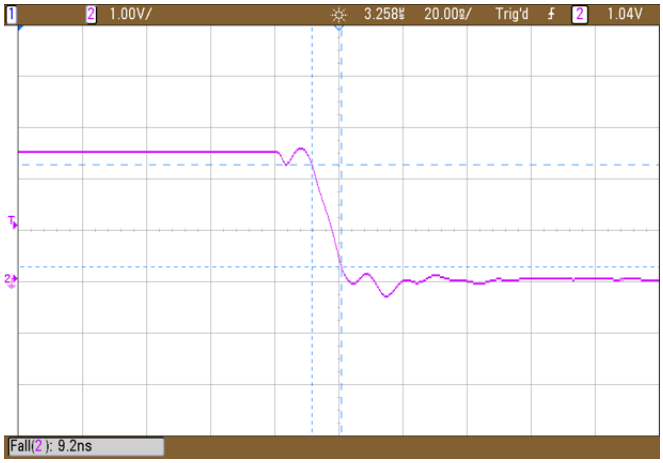


Figure 12. Fall Time of IR_TXD (Data)

9 Power Supply Recommendations

All power rails require a 10-µF capacitor or 1-µF capacitors for stability and noise immunity. These bulk capacitors can be placed anywhere on the power rail. The smaller decoupling capacitors must be placed as close to the power pins of the TIR1000 device as possible with an optimal grouping of two of differing values per pin.

10 Layout

10.1 Layout Guidelines

There is no fundamental information about how many layers should be used and how the board stackup should look. Again, the easiest way the get good results is to use the design from the EVMs of Texas Instruments. The magazine *Elektronik Praxis* has published an article with an analysis of different board stackups. These are listed in Table 3. Generally, the use of microstrip traces needs at least two layers, whereas one of them must be a GND plane. Better is the use of a four-layer PCB, with a GND and a VCC plane and two signal layers. If the circuit is complex and signals must be routed as stripline, because of propagation delay and/or characteristic impedance, a six-layer stackup should be used.

Table 3. Possible Board Stackup on a Four-Layer PCB

	MODEL 1	MODEL 2	MODEL 3	MODEL 4
Layer 1	SIG	SIG	SIG	GND
Layer 2	SIG	GND	GND	SIG
Layer 3	VCC	VCC	SIG	VCC
Layer 4	GND	SIG	VCC	SIG
Decoupling	Good	Good	Bad	Bad
EMC	Bad	Bad	Bad	Bad
Signal integrity	Bad	Bad	Good	Bad
Self disturbance	Satisfaction	Satisfaction	Satisfaction	High

Avoid right-angle bends in a trace and try to route them at least with two 45° corners. To minimize any impedance change, the best routing would be a round bend as shown in Figure 13.

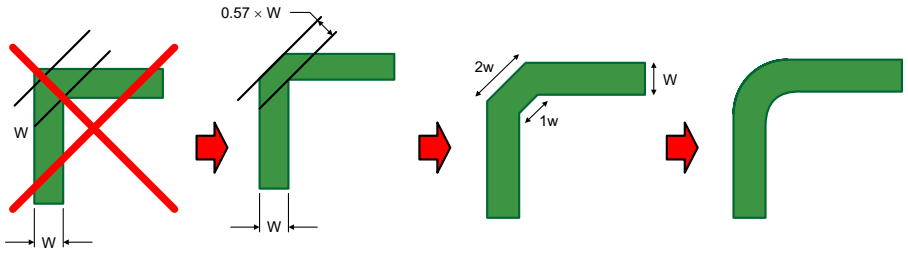


Figure 13. Poor and Good Right Angle Bends

10.2 Layout Example

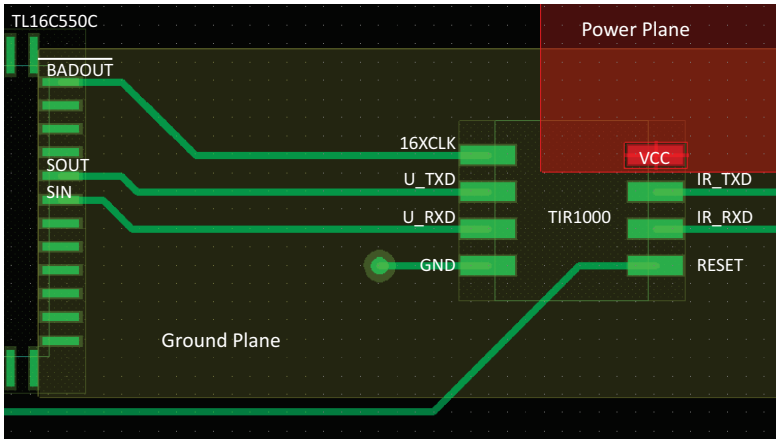


Figure 14. Layout Example

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
IrDA is a trademark of Infrared Data Association.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TIR1000IPS	ACTIVE	SO	PS	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	IR1000I	Samples
TIR1000IPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	IR1000I	Samples
TIR1000IPW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	R1000I	Samples
TIR1000IPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	R1000I	Samples
TIR1000PS	ACTIVE	SO	PS	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	IR1000	Samples
TIR1000PSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	IR1000	Samples
TIR1000PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	IR1000	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

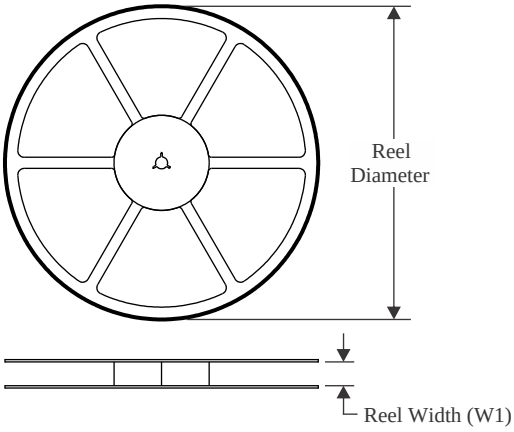
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

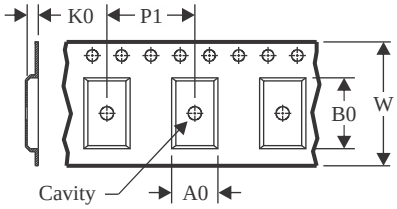
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

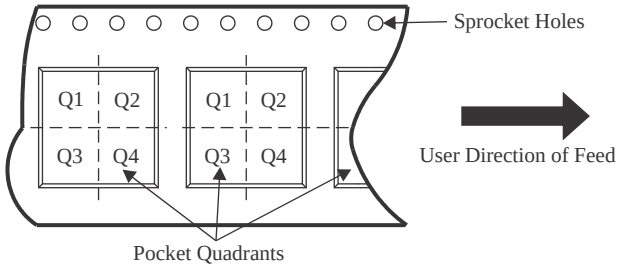


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

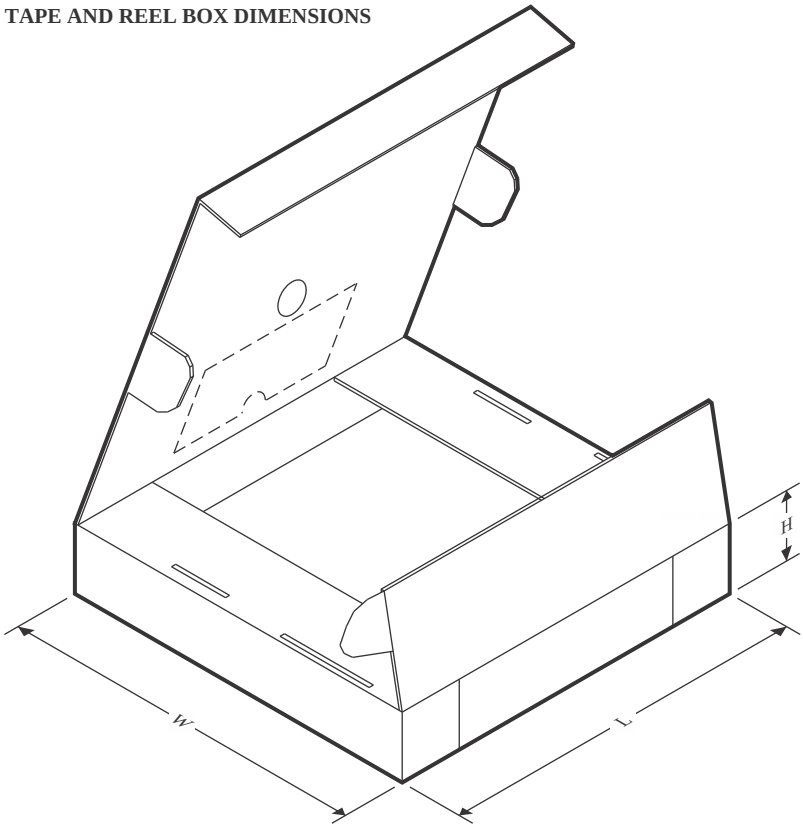
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TIR1000IPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.5	12.0	16.0	Q1
TIR1000IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TIR1000PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.5	12.0	16.0	Q1
TIR1000PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

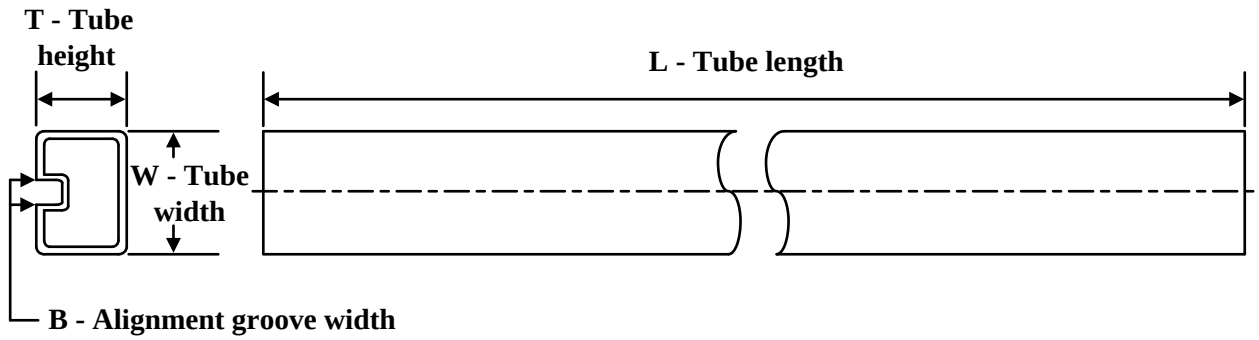
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TIR1000IPSR	SO	PS	8	2000	356.0	356.0	35.0
TIR1000IPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TIR1000PSR	SO	PS	8	2000	356.0	356.0	35.0
TIR1000PWR	TSSOP	PW	8	2000	356.0	356.0	35.0

TUBE

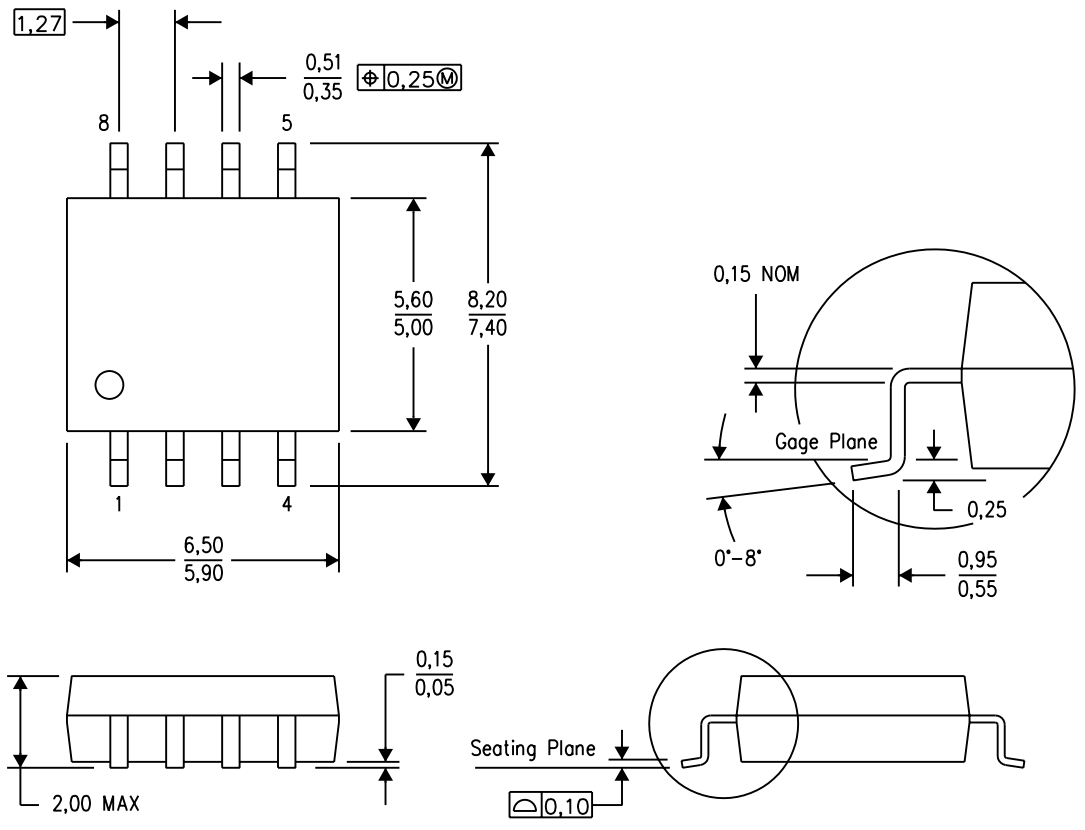


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TIR1000IPS	PS	SOP	8	80	530	10.5	4000	4.1
TIR1000IPW	PW	TSSOP	8	150	530	10.2	3600	3.5
TIR1000PS	PS	SOP	8	80	530	10.5	4000	4.1

MECHANICAL DATA

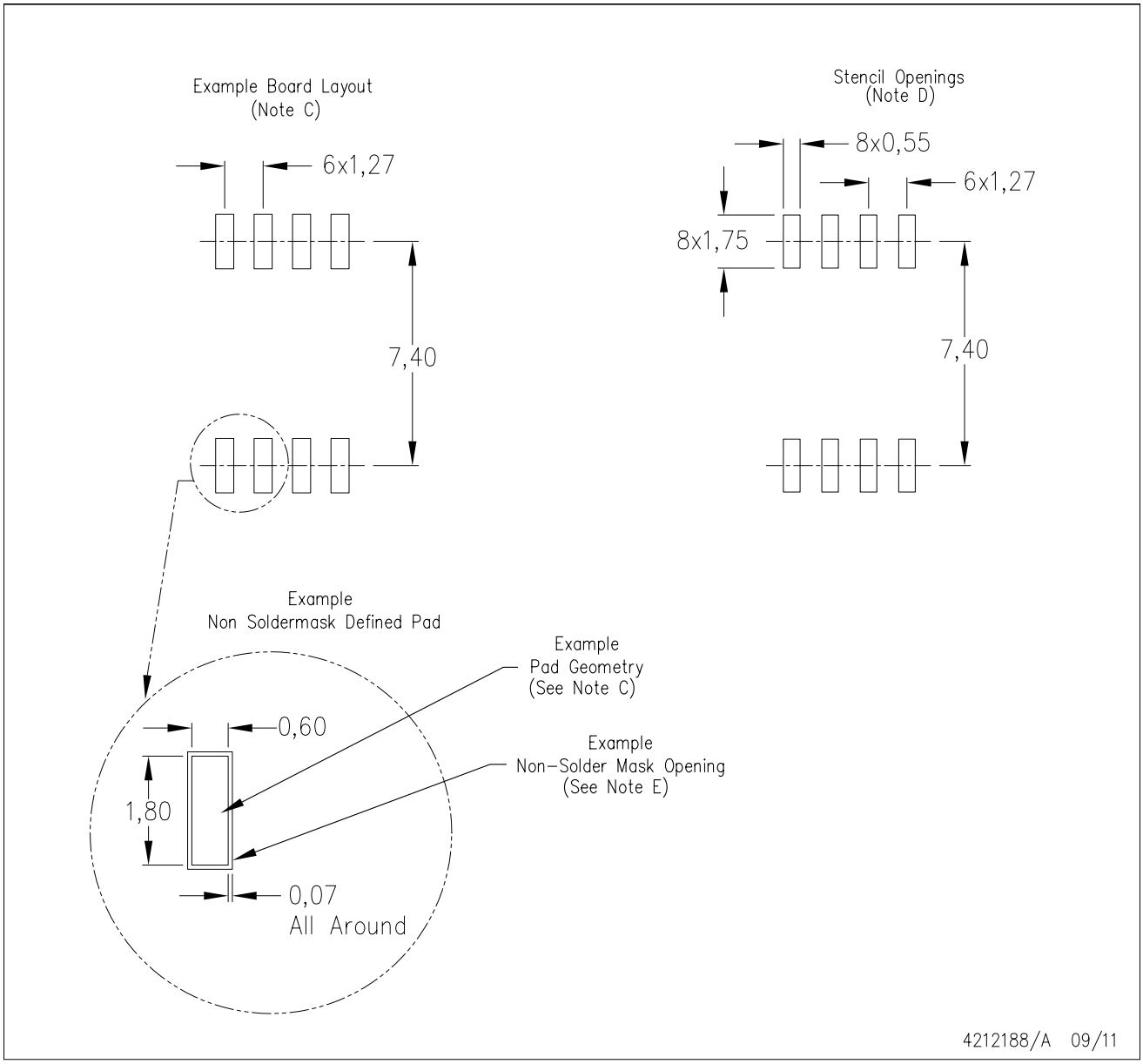
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



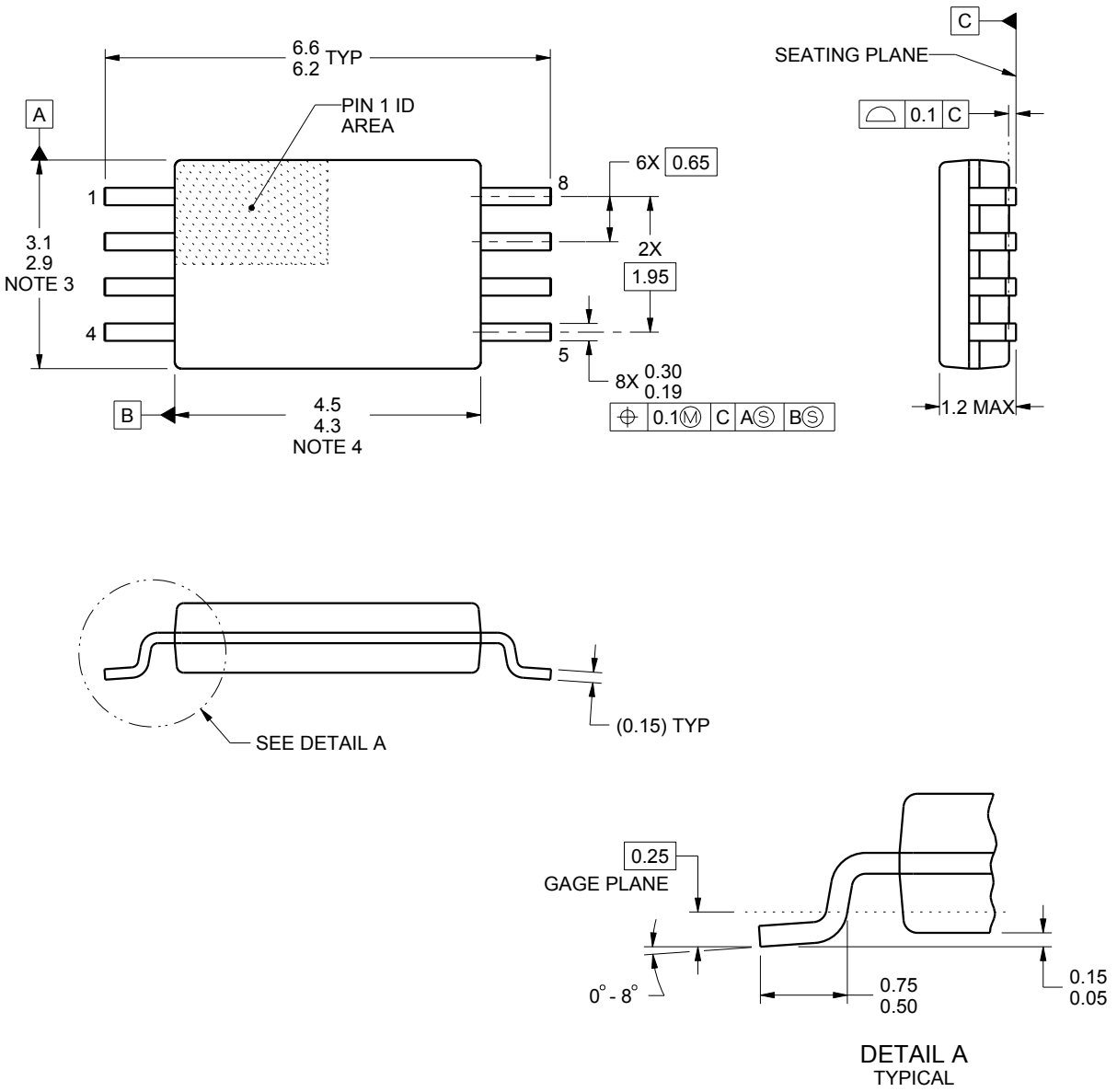
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0008A

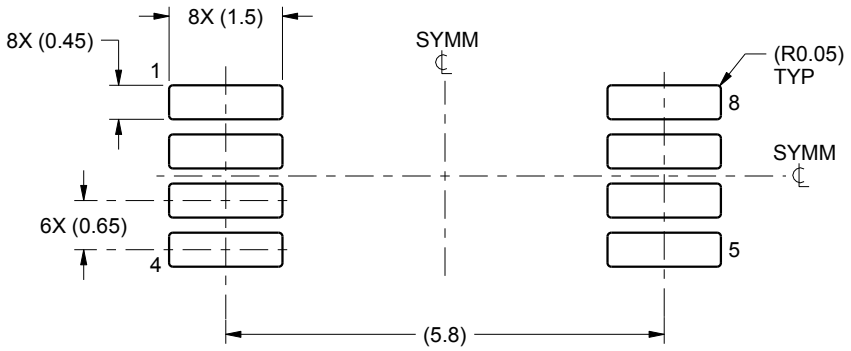
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

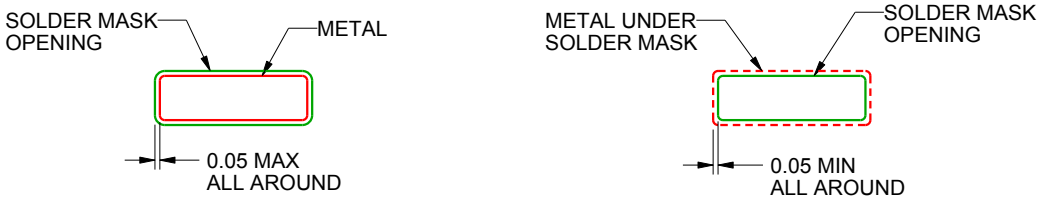


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

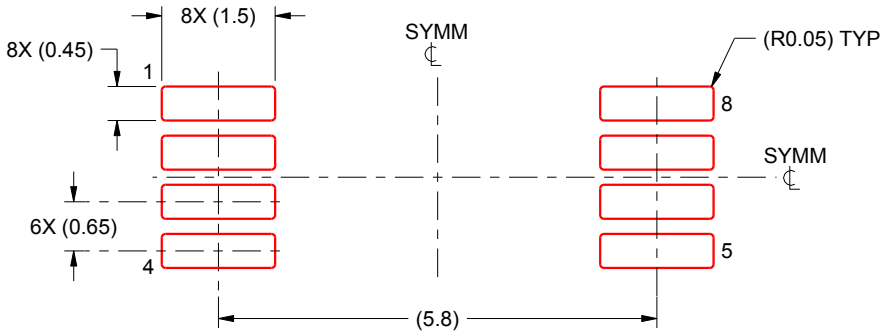


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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