THE DATASHEET OF

THS7303PWR

www.win-source.net 0086-755-83957316

3-Channel, Low-Power Video Amplifier with I²C Control, Selectable Filters, 6-dB Gain, SAG Correction, 2:1 Input MUX, and Selectable Input Bias Modes

Check for Samples: THS7303

FEATURES

- 3-Video Amplifiers for CVBS, S-Video , Y'U'V', SD/ED/HD Y'P'$_B$P'$_R$, and G'B'R' (R'G'B')
- I²C™ Control of All Functions
- Integrated Low-Pass Filters
  - 5th-Order Butterworth Characteristics
  - Selectable Corner Frequencies of 9-MHz, 16-MHz, 35-MHz, and Bypass (190-MHz)
- Selectable Input Bias Modes
  - AC-Coupled with Sync-Tip-Clamp
  - AC-Coupled with Bias
  - DC-Coupled with 135-mV Input Shift
  - DC-Coupled
- 2:1 Input MUX Allows Multiple Input Sources
- Built-in 6-dB Gain (2 V/V)
- SAG Correction Capable
- 2.7-V to 5-V Single Supply Operation
- Low 16.6-mA (3.3 V) Total Quiescent Current
- Individual Disable (< 1 µA) and Mute Control
- Rail-to-Rail Output:
  - Output Swings within 100 mV from the Rails to Allow AC or DC Output Coupling
  - Supports Driving Two Lines per Channel
- Low Differential Gain/Phase of 0.13%/0.55°

APPLICATIONS

- Set Top Box Output Video Buffering
- PVR/DVDR Output Buffering
- USB/Portable Low Power Video Buffering

DESCRIPTION

Fabricated using the new complementary silicon-germanium (SiGe) BiCom-3 process, the THS7303 is a low-power, single-supply, 2.7-V to 5-V, 3-channel integrated video buffer. It incorporates a selectable fifth-order Butterworth filter to eliminate data converter images. The 9-MHz filter is a perfect choice for SDTV video including composite (CVBS), S-Video, and 480i/576i Y'P'$_B$P'$_R$, and G'B'R' (R'G'B') signals. The 16-MHz filter is ideal for EDTV 480p/576p Y'P'$_B$P'$_R$, G'B'R', and VGA signals. The 35-MHz filter is useful for HDTV 720p/1080i Y'P'$_B$P'$_R$, G'B'R', and SVGA/XGA signals. For 1080p or SXGA/UXGA signals, the filter can be bypassed allowing a 190-MHz bandwidth, 300-V/µs amplifier to buffer the signal.

Each channel of the THS7303 is individually I²C configurable for all functions which makes it flexible for any application. Its rail-to-rail output stage allows for both ac and dc coupling applications. The 6-dB gain along with the built-in SAG correction allows for maximum flexibility as an output video buffer.

The 16.6-mA total quiescent current (55 mW total power) makes the THS7303 an excellent choice for USB powered or portable video applications. While fully disabled, the THS7303 consumes less than 1 µA making it ideal for energy sensitive applications.

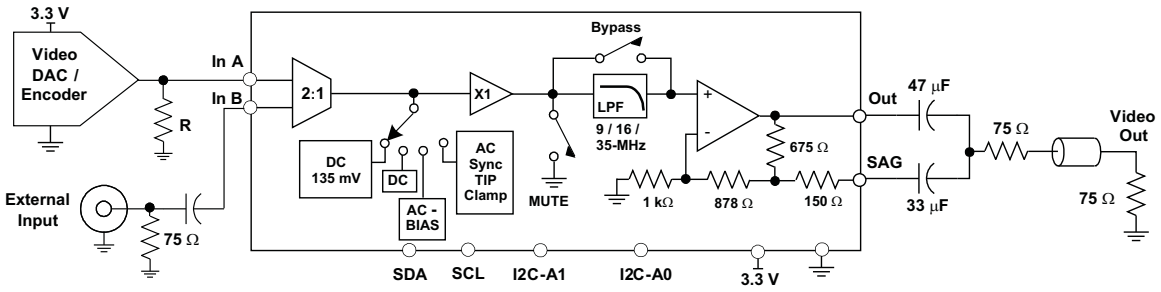

Figure 1. 3.3-V, Single-Supply, DC-Input/AC-Video Output System with SAG Correction (1 of 3 Channels Shown)

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

As part of the THS7303 flexibility, the 2:1 MUX input can be selected for ac- or dc-coupled inputs. The ac-coupled modes include a sync-tip-clamp option for CVBS/Y'/G'/B'/R' with sync or a fixed bias for the C'/P'$_B$/P'$_R$ non-sync channels. The dc input options include a dc input or a (dc + 135-mV) input offset shift to allow for a full sync dynamic range at the output with 0-V input.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	TRANSPORT MEDIA, QUANTITY
THS7303PW	TSSOP-20	PW	Rails, 70
THS7303PWR			Tape and Reel, 2000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted).(1)

PARAMETER			UNIT
V_{SS}	Supply voltage, V_{S+} to GND		5.5 V
V_I	Input voltage		–0.4 V to V_{S+}
I_O	Output current		±125 mA
	Continuous power dissipation		See Dissipation Ratings Table
T_J	Maximum junction temperature, any condition(2)		+150°C
T_J	Maximum junction temperature, continuous operation, long term reliability(3)		+125°C
T_{stg}	Storage temperature range		–65°C to +150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		+300°C
	ESD ratings	HBM	2000 V
		CDM	750 V
		MM	100 V

(1) Stresses above those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied Exposure to absolute maximum rated conditions for extended periods may degrade device reliability.
(2) The absolute maximum junction temperature under any condition is limited by the constraints of the silicon process.
(3) The absolute maximum junction temperature for continuous operation is limited by the package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

DISSIPATION RATINGS

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	POWER RATING(1) (T_J = +125°C)	
			T_A = +25°C	T_A = +85°C
TSSOP-20 (PW)	32.3	83(2)	1.2 W	0.48 W

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	NOM	MAX	UNIT
V_{SS}	Supply voltage, V_{S+}	2.7		5	V
T_A	Ambient temperature	–40		+85	°C

(1) Power rating is determined with a junction temperature of +125°C. This is the point where distortion starts to substantially increase and long-term reliability starts to be reduced. Thermal management of the final PCB should strive to keep the junction temperature at or below +125°C for best performance and reliability.
(2) This data was taken with the JEDEC High-K test PCB. For the JEDEC low-K test PCB, the θ_{JA} is +125.8°C.

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ELECTRICAL CHARACTERISTICS: V_{S+} = 3.3 V

R_L = 150 Ω to GND, filter select = 9 MHz, input bias = dc, and SAG pin shorted to the output pin (unless otherwise noted).

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE			UNITS	MIN/MAX
		+25°C	+25°C	0°C to +70°C	–40°C to +85°C		
AC PERFORMANCE							
Small-signal bandwidth (–3 dB) V_O – 0.2 V_{PP}	Filter Select = 9 MHz(1)	9	7.6/10.4	7.4/10.6	7.3/10.7	MHz	Min/Max
	Filter select = 16 MHz(1)	16	13.4/18.6	13.1/18.9	13/19	MHz	Min/Max
	Filter select = 35 MHz(1)	35	29.4/40.6	29.1/40.9	29/41	MHz	Min/Max
	Filter select = bypass	175				MHz	
Large-signal bandwidth (–3 dB) V_O – 2 V_{PP}	Filter select = 9 MHz	9				MHz	
	Filter select = 16 MHz	16				MHz	
	Filter select = 35 MHz	35				MHz	
	Filter select = bypass	83				MHz	
Slew rate	Filter select = bypass, V_O = 2 V_{PP}	300				V/µs	
Group delay at 100 kHz	Filter select = 9 MHz	54				ns	
	Filter select = 16 MHz	31.5				ns	
	Filter select = 35 MHz	17				ns	
	Filter select = bypass	3				ns	
Group delay variation with respect to 100 kHz	Filter select = 9 MHz, at 5.1 MHz	10.5				ns	
	Filter select = 16 MHz, at 11 MHz	8				ns	
	Filter select = 35 MHz, at 27 MHz	4.8				ns	
Group delay matching	All filters: channel-to-channel	0.5				ns	
Attenuation with respect to 100 kHz	Filter select = 9 MHz, at 5.75 MHz	0.2	-0.3/0.9	-0.5/1.1	-0.6/1.2	dB	Min/Max
	Filter select = 9 MHz, at 27 MHz	43	33	32	31	dB	Min
	Filter select = 16 MHz, at 11 MHz	0.25	-0.3/0.9	-0.5/1.1	-0.6/1.2	dB	Min/Max
	Filter select = 16 MHz, at 54 MHz	44	33	32	31	dB	Min
	Filter select = 35 MHz, at 27 MHz	0.7	-0.3/2.7	-0.5/2.8	-0.6/2.9	dB	Min/Max
	Filter select = 35 MHz, at 74 MHz	28	15	14	13	dB	Min
Mute feedthrough	Filter select = bypass, at 30 MHz	-73				dB	
Differential gain	Filter select = 9 MHz, NTSC/PAL	0.13/0.27				%	
Differential phase	Filter select = 9 MHz, NTSC/PAL	0.55/0.65				°	
Total harmonic distortion f = 1 MHz, 2 V_{PP}	Filter select = 9 MHz	–59				dB	
	Filter select = 16 MHz	–62				dB	
	Filter select = 35 MHz	–58				dB	
	Filter select = bypass	–60				dB	
Signal-to-noise ratio (unified weighting per CCIR 576-2 recommendation)	Filter select = 9 MHz, 480i source	84				dB	
	Filter select = 16 MHz, 480p source	82				dB	
	Filter select = 35 MHz, 720p source	79				dB	
	Filter select = bypass(2), 720p source	67				dB	
Channel-to-channel crosstalk (V_O = 2 V_{PP})	Filter select = 9 MHz, at 1 MHz	–65				dB	
	Filter select = 16 MHz, at 1 MHz	–67				dB	
	Filter select = 35 MHz, at 1 MHz	–69				dB	
	Filter select = bypass, at 1 MHz	–70				dB	
MUX isolation	Filter select = 9 MHz, at 5.1 MHz	70				dB	
	Filter select = 16 MHz, at 11 MHz	69				dB	
	Filter select = 35 MHz, at 27 MHz	69				dB	
	Filter select = bypass, at 60 MHz	73				dB	
AC gain: all channels	f = 100 kHz	6	5.7/6.3	5.65/6.35	5.65/6.35	dB	Min/Max
Output impedance	f = 10 MHz	0.7				Ω	

(1) Min/Max values listed are specified by design only. PCB capacitance affects the filter characteristics, especially the 35-MHz and bypass mode responses.
(2) Bandwidth up to 100-MHz, no weighting, tilt null.

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ELECTRICAL CHARACTERISTICS: V_{S+} = 3.3 V (continued)

R_L = 150 Ω to GND, filter select = 9 MHz, input bias = dc, and SAG pin shorted to the output pin (unless otherwise noted).

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE				
		+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNITS	MIN/MAX
DC PERFORMANCE							
Output offset voltage	Bias = dc	35	90	95	95	mV	Max
Average offset voltage drift	Bias = dc				20	µV/°C	
Bias output voltage	Bias = dc + 135 mV, V_I = 0 V	290	235/345	215/360	200/375	mV	Min/Max
	Bias = ac	1.65	1.5/1.8	1.45/1.85	1.45/1.85	V	Min/Max
Sync-tip-clamp output voltage	Bias = ac STC	290	210/370	200/380	195/385	mV	Min/Max
Input bias current	Bias = dc, implies I_B out of the pin	–0.6	–4	–5	–5	µA	Max
Average bias current drift	Bias = dc				10	nA/°C	
Sync-tip-clamp bias current	Bias = ac STC, low bias	1.8	0.6/3.3	0.5/3.5	0.4/3.6	µA	Min/Max
	Bias = ac STC, mid bias	5.8	4.3/8.2	4.1/8.4	4/8.5	µA	Min/Max
	Bias = ac STC, high bias	7.8	6.2/10.8	6/11	5.9/11.1	µA	Min/Max
INPUT CHARACTERISTICS							
Input voltage range	Bias = dc, limited by output	0/1.57	0/1.52	0/1.47	0/1.47	V	Min/Max
Input resistance	Bias = ac bias mode	19				kΩ	
	Bias = dc, dc + 135 mV, ac STC	3				MΩ	
Input capacitance		2				pF	
OUTPUT CHARACTERISTICS							
High output voltage swing	R_L = 150 Ω to +1.65V	3.15	2.9	2.8	2.8	V	Min
	R_L = 150 Ω to GND	3.05	2.85	2.75	2.75	V	Min
	R_L = 75 Ω to +1.65V	3.05	2.8	2.7	2.7	V	Min
	R_L = 75 Ω to GND	2.9	2.65	2.55	2.55	V	Min
Low output voltage swing	R_L = 150 Ω to +1.65V	0.14	0.24	0.27	0.28	V	Max
	R_L = 150 Ω to GND	0.09	0.17	0.2	0.21	V	Max
	R_L = 75 Ω to GND	0.24	0.33	0.36	0.37	V	Max
	R_L = 75 Ω to GND	0.09	0.17	0.2	0.21	V	Max
Output current	R_L = 10 Ω to +1.65V, sourcing	70	45	42	40	mA	Min
	R_L = 10 Ω to +1.65V, sinking	70	45	42	40	mA	Min
POWER SUPPLY							
Maximum operating voltage		3.3	5.5	5.5	5.5	V	Max
Minimum operating voltage		3.3	2.6	2.6	2.6	V	Min
Maximum quiescent current	Per channel V_I = 200 mV	6	7.2	7.4	7.5	mA	Max
Minimum quiescent current	Per channel V_I = 200 mV	6	4.8	4.6	4.5	mA	Min
Total quiescent current	All channels on, V_I = 200 mV(3)	16.6				mA	
Power-supply rejection (+PSRR)	V_{S+} = 3.5 V to 3.1 V	62	37	35	35	dB	Min
DISABLE CHARACTERISTICS							
Quiescent current	All 3 channels disabled (4)	0.1				µA	
Turn-on time delay (t_{ON})	Time reaches 50% of final value after I^2C control is completed	5				µs	
Turn-on time delay (t_{OFF})		2				µs	
DIGITAL CHARACTERISTICS							
High-level input voltage V_{IH}		2.3				V	Typ
Low-level input voltage V_{IL}		1.0				V	Typ

(3) Due to sharing of internal bias circuitry, the quiescent current (with all channels operating) is less than the single individual channel quiescent currents added together.

(4) Note that the I^2C circuitry is still active while in Disable mode. The current shown is while there is no activity with the device I^2C circuitry.

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ELECTRICAL CHARACTERISTICS: V_{S+} = 5 V

R_L = 150 Ω to GND, filter select = 9 MHz, input bias = dc, and SAG pin shorted to the output pin (unless otherwise noted).

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE				
		+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNITS	MIN/MAX
AC PERFORMANCE							
Small-signal bandwidth (–3 dB) V_O – 0.1 V_{PP}	Filter select = 9 MHz(1)	9	7.6/10.4	7.4/10.6	7.3/10.7	MHz	Min/Max
	Filter select = 16 MHz(1)	16	13.4/18.6	13.1/18.9	13/19	MHz	Min/Max
	Filter select = 35 MHz(1)	35	29.4/40.6	29.1/40.9	29/41	MHz	Min/Max
	Filter select = bypass	190				MHz	
Large-signal bandwidth (–3 dB) V_O – 2 V_{PP}	Filter select = 9 MHz	9				MHz	
	Filter select = 16 MHz	16				MHz	
	Filter select = 35 MHz	35				MHz	
	Filter select = bypass	90				MHz	
Slew rate	Filter select = bypass	320				V/µs	
Group delay at 100 kHz	Filter select = 9 MHz	53				ns	
	Filter select = 16 MHz	31				ns	
	Filter select = 35 MHz	16.5				ns	
	Filter select = bypass	2.9				ns	
Group delay variation with respect to 100 kHz	Filter select = 9 MHz, at 5.1 MHz	10.5				ns	
	Filter select = 16 MHz, at 11 MHz	7.5				ns	
	Filter select = 35 MHz, at 27 MHz	4.5				ns	
Group delay matching	All filters: channel-to-channel	0.5				ns	
Attenuation with respect to 100 kHz	Filter select = 9 MHz, at 5.75 MHz	0.2	-0.3/0.9	-0.5/1.1	-0.6/1.2	dB	Min/Max
	Filter select = 9 MHz, at 27 MHz	42	33	32	31	dB	Min
	Filter select = 16 MHz, at 11 MHz	0.25	-0.3/0.9	-0.5/1.1	-0.6/1.2	dB	Min/Max
	Filter select = 16 MHz, at 54 MHz	44	33	32	31	dB	Min
	Filter select = 35 MHz, at 27 MHz	0.7	-0.3/2.7	-0.5/2.8	-0.6/2.9	dB	Min/Max
	Filter select = 35 MHz, at 74 MHz	28	15	14	13	dB	Min
Mute feedthrough	Filter select = bypass, at 30 MHz	73				dB	
Differential gain	Filter select = 9 MHz, NTSC/PAL	0.2/0.35				%	
Differential phase	Filter select = 9 MHz, NTSC/PAL	0.73/0.86				°	
Total harmonic distortion f = 1 MHz, 2 V_{PP}	Filter select = 9 MHz	–61				dB	
	Filter select = 16 MHz	–66				dB	
	Filter select = 35 MHz	–66				dB	
	Filter select = bypass	–67				dB	
Signal-to-noise ratio (unified weighting per CCIR 576-2 recommendation)	Filter select = 9 MHz, 480i source	84				dB	
	Filter select = 16 MHz, 480p source	82				dB	
	Filter select = 35 MHz, 720p source	79				dB	
	Filter select = bypass(2), 720p source	67				dB	
Channel-to-channel crosstalk	Filter select = 9 MHz: at 1 MHz	–65				dB	
	Filter select = 16 MHz: at 1 MHz	–67				dB	
	Filter select = 35 MHz: at 1 MHz	–69				dB	
	Filter select = bypass: at 1 MHz	–70				dB	
MUX isolation	Filter select = 9 MHz: at 5.1 MHz	70				dB	
	Filter select = 16 MHz: at 11 MHz	69				dB	
	Filter select = 35 MHz: at 27 MHz	71				dB	
	Filter select = bypass: at 60 MHz	68				dB	
AC gain: all channels	f = 100 kHz	6	5.7/6.3	5.65/6.35	5.65/6.35	dB	Min/Max
Output impedance	f = 10 MHz	0.7				Ω	

(1) Min/Max values listed are specified by design only. PCB capacitance affects the filter characteristics, especially the 35-MHz and bypass mode responses.
(2) Bandwidth up to 100-MHz, no weighting, tilt null.

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ELECTRICAL CHARACTERISTICS: V_{S+} = 5 V (continued)

R_L = 150 Ω to GND, filter select = 9 MHz, input bias = dc, and SAG pin shorted to the output pin (unless otherwise noted).

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE				
		+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNITS	MIN/MAX
DC PERFORMANCE							
Output offset voltage	Bias = dc	30	90	95	95	mV	Max
Average offset voltage drift	Bias = dc				20	µV/°C	
Bias output voltage	Bias = dc + 135 mV, V_I = 0 V	290	235/345	215/360	200/375	mV	Min/Max
	Bias = ac	2.5	2.3/2.7	2.25/2.75	2.25/2.75	V	Min/Max
Sync-tip-clamp output voltage	Bias = ac STC	300	230/375	215/385	210/390	mV	Min/Max
Input bias current	Bias = dc, implies I_B out of the pin	–0.6	–4	–5	–5	µA	Max
Average bias current drift	Bias = dc				10	nA/°C	
Sync-tip-clamp bias current	Bias = ac STC, low bias	1.9	0.6/3.3	0.5/3.5	0.4/3.6	µA	Min/Max
	Bias = ac STC, mid bias	6	4.3/8.2	4.1/8.4	4/8.5	µA	Min/Max
	Bias = ac STC, high bias	8.2	6.2/10.8	6/11	5.9/11.1	µA	Min/Max
INPUT CHARACTERISTICS							
Input voltage range	Bias = dc, limited by output	0/2.4	0/2.35	0/2.3	0/2.3	V	Min/Max
Input resistance	Bias = ac bias mode	19				kΩ	
	Bias = dc, dc + 135 mV, ac STC	3				MΩ	
Input capacitance		2				pF	
OUTPUT CHARACTERISTICS							
High output voltage swing	R_L = 150 Ω to +2.5V	4.8	4.4	4.3	4.3	V	Min
	R_L = 150 Ω to GND	4.65	4.2	4.1	4.1	V	Min
	R_L = 75 Ω to +2.5V	4.7	4.3	4.2	4.2	V	Min
	R_L = 75 Ω to GND	4.4	4.1	4	4	V	Min
Low output voltage swing	R_L = 150 Ω to +2.5V	0.2	0.34	0.37	0.37	V	Max
	R_L = 150 Ω to GND	0.1	0.23	0.26	0.27	V	Max
	R_L = 75 Ω to GND	0.35	0.46	0.5	0.5	V	Max
	R_L = 75 Ω to GND	0.1	0.23	0.26	0.27	V	Max
Output current	R_L = 10 Ω to +2.5V, sourcing	85	60	57	55	mA	Min
	R_L = 10 Ω to +2.5V, sinking	85	60	57	55	mA	Min
POWER SUPPLY							
Maximum operating voltage		5	5.5	5.5	5.5	V	Max
Minimum operating voltage		5	2.6	2.6	2.6	V	Min
Maximum quiescent current	Per channel V_I = 200 mV	6.6	7.9	8.1	8.2	mA	Max
Minimum quiescent current	Per channel V_I = 200 mV	6.6	5.3	5.1	5	mA	Min
Total quiescent current	All channels on, V_I = 200 mV(3)	18.9				mA	
Power-supply rejection (+PSRR)	V_{S+} = 5.2 V to 4.8 V	66	38	36	36	dB	Min
DISABLE CHARACTERISTICS							
Quiescent current	All 3 channels disabled (4)	0.5				µA	
Turn-on time delay (t_{ON})	Time reaches 50% of final value after I^2C control is completed	5				µs	
Turn-on time delay (t_{OFF})		2				µs	
DIGITAL CHARACTERISTICS							
High-level input voltage V_{IH}		3.5				V	Typ
Low-level input voltage V_{IL}		1.5				V	Typ

(3) Due to sharing of internal bias circuitry, the quiescent current (with all channels operating) is less than the single individual channel quiescent currents added together.

(4) Note that the I^2C circuitry is still active while in Disable mode. The current shown is while there is no activity with the device I^2C circuitry.

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TIMING REQUIREMENTS(1)

At V_{S+} = 2.7 V to 5 V, unless otherwise noted.

PARAMETER		STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
f_{SCL}	Clock frequency, SCL	0	100	0	400	kHz
$t_{w(H)}$	Pulse duration, SCL high	4		0.6		µs
$t_{w(L)}$	Pulse duration, SCL low	4.7		1.3		µs
t_r	Rise time, SCL and SDA		1000		300	ns
t_f	Fall time, SCL and SDA		300		300	ns
$t_{su(1)}$	Setup time, SDA to SCL	250		100		ns
$t_{h(1)}$	Hold time, SCL to SDA	0		0		ns
$t_{(buf)}$	Bus free time between stop and start conditions	4.7		1.3		µs
$t_{su(2)}$	Setup time, SCL to start condition	4.7		0.6		µs
$t_{h(2)}$	Hold time, start condition to SCL	4		0.6		µs
$t_{su(3)}$	Setup time, SCL to stop condition	4		0.6		µs
C_b	Capacitive load for each bus line		400		400	pF

(1) The THS7303 I^2C address = 01011(A1)(A0)(R/W). See the Application Information section for more information.

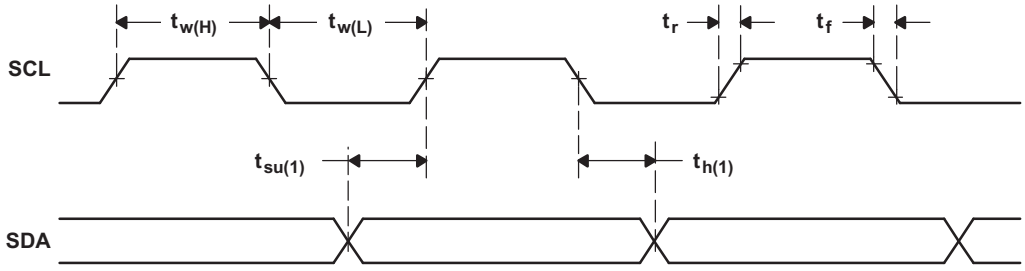

Figure 2. SCL and SDA Timing

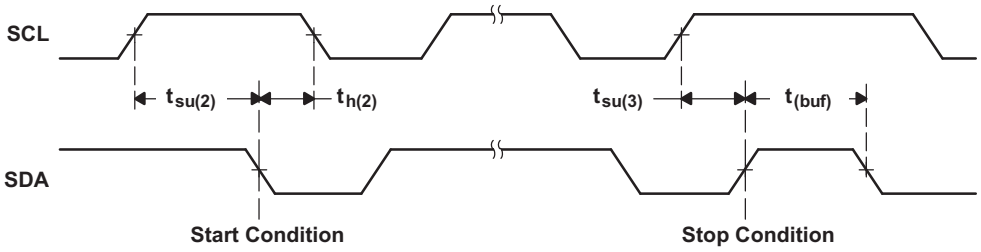

Figure 3. Start and Stop Conditions

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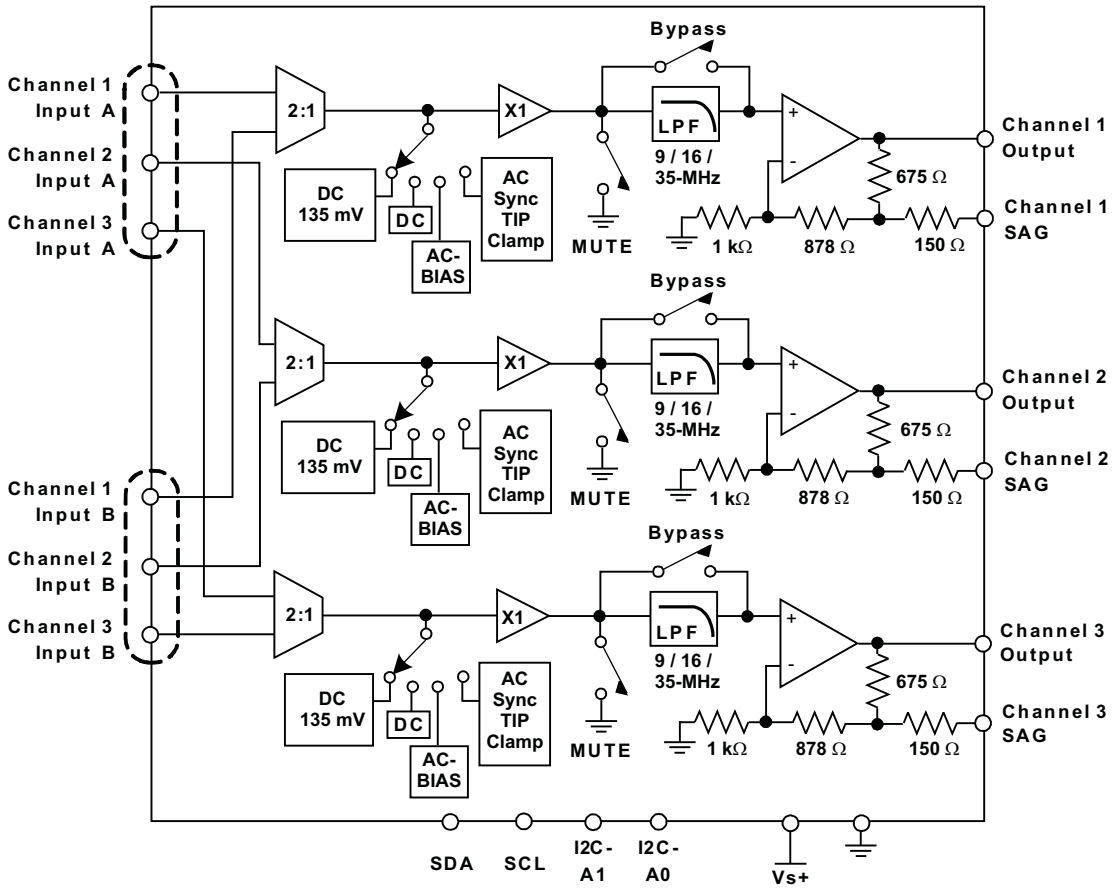
FUNCTIONAL BLOCK DIAGRAM



NOTE: The I^2C address of the THS7303 is 01011(A1)(A0)(R/W).

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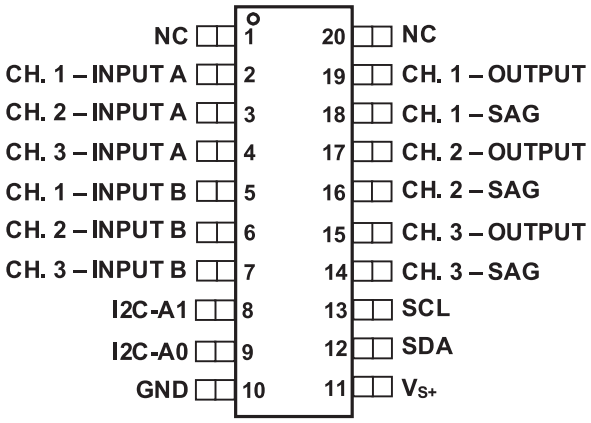
PIN CONFIGURATION

PW PACKAGE
TSSOP-20
(TOP VIEW)



PIN DESCRIPTIONS

PIN		DESCRIPTION
NAME	NO.	
N/C	1, 20	No internal connection. It is recommended, but not required, to connect these pins to GND.
CH. 1 – INPUT A	2	Video input channel 1, input A
CH. 2 – INPUT A	3	Video input channel 2, input A
CH. 3 – INPUT A	4	Video input channel 3, input A
CH. 1 – INPUT B	5	Video input channel 1, input B
CH. 2 – INPUT B	6	Video input channel 2, input B
CH. 3 – INPUT B	7	Video input channel 3, input B
I2C-A1	8	I^2C slave address control bit A1. Connect to V_{S+} for a logic 1 preset value or GND for a logic 0 preset value.
I2C-A0	9	I^2C slave address control bit A0. Connect to V_{S+} for a logic 1 preset value or GND for a logic 0 preset value.
GND	10	Ground reference pin for all internal circuitry.
V_{S+}	11	Positive power-supply input pin. Connect to 2.7 V to 5 V.
SDA	12	Serial data line of the I^2C bus. Pull-up resistor should have a minimum value of 2 kΩ and a maximum value of 19 kΩ. Pull up to V_{S+}.
SCL	13	I^2C bus clock line. Pull-up resistor should have a minimum value of 2 kΩ and a maximum value of 19 kΩ. Pull up to V_{S+}.
CH. 3 – SAG	14	Video output channel 3 SAG correction pin. If SAG is not used, connect directly to CH. 3 – OUTPUT pin.
CH. 3 – OUTPUT	15	Video output channel 3 from either CH. 3 – INPUT A or CH. 3 – INPUT B.
CH. 2 – SAG	16	Video output channel 2 SAG correction pin. If SAG is not used, connect directly to CH. 2 – OUTPUT pin.
CH. 2 – OUTPUT	17	Video output channel 2 from either CH. 2 – INPUT A or CH. 2 – INPUT B.
CH. 1 – SAG	18	Video output channel 1 SAG correction pin. If SAG is not used, connect directly to CH. 1 – OUTPUT pin.
CH. 1 – OUTPUT	19	Video output channel 1 from either CH. 1 – INPUT A or CH. 1 – INPUT B.

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TYPICAL CHARACTERISTICS

R_L = 150 Ω to GND and dc-coupled input and output, unless otherwise noted.

TOTAL QUIESCENT CURRENT vs SUPPLY VOLTAGE

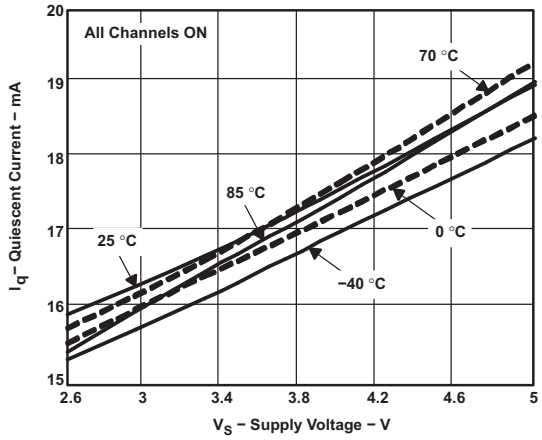

Figure 4.

INPUT BIAS CURRENT vs SUPPLY VOLTAGE

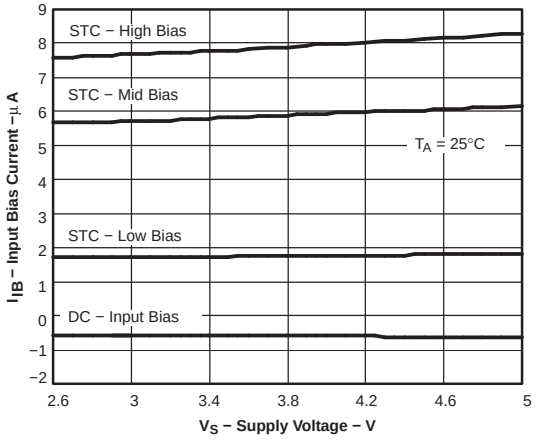

Figure 5.

MUTE FEEDTHROUGH vs FREQUENCY

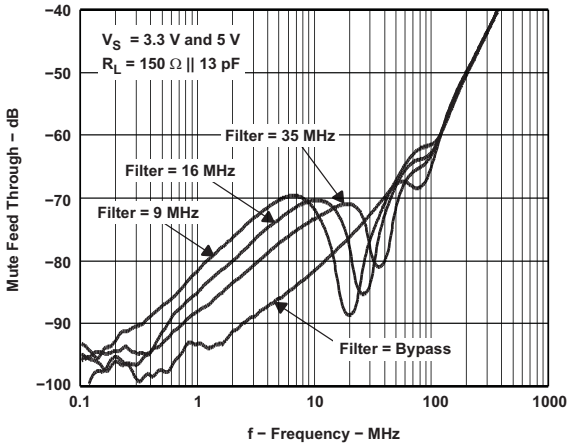

Figure 6.

CROSSTALK vs FREQUENCY

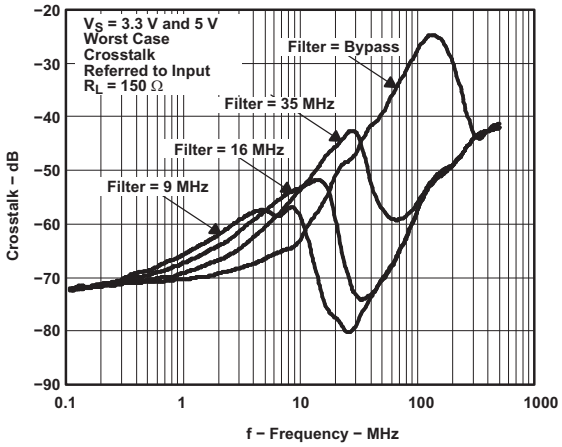

Figure 7.

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TYPICAL CHARACTERISTICS: V_{S+} = 3.3 V

R_L = 150 Ω to GND and dc-coupled input and output, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE

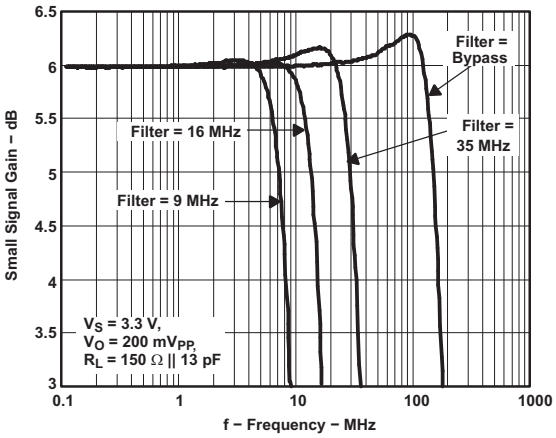

Figure 8.

SMALL-SIGNAL FREQUENCY RESPONSE

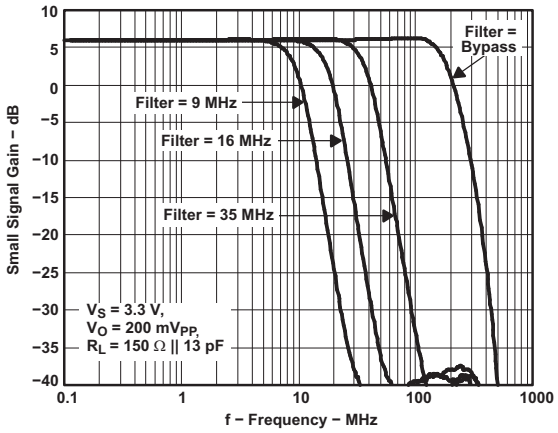

Figure 9.

GROUP DELAY vs FREQUENCY

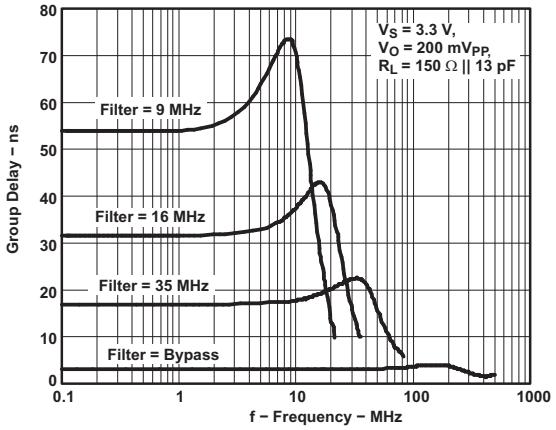

Figure 10.

PHASE RESPONSE vs FREQUENCY

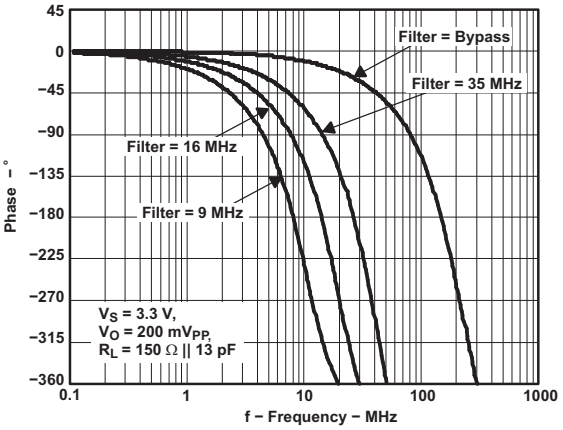

Figure 11.

SMALL- AND LARGE-SIGNAL FREQUENCY RESPONSE

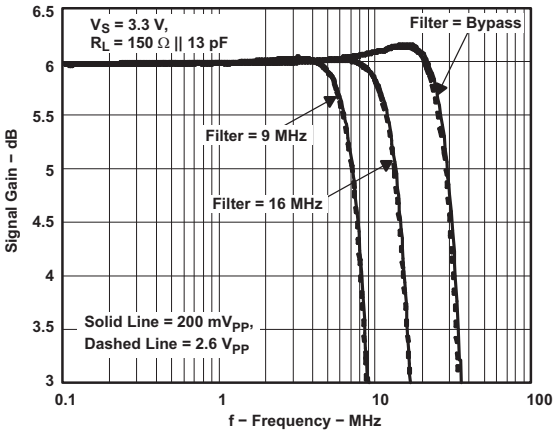

Figure 12.

SMALL- AND LARGE-SIGNAL FREQUENCY RESPONSE

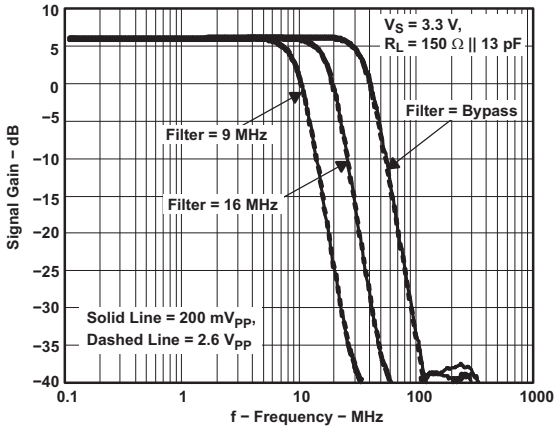

Figure 13.

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TYPICAL CHARACTERISTICS: V_{S+} = 3.3 V (continued)

R_L = 150 Ω to GND and dc-coupled input and output, unless otherwise noted.

SMALL- AND LARGE-SIGNAL FREQUENCY RESPONSE

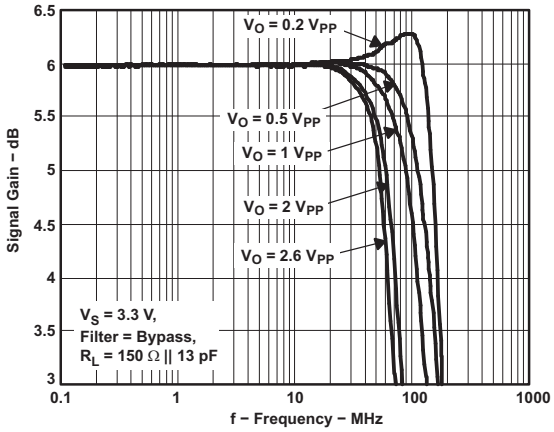

Figure 14.

OUTPUT IMPEDANCE vs FREQUENCY

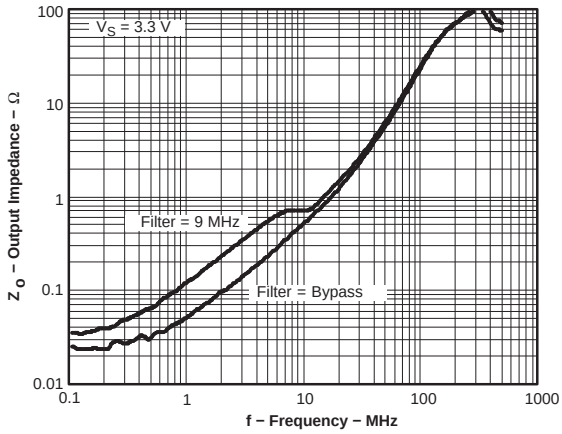

Figure 15.

3.3-V DIFFERENTIAL GAIN

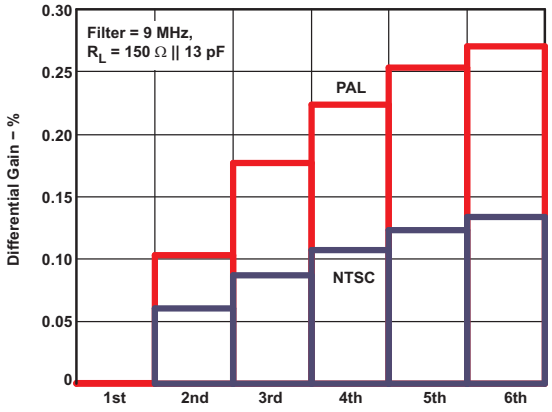

Figure 16.

3.3-V DIFFERENTIAL PHASE

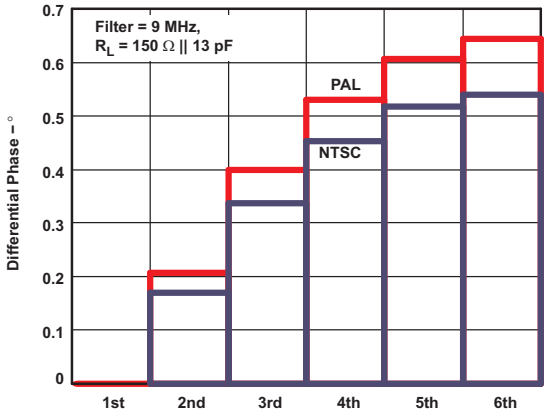

Figure 17.

HD2 vs FREQUENCY

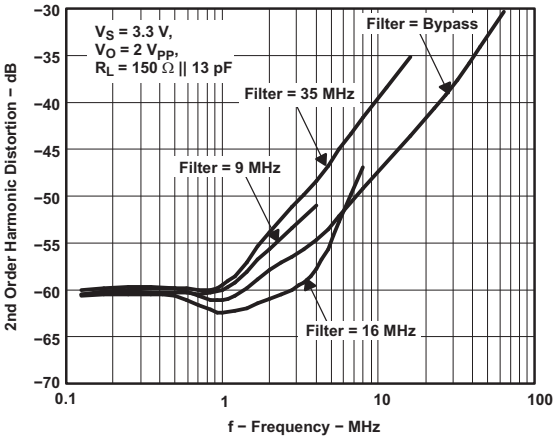

Figure 18.

HD3 vs FREQUENCY

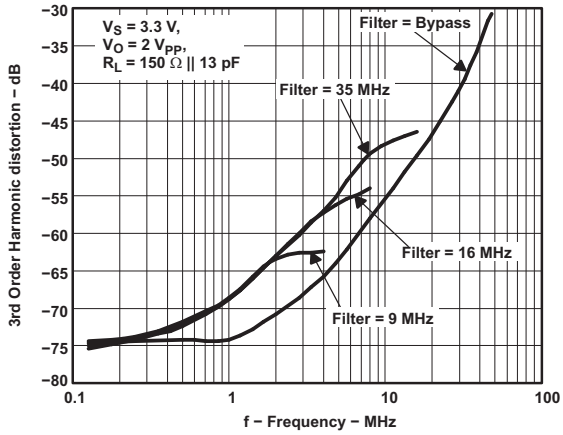

Figure 19.

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TYPICAL CHARACTERISTICS: V_{S+} = 3.3 V (continued)

R_L = 150 Ω to GND and dc-coupled input and output, unless otherwise noted.

HD2 vs OUTPUT VOLTAGE

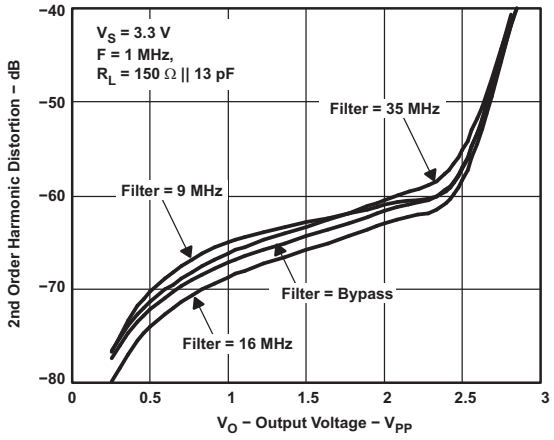

Figure 20.

HD3 vs OUTPUT VOLTAGE

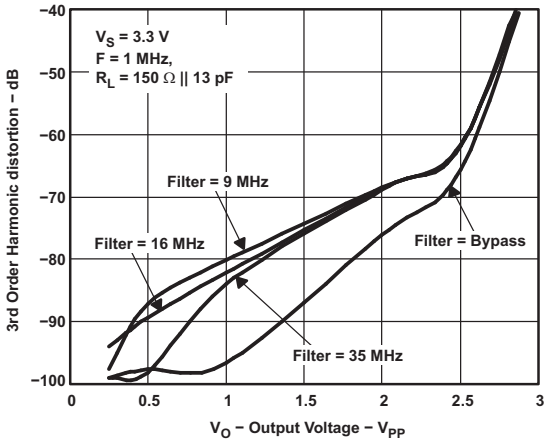

Figure 21.

SMALL-SIGNAL FREQUENCY RESPONSE WITH CAPACITIVE LOADING

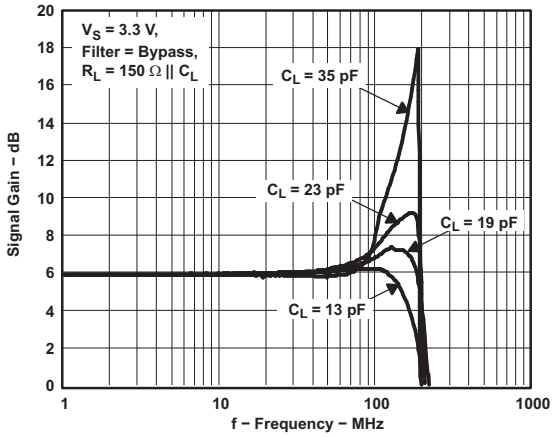

Figure 22.

SMALL-SIGNAL FREQUENCY RESPONSE WITH 19 pF CAPACITIVE LOAD

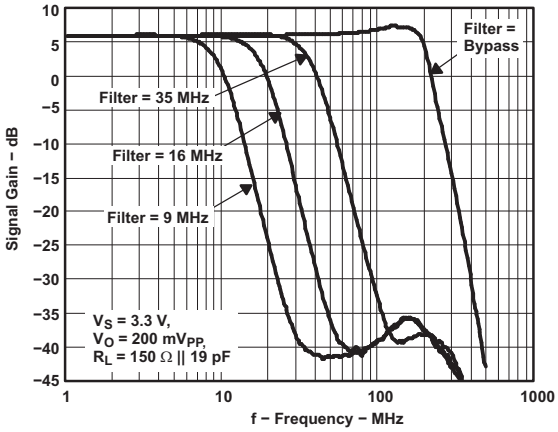

Figure 23.

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TYPICAL CHARACTERISTICS: V_{S+} = 3.3 V (continued)

R_L = 150 Ω to GND and dc-coupled input and output, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE WITH 23 pF CAPACITIVE LOAD

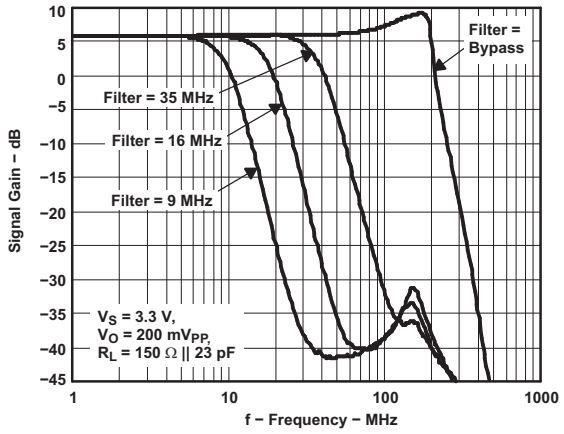

Figure 24.

SMALL-SIGNAL FREQUENCY RESPONSE WITH 35 pF CAPACITIVE LOAD

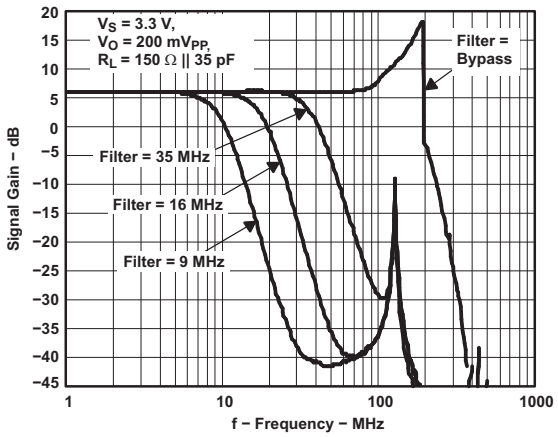

Figure 25.

SMALL-SIGNAL PULSE RESPONSE

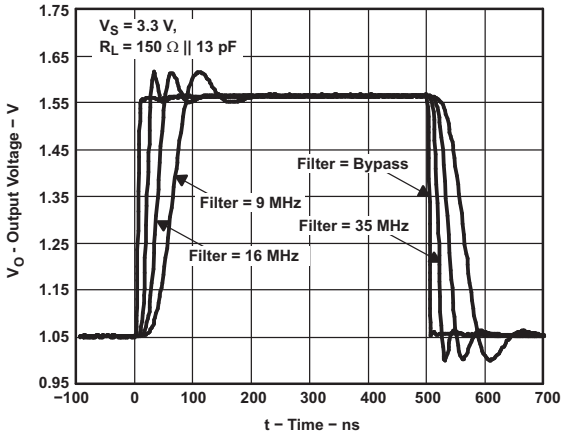

Figure 26.

LARGE-SIGNAL PULSE RESPONSE

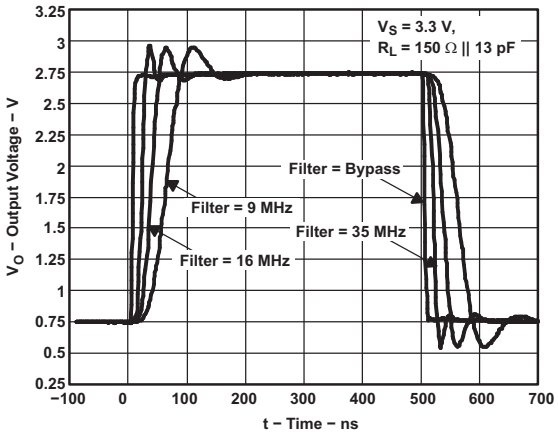

Figure 27.

NTSC - 2T RESPONSE

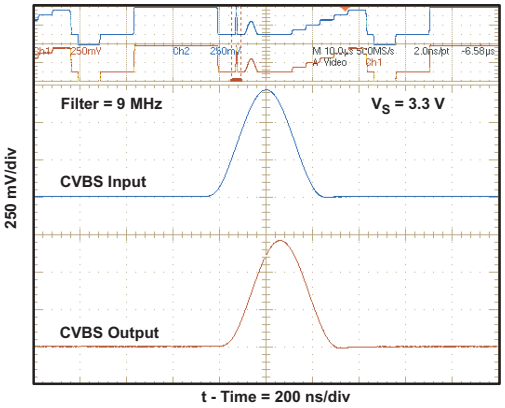

Figure 28.

PAL - 12.5T RESPONSE

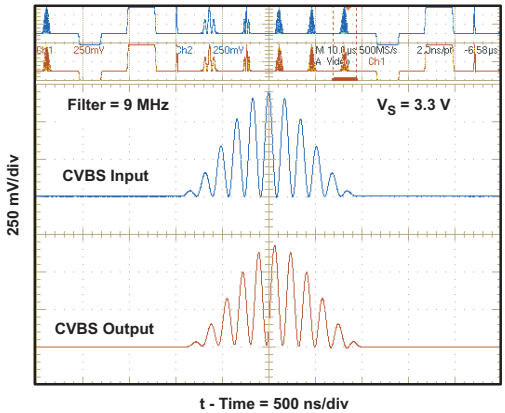

Figure 29.

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TYPICAL CHARACTERISTICS: V_{S+} = 3.3 V (continued)

R_L = 150 Ω to GND and dc-coupled input and output, unless otherwise noted.

576p - 2T PULSE RESPONSE

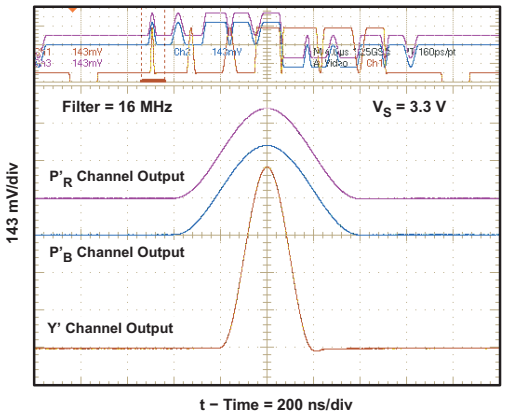

Figure 30.

720p - 2T PULSE RESPONSE

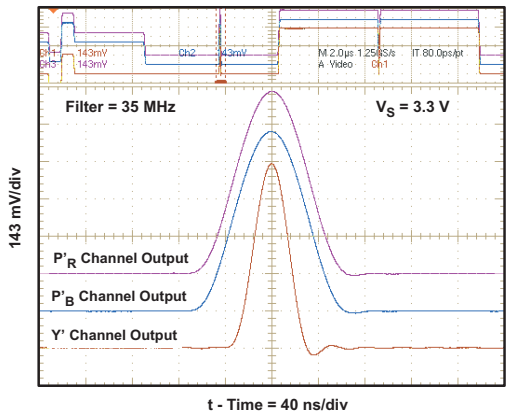

Figure 31.

SLEW RATE vs OUTPUT VOLTAGE

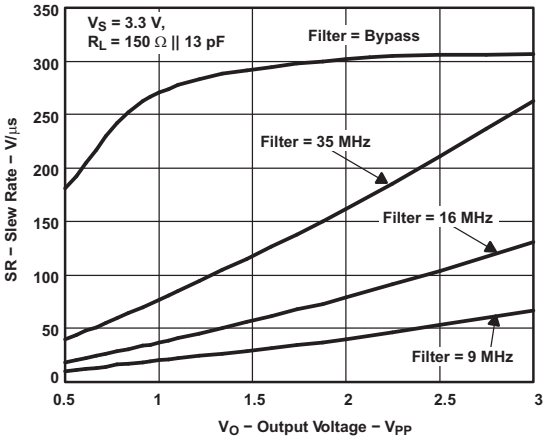

Figure 32.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

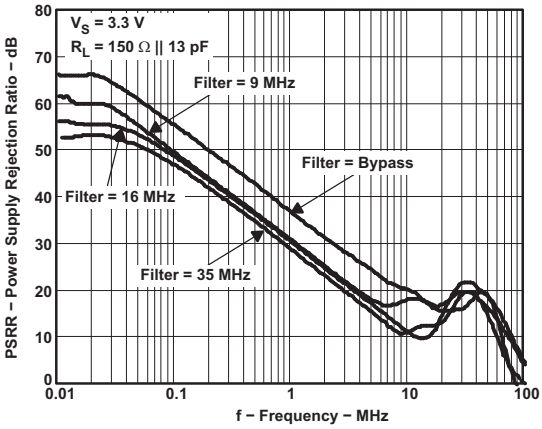

Figure 33.

TYPICAL CHARACTERISTICS: V_{S+} = 3.3 V (continued)

R_L = 150 Ω to GND and dc-coupled input and output, unless otherwise noted.

MUX FEEDTHROUGH vs FREQUENCY

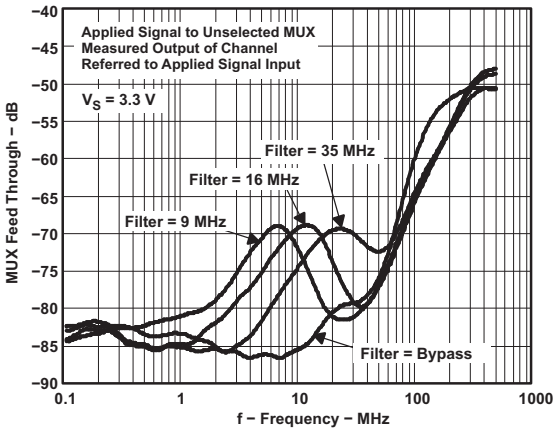

Figure 34.

INPUT BIAS CURRENT vs TEMPERATURE

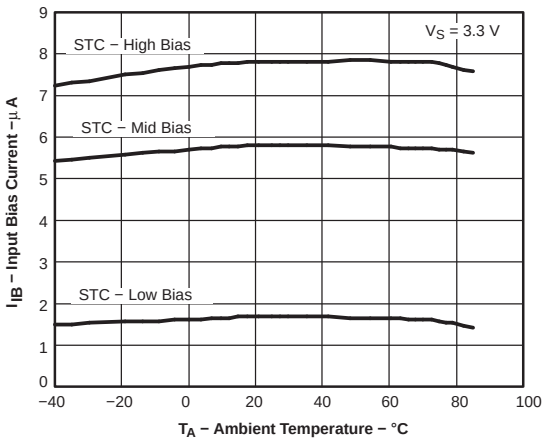

Figure 35.

TYPICAL CHARACTERISTICS: V_{S+} = 5 V

R_L = 150 Ω to GND and dc-coupled input and output, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE

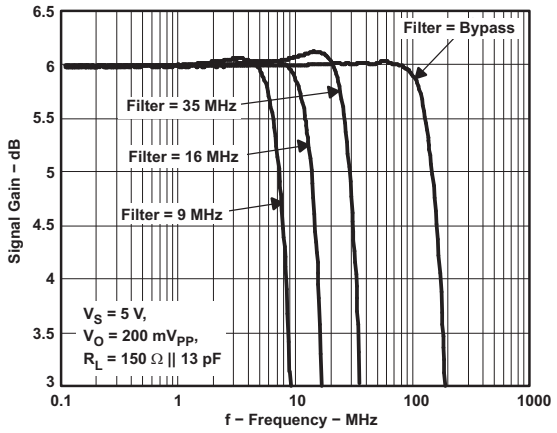

Figure 36.

SMALL-SIGNAL FREQUENCY RESPONSE

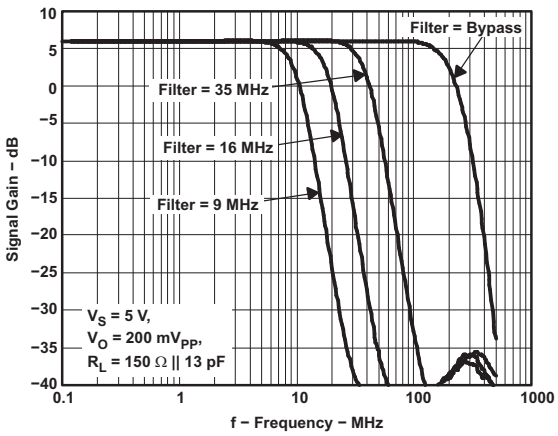

Figure 37.

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TYPICAL CHARACTERISTICS: V_{S+} = 5 V (continued)

R_L = 150 Ω to GND and dc-coupled input and output, unless otherwise noted.

GROUP DELAY vs FREQUENCY

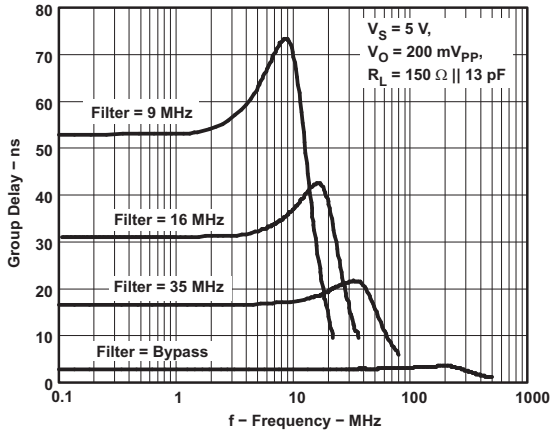

Figure 38.

PHASE vs FREQUENCY

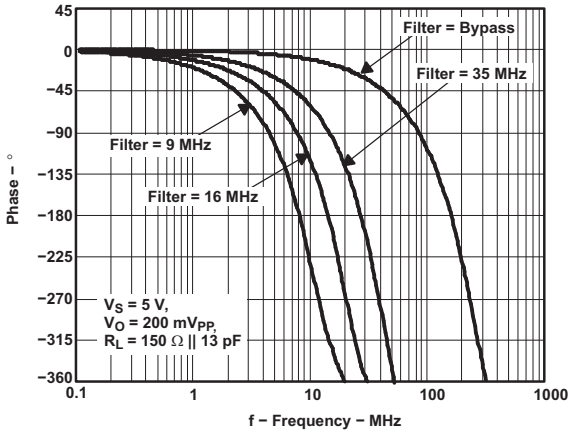

Figure 39.

SMALL- AND LARGE-SIGNAL FREQUENCY RESPONSE

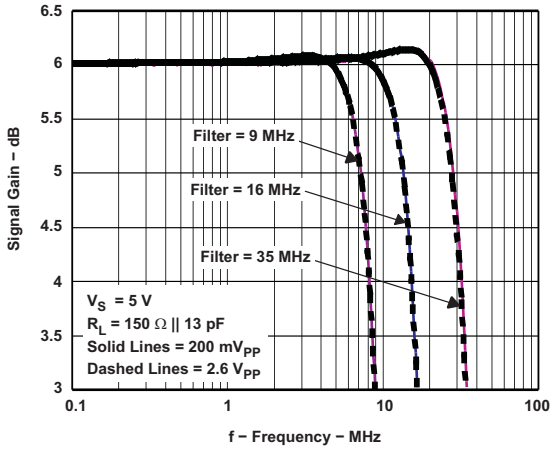

Figure 40.

SMALL- AND LARGE-SIGNAL FREQUENCY RESPONSE

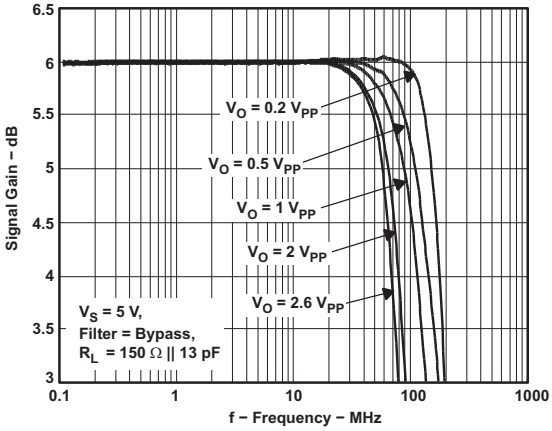

Figure 41.

5-V DIFFERENTIAL GAIN

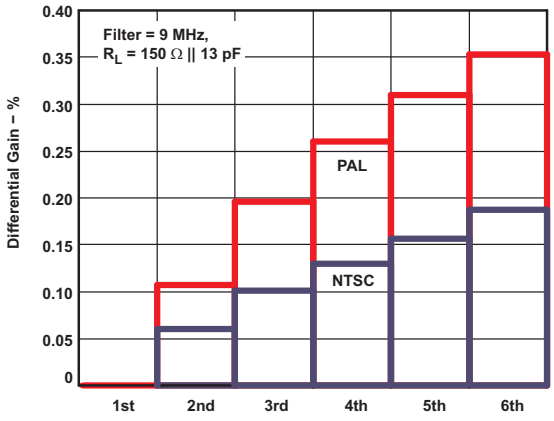

Figure 42.

5-V DIFFERENTIAL PHASE

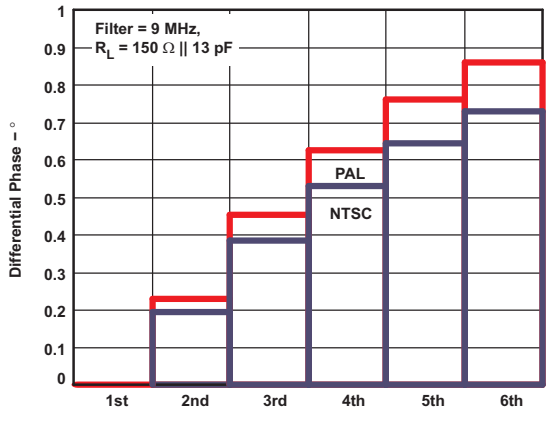

Figure 43.

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TYPICAL CHARACTERISTICS: V_{S+} = 5 V (continued)

R_L = 150 Ω to GND and dc-coupled input and output, unless otherwise noted.

HD2 vs FREQUENCY

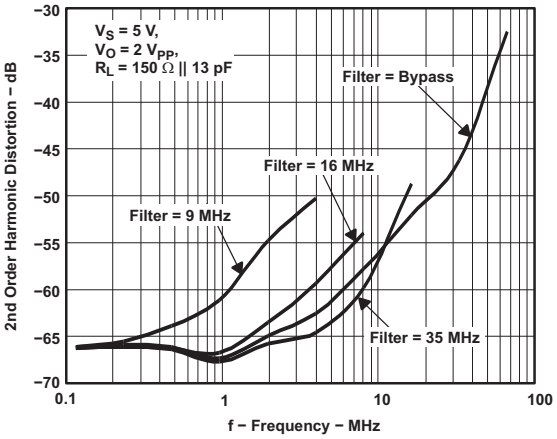

Figure 44.

HD3 vs FREQUENCY

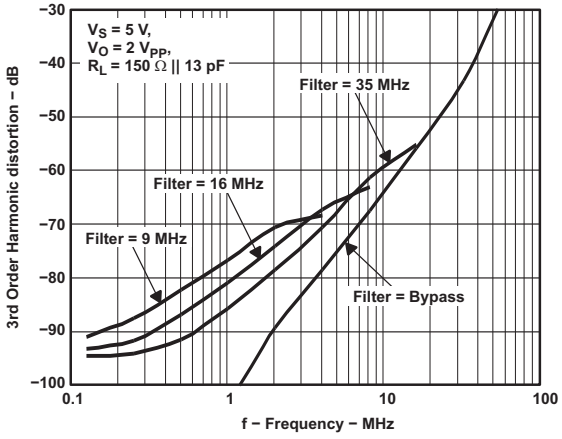

Figure 45.

HD2 vs OUTPUT VOLTAGE

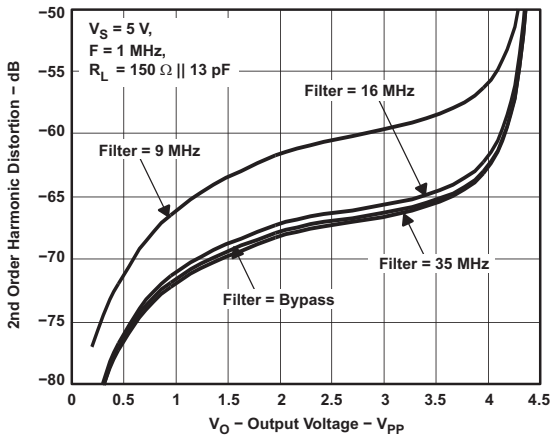

Figure 46.

HD3 vs OUTPUT VOLTAGE

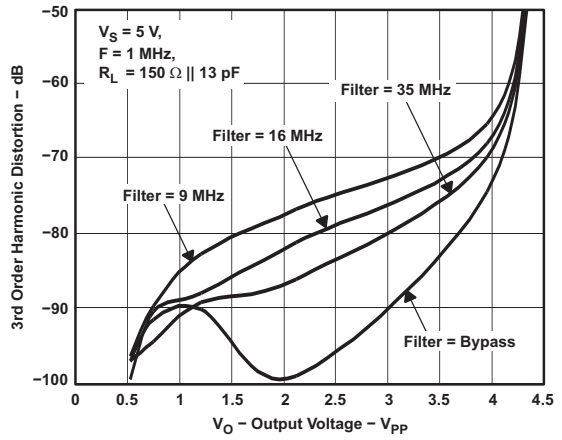

Figure 47.

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TYPICAL CHARACTERISTICS: V_{S+} = 5 V (continued)

R_L = 150 Ω to GND and dc-coupled input and output, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE WITH CAPACITIVE LOADING

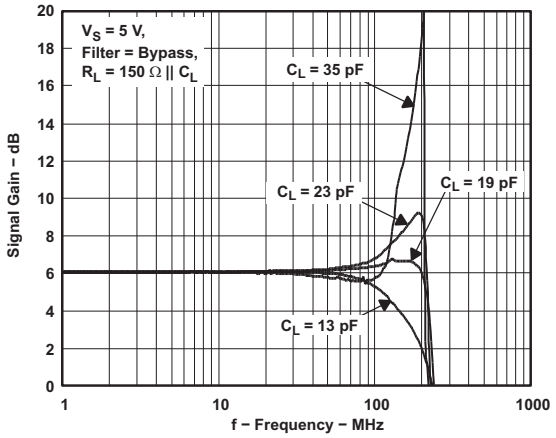

Figure 48.

SMALL-SIGNAL FREQUENCY RESPONSE WITH 19 pF CAPACITIVE LOAD

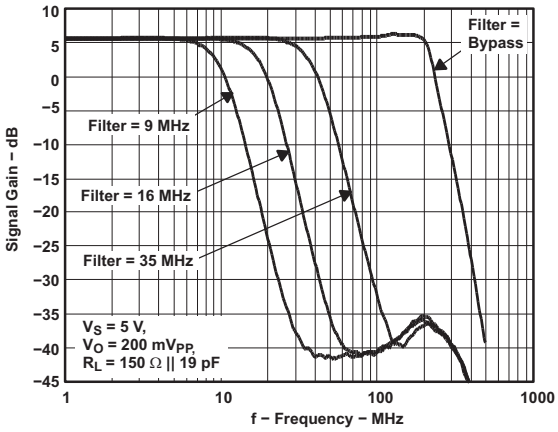

Figure 49.

SMALL-SIGNAL FREQUENCY RESPONSE WITH 23 pF CAPACITIVE LOAD

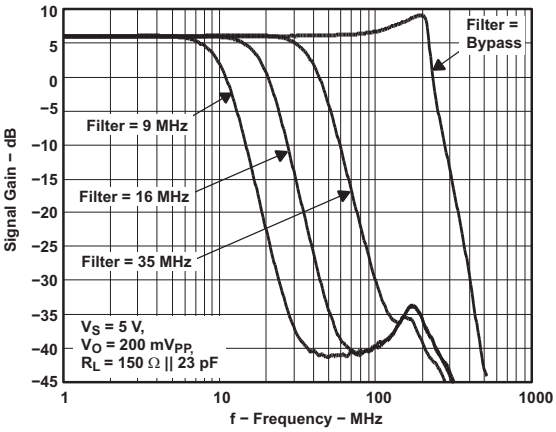

Figure 50.

SMALL-SIGNAL FREQUENCY RESPONSE WITH 35 pF CAPACITIVE LOAD

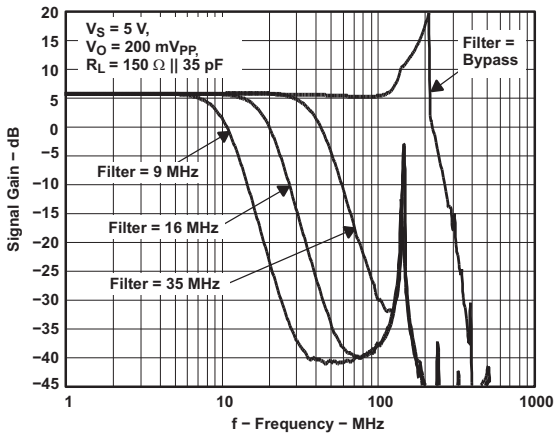

Figure 51.

SMALL-SIGNAL PULSE RESPONSE

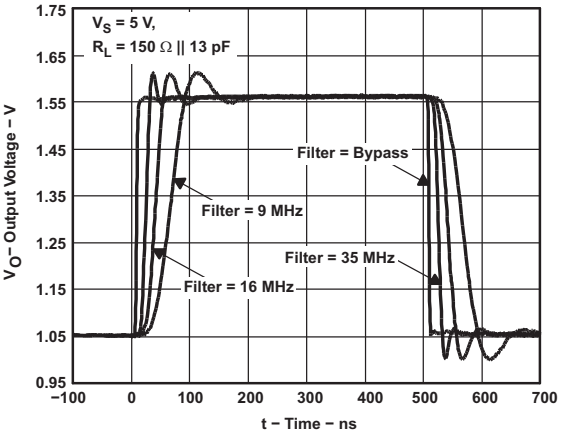

Figure 52.

LARGE-SIGNAL PULSE RESPONSE

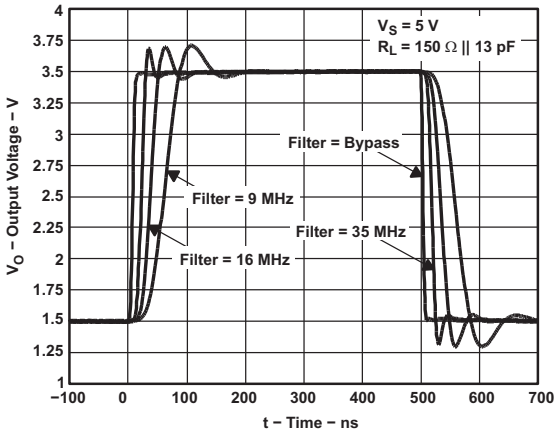

Figure 53.

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TYPICAL CHARACTERISTICS: V_{S+} = 5 V (continued)

R_L = 150 Ω to GND and dc-coupled input and output, unless otherwise noted.

SLEW RATE vs OUTPUT VOLTAGE

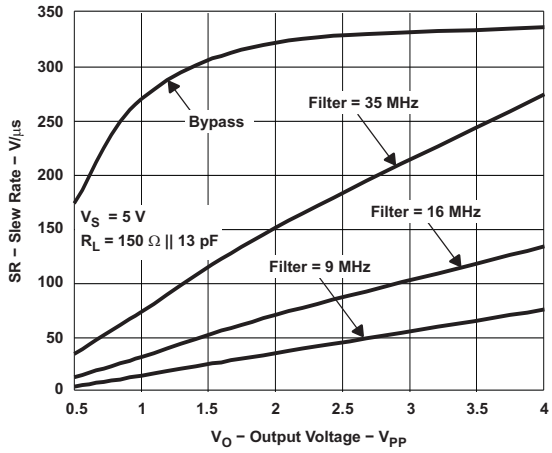

Figure 54.

OUTPUT IMPEDANCE vs FREQUENCY

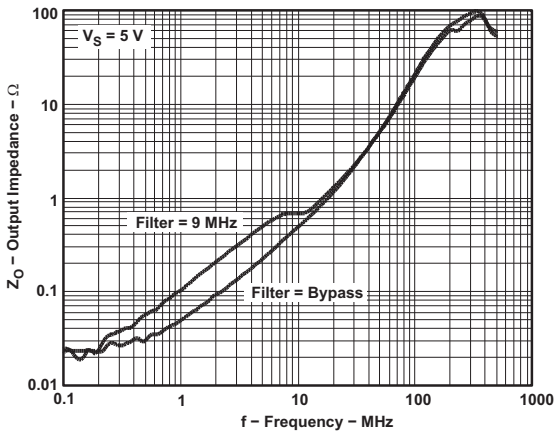

Figure 55.

MUX FEEDTHROUGH vs FREQUENCY

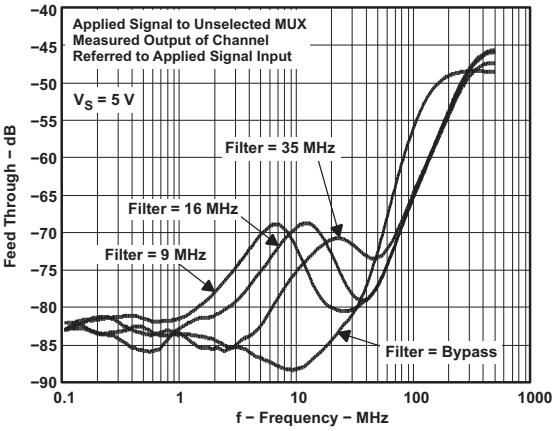

Figure 56.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

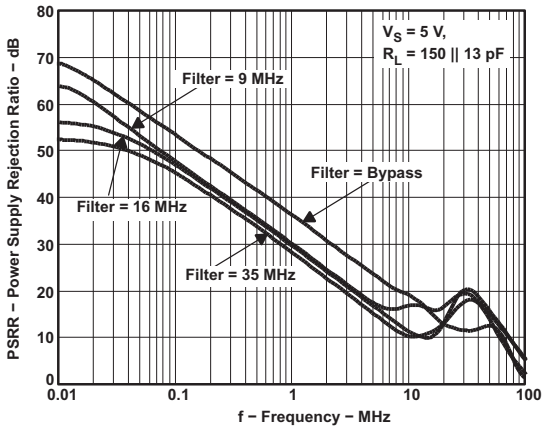

Figure 57.

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APPLICATION INFORMATION

The THS7303 is targeted for video output buffer applications. Although it can be used for numerous other applications, the needs and requirements of the video signal are the most important design parameters of the THS7303. Built on the complementary silicon germanium (SiGe) BiCom-3 process, the THS7303 incorporates many features not typically found in integrated video parts while consuming low power. Each channel configuration is completely independent of the other channels. This allows for configurations for each channel to be dictated by the end user and not the device. This results in a highly flexible system for most video systems. The THS7303 contains the following features:

- I^2C Interface for easy interfacing to the system.
- Single-supply 2.7-V to 5-V operation with low total quiescent current of 16.6 mA with 3.3-V supply and 18.9 mA with 5-V supply.
- 2:1 input MUX.
- Input configuration accepting dc, dc + 135 mV shift, ac bias, or ac sync-tip-clamp selection.
- Selectable fifth-order, low-pass filter for DAC reconstruction or ADC image rejection :
  - 9-MHz for SDTV NTSC and 480i, PAL/SECAM and 576i, S-Video, and G'B'R' (R'G'B') signals.
  - 16-MHz for EDTV 480p and 576p $Y'P'_BP'_R$ signals, G'B'R', and VGA signals.
  - 35-MHz for HDTV 720p and 1080i $Y'P'_BP'_R$ signals, G'B'R', and SVGA/XGA signals.
  - Bypass mode for passing HDTV 1080p $Y'P'_BP'_R$, G'B'R', and SXGA/UXGA signals.
- Internal fixed gain of 2 V/V (6 dB) buffer that can drive two video lines per channel with dc coupling, traditional ac coupling, or SAG corrected ac coupling.
- Disable mode that reduces quiescent current to as low as 0.1-µA or a mute function that keeps the THS7303 powered on, but does not allow a signal to pass through.
- Signal flow-through configuration using a 20-pin TSSOP package that complies with the latest lead-free (RoHS compatible) and green manufacturing requirements.

OPERATING VOLTAGE

The THS7303 is designed to operate from 2.7 V to 5 V over a –40°C to +85°C temperature range. The impact on performance over the entire temperature range is negligible due to the implementation of thin film resistors and low-temperature coefficient capacitors.

The power supply pins should have a 0.1-µF to 0.01-µF capacitor placed as close as possible to these pins. Failure to do so may result in the THS7303 outputs ringing or oscillating. Additionally, a large capacitor, such as 22 µF to 100 µF, should be placed on the power-supply line to minimize issues with 50/60 Hz line frequencies.

INPUT VOLTAGE

The THS7303 input range allows for an input signal range from ground to (V_{S+} – 1.4 V). However, as a result of the internal fixed gain of 2 V/V (6 dB), the output is the limiting factor for the allowable linear input range. For example, with a 5-V supply, the linear input range is from GND to 3.6 V. Because of the gain, the linear output range limits the allowable linear input range to be from GND up to 2.5 V.

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INPUT OVERVOLTAGE PROTECTION

The THS7303 is built using a high-speed complementary bipolar and CMOS process. The internal junction breakdown voltages are low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All input and output device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 58.

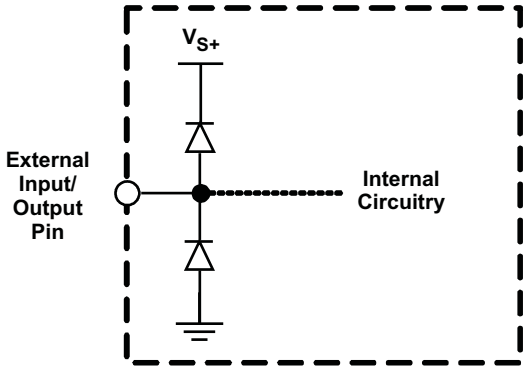

Figure 58. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above and below the supplies. The protection diodes can typically support 30-mA of continuous current when overdriven.

TYPICAL CONFIGURATION and VIDEO TERMINOLOGY

A typical application circuit using the THS7303 as a video buffer is shown in Figure 59. It shows a DAC (or encoder such as the THS8200) driving the three input channels of the THS7303. Although the high-definition video (HD) or enhanced-definition (ED) $Y'P'_BP'_R$ (sometimes Y'U'V' is used or it is incorrectly labeled $Y'C'_BC'_R$) channels are shown, these channels can easily be S-Video Y'C' channels and the composite video baseband signal (CVBS) of a standard definition video (SD) system. These signals can also be G'B'R' (R'G'B') signals or other variations. Note that for computer signals the sync should be embedded within the signal for a system with only 3-outputs. This is sometimes labeled as R'G'sB' (sync on green) or R'sG'sB's (sync on all signals).

The second set of inputs (B-Channels) shown are being driven from an external input typically used as a pass-through function. These are either HD, ED, or SD video signals. The flexibility of the THS7303 allows for almost any input signal to be driven into the THS7303 regardless of the other set of inputs. Control of the I^2C configures each channel of the THS7303 independently of the other channels. For example, the THS7303 can be configured to have Channel 1 Input connected to input A with 35-MHz LPF while Channels 2 and 3 are connected to input B with 16-MHz LPF. See the various sections explaining the I^2C interface later in this data sheet for more information.

Note that the Y' term is used for the luma channels throughout this document rather than the more common luminance (Y) term. The reason is to account for the definition of luminance as stipulated by the CIE - International Commission on Illumination. Video departs from true luminance since a nonlinear term, gamma, is added to the true RGB signals to form R'G'B' signals. These R'G'B' signals are then used to mathematically create luma (Y'). Thus luminance (Y) is not maintained requiring a difference in terminology.

This rationale is also used for the chroma (C') term. Chroma is derived from the non-linear R'G'B' terms and thus it is nonlinear. Chominance (C) is derived from linear RGB giving the difference between chroma (C') and chrominance (C). The color difference signals (P'_B / P'_R / U' / V') are also referenced this way to denote the nonlinear (gamma corrected) signals.

R'G'B' (commonly mislabeled RGB) is also called G'B'R' (again commonly mislabeled as GBR) in professional video systems. The SMPTE component standard stipulates that the luma information is placed on the first channel, the blue color difference is placed on the second channel, and the red color difference signal is placed on the third channel. This is consistent with the $Y'P'_BP'_R$ nomenclature. Because the luma channel (Y') carries the sync information and the green channel (G') also carries the sync information, it makes logical sense that G' be

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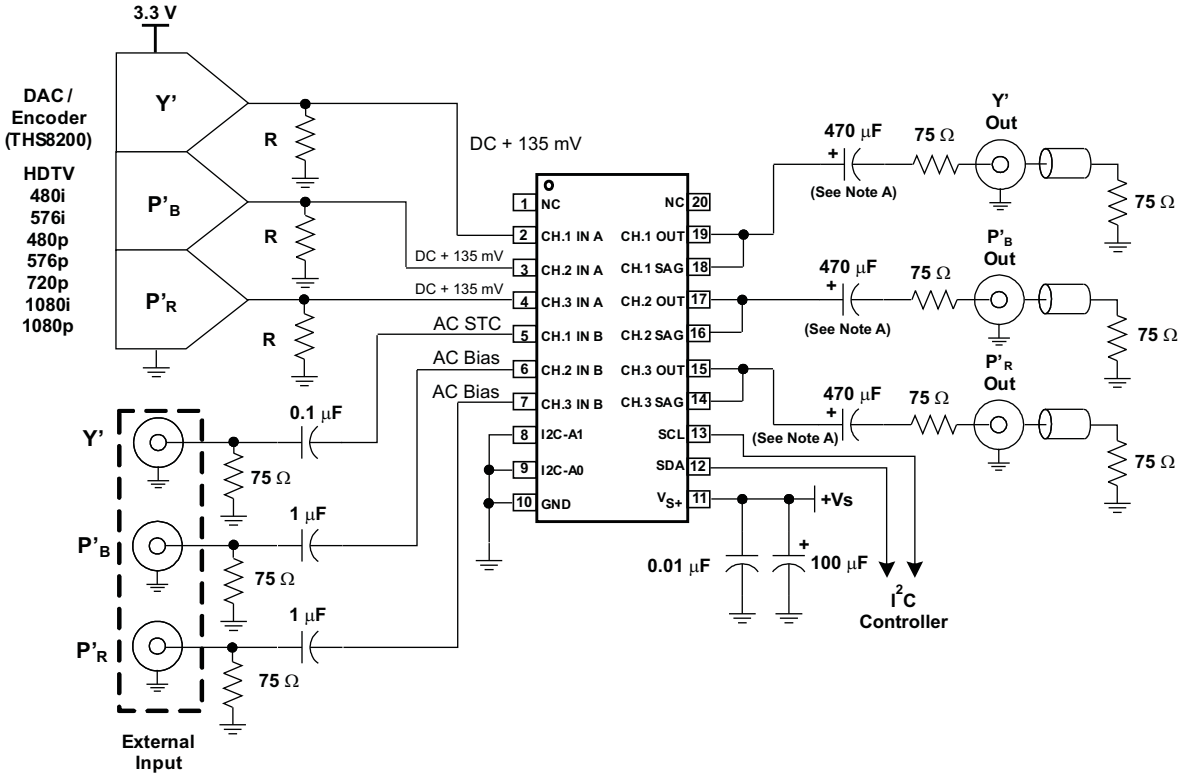
placed first in the system. Since the blue color difference channel (P'_B) is next and the red color difference channel (P'_R) is last, then it also makes logical sense to place the B' signal on the second channel and the R' signal on the third channel respectfully. Thus hardware compatibility is better achieved when using G'B'R' rather than R'G'B'. Note that for many G'B'R' systems sync is embeded on all three channels, but may not always be the case in all systems.



A. Due to the high frequency content of the video signal, it is recommended, but not required, to add a 0.01-µF capacitor in parallel with these large capacitors.

Figure 59. Typical Y'$P'_BP'_R$ Inputs From DC-Coupled Encoder/DAC and AC-Coupled External Inputs With AC-Coupled Line Driving

INPUT MODES OF OPERATION: DC

The inputs to the THS7303 allows for both ac-coupled and dc-coupled inputs. Many DACs or video encoders can be dc-connected to the THS7303. However, one of the drawbacks to dc coupling is when 0 V is applied to the input of the THS7303. Although the input of the THS7303 allows for a 0-V input signal, the output swing of the THS7303 cannot yield a 0-V signal. This applies to any traditional single-supply amplifier because of the limitations of the output transistors. Both CMOS and bipolar transistors cannot go to 0 V while sinking a significant amount of current. This trait of a transistor is also the same reason why the highest output voltage is always less than the power-supply voltage when sourcing a significant amount of current.

The internal gain is fixed at 6 dB (2 V/V) regardless of the configuration of the THS7303, and dictates what the allowable linear input voltage range is without clipping concerns. For example, if the power supply is set to 3 V, the maximum output is about 2.9 V. Thus, to avoid clipping, the allowable input is 2.9 V / 2 = 1.45 V. This is true for up to the maximum recommended 5-V power supply that allows about a 4.9 V / 2 = 2.45 V input range while avoiding clipping on the output.

The input impedance of the THS7303 in this mode of operation is > 1 MΩ. This is a result of the input buffer being configured as a unity gain amplifier, as shown in Figure 60.

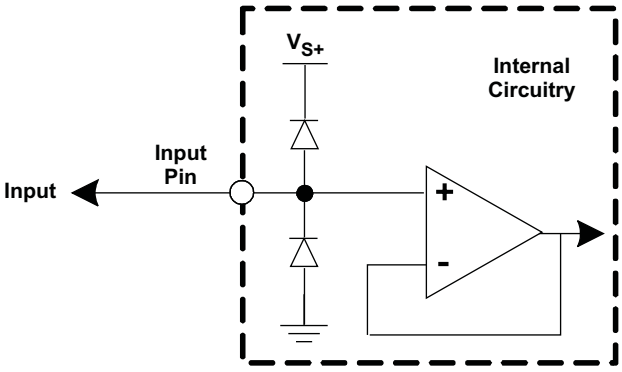


Figure 60. Equivalent DC Input Mode Circuit

The input stage of the THS7303 is designed with PNP bipolar transistors. There is a finite amount of bias current flowing *out* of the THS7303 input pin. This bias current (typically about 0.6 µA), must have a path to flow or else the input stage voltage increases. For example, if there is a 1-MΩ resistance to ground on the input node, the resulting voltage appearing at the input node is 0.6 µA x 1 MΩ = 0.6 V. Therefore, it should be noted that if a channel is powered on and has no input termination, the input bias current causes the input stage to float high until saturation of the input stage exists, approximately 1.4 V from the power supply. Typically, this is not a concern because most terminations result in an equivalent source impedance of 37.5 Ω to 300 Ω.

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INPUT MODES OF OPERATION: DC + 135-mV SHIFT

Clipping occurs with a 0-V applied input signal when the input mode is set to dc. The clipping can reduce the sync amplitudes (both horizontal and vertical sync amplitudes) on the video signal. A problem occurs if the receiver of this video signal uses an AGC loop to account for losses in the transmission line. Some video AGC circuits derive gain from the horizontal sync amplitude. If clipping occurs on the sync amplitude, then the AGC circuit can increase the gain too much, resulting in too much luma and/or chroma amplitude gain correction. This may result in a picture with an overly bright display with too much color saturation.

Other AGC circuits use the chroma burst amplitude for amplitude control, and a reduction in the sync signals does not alter the proper gain setting. It is good engineering design practice to ensure saturation/clipping does not take place. Transistors always take a finite amount of time to come out of saturation. This saturation could possibly result in timing delays or other aberrations on the signals.

To eliminate saturation/clipping problems, the THS7303 has a dc + 135 mV shift input mode. This mode takes the input voltage and adds an internal +135 mV shift to the signal. Since the THS7303 also has a gain of 6 dB (2 V/V), the resulting output with a 0-V applied input signal is about 270 mV. The THS7303 rail-to-rail output stage can create this level while connected to a typical video load. This ensures that no saturation/clipping of the sync signals occurs. This is a constant shift regardless of the input signal. For example, if a 1-V input is applied, the output is at 2.27 V.

As with the dc-input mode, the input impedance of the THS7303 is > 1 MΩ. Additionally, the same input bias current of about 0.6 µA appears at the input. Following the same precautions as stipulated with the dc-input mode of operation minimizes any potential issues. Figure 61 shows the equivalent input circuit while in the dc + 135 mV shift mode of operation. Note that the internal voltage shift does not appear at the input pin, only the output pin.

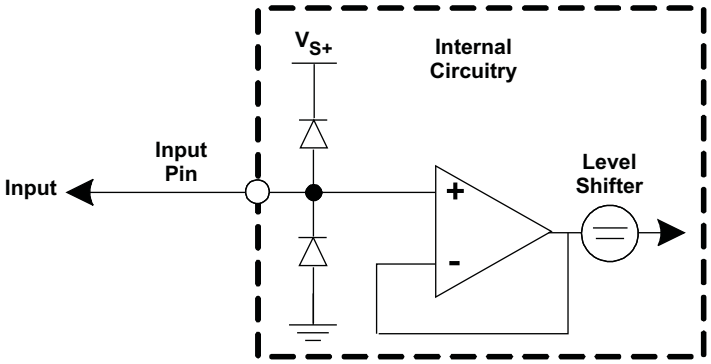
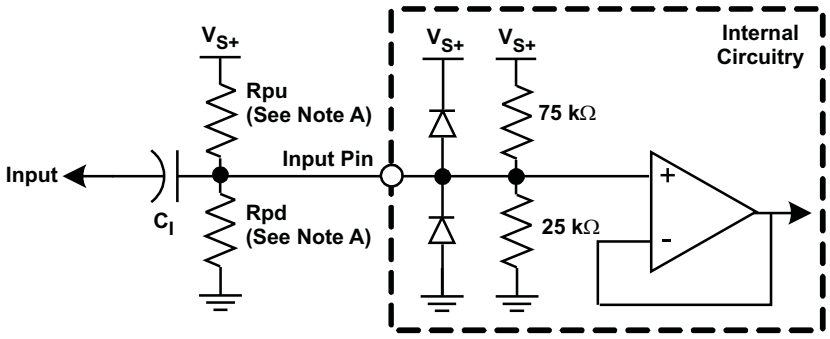


Figure 61. Equivalent DC + 135 mV Input Mode Circuit

INPUT MODES OF OPERATION: AC BIAS

Other applications require an ac-coupled input. The ac-coupling ensures that a source dc-input bias level does not alter, or clip, the resulting output video signal. The first ac-coupling mode is the AC Bias mode, where a simple internal dc bias voltage is applied to the input signal on the THS7303-side of the external coupling capacitor.

The applied dc bias voltage is set internally by a simple resistor divider circuit, as shown in Figure 62. The dc bias voltage is set to V_{S+} / 4. With a 3.3-V power supply, the input bias voltage is nominally 0.825 V; with 5-V supply, the input bias voltage is nominally 1.25 V. The input impedance with this mode is approximately 19-kΩ. With a 1-µF input capacitor, it sets a high-pass corner frequency of about 9 Hz. If a lower frequency is desired, increasing the capacitor decreases the corner frequency proportionally. For example, using a 4.7-µF capacitor results in a 1.8-Hz high-pass corner frequency, and results in lower droop (tilt). Using any capacitor value is acceptable for this mode of operation.



A. Use external pull-up and/or pull-down resistors if changing the ac-bias input voltage is desired.

Figure 62. Equivalent AC Bias Input Mode Circuit

It is sometimes desirable to adjust the bias voltage to another level other than the one dictated by the internal resistors. There are two ways this adjustment is accomplished:

1. The first method is to add an external resistor between the input pin and either the V_{S+} or GND. This creates a new bias voltage equal to V_{S+}× [25 k / {25 k + (75 k || R_{PU})}] for raising the bias voltage, or V_{S+} × [(25 k || R_{PD}) / {(25 k || R_{PD}) + 75 k}] for reducing the bias voltage.
2. The second method to set the ac bias voltage is to use the R_{PU} and R_{PD} external resistors, but place the THS7303 in dc input bias mode. Because the dc mode is very high impedance, the resulting bias voltage is equal to approximately V_{S+} × (R_{PD} / {R_{PD} + R_{PU}}). Due to the input bias current, there will be a difference between the true dc bias voltage and the theoretical bias voltage.

This mode of operation is recommended for use with chroma (C'), P'_B, P'_R, U', V', and other non-sync signals.

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INPUT MODES OF OPERATION: AC SYNC-TIP-CLAMP

The last input mode of operation is the ac with sync-tip-clamp (STC), which also requires a capacitor in series with the input. Note that while the term sync-tip-clamp is used throughout this document, the THS7303 is better termed as a dc restoration circuit based on the way this function is performed. This circuit is an active clamp circuit and not a passive diode clamp function. This function should be used when ac coupling is desired with signals that have sync signals embedded such as CVBS, Y', and G' signals.

The input to the THS7303 has an internal control loop which sets the lowest input applied voltage to clamp at approximately 135 mV. Like the dc + 135 mV input shift, the resulting output voltage low level is about 270 mV. If the input signal tries to go below the 135-mV level, the internal control loop of the THS7303 sources up to 2 mA of current to increase the input voltage level on the THS7303 input side of the coupling capacitor. As soon as the voltage goes above the 135-mV level, the loop stops sourcing current.

One of the concerns about the sync-tip-clamp level is how the clamp reacts to a sync edge that has overshoot that is common in VCR signals or reflections found in poor PCB layouts. Ideally the STC should not react to the overshoot voltage of the input signal. Otherwise, this could result in clipping on the rest of the video signal because there may be too much increase in the bias voltage.

To help minimize this input signal overshoot problem, the patent-pending internal STC control loop in the THS7303 has an I^2C selectable low-pass filter as shown in Figure 63. This filter can be selected to be about 500 kHz, 2.5 MHz, or 5 MHz. The 500-kHz filter is useful when the THS7303 fifth-order low-pass filter is selected for 9-MHz operation. The effect of this filter is to slow down the response of the control loop so as not to clamp on the input overshoot voltage, but rather the flat portion of the sync signal when the ringing should be settled out. The 2.5-MHz filter is best suited for use in conjunction with the 16-MHz signal LPF to account for the faster sync times associated with the higher rate video signals. For HDTV signals, the 5-MHz STC filter should be selected to allow for the faster sync rates to properly set the clamp level. Any STC filter can be selected regardless of the signal or system filter.

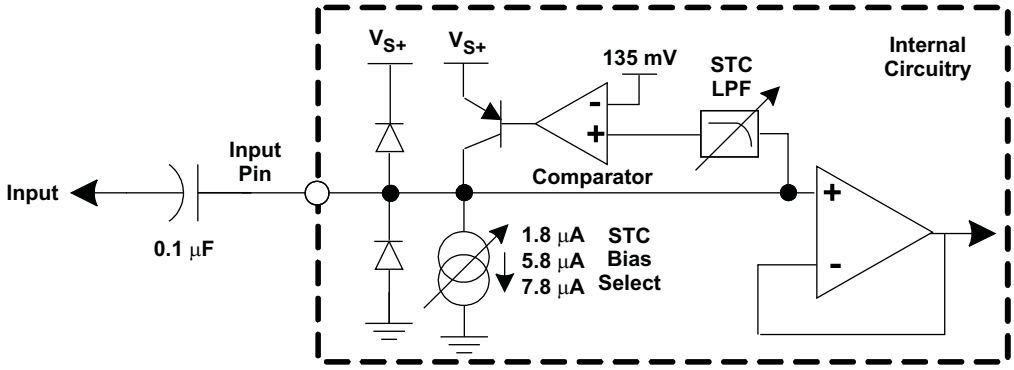

Figure 63. Equivalent AC Sync-Tip-Clamp Input Mode Circuit

As a result of this selectable delay, the sync has an apparent voltage shift occurring between 15 ns and 2 μs after the sync falling edge, depending on the STC LPF. The amount of shift depends on the amount of droop in the signal as dictated by the input capacitor and the STC input bias current selection. Because the sync is primarily for timing purposes with syncing occurring on the edge of the sync signal, this shift is transparent in most systems. Note that if the source signal is known to be good, selecting the 5-MHz STC LPF is recommended for all sources

While this feature may not fully eliminate overshoot issues on the input signal in case of really bad overshoot and/or ringing, the STC system should help minimize improper clamping levels. As an additional method to help minimize this issue, an external capacitor (example: 10 pF to 47 pF) to ground in parallel with the external termination resistors can help filter overshoot problems.

It should be noted that this STC system is dynamic and does not rely upon timing in any way. It only depends on the voltage appearing at the input pin at any given point in time. The STC filtering helps minimize level shift problems associated with switching noises or short spikes on the signal line. This helps ensure a robust STC system.

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When the ac sync-tip-clamp (STC) operation is used, there must also be some finite amount of discharge bias current. As previously described, if the input signal goes below the 135-mV clamp level, the internal loop of the THS7303 sources current to increase the voltage appearing at the input pin. As the difference between the signal level and the 135-mV reference level increases, the amount of source current increases proportionally, supplying up to 2-mA of current. Thus, the time to re-establish the proper STC voltage can be very fast. If the difference is small, then the source current is also small to account for minor voltage droop.

What happens if the input signal goes above the 135-mV input level? The problem is the video signal is always above this level and must not be altered in any way. However, if the sync level of the input signal is above the 135-mV level, then the internal discharge (sink) current reduces the ac-coupled bias signal to the proper 135-mV level.

This discharge current must not be large enough to alter the video signal appreciably or picture quality issues may arise. This is often seen by looking at the tilt (droop) of a constant luma signal being applied, and looking at the resulting output level. The associated change in luma level from the beginning of the video line to the end of the video line is the amount of line tilt (droop). The amount of tilt can be seen by the general formula:

$$I = C\ dV/dt$$

where I is the discharge current and C is the external coupling capacitor which is typically 0.1 µF. If the current (I) and the capacitor (C) are constant, then the tilt is governed by:

$$I/C = dV/dt$$

If the discharge current is small, then the amount of tilt is low, which is good. However, the amount of time for the system to capture the sync signal may be too long. This is also termed *hum* rejection. Hum arises from the ac line voltage frequency of 50 Hz or 60 Hz. The value of the discharge current and the ac-coupling capacitor combine to dictate the hum rejection and the amount of line tilt.

Because many users have different thoughts about the proper amount of hum rejection and line tilt, the THS7303 has incorporated a variable sink bias current selectable through the I^2C interface. The Low Bias mode selects approximately 1.8-µA of dc sink bias current for low line tilt. If more hum rejection is desired, then selecting the Mid Bias mode increases the dc sink bias current to approximately 5.8 µA. For severe environments, the High Bias mode has about 7.8 µA of dc sink bias current. The drawback to these higher bias modes is an increase in line tilt, but with an increase in hum rejection. The other method to change the hum rejection and line tilt is to change the input capacitor used. An increase in the capacitor from 0.1 µF to 0.22 µF decreases the hum rejection and line tilt by a factor of 2.2. A decrease of this input capacitor accomplishes the opposite effect. Note that the amplifier input bias current of nominally 0.6 µA has already been taken into account when stipulating the 1.8-µA, 5.8-µA, and 7.8-µA current sink values.

To ensure proper stability of the ac STC control loop, the source impedance must be less than 600-Ω and the input capacitor must be greater than 0.01 µF. Otherwise, there is a possibility of the control loop ringing. The ringing appears on the output of the THS7303. Similar to the dc modes of operation, many DACs and encoders use a resistor to establish the output voltage. These resistors are typically less than 300 Ω. Thus, stability of the ac STC loop is ensured. If the source impedance looking from the THS7303 input perspective is high or open, then adding a 300-Ω resistor to GND ensures proper operation of the THS7303.

If a MUX channel is not required in the system, it is recommended to place a 75-Ω resistor to GND. This is not required, but it helps minimize any potential issues.

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OUTPUT MODES OF OPERATION: DC COUPLED

The THS7303 incorporates a rail-to-rail output stage that can be used to drive the line directly without the need for large ac-coupling capacitors. This is accomplished by connecting the output pin of each channel directly to the SAG output pin of the corresponding channel as shown in Figure 64. This offers the best line tilt and field tilt (or droop) performance since there is no ac coupling occurring. Keep in mind that if the input is ac coupled, then the resulting tilt due to the input ac coupling is still seen on the output regardless of the output coupling. The 70-mA output current drive capability of the THS7303 is designed to drive two video lines simultaneously (essentially a 75-Ω load), while keeping the output dynamic range as wide as possible.

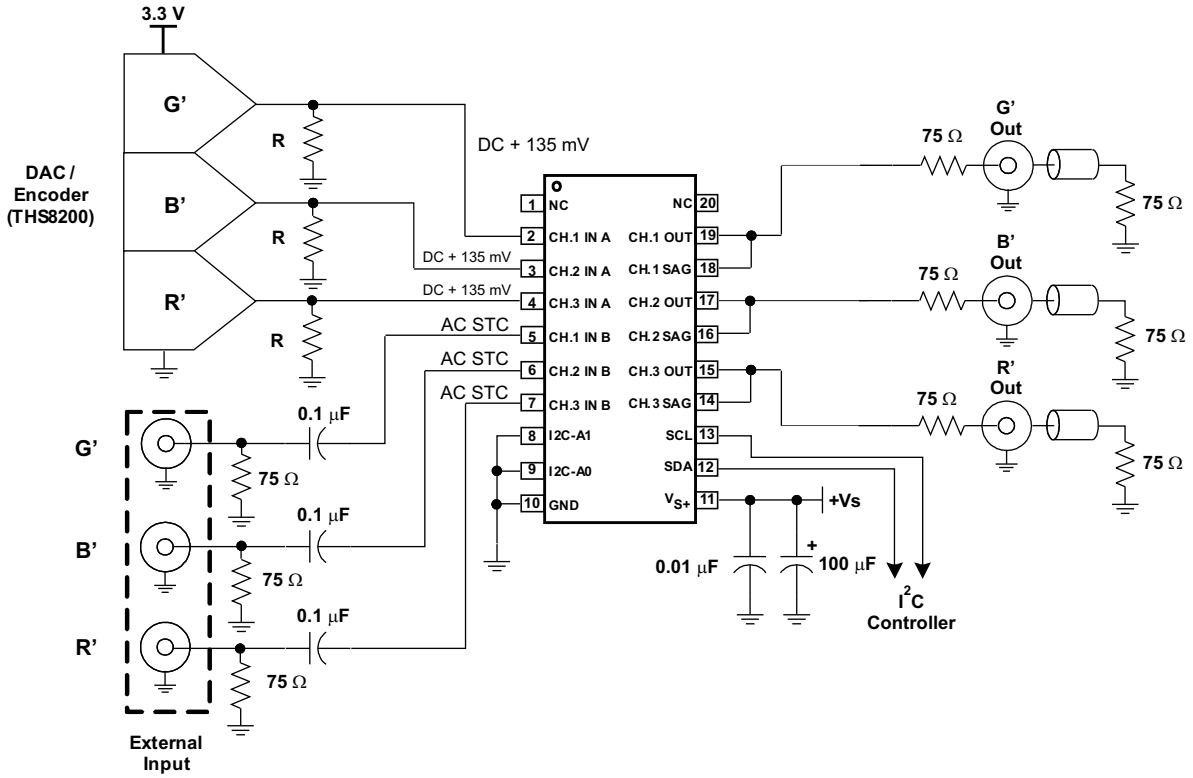

Figure 64. Typical G'B'R' (R'G'B') System With DC-Coupled Line Driving

One concern of dc coupling is if the line is terminated to ground. When the AC-Bias Input mode is selected, the output of the THS7303 is at mid-rail. With two lines terminated to ground, this creates a dc current path to exist that results in a slightly decreased high output voltage swing resulting in an increase in power dissipation of the THS7303. While the THS7303 is designed to operate with a junction temperature of up to +125°C, care must be taken to ensure that the junction temperature does not exceed this level or else long-term reliability could suffer. Although this configuration adds less than 10 mW of power dissipation per channel, the overall low power dissipation of the THS7303 design minimizes potential thermal issues even when using the TSSOP package at high ambient temperatures.

Note that the THS7303 can drive the line with dc coupling regardless of the input mode of operation. The only requirement is to make sure the video line has proper termination in series with the output pin (typically 75 Ω). This helps isolate capacitive loading effects from the THS7303 output. Failure to isolate capacitive loads may result in instabilities with the output buffer, potentially causing ringing or oscillations to appear. The stray capacitance appearing directly at the THS7303 output pins should be kept below 25 pF for best performance. When driving two video lines, each line should have its own 75-Ω source termination resistors to isolate the lines from each other.

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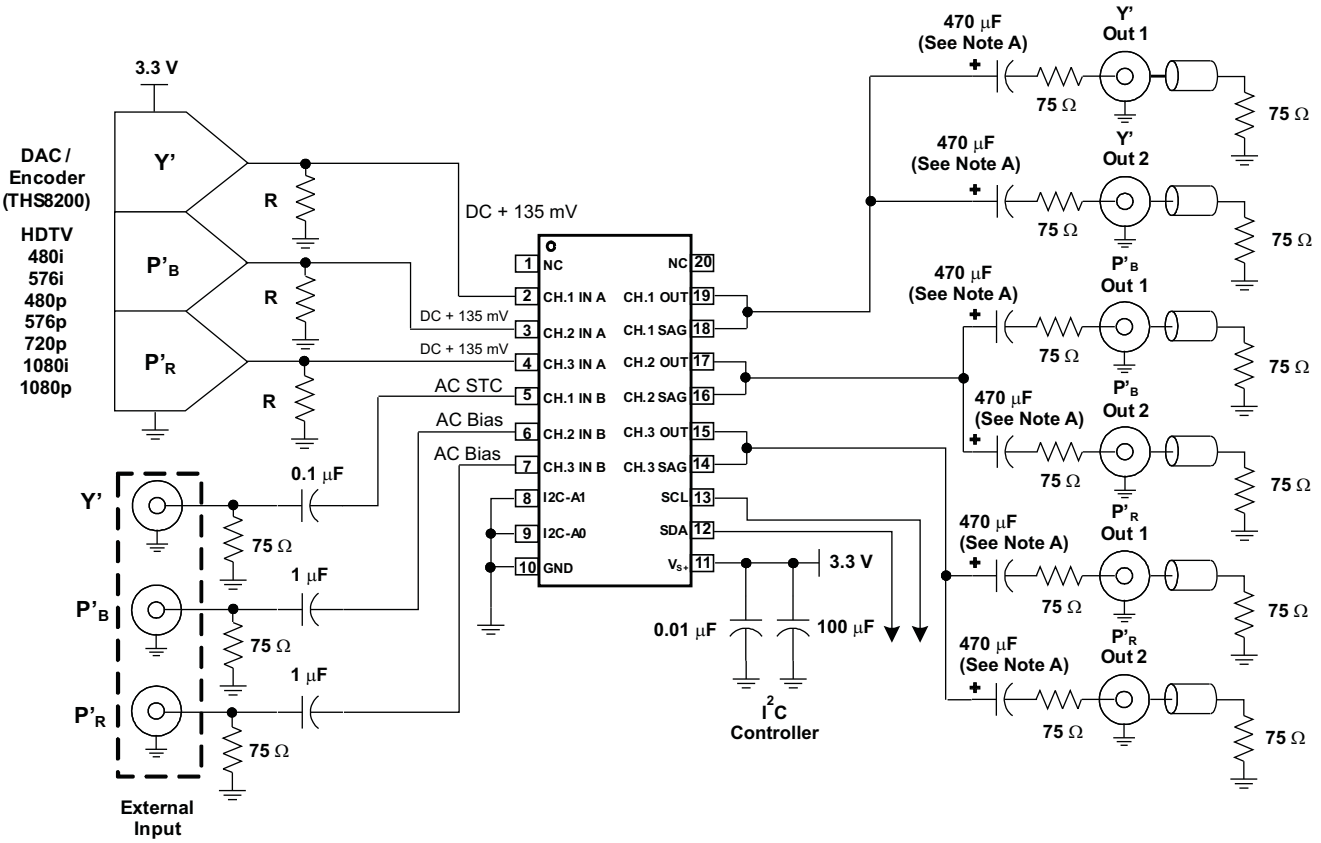
OUTPUT MODES OF OPERATION: AC-COUPLED

The most common method of coupling the video signal to the line is by using a large capacitor. This capacitor is typically between 220 µF and 1000 µF, although 470 µF is most common. This value of this capacitor must be this large to minimize the line tilt (droop) and/or field tilt associated with ac coupling as described previously in this document. Just like the dc output configuration, connection of the output pin of each channel directly to the SAG output pin of the corresponding channel should be as close as possible to the output pins of the THS7303.

The most common reason ac coupling is used is to ensure full interoperability with the receiving video system. This ensures that regardless of the reference dc voltage used on the transmit side of the video signal, the receive side will re-establish the dc reference voltage to its own requirements without any interaction from the transmit side dc bias voltage.

As with the dc output mode of operation, each line should have a 75-Ω source termination resistor in series with the ac-coupling capacitor. If two lines are to be driven, it is best to have each line use its own capacitor and resistor rather than sharing these components, as shown in Figure 65.This helps ensure line-to-line dc isolation and other potential problems. Using a single 1000-µF capacitor for two lines can be done, but there is a chance for interference between the two receivers.



A. Due to the high frequency content of the video signal, it is recommended, but not required, to add a 0.01-µF capacitor in parallel with these large capacitors.

Figure 65. Typical Y'P'$_B$P'$_R$ System Driving 2 AC-Coupled Video Lines

Because of the edge rates and frequencies of operation, it is recommended (but not required) to place a 0.1-µF to 0.01-µF capacitor in parallel with the large 220-µF to 1000-µF capacitors. These large value capacitors are most commonly aluminum electrolytic. It is well known that these capacitors have significantly large equivalent series resistance (ESR), and their impedance at high frequencies is large as a result of the associated inductances involved with their construction. The small 0.1-µF to 0.01-µF capacitors help pass these high-frequency (> 1 MHz) signals with lower impedance than the large capacitors. This is especially true when HD and computer R'G'B' signals are being used. Their associated edge rates and frequency content can reach beyond 30-MHz for HD signals and can be over 100-MHz for R'G'B' signals—frequencies that typical aluminum electrolytic capacitors typically cannot pass effectively.

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Although it is common to use the same capacitor values for all the video lines, the frequency bandwidth of the chroma signal in a S-Video system are not required to go as low or as high as the frequency of the luma channel. Thus, the capacitor values of the chroma line(s) can be smaller, such as 0.1 µF.

OUTPUT MODES OF OPERATION: AC-COUPLED WITH SAG CORRECTION

Other than the line droop issue, ac coupling has two other potential issues: size and cost. A 330-µF to 1000-µF capacitor is large and can be quite costly in a system. Multiply these items by the number of channels, and the size and cost can be significant. However, it is still desirable to use ac coupling to insure interoperability among video devices.

The SAG nomenclature represents signal amplitude gain correction in this document. SAG correction is a method that is used to ac-couple the video signal while using much smaller value capacitors. SAG correction is accomplished by manipulating the feedback network of the output buffer. The THS7303 was designed to take advantage of this compensation scheme, while minimizing the number of external components required. Figure 66 shows the basic configuration of the output buffer stage along with the SAG configuration driving a single video line.

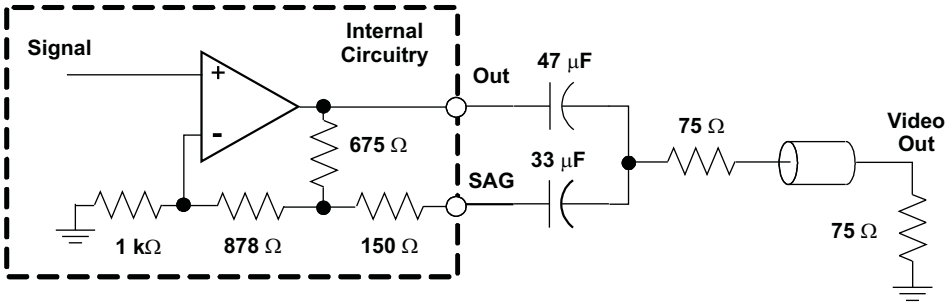

Figure 66. THS7303 Output Buffer Using SAG Corrected AC-Coupling

SAG compensation can be analyzed by looking at low frequency operation and high frequency operation. At low frequencies, the impedance of the capacitors are high and the corresponding gain of the amplifier is:

$$1 + \left(\frac{(675 + 878)}{1k}\right) = 2.55\ V/V\ (+\ 8.1\ dB). \quad (1)$$

At high frequencies, the impedance of the capacitors are low and the resulting gain of the amplifier is:

$$1 + \left(\frac{[(675 \parallel 150) + 878]}{1k}\right) = 1 + \left(\frac{1k}{1k}\right) = 2\ V/V\ (+\ 6.0\ dB) \quad (2)$$

which is needed to counteract the doubly-terminated 75-Ω output divider (–6 dB) circuit, resulting in the video-out signal equaling the input signal amplitude.

When the SAG output pin is connected directly to the amplifier output, as found in the dc-coupled and the ac-coupled configurations, the gain is configured properly at 2 V/V (6 dB). The SAG pin is part of the negative feedback network. Thus, the capacitors and traces should be constructed as close as possible to the THS7303 to minimize parasitic issues. Failure to do so may result in ringing of the video signal.

If these large capacitors must be placed further than 15 mm away from the THS7303, it is recommended that a 0.01-µF capacitor be placed between the output of the channel and the SAG pin. This capacitor should be placed as close as possible to the THS7303 to minimize stray capacitance and inductance issues. Since SAG correction targets the low frequency operation area, there is no drawback of adding this high frequency capacitor to the circuit.

When SAG correction is used, the low-frequency gain is higher than the high-frequency gain (8.1 dB versus 6 dB). This gain counter acts the attenuation of the signal because of the increase in the 47-µF capacitor impedance. This amplifier gain increase is determined by the 33-µF capacitor (and associated internal resistor values) and causes a *Q* enhancement to occur at low frequencies (typically at about 15 Hz). The ratio of these capacitor values determines the frequency and amplitude of this enhancement.

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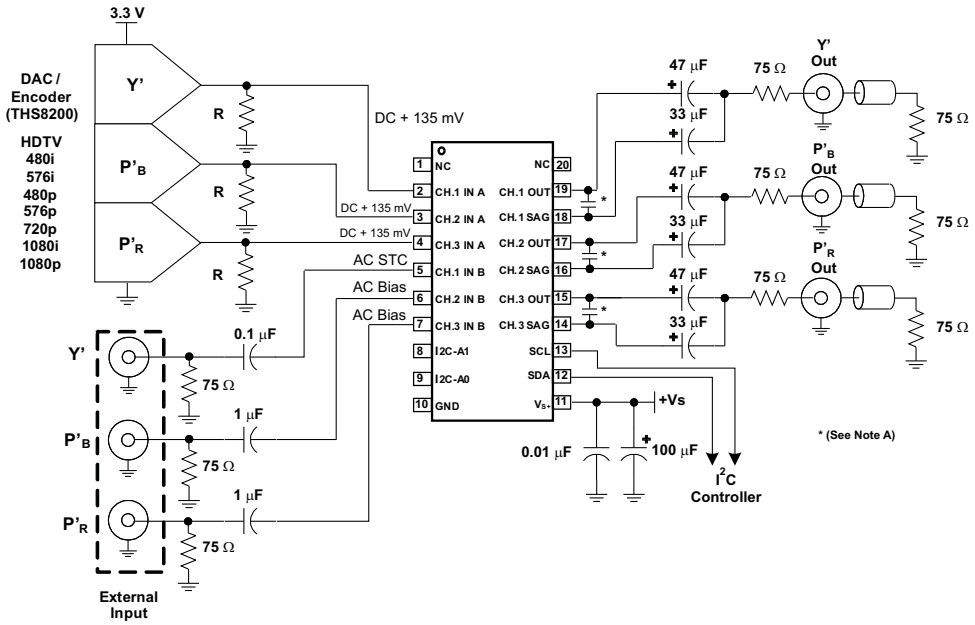
The internal resistor values were chosen to optimize the system while using the 47-µF and 33-µF capacitors, and to approximate the performance of a single 330-µF capacitor. These capacitors can be a different value if desired, but the characteristics of the system are altered accordingly. For example, if 22-µF capacitors are used for both sections, then there are increases in line tilt and field tilt. For some systems, this may be considered acceptable (for example, 720p Y' signals with the associated faster line rates). Using larger values, such as 68 µF and 47 µF respectively, decreases field time distortion even further, and approaches the performance of a single 470-µF capacitor.

It is important to note that the dc gain is about 2.55 V/V. Thus, if the input has a dc bias, the output dc bias is 2.55 times the input. For example, this results in an output bias point of 355 mV for the dc + 135 mV shift. Additionally, if the ac bias input mode is selected, the dc operating point is $V_{S+}/4 \times 2.55$, or 2.1 V with 3.3-V supply and 3.2 V with 5-V supply. This additional offset should not hinder the performance of the THS7303 because there is still plenty of voltage headroom between the dc operating point and the rail-to-rail output capability.

One possible concern about this configuration is that the low-frequency gain enhancement may cause saturation of the signal when low power-supply voltages (such as 3 V) are used. The internal resistors were chosen to minimize the low-frequency gain so that saturation is minimized. Other SAG correction devices have much higher low-frequency gain (10 dB or higher), which when coupled with low power-supply voltages, can easily create clipping on the output of the amplifier, both dynamically and at dc. Other SAG correction devices do not use a resistor in series with the SAG pin. Neglecting this resistor can result in a large *Q* enhancement causing possible saturation issues. These systems typically require much larger capacitor values to minimize this problem, which ultimately minimizes the benefits of SAG correction.

Figure 67 shows a SAG-corrected configuration for the THS7303. If a S-Video chroma channel is being configured, there is no reason for SAG correction because the coupling capacitor is typically small at 0.1 µF. Thus, tying the output pin directly to the SAG output pin is recommended along with a 0.1-µF capacitor.

Note that increasing the gain of the THS7303 can be easilly accomplished by using the SAG pin. Simply placing a resistor, R_{SAG}, between the SAG pin and GND increases the gain by forming a resistor divider on the signal feedback path. The resulting gain becomes $V_{OUT}/V_{IN} = 2.553 + (1268 / (150 + R_{SAG}))$.



A. If the SAG correction capacitors are more than 15 mm from the THS7313, add a 0.01µF capacitor as shown.

Figure 67. Typical Y'P'$_B$P'$_R$ System Driving SAG Corrected AC-Coupled Video Lines

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INCREASING GAIN

The gain of the THS7303 can easily be increased by using the SAG pin. As a result of the resistor configuration, a T-network in the feedback path is formed. This feedback path allows for the SAG function to work properly, but at the same time it allows for higher gains than the default 2 V/V (6 dB). Figure 68 shows how gain is easily increased for each channel. Be sure to keep the R_G resistor as close as possible to the SAG pin to minimize any stability concerns.

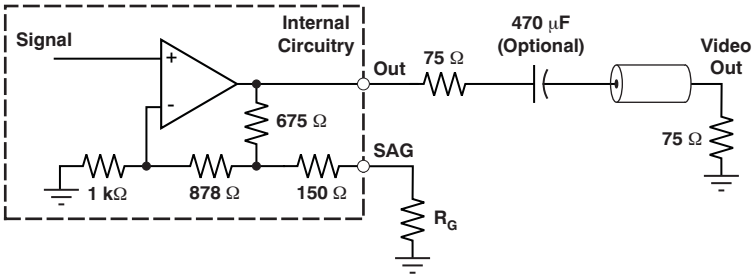

Figure 68. Increasing Output Gain of the THS7303

The formula for the gain becomes:

$$\text{Gain (V/V)} = 2.553 + \left(\frac{1268}{150 + R_G}\right)$$

or

$$R_G\ (\Omega) = \left(\frac{1268}{\text{Gain (V/V)} - 2.553}\right) - 150$$

For example, if the desired gain is 5.6 V/V, then R_G should be 267 Ω. Note that the internal resistors do have tolerances associated with the respective absolute values. Because of the silicon process, resistor-to-resistor matching is very tight when looked at as a ratio to each other. Compared to an external resistor, however, there is a greater variation in the gain of the system.

There are a few drawbacks when implementing this feature. One concern is that the SAG functionality no longer can be used. A second drawback is that the offset voltage increases proportionally with the gain. For example, if DC + Shift mode is used (normally, this mode has approximately 290-mV offset with 2-V/V gain), then with 5.6-V/V gain the output offset voltage becomes 145 mV × 5.6 V/V = 812 mV. As a result of this higher offset and the potential risk of clipping of the signal on the high side, using a higher supply voltage, such as 5 V, is recommended.

One possible option if a 3.3-V supply is desired is to use dc-only input without the level shift. The output offset is nominally 35 mV × Gain (V/V); or, for this example, 35 mV × 5.6 V/V = 196 mV. Even with a 100% color-saturated CVBS signal, there should be no clipping on the high side.

One benefit of using the THS7303 for higher gain versus using the THS7353 device is the gain bandwidth product (GBP) of the output amplifier; this characteristic becomes more important with the THS7353 because the THS7353 is unity gain while the THS7303 is specified with a 2-V/V gain. For example, the THS7303 has a bypass mode bandwidth of 190-MHz with a gain of 2 V/V. If the gain is increased to 4 V/V, then the bandwidth should decrease to approximately 95 MHz. This increase should have minimal impact on any of the filter characteristics. In comparison, the THS7353 has a bypass mode bandwidth of 150 MHz. If the THS7353 is configured for a gain of 4 V/V, the bandwidth drops to approximately 37.5 MHz, and has an impact on the performance of the 35-MHz filter.

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LOW-PASS FILTER AND BYPASS MODES

Each channel of the THS7303 incorporates a fifth-order low-pass filter. These video reconstruction filters minimize DAC images from being passed onto the video receiver. Depending on the receiver design, failure to eliminate these DAC images can cause picture quality problems due to aliasing of the ADC. Another benefit of the filter is smoothing out aberrations in the signal that some DACs produce if their own internal filtering is not adequate. This smoothing helps with picture quality and insures the signal meets video bandwidth requirements.

Each filter has a Butterworth characteristic associated to it. The benefit of the Butterworth response is that the frequency response is flat, with a relatively steep initial attenuation at the corner frequency. The problem with this characteristic is that the group delay rises near the corner frequency. Group delay is defined as the change in phase (radians/second) divided by a change in frequency. An increase in group delay corresponds to a time domain pulse response that has overshoot and some possible ringing associated with the overshoot.

The use of other type of filters, such as elliptic or chebyshev, are not recommended for video applications because of their very large group delay variations near the corner frequency, resulting in significant overshoot and ringing. While these elliptic or chebyshev filters may help meet the video standard specifications with respect to amplitude attenuation, their group delay is well beyond the standard specifications. Couple this with the fact that video can go from a white pixel to a black pixel over and over again, ringing can easily occur. Ringing typically causes a display to have *ghosting* or *fuzziness* appear on the edges of a sharp transition. On the other hand, a Bessel filter has an ideally flat group delay response, but the rate of attenuation is typically too low for acceptable image rejection. Thus, the Butterworth filter is a respectable compromise for both attenuation and group delay.

The THS7303 filter has a slightly lower group delay variation near the corner frequency compared to an ideal Butterworth filter. This results in a time domain pulse response which still has some overshoot, but not as much as a true Butterworth filter. Additionally, the initial rate of attenuation in the frequency response is not as fast as an ideal Butterworth response, but it is an acceptable initial rate of attenuation considering the pulse and group delay characteristic benefits.

The THS7303 filters have a nominal corner (–3 dB) frequency selectable at 9 MHz, 16 MHz, and 35 MHz along with a bypass mode. The 9-MHz filter is ideal for standard definition (SD) NTSC, PAL, and SECAM composite video (CVBS) signals. It is also useful for S-Video signals (Y'C'), 480i / 576i $Y'P'_BP'_R$, G'B'R', and Y'U'V' video signals. The –3-dB corner frequency was designed to be 9 MHz to allow a maximally flat video signal while achieving over 40-dB of attenuation at 27 MHz—a common frequency between the ADC second and third Nyquist zones found in many video receivers. This is important because any signal appearing around this frequency can appear in the baseband as a result of aliasing effects of an analog-to-digital converter found in a receiver.

The 9-MHz filter frequency was chosen to account for process variations in the THS7303. To ensure the required video frequencies are the least affected, the filter corner frequency must be high enough to allow for component variations. Another consideration is the attenuation must be large enough to ensure the anti-aliasing/reconstruction filtering meets the system demands. Thus, the selection of the filter frequencies was not chosen arbitrarily.

The 16-MHz filter was designed to pass 480p and 576p $Y'P'_BP'_R$ and G'B'R' video signals, sometimes referred as enhanced definition (ED). Additionally, this filter can be used to pass computer VGA signals with flat frequency response in the video spectrum. The 16-MHz filter can also be used for SD signals to ensure there is no amplitude aberration, and to have an exceptional low group delay within the SD video frequency range.

The 35-MHz filter is designed to pass high definition (HD) 720p and 1080i $Y'P'_BP'_R$ video signals along with G'B'R' (R'G'B') SVGA and XGA signals. If a 4:2:2 system is used, the $P'_BP'_R$ channels do not require the full bandwidth as required by the Y' channel. However, it is still recommended to use the same filter frequency of the Y' channel to match the group delay and timing of all three signals. Otherwise, extra delay compensation is required to minimize timing variations. This filter is also useful for passing 480p/576p signals with little amplitude or group delay variations within the ED frequency range.

The THS7303 bypass mode has a 190-MHz bandwidth (–3 dB) and a 300 V/µs slew rate to pass G'B'R' (R'G'B') SXGA and UXGA signals with little degradation. This bypass mode is also useful for HDTV 1080p signals that require a 60-MHz video signal bandwidth.

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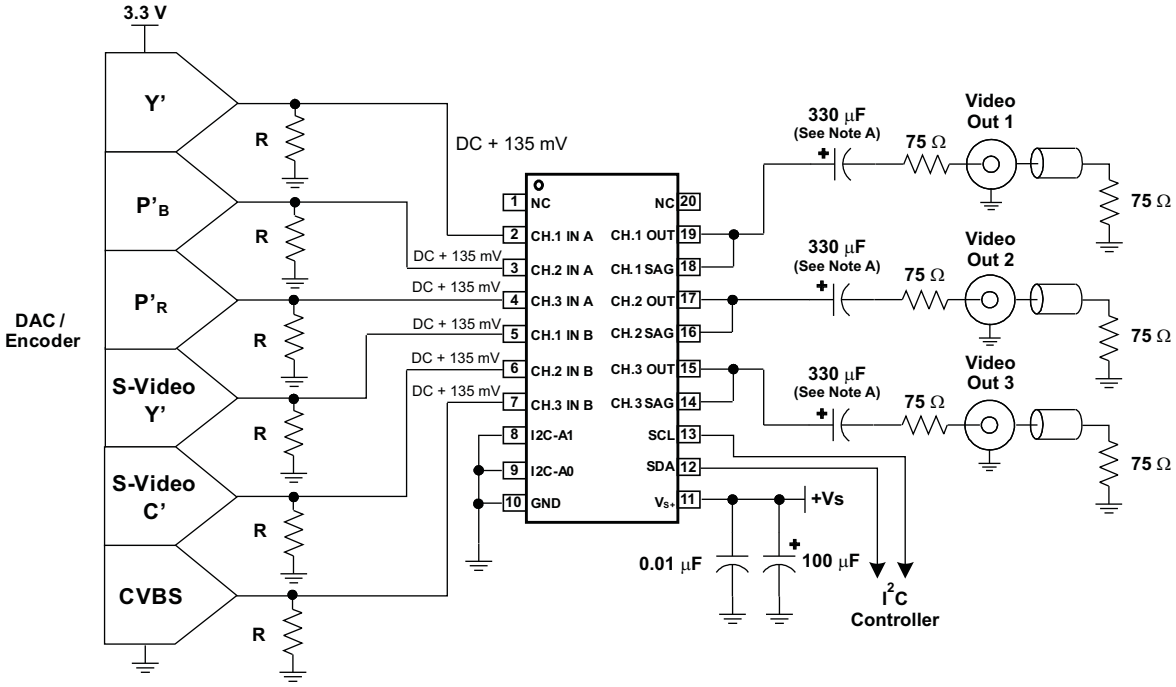
The I^2C interface of the THS7303 allows each channel to be configured totally independent of the other channels. One of the benefits is that a multiple output encoder (or DAC) can be routed through one THS7303 with the proper input configuration and low-pass filter required regardless of the signal. This is useful for a portable system or in a low-cost system where only one set (or two sets in parallel) is desired on the output of the system. An update of the I^2C commands changes the THS7303 channels. An example is shown in Figure 69 where the input MUX allows for one set of HDTV signals to be put into the THS7303, and then through an I^2C update, a SDTV set of signals is sent through the THS7303 with the proper input mode and low-pass filters.



A. Due to the high frequency content of the video signal, it is recommended, but not required, to add a 0.01-µF capacitor in parallel with these large capacitors.

Figure 69. Typical SD/ED/ and HD Video and SDTB Encoder DAC Driving a Single THS7303

Although the circuit of Figure 69 conserves space and cost, the reuse of the output connections may not be the best solution. For a complete 6-channel system, it is better to use the THS7303 and the THS7313 (see SLOS483) together, as shown in Figure 70. The THS7313 is targeted for SDTV signals and is limited to an 8-MHz filter. As discussed in the I^2C section, it is easy to have both parts in one system because the I^2C address of each part can be one of four discrete addresses by the logic appearing on the I^2C-A1 and I^2C-A0 lines.

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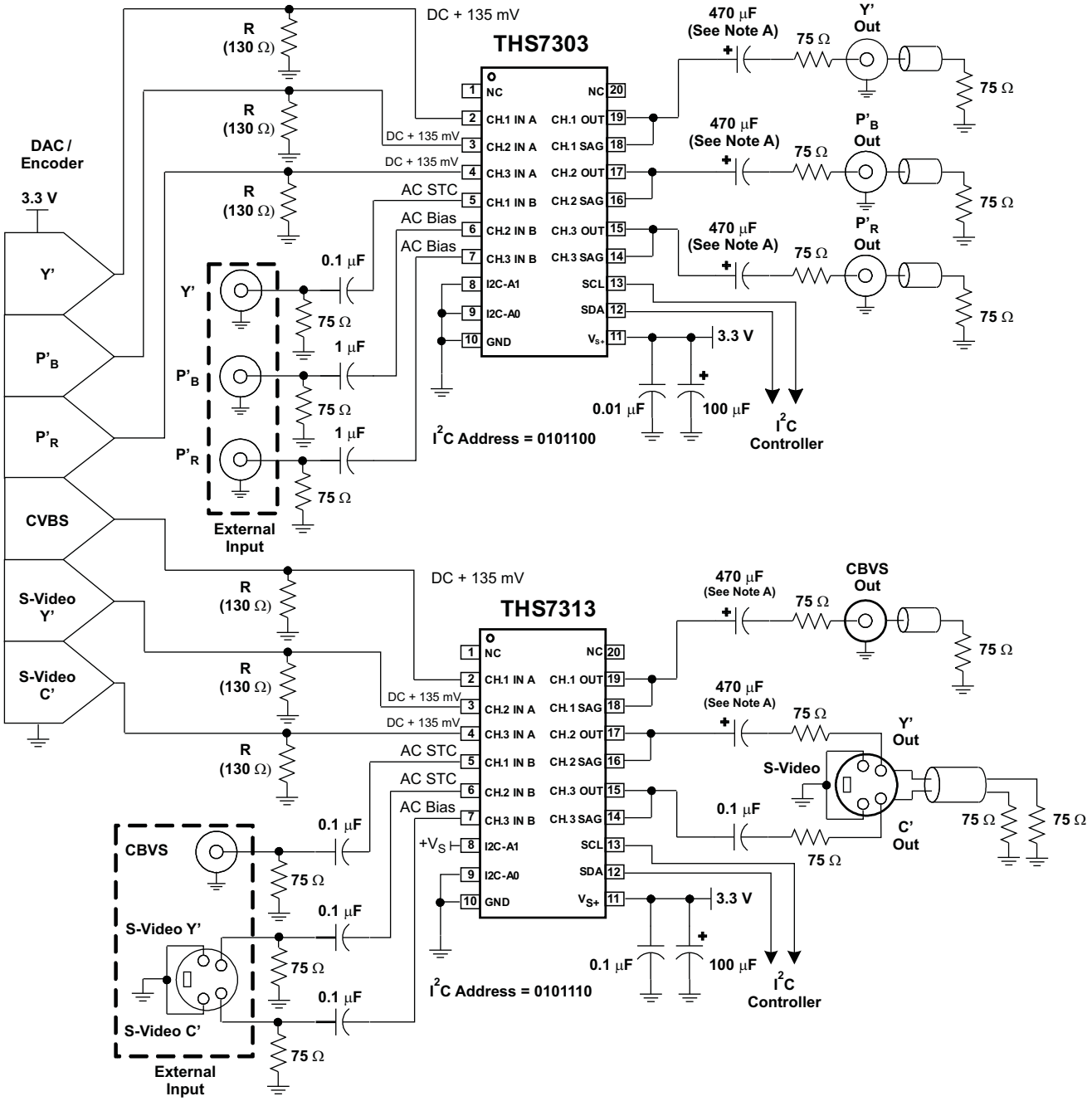

A. Due to the high frequency content of the video signal, it is recommended, but not required, to add a 0.01-µF capacitor in parallel with these large capacitors.

Figure 70. Typical 6-Channel SDTV/EDTV/HDTV Encoder Interfacing to a THS7303 and a THS7313

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BENEFITS OF THS7303 OVER PASSIVE FILTERING

Two key benefits of using an integrated filter system such as the THS7303 over a passive system are PCB area and filter variations. The small TSSOP-20 package for three video channels is much smaller over a passive RLC network, especially a 5-pole passive network that cannot easily change filter corner frequencies. Add in the fact that inductors normally have ±15% to ±20% tolerance, and capacitors typically have ±10% tolerances or more. Using a Monte Carlo analysis shows that the filter corner frequency (–3 dB), flatness (–1 dB), *Q* factor (or peaking), and channel-to-channel delay have wide variations. These variations can lead to potential performance and quality issues in mass-production environments. The THS7303 solves most of these problems with the corner frequency being essentially the only variable.

One concern about an active filter in an integrated circuit is the variation of the filter characteristics when the ambient temperature and the subsequent die temperature change. To minimize temperature effects, the THS7303 uses low temperature coefficient resistors and high-quality, low temperature coefficient capacitors found in the BiCom-3 process. The filters have been specified by design to account for process variations and temperature variations to maintain proper filter characteristics. This maintains the low channel-to-channel time delay that is required for proper video signal performance.

Two additional benefits of a THS7303 over a passive RLC filter are the input and output impedances. The input impedance presented to the DAC varies significantly with a passive network and may cause voltage variations over frequency. The THS7303 input impedance is very high, depending on the input bias mode configuration. This impedance, plus the 2-pF input capacitance along with the PCB trace capacitance, has negligible impact on the input impedance. Therefore, the voltage variation appearing at the DAC output is significantly better controlled with the THS7303.

On the output side of the filter, a passive filter also has a wide impedance variation over frequency. The EIA770 specifications require that the return loss be at least 25dB over the video frequency range of usage. For a video system, this condition implies the source impedance (including the source, the series resistor, and the filter) must be better than 75Ω +9/-8Ω. The THS7303 is an op amp that approximates an ideal voltage source. A voltage source is desirable because the output impedance is very low and can source and sink current. To properly match the transmission line characteristic impedance of a video line, a 75-Ω series resistor is placed on the output. To minimize reflections and maintain a good return loss, this output impedance must maintain a 75-Ω impedance. The wide impedance variation of a passive filter cannot ensure this consistent performance. The THS7303 has approximately 0.7-Ω of output impedance at 6.75-MHz with the SD filter, and approximately 2.5-Ω at 30MHz with the HD filter. Thus, a system is matched much better with a THS7303 compared to a passive filter.

One last benefit of the THS7303 over a passive filter is power dissipation. A DAC driving a video line must be able to drive a 37.5-Ω load. This includes the receiver 75-Ω resistor and the 75-Ω impedance matching resistor next to the DAC to maintain the source impedance requirement. This forces the DAC to drive at least 1.25 V_{PEAK} (100% Saturation CVBS)/37.5Ω = 33.3mA. A DAC is a current-steering element and this amount of current flows internally to the DAC even if the output is 0-V. Thus, power dissipation in the DAC may be very high, especially when three channels are being driven. Using the THS7303, with a high input impedance and the capability to drive up to two video lines per channel, can reduce the DAC power dissipation significantly because the resistance the DAC is driving can be substantially increased. It is common to set this in a DAC by a current-setting resistor on the DAC. Thus, the resistance can be 300-Ω or more. This substantially reduces the current drive demands from the DAC and saves a substantial amount of power. For example, if driving a 37.5-Ω load, a 3.3-V, three-channel DAC dissipates 330mW just for the steering current capability (3 ch × 33.3 mA × 3.3 V). With a 300-Ω load, the DAC power dissipation would only be 41mW (3 ch × 4.16 mA × 3.3 V) as a result of the reduced current steering.

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I²C INTERFACE NOTES

The I²C interface is used to access the internal registers of the THS7303. I²C is a two-wire serial interface developed by Philips Semiconductor (see the I²C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device. The THS7303 works as a slave and supports the standard mode transfer (100 kbps) and fast mode transfer (400 kbps) as defined in the I²C-Bus specification. The THS7303 has been tested to be fully functional but not ensured with the high-speed mode (3.4 Mbps).

The basic I²C start and stop access cycles are shown in Figure 71.

The basic access cycle consists of:

- A start condition
- A slave address cycle
- Any number of data cycles
- A stop condition

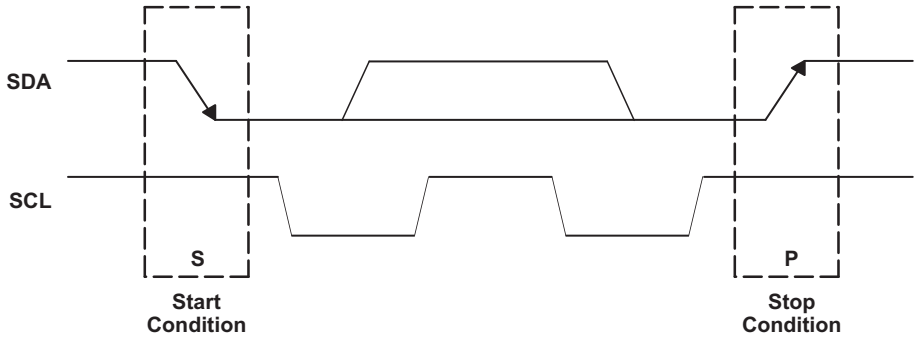

Figure 71. I²C Start and Stop Conditions

GENERAL I²C PROTOCOL

- The master initiates data transfer by generating a start condition (S). A start condition exists when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 71. All I²C-compatible devices should recognize the start condition.
- The master then generates the SCL pulses and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data are valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 72). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 73) by pulling the SDA line low during the entire high period of the ninth SCL cycle. On detecting this acknowledge, the master knows that a communication link with a slave has been established.
- The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver must acknowledge the data sent by the transmitter. Thus, an acknowledge signal (A) can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary (see Figure 74).
- To signal the end of the data transfer, the master generates a stop condition (P) by pulling the SDA line from low to high while the SCL line is high (see Figure 71). This releases the bus and stops the communication link with the addressed slave. All I²C-compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

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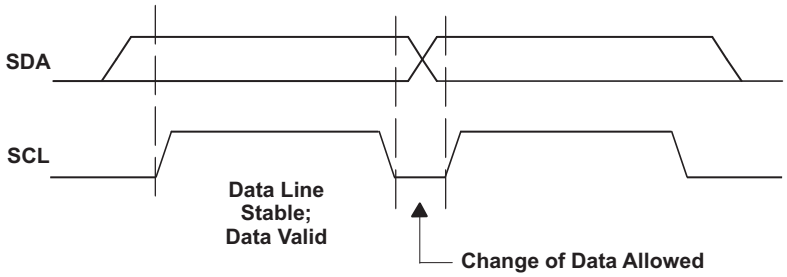

Figure 72. I²C Bit Transfer

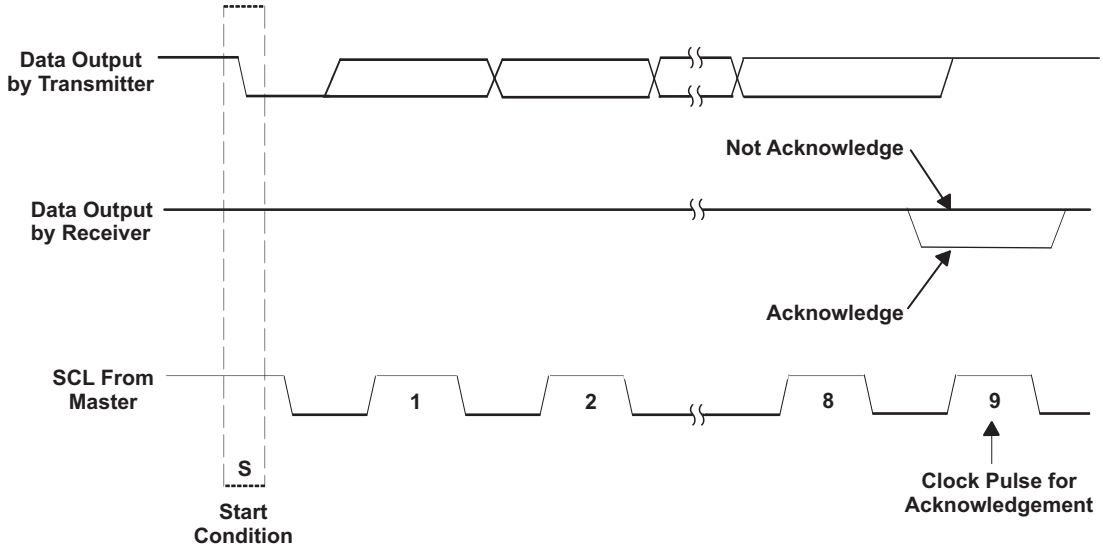

Figure 73. I²C Acknowledge

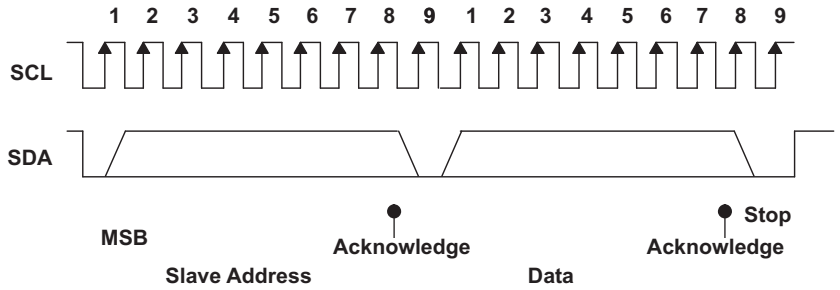

Figure 74. I²C Address and Data Cycles

During a write cycle, the transmitting device must not drive the SDA signal line during the acknowledge cycle, so that the receiving device may drive the SDA signal low. After each byte transfer following the address byte, the receiving device pulls the SDA line low for one SCL clock cycle. A stop condition is initiated by the transmitting device after the last byte is transferred. An example of a write cycle can be found in Figure 75 and Figure 76. Note that the THS7303 does not allow multiple write transfers to occur. See the *Example: Writing to the THS7303* section for the proper procedure on writing to the THS7303.

During a read cycle, the slave receiver acknowledges the initial address byte if it decodes the address as its address. Following this initial acknowledge by the slave, the master device becomes a receiver and acknowledges data bytes sent by the slave. When the master has received all of the requested data bytes from the slave, the not acknowledge ($\overline{A}$) condition is initiated by the master by keeping the SDA signal high just before it asserts the stop condition. This sequence terminates a read cycle, as shown in Figure 77 and Figure 78. Note that the THS7303 does not allow multiple read transfers to occur. See the *Example: Reading from the THS7303* section for the proper procedure on reading from the THS7303.

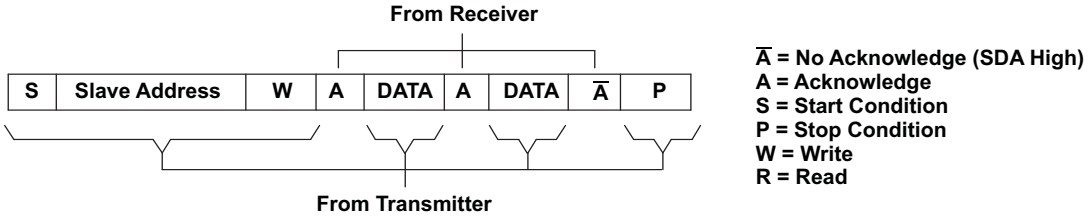

Figure 75. I²C Write Cycle

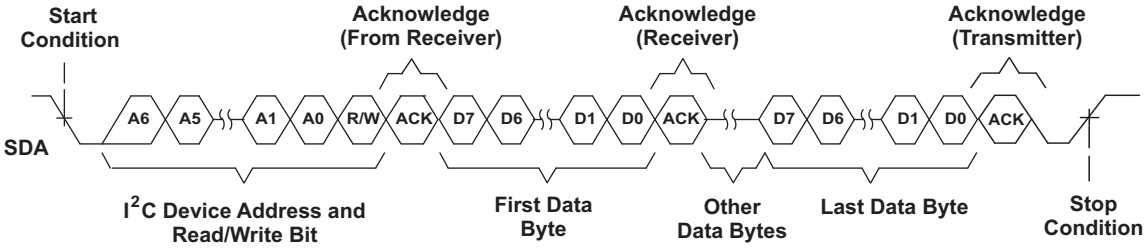

Figure 76. Multiple Byte Write Transfer

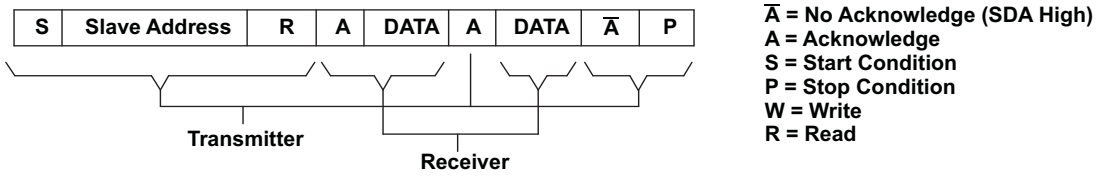

Figure 77. I²C Read Cycle

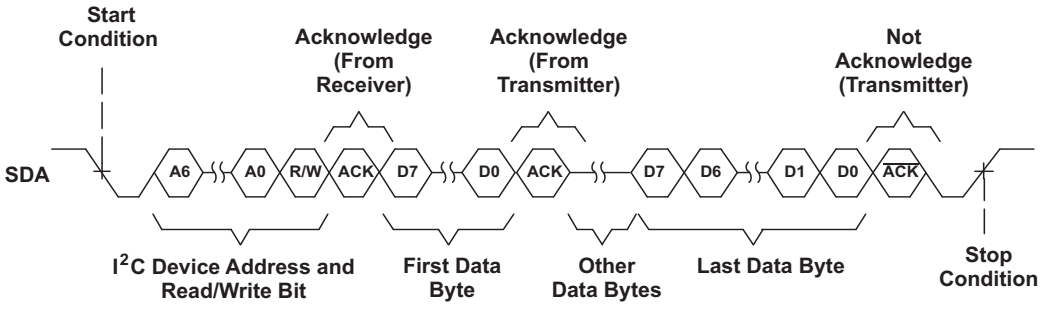

Figure 78. Multiple Byte Read Transfer

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I²C DESIGN NOTES: ISSUES AND SOLUTIONS

The THS7303 requires some special attention to the I²C function that is usually not required. These are known design issues, but there are simple work-arounds that allow the THS7303 to perform within any I²C system.

The first known I²C issue is with respect to the power-up condition. On power up, the THS7303 registers are in a random state from device to device. The registers remain in this random state until a valid write sequence is made to the THS7303. A total of 9 bytes of data completely configure all channels of the THS7303. Therefore, configuring the THS7303 should be done on power-up of the system. Note that one such random state (acknowledge state or ACK) can be engaged. While ACK is engaged, the THS7303 pulls the SDA line low and the master cannot send data to any device on the I²C bus. To circumvent this state, at least one SCL cycle must be completed and then the acknowledge state disengages.

While one SCL cycle normally eliminates any issues, the internal FIFO buffer may have random bits internally to the THS7303. To completely clear all eight bits of this buffer, run 8-cycles (or 8-bits or 1-byte) on the SCL line. While there are several different methods to run SCL cycles, the simplest is to have the master send a 0x00 hex code to the I²C bus on power-up, ignoring any ACK state. Note that the SCL cycle should occur only after the power-supply voltage of the THS7303 is at least 2.7 V. Failure to follow this step may cause the THS7303 to ignore the SCL cycles.

Another known issue with the I²C function is that the internal SDA/SCL buffers are susceptible to high-frequency noise. This noise can come from switch-mode power supplies, digital processors, or other high-frequency noise generators. While the THS7303 includes buffers with hysterisis on the front-end, these are placed after a low-gain CMOS buffer used as an ESD protection element. The noise susceptibility in real-world systems is very low; however, it can be an issue in some noisy or compact systems. The simple solution, which has shown to solve the issue, is to place a RC filter on each I²C line. Real-world results show that using a 100-Ω resistor in series on each SDA/SCL line along with a 22 pF capacitor from each SDA/SCL line to ground eliminates the noise susceptibility issue. These RC filters should be placed as close as possible to the THS7303 SDA/SCL input pins. Other solutions have shown that not using a series resistor and only using a larger value capacitor (such as 100 pF to 220 pF) has worked, but the RC solution is more robust.

One last real-world issue that has appeared relates to the value of the pull-up resistor on the SDA and SCL lines. While the standard allows for between 2 kΩ and 19 kΩ for this pull-up resistor, practice has shown that keeping this value lower works best. Typical values should be between 2 kΩ and 3.3 kΩ, with 2.7 kΩ being the most common.

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SLAVE ADDRESS

The slave address byte is the first byte received following the start condition from the master device. The first five bits (MSBs) of the address are factory preset to '01011'. The next two bits of the THS7303 address are controlled by the logic levels appearing on the I^2C A1 and I^2C A0 pins. The I^2C A1 and I^2C A0 address inputs can be connected to V_{S+} for logic 1, GND for logic 0, or can be actively driven by TTL/CMOS logic levels. The device address is set by the state of these pins and is not latched. Thus, a dynamic address control system can be used to incorporate several devices on the same system. Up to four THS7303 devices can be connected to the same I^2C bus without requiring additional glue logic. Table 1 lists the possible addresses for the THS7303

Table 1. THS7303 Slave Addresses

FIXED ADDRESS					SELECTABLE WITH ADDRESS PINS		READ/WRITE BIT
Blt 7 (MSB)	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2 (A1)**	**BIT 1 (A0)**	**BIT 0**
0	1	0	1	1	0	0	0
0	1	0	1	1	0	0	1
0	1	0	1	1	0	1	0
0	1	0	1	1	0	1	1
0	1	0	1	1	1	0	0
0	1	0	1	1	1	0	1
0	1	0	1	1	1	1	0
0	1	0	1	1	1	1	1

CHANNEL SELECTION REGISTER DESCRIPTION (SUB-ADDRESS)

The THS7303 operates using only a single-byte transfer protocol similar to Figure 75 and Figure 77. The internal sub-address registers, and the functionality of each, are found in Table 2. When writing to the device, it is required to send one byte of data to the corresponding internal sub-address. If control of all three channels is desired, then the master must cycle through all the sub-addresses (channels) one at a time; see the Example: Writing to the THS7303 section for the proper procedure of writing to the THS7303.

During a read cycle, the THS7303 sends the data in its selected sub-address (or channel) in a single transfer to the master device requesting the information. See the *Example: Reading from the THS7303* section for the proper procedure on reading from the THS7303.

Table 2. THS7303 Channel Selection Register Bit Assignments

REGISTER NAME	BIT ADDRESS (b7b6b5....b0)
Channel 1	0000 0001
Channel 2	0000 0010
Channel 3	0000 0011

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CHANNEL REGISTER BIT DESCRIPTIONS

Each bit of the sub-address (channel selection) control register as described in Table 2 allows the user to individually control the functionality of the THS7303. The benefit of this process allows the functionality of each channel to be controlled independently of the other channels. The bit description is decoded in Table 3.

Table 3. THS7303 Channel Register Bit Decoder Table

BIT	FUNCTION	BIT VALUE(S)	RESULT
(MSB) 7, 6	STC Low-Pass Filter Selection	0 0	500-kHz filter—Useful for 9-MHz video LPF
		0 1	2.5-MHz filter—Useful for 16-MHz video LPF
		1 0	5-MHz filter—Useful for 35-MHz/bypass video LPF
		1 1	5-MHz filter—Useful for 35-MHz/bypass video LPF
5	Input MUX Selection	0	Input A select
		1	Input B select
4 , 3	Low-Pass Filter Frequency Selection	0 0	9-MHz LPF—Useful for SDTV, S-Video, 480i/576i
		0 1	16-MHz LPF—Useful for EDTV 480p/576p and VGA
		1 0	35-MHz LPF—Useful for 720p, 1080i, and SVGA/XGA
		1 1	Bypass LPF—Useful for 1080p and SXGA/UXGA
2, 1, 0 (LSB)	Input Bias Mode Selection and Disable Control	0 0 0	Disable channel—Conserves power
		0 0 1	Channel on—Mute function—No output
		0 1 0	Channel on—DC bias select
		0 1 1	Channel on—DC bias + 135 mV offset select
		1 0 0	Channel on—AC bias select
		1 0 1	Channel on—Sync-tip-clamp with low bias
		1 1 0	Channel on—Sync-tip-clamp with mid bias
		1 1 1	Channel on—Sync-tip-clamp with high bias

Bits 7 (MSB) and 6 – Controls the AC Sync-Tip-Clamp Low-Pass Filter function. If ac STC mode is not used, this function is ignored.

Bit 5 – Controls the input MUX of the THS7303.

Bits 4 and 3 – Controls the fifth-order low-pass filter –3 dB corner frequency or the bypass mode of operation.

Bits 2, 1, and 0 (LSB) – Selects the input biasing of the THS7303 and the power-savings function. When sync-tip-clamp is selected, the dc input sink bias current is also selectable.

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EXAMPLE: WRITING TO THE THS7303

To initiate a write operation to the THS7303, an I^2C master generates a start condition (S) followed by the THS7303 I^2C address (as shown below) in MSB first bit order, followed by a '0' to indicate a write cycle. After receiving an acknowledge from the THS7303, the master presents the sub-address (channel) it wants to write consisting of one byte of data, MSB first. The THS7303 acknowledges the byte after completion of the transfer. Finally the master presents the data it wants to write to the register (channel) and the THS7303 acknowledges the byte. The I^2C master then terminates the write operation by generating a stop condition (P). Note that the THS7303 does not support multi-byte transfers. To write to all three channels (or registers), this procedure must be repeated for each register, one series at a time (that is, repeat steps 1 through 8 for each channel).

Example of THS7303 Write Operation:

Step 1	0
I^2C Start (Master)	S

Step 2	7	6	5	4	3	2	1	0
I^2C General Address (Master)	0	1	0	1	1	X	X	0

Where each *X* logic state is defined by I^2C A1 and I^2C A0 pins being tied to either V_{S+} or GND.

Step 3	9
I^2C Acknowledge (Slave)	A

Step 4	7	6	5	4	3	2	1	0
I^2C Write Channel Address (Master)	0	0	0	0	0	0	Addr	Addr

Where *Addr* is determined by the values shown in Table 2.

Step 5	9
I^2C Acknowledge (Slave)	A

Step 6	7	6	5	4	3	2	1	0
I^2C Write Data (Master)	Data	Data	Data	Data	Data	Data	Data	Data

Where *Data* is determined by the values shown in Table 3.

Step 7	9
I^2C Acknowledge (Slave)	A

Step 8	0
I^2C Stop (Master)	P

For Step 6, an example of the proper bit control for selecting Input B of the MUX, a 720p Y' channel signal with ac STC lowest line tilt and with the shortest sync filter is 1111 0101.

For Step 7, the ACK state means the THS7303 pulls the SDA line low until the next cycle on the SCL line.

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EXAMPLE: READING FROM THE THS7303

The read operation consists of two phases. The first phase is the address phase, where an I^2C master initiates a write operation to the THS7303 by generating a start condition (S) followed by the THS7303 I^2C address in MSB first bit order, followed by a '0' to indicate a write cycle. After receiving acknowledges from the THS7303, the master presents the sub-address (channel) of the register it wants to read. After the cycle is acknowledged (A), the master terminates the cycle immediately by generating a stop condition (P).

The second phase is the data phase. In this phase, an I^2C master initiates a read operation to the THS7303 by generating a start condition followed by the THS7303 I^2C address in MSB first bit order, followed by a '1' to indicate a read cycle. After an acknowledge from the THS7303, the I^2C master receives one byte of data from the THS7303. After the data byte has been transferred from the THS7303 to the master, the master generates a not acknowledge ($\overline{A}$) followed by a stop. As with the write function, in order to read all channels, steps 1 through 11 must be repeated for each channel desired.

Example of THS7303 Read Phase 1:

Step 1	0
I^2C Start (Master)	S

Step 2	7	6	5	4	3	2	1	0
I^2C General Address (Master)	0	1	0	1	1	X	X	0

Where each *X* logic state is defined by I^2C A1 and I^2C A0 pins being tied to either V_{S+} or GND.

Step 3	9
I^2C Acknowledge (Slave)	A

Step 4	7	6	5	4	3	2	1	0
I^2C Read Channel Address (Master)	0	0	0	0	0	0	Addr	Addr

Where *Addr* is determined by the values shown in Table 2.

Step 5	9
I^2C Acknowledge (Slave)	A

Step 6	0
I^2C Start (Master)	P

Example of THS7303 Read Phase 2:

Step 7	0
I^2C Start (Master)	S

Step 8	7	6	5	4	3	2	1	0
I^2C General Address (Master)	0	1	0	1	1	X	X	1

Where each *X* logic state is defined by I^2C A1 and I^2C A0 pins being tied to either V_{S+} or GND.

Step 9	9
I^2C Acknowledge (Slave)	A

Step 10	7	6	5	4	3	2	1	0
I^2C Read Data (Slave)	Data	Data	Data	Data	Data	Data	Data	Data

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Where *Data* is determined by the logic values contained in the channel register.

Step 11	9
I^2C Not-Acknowledge (Master)	$\overline{A}$

Step 12	0
I^2C Stop (Master)	P

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EVALUATION MODULE

To evaluate the THS7303, an evaluation module (EVM) is available. Because the THS7303 is controlled by the I^2C lines, additional control is required rather than simple switches. To keep the control as easy as possible, a USB-to-I^2C interface was designed onto the EVM. A computer running either Windows® 2000 or XP is then connected to the EVM through the USB cable. A computer program interface was created for graphical control of the THS7303 that allows both read and write functions to be performed. The EVM comes with a CD-ROM loaded with all the required software to install the command software onto the computer.

To program the THS7303, select the channel, the filter, and the mode of operation and then click the Execute button. The *Req Done* light on the computer screen is lit to confirm the command was executed by the THS7303. The same procedure is done for each channel. To read the THS7303 registers, change the switch to *Read*, select the channel, and then click the Execute button. The resulting register content appears in hexadecimal code.

Note that the USB-to-I^2C interface circuitry must be powered by a 3.3-V supply only. Additionally, the I^2C circuitry section must be powered on either at the same time as the THS7303 or before power is applied to the THS7303. This is because the TAS1020 device must complete reading the EEPROM to program its core. The yellow LED in the I^2C section is lit if the TAS1020 was programmed properly. If this LED is not lit, then the power should be cycled to reset the USB-to-I^2C TAS1020 chip.

The communication between the computer and the THS7303 EVM over USB is not plug-and-play. Instead, the system must be powered up in sequence for proper communication. Follow this procedure to start the program:

1. Make sure the computer program (*THS73x3EVM Control* program) is not turned on, and make sure there is no power applied to the EVM (both 3.3 V and the V_A (THS7303) power). Check that the USB cable is plugged into both the computer and the EVM.
2. Apply both 3.3-V and the V_A power to the THS73x3 EVM. The USB ACTIVE LED (D2) must be lit yellow. If D2 s not lit, then there is a EEPROM communication problem between U2 and U3. This must be corrected before going any further.

NOTE

It is very important to apply power to the THS7303 EVM and have the yellow LED lit before starting the program on the computer. Failure to follow this step will result in the computer program not recognizing the EVM and there will be no communication between the computer and the EVM. If power is removed for any reason, shutdown the computer program, apply power to the THS7303 EVM with the yellow LED lit, and then restart the computer program as indicated here.

3. Configure the I^2C address jumpers (JP1 and JP2) for the desired I^2C addressing. With the jumpers removed, the two LSBs are *00*.
4. With D2 lit, now start the computer program (*THS73x3 EVM Control*). Configure the program as desired, making sure that the address of the THS73x3 matches the jumper settings JP1 and JP2. By default, *00* matches the EVM with the jumpers removed.
5. Once configured, pressing the **Execute** button writes the code to the THS73x3 EVM and sends the proper I^2C codes to the THS73x3. The computer program should show a *green* light; this light indicates proper communication to the THS73x3 is occurring.

Table 4 is a bill of materials; the board layout is found in Figure 79 to Figure 82.

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Table 4. Bill of Materials for THS7303 EVM

ITEM	DESCRIPTION	SMD SIZE	REFERENCE DESIGNATOR	PCB QUANTITY	MANUFACTURER PART NUMBER(1)	DISTRIBUTOR PART NUMBER
1	BEAD, FERRITE, 2.5A, 80 OHM	0805	FB1, FB2, FB3	3	(TDK) MPZ2012S331A	(DIGI-KEY) 445-1569-1-ND
2	CAP, 22uF, TAN, 6.3V, 10%, LO ESR	A	C30	1	(AVX) TPSA226K006R0900	(DIGI-KEY) 478-1754-1-ND
3	CAP, 100uF, TAN, 10V, 10%, LO ESR	C	C5	1	(AVX) TPSC107K010R0100	(DIGI-KEY) 478-1765-1-ND
4	OPEN	0805	C2, C3, C8, C11, C12, C14, C17, C21, C23	9		
5	CAP, 33pF, CERAMIC, 50V, NPO	0805	C31, C32	2	(AVX) 08055A330JAT2A	(DIGI-KEY) 478-1310-1-ND
6	CAP, 47pF, CERAMIC, 50V, NPO	0805	C27, C29	2	(AVX) 08055A470JAT2A	(DIGI-KEY) 478-1312-1-ND
7	CAP, 100pF, CERAMIC, 50V, NPO	0805	C34	1	(AVX) 08055A101JAT2A	(DIGI-KEY) 478-1316-1-ND
8	CAP, 1000pF, CERAMIC, 100V, NPO	0805	C33	1	(AVX) 08051A102JAT2A	(DIGI-KEY) 478-1290-1-ND
9	CAP, 0.01uF, CERAMIC, 100V, X7R	0805	C19, C28	2	(AVX) 08051C103KAT2A	(DIGI-KEY) 478-1358-1-ND
10	CAP, 0.1uF, CERAMIC, 50V, X7R	0805	C4, C6, C9, C13, C16, C22, C25, C26, C43, C44, Z4	11	(AVX) 08055C104KAT2A	(DIGI-KEY) 478-1395-1-ND
11	CAP, 1uF, CERAMIC, 16V, X7R	0805	C18, C35, C36, C37, C38, C39, C40, C41, C42, Z5, Z6	11	(TDK) C2012X7R1C105K	(DIGI-KEY) 445-1358-1-ND
12	CAP, ALUM, 470uF, 10V, 20%	F	C1, C10, C20	3	(CORNELL) AFK477M10F24B	(NEWARK) 97C7597
13	CAP, ALUM, 33uF, 25V, 20%	C	C7, C15, C24	3	(CORNELL) AFK336M25C12B	(NEWARK) 97C7564
14	OPEN	0603	R47, R48, R49, R51	4		
15	RESISTOR, 0 OHM	0603	R1, R2, R3, R4, R6, R7, R19, R20, R23	9	(ROHM) MCR03EZPJ000	(DIGI-KEY) RHM0.0GCT-ND
16	RESISTOR, 2.74K OHM, 1/8W, 1%	0603	R41, R61	2	(ROHM) MCR03EZPFX2741	(DIGI-KEY) RHM2.7KHCT-ND
17	OPEN	0805	R15, R16, R28	3		
18	RESISTOR, 0 OHM	0805	R9, R13, R21, Z1, Z2, Z3	6	(ROHM) MCR10EZHJ000	(DIGI-KEY) RHM0.0ACT-ND
19	RESISTOR, 10 OHM, 1/8W, 1%	0805	R39, R44, R45, R52	4	(ROHM) MCR10EZHF10R0	(DIGI-KEY) RHM10.0CCT-ND
20	RESISTOR, 27.4 OHM, 1/8W, 1%	0805	R30, R31	2	(ROHM) MCR10EZHF27.4	(DIGI-KEY) RHM27.4CCT-ND
21	RESISTOR, 75 OHM, 1/8W, 1%	0805	R5, R8, R10, R11, R12, R14, R17, R18, R22	9	(ROHM) MCR10EZHF75.0	(DIGI-KEY) RHM75.0CCT-ND
22	RESISTOR, 100 OHM, 1/8W, 1%	0805	R50	1	(ROHM) MCR10EZHF1000	(DIGI-KEY) RHM100CCT-ND
23	RESISTOR, 200 OHM, 1/8W, 1%	0805	R26, R27	2	(ROHM) MCR10EZHF2000	(DIGI-KEY) RHM200CCT-ND
24	RESISTOR, 649 OHM, 1/8W, 1%	0805	R33, R60	2	(ROHM) MCR10EZHF0649	(DIGI-KEY) RHM649CCT-ND
25	RESISTOR, 1.0K OHM, 1/8W, 1%	0805	R29	1	(ROHM) MCR10EZHF1001	(DIGI-KEY) RHM1.00KCCT-ND
26	RESISTOR, 1.5K OHM, 1/8W, 1%	0805	R32	1	(ROHM) MCR10EZHF1501	(DIGI-KEY) RHM1.50KCCT-ND
27	RESISTOR, 2.21K OHM, 1/8W, 1%	0805	R34, R35	2	(ROHM) MCR10EZHF2211	(DIGI-KEY) RHM2.21KCCT-ND

(1) Manufacturer part numbers are used for test purposes only.

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Table 4. Bill of Materials for THS7303 EVM (continued)

ITEM	DESCRIPTION	SMD SIZE	REFERENCE DESIGNATOR	PCB QUANTITY	MANUFACTURER PART NUMBER(1)	DISTRIBUTOR PART NUMBER
28	RESISTOR, 3.09K OHM, 1/8W, 1%	0805	R43	1	(ROHM) MCR10EZHF3091	(DIGI-KEY) RHM3.09KCCT-ND
29	RESISTOR, 10K OHM, 1/8W, 1%	0805	R24, R25, R40, R42	4	(ROHM) MCR10EZHF1002	(DIGI-KEY) RHM10.0KCCT-ND
30	RESISTOR, 20K OHM, 1/8W, 1%	0805	R46	1	(ROHM) MCR10EZHF2002	(DIGI-KEY) RHM20.0KCCT-ND
31	LED, GREEN	0805	D1	1	(LITE-ON) LTST-C171GKT	(DIGI-KEY) 160-1423-1-ND
32	LED, YELLOW	0805	D2	1	(LITE-ON) LTST-C171YKT	(DIGI-KEY) 160-1431-1-ND
33	IC, CONV, SERIAL TO USB		U3	1	(TI) TAS1020BPFB	(DIGI-KEY) TAS1020BPFB
34	IC, SERIAL, EEPROM, 64K	8-SOIC	U2	1	(MICROCHIP) 24LC64-I/SN	(DIGI-KEY) 24LC64-I/SN-ND
35	CRYSTAL, 6.00MHz., SMT	HCM49	X1	1	(CITIZEN) HCM49-6.000MABJT	(DIGI-KEY) 300-6112-1-ND
36	OPEN	SOT-23	U4, U5	2		
37	JACK, BANANA RECEPTANCE, 0.25" DIA. HOLE		J4, J5, J16, J17	4	(SPC) 813	(NEWARK) 39N867
38	SWITCH, SMD GULL WING	4MM	S1	1	(BOURNS) 7914G-1-000E	(DIGI-KEY) 7914G-000ETR-ND
39	CONNECTOR, RCA, JACK, R/A		J1, J2, J12	3	(CUI) RCJ-32265	(DIGI-KEY) CP-1446-ND
40	CONNECTOR, USB, RTANG, FEMALE	B	J15	1	(ASSMANN) AU-Y1007	(DIGI-KEY) AE1085-ND
41	CONNECTOR, BNC, JACK, 75 OHM		J3, J6, J7, J8, J9, J10, J11, J13, J14	9	(AMPHENOL) 31-5329-72RFX	(NEWARK) 93F7554
42	HEADER, 0.1" CTRS, 0.025" SQ. PINS	2 POS.	JP1, JP2, JP3	3	(SULLINS) PZC36SAAN	(DIGI-KEY) S1011-36-ND
43	SHUNTS		JP1, JP2, JP3	3	(SULLINS) SSC02SYAN	(DIGI-KEY) S9002-ND
44	TEST POINT, RED		TP1, TP2, TP5, TP6, TP7	5	(KEYSTONE) 5000	(DIGI-KEY) 5000K-ND
45	TEST POINT, BLACK		TP3, TP4	2	(KEYSTONE) 5001	(DIGI-KEY) 5001K-ND
46	IC, THS7303		U1	1	(TI) THS7303PW	
47	STANDOFF, 4-40 HEX, 0.625" LENGTH			4	(KEYSTONE) 1808	(NEWARK) 89F1934
48	SCREW, PHILLIPS, 4-40, .250"			4	(BF) PMS 440 0031 PH	(DIGI-KEY) H343-ND
49	BOARD, PRINTED CIRCUIT			1	EDGE # 6469005 REV.B	

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EVM BOARD LAYERS

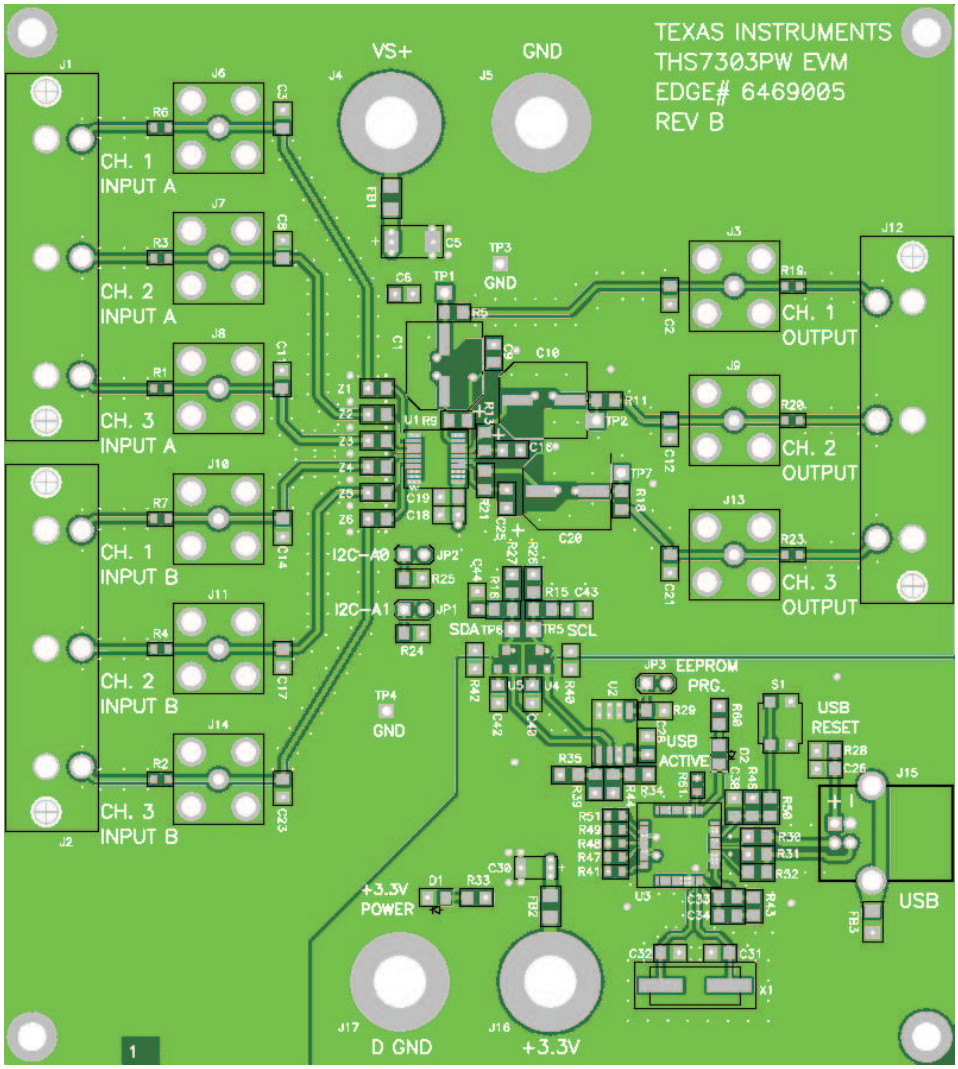

Figure 79. Top Layer: Signal Layer

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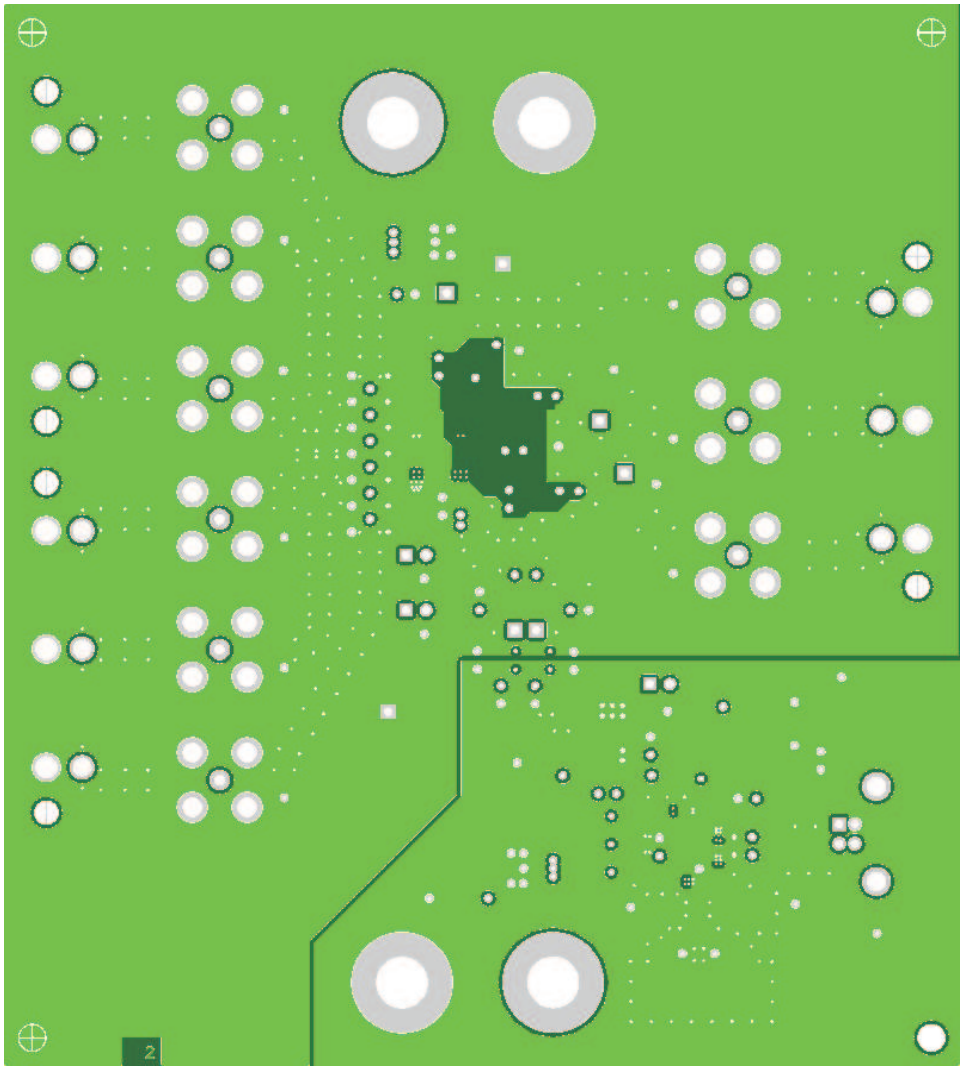

Figure 80. Layer Two: Ground Layer

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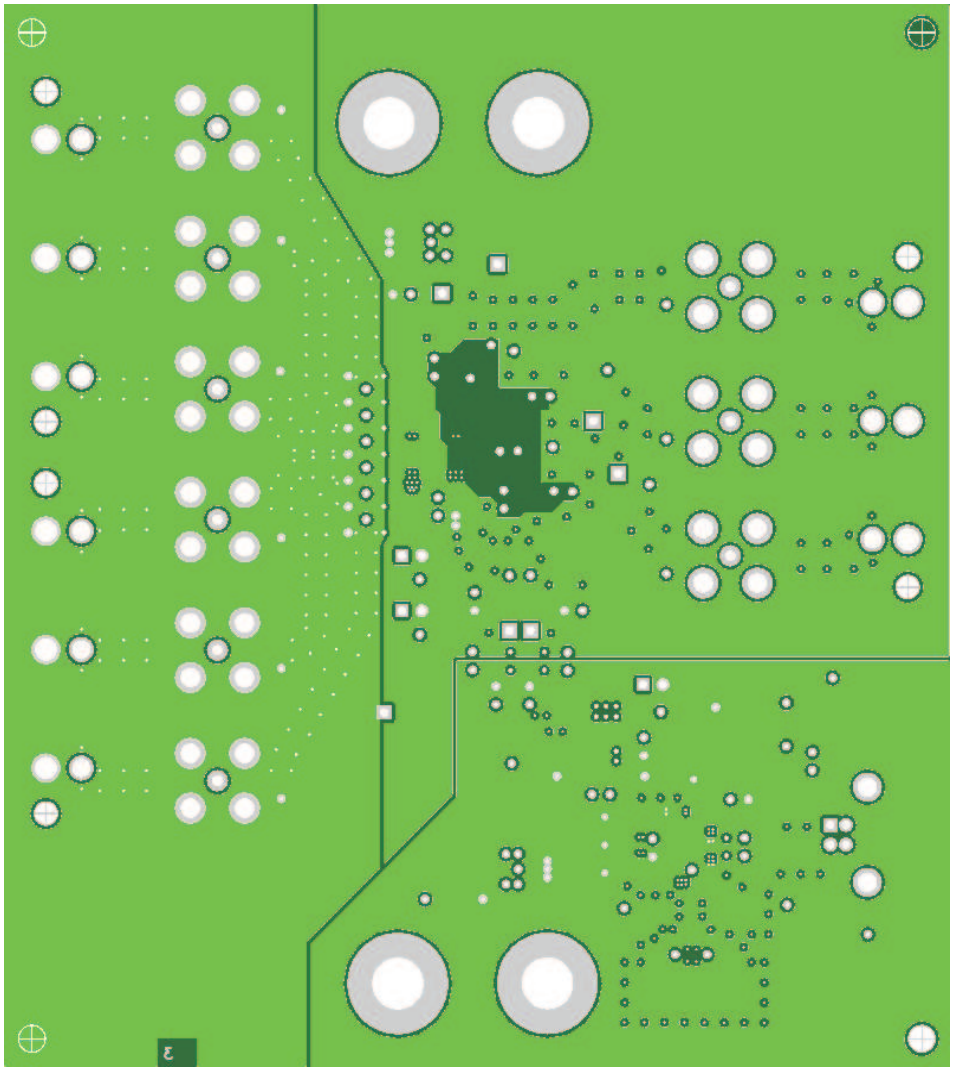

Figure 81. Layer Three: Power and Ground Layer

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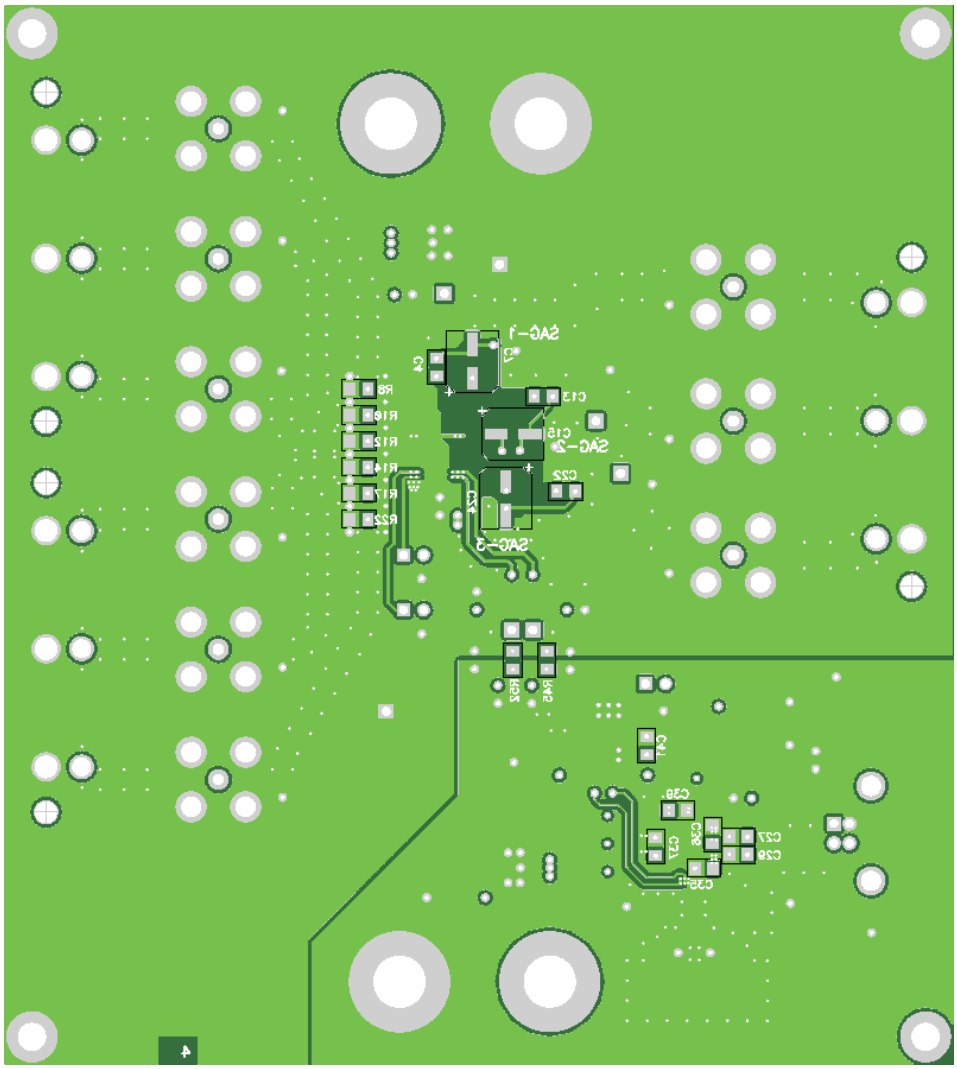

Figure 82. Bottom Layer: Signal Layer

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December, 2008) to Revision B **Page**

- Added *Digital Characteristics* section specifications to 3.3-V Electrical Characteristics 4
- Added *Digital Characteristics* section specifications to 5-V Electrical Characteristics 6
- Added *Increasing Gain* section 33
- Updated *Evaluation Module* section 47

Changes from Original (October, 2005) to Revision A **Page**

- Changed format and flow of data sheet to match current standard 1
- Changed Package/Ordering Information table quantities 2

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 0 V to 3 V and the output voltage range of 0 V to 5 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +100°C. The EVM is designed to operate properly with certain components above +100° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
THS7303PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS7303PW	Samples
THS7303PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS7303PW	Samples
THS7303PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS7303PW	Samples
THS7303PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS7303PW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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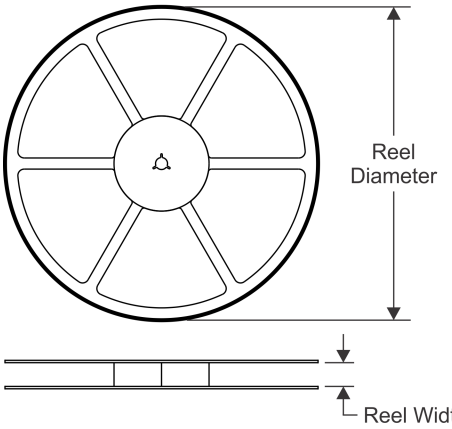
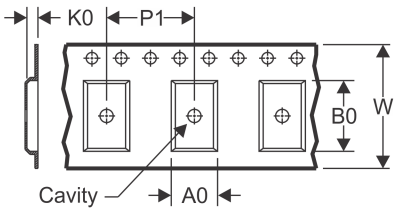
TAPE AND REEL INFORMATION

REEL DIMENSIONS

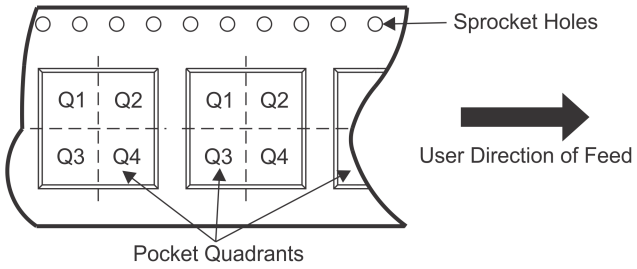


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

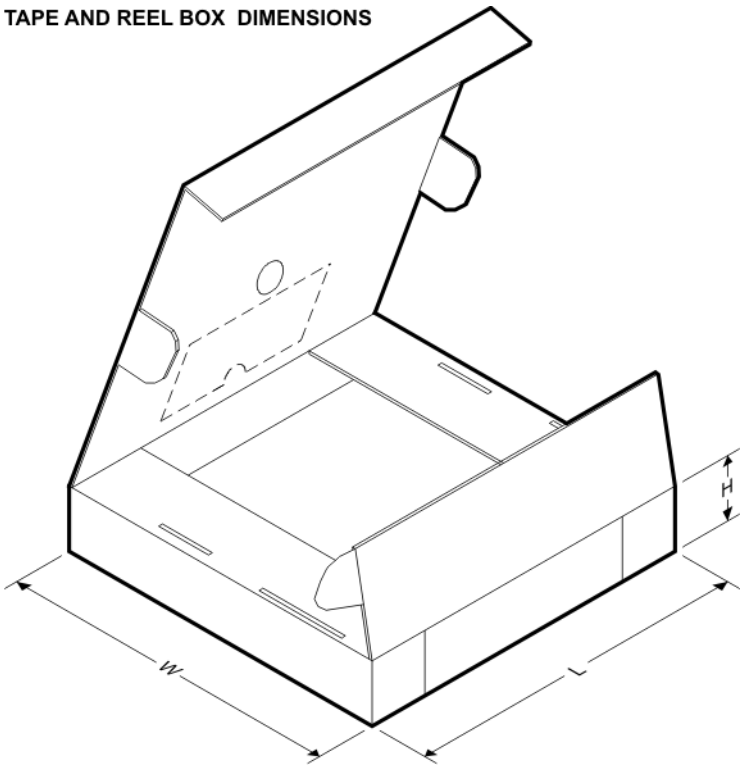
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS7303PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

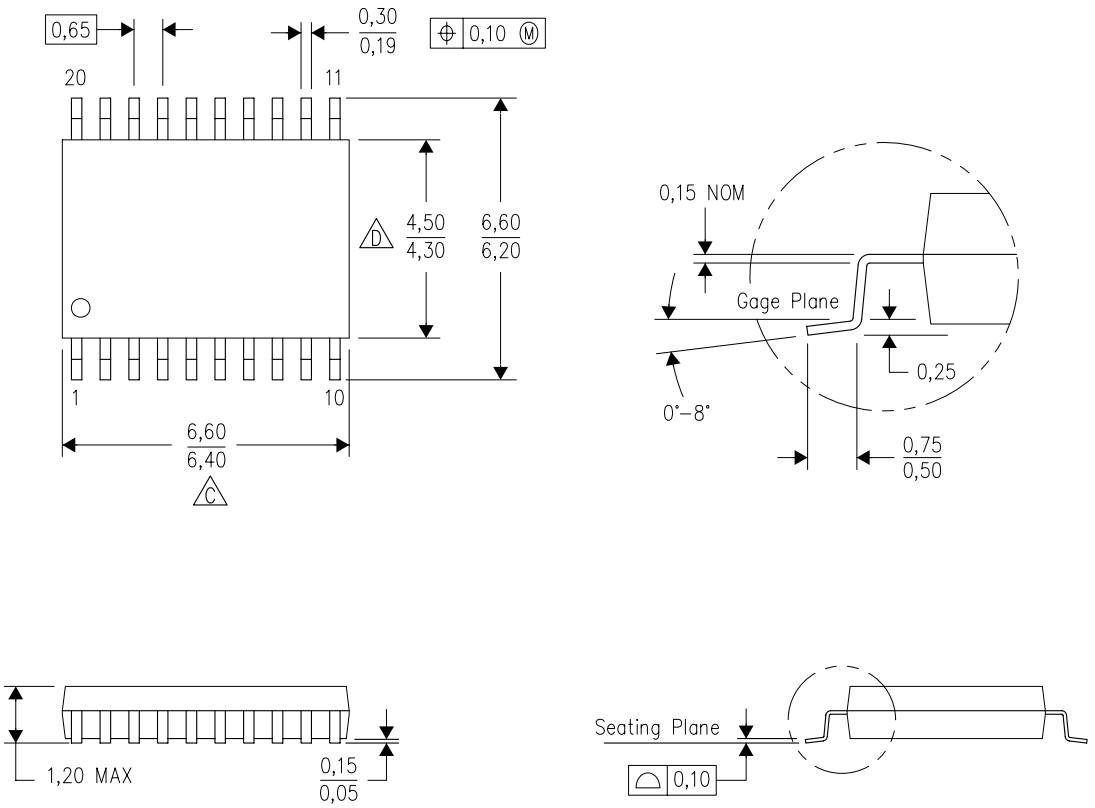
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS7303PWR	TSSOP	PW	20	2000	350.0	350.0	43.0

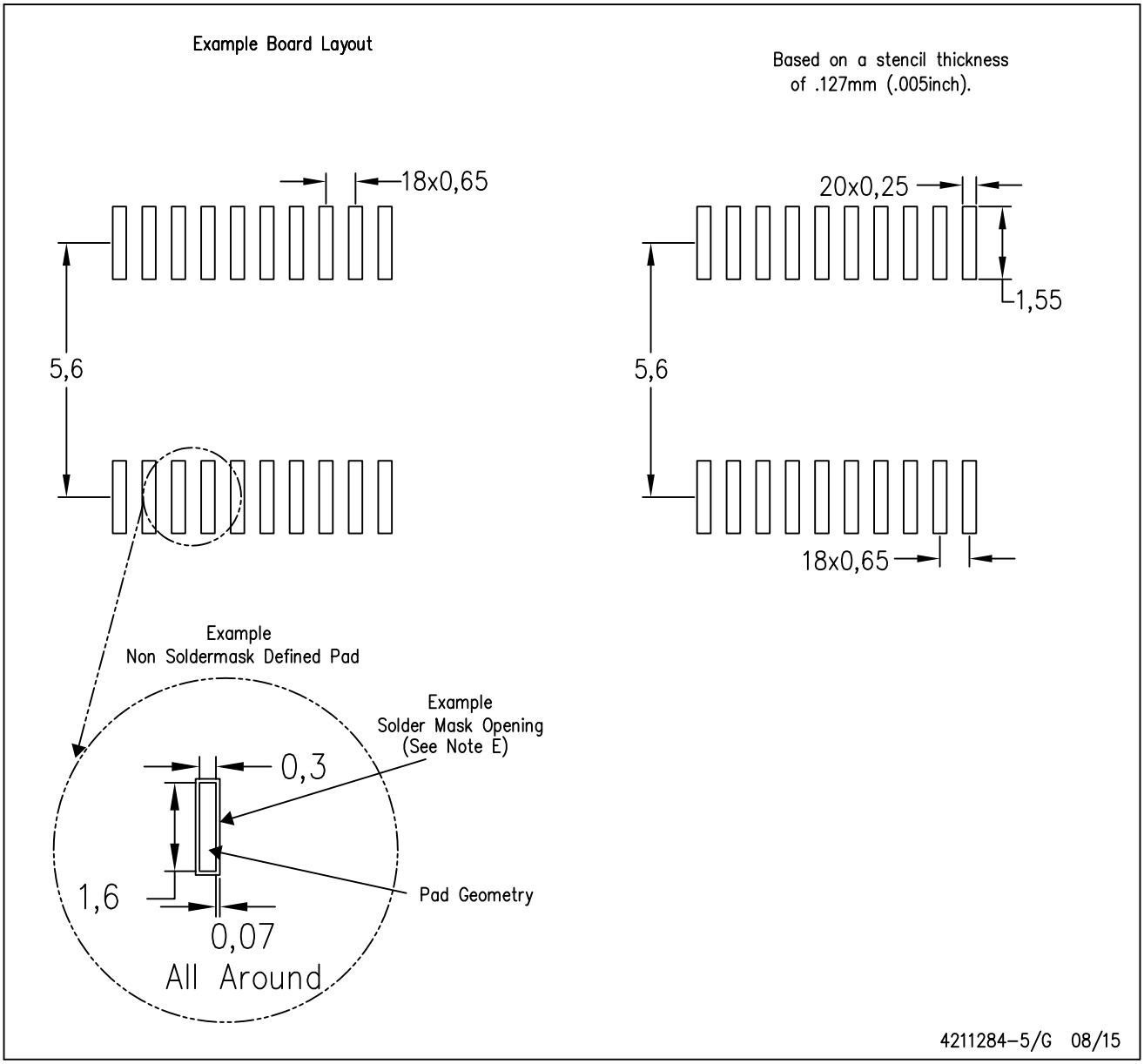
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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