THE DATASHEET OF

TDA8020HL/C1,118

DATA SHEET

TDA8020HL
Dual IC card interface

Product specification
Supersedes data of 2001 Aug 15

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Philips
Semiconductors

PHILIPS

Dual IC card interface TDA8020HL

FEATURES

- Two independent 6 contacts smart card interfaces
- Supply voltage to the cards: V_{CC} = 5 V and I_{CC} up to 60 mA or 3 V ±5% and I_{CC} up to 55 mA
- Integrated DC-to-DC converter (doubler, tripler or follower) for allowing power supply from 2.7 to 6.5 V
- Independent supply voltage for interface signals (from 1.5 to 6.5 V)
- Control and status via the I^2C-bus
- Four possible devices in parallel due to two I^2C-bus address pins
- Electrical specifications according to ISO 7816 or EMV2000
- Automatic activation and deactivation sequences by means of integrated sequencers
- Automatic clock count and reset toggling during warm or cold reset
- Interrupt request output to the controller
- 6 kV ESD protection on cards contacts
- Automatic emergency deactivation in the event of supply drop-out, overload, overheating, card take-off or DC-to-DC malfunctioning
- Current limitation on pins CLK, RST, I/O and V_{CC}
- Integrated voltage supervisor for power-on reset and drop-out detection.

APPLICATIONS

- Set top boxes
- Banking terminals
- Internet terminals.

GENERAL DESCRIPTION

The TDA8020HL is a one-chip dual smart card interface. Controlled by the I^2C-bus, it guarantees conformity to ISO 7816 or EMV2000 with very few external components.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8020HL/C1	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1
TDA8020HL/C2	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage on pins V_{DD} and V_{DDA}		2.7	–	6.5	V
V_{DDI}	supply voltage for interface signals		1.5	–	V_{DD}	V
I_{DD}	supply current	V_{DD} = 3.3 V; inactive mode	–	–	150	µA
		V_{DD} = 3.3 V; Power-down mode; 2 cards activated; $V_{CC1} = V_{CC2}$ = 5 V; $I_{CC1} = I_{CC2}$ = 100 µA; CLK1 and CLK2 stopped	–	–	2	mA
		V_{DD} = 3.3 V; active mode; $V_{CC1} = V_{CC2}$ = 5 V; $I_{CC1} + I_{CC2}$ = 80 mA; CLK1 = CLK2 = 5 MHz	–	–	400	mA
		V_{DD} = 3.3 V; active mode; $V_{CC1} = V_{CC2}$ = 3 V; $I_{CC1} = I_{CC2}$ = 10 mA; CLK1 = CLK2 = 5 MHz	–	–	80	mA
I_{DDA}	DC-to-DC converter supply current	inactive mode; V_{DDA} = 5 V; f_{xtal} = 10 MHz	–	–	0.1	mA
		active mode; V_{DDA} = 5 V; f_{xtal} = 10 MHz; no load	–	–	10	mA
Card supply						
V_{CC1}, V_{CC2}	card supply voltage including ripple	5 V card; DC I_{CC} < 60 mA	4.75	–	5.25	V
		5 V card; AC current spikes of 40 nAs	4.65	–	5.25	V
		3 V card; DC I_{CC} < 55 mA	2.85	–	3.15	V
		3 V card; AC current spikes of 40 nAs	2.76	–	3.20	V
$V_{ripple(p-p)}$	ripple voltage (peak-to-peak value)	20 kHz to 200 MHz	–	–	350	mV
I_{CC1}, I_{CC2}	card supply current	0 V to 5 V	–	–	60	mA
		0 V to 3 V	–	–	55	mA
General						
V_{th1}	threshold voltage for the supervisor on V_{DD}		2.1	–	2.4	V
V_{hys1}	hysteresis on V_{th1}		50	–	100	mV
t_{de}	deactivation cycle duration		50	80	100	µs
P_{tot}	continuous total power dissipation	T_{amb} = –40 to +85 °C	–	–	0.50	W
T_{amb}	ambient temperature	TDA8020HL/C1	–30	–	+85	°C
		TDA8020HL/C2	–40	–	+85	°C

BLOCK DIAGRAM

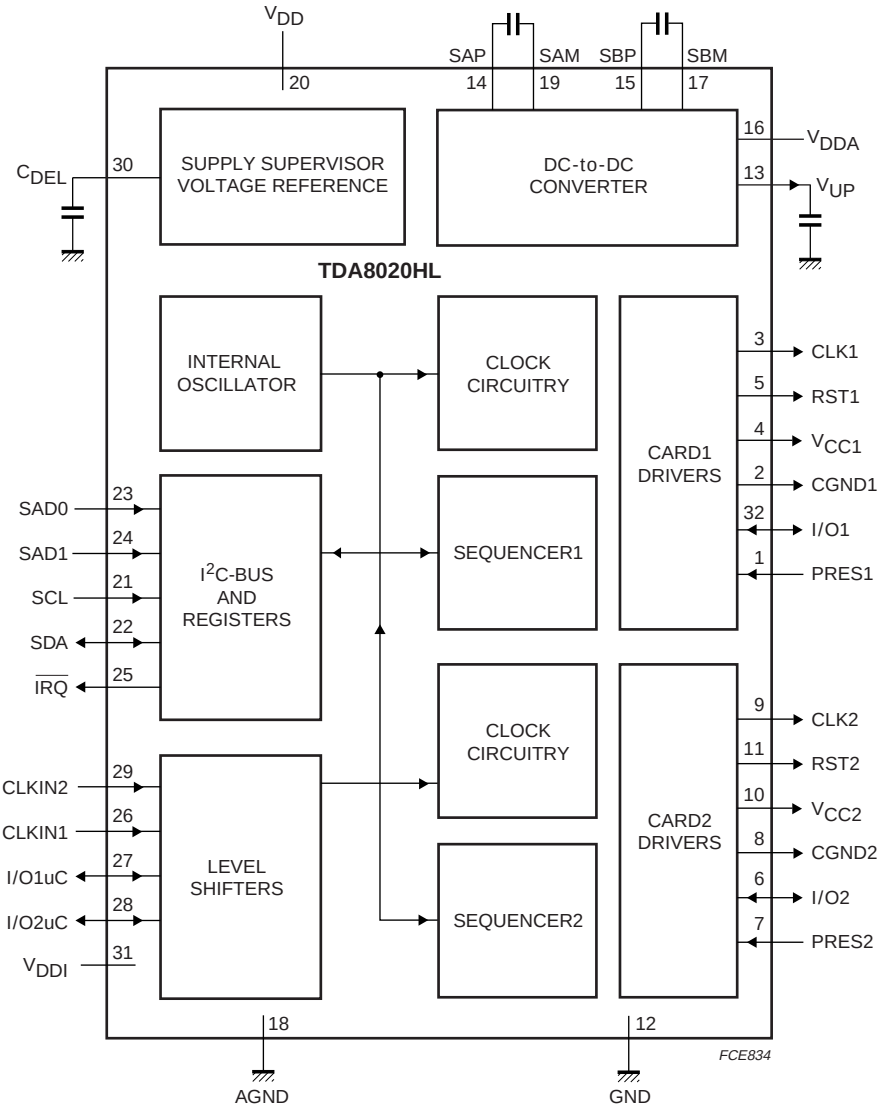


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
PRES1	1	I	card 1 presence contact input (active HIGH)
CGND1	2	supply	ground connection output to card 1 (C5 contact)
CLK1	3	O	clock output to card 1 (C3 contact)
V_{CC1}	4	supply	supply voltage output to card 1 (C1 contact); decouple to pin CGND1 with 2×100 nF capacitors with ESR < 100 mΩ
RST1	5	O	reset output to card 1 (C2 contact)
I/O2	6	I/O	I/O contact to card 2 (C7 contact); internal 15 kΩ pull-up resistance to pin V_{CC2}
PRES2	7	I	card 2 presence contact input (active HIGH)
CGND2	8	supply	ground connection output to card 2 (C5 contact)
CLK2	9	O	clock output to card 2 (C3 contact)
V_{CC2}	10	supply	supply voltage output to card 2 (C1 contact); decouple to pin CGND2 with 2×100 nF capacitors with ESR < 100 mΩ
RST2	11	O	reset output to card 2 (C2 contact)
GND	12	supply	ground connection
V_{UP}	13	I/O	output of DC-to-DC converter; a 220 nF capacitor with ESR < 100 mΩ must be connected to pin AGND
SAP	14	I/O	capacitor connection for the DC-to-DC converter; a 220 nF capacitor with ESR < 100 mΩ must be connected between pins SAP and SAM
SBP	15	I/O	capacitor connection for the DC-to-DC converter; a 220 nF capacitor with ESR < 100 mΩ must be connected between pins SBP and SBM
V_{DDA}	16	supply	analog supply voltage for the DC-to-DC converter
SBM	17	I/O	capacitor connection for the DC-to-DC converter; a 220 nF capacitor with ESR < 100 mΩ must be connected between pins SBP and SBM
AGND	18	supply	analog ground for the DC-to-DC converter
SAM	19	I/O	capacitor connection for the DC-to-DC converter; a 220 nF capacitor with ESR < 100 mΩ must be connected between pins SAP and SAM
V_{DD}	20	supply	power supply voltage
SCL	21	I	serial clock input of I^2C-bus (open drain)
SDA	22	I/O	serial data input/output of I^2C-bus (open drain)
SAD0	23	I	I^2C-bus address selection input 0
SAD1	24	I	I^2C-bus address selection input 1
$\overline{IRQ}$	25	O	interrupt request output to host (open drain; active LOW)
CLKIN1	26	I	external clock input for card 1
I/O1uC	27	I/O	I/O connection to host for card 1; internal 11 kΩ pull-up resistor to V_{DDI}
I/O2uC	28	I/O	I/O connection to host for card 2; internal 11 kΩ pull-up resistor to V_{DDI}
CLKIN2	29	I	external clock input for card 2
C_{DEL}	30	I/O	delay capacitor connection for the voltage supervisor (1 ms per 2 nF)
V_{DDI}	31	I	interface signals reference supply voltage
I/O1	32	I/O	I/O contact to card 1 (C7 contact); internal 14 kΩ pull-up resistor to V_{CC1}

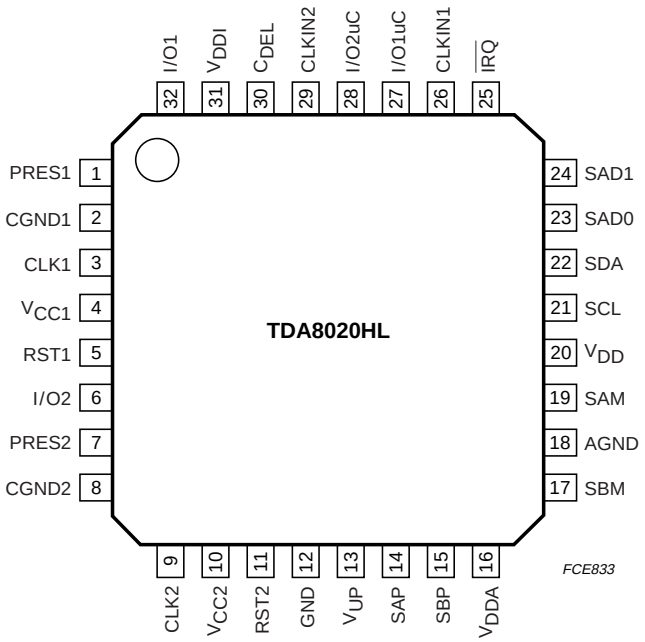


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Throughout this specification, it is assumed that the reader is familiar with ISO 7816 terminology.

Supply

The TDA8020HL operates with a supply voltage from 2.7 to 6.5 V. An integrated voltage supervisor ensures that no spike appears on cards contacts during power-on or off. The supervisor also initializes the device, and forces an automatic emergency deactivation of the contacts in the event of a supply drop-out.

As long as the supply voltage is below the threshold voltage V_{th1}, the capacitor C_{DEL} remains uncharged. When the supply voltage reaches V_{th1} and V_{hys1}, then C_{DEL} is charged with a small current source of approximately 2 μA. When the voltage on C_{DEL} reaches V_{th2}, then the supervisor is no longer active. As long as the supervisor is active (pin $\overline{IRQ}$ is LOW), bit SUPL in the status register is set. When pin $\overline{IRQ}$ goes HIGH the voltage supervisor becomes inactive (see Fig.3).

Separate supply pins are used for the DC-to-DC converter, allowing specific decoupling for counteracting the noise the switching transistors may induce on the supply.

A specific reference supply voltage, V_{DDI}, is used for the interface signals CLKIN1, CLKIN2, I/O1uC, I/O2uC, SAD0, SAD1, SCL, SDA and $\overline{IRQ}$, which can be lower than V_{DD} (minimum 1.5 V), thus allowing direct control with a low voltage supplied device.

Pins SCL, SDA and $\overline{IRQ}$ are open-drain outputs, and may be externally pulled up to a voltage higher than V_{DD}.

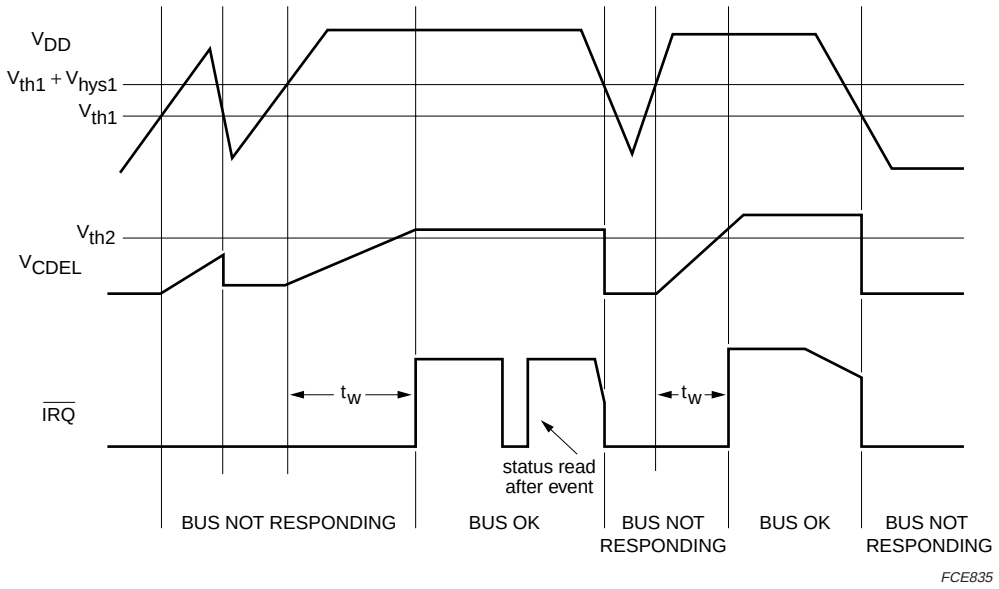


Fig.3 Voltage supervisor.

DC-to-DC converter

V_{CC1} is the supply voltage for card 1 contacts and V_{CC2} is the supply voltage for card 2 contacts. Card 1 and card 2 may be independently powered-down, powered at 5 V or powered at 3 V. A capacitor type step-up converter is used for generating these voltages. This step-up converter acts either as a doubler, tripler or follower. An hysteresis of 100 mV is present on the different threshold voltages.

If V_{CC} is the maximum value of V_{CC1} and V_{CC2}, then there are 5 possible situations:

- $V_{DD} < 3.4$ V and $V_{CC} = 3$ V: in this case, the DC-to-DC converter acts as a doubler with a regulation of approximately 4.0 V
- $V_{DD} < 3.4$ V and $V_{CC} = 5$ V: in this case, the DC-to-DC converter acts as a tripler with a regulation of approximately 5.5 V
- $V_{DD} > 3.5$ V and $V_{CC} = 3$ V: in this case, the DC-to-DC converter acts as a follower: V_{DD} is applied on V_{UP}
- $5.8 \text{ V} > V_{DD} > 3.5$ V and $V_{CC} = 5$ V: in this case, the DC-to-DC converter acts as a doubler with a regulation of approximately 5.5 V
- $V_{DD} > 5.9$ V and $V_{CC} = 5$ V: in this case, the DC-to-DC converter acts as a follower and V_{DD} is applied on V_{UP}.

The output voltage, V_{UP}, is fed internally to the V_{CC} generators. V_{CC1}, V_{CC2} and CGND1, CGND2 are used as a reference for all other cards contacts.

The sum of I_{CC1} and I_{CC2} shall not exceed 80 mA, which means that when a card is drawing its maximum current (around 60 mA at $V_{CC} = 5$ V, 55 mA at $V_{CC} = 3$ V), the other card should be set in low power consumption mode (less than 20 or 25 mA). Note that during the card Advice to Receive (ATR) process, the current may be maximum; so, a card should only be activated if the other card draws less than 20 or 25 mA. The DC-to-DC converter is supplied via separate supply pins V_{DDA} and AGND to allow decoupling separate from the other supply pins.

During normal operation or activation, each card is allowed to draw independently a current of up to 60 mA at $V_{CC} = 5$ V or up to 55 mA at $V_{CC} = 3$ V, with a supply voltage from 2.7 V up to 6.5 V provided the sum of I_{CC1} and I_{CC2} does not exceed 80 mA.

If $V_{DD} > 3$ V, for 5 V cards, then both cards can draw up to 60 mA at the same time.

If $V_{DD} > 3$ V, for 3 V cards, then both cards can draw up to 55 mA at the same time.

I²C-bus

A 400 kHz I²C-bus slave interface is used for configuring the device and reading the status.

I²C-BUS PROTOCOL

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The serial bus consists of two bidirectional lines; one for data (SDA), and one for the clock (SCL).

Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

BUS CONDITIONS

The following bus conditions have been defined:

- Bus not busy: both data and clock lines remain HIGH
- Start data transfer: a change in the state of the data line, from HIGH-to-LOW, while the clock is HIGH, defines the START condition
- Stop data transfer: a change in the state of the data line, from LOW-to-HIGH, while the clock is HIGH, defines the STOP condition
- Data valid: the state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per data bit.

DATA TRANSFER

Each data transfer is initiated with a START condition and terminated with a STOP condition.

Data transfer is unlimited in the read mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

The TDA8020HL operates in standard mode (100 kHz clock rate) and fast mode (400 kHz clock rate) defined in the I²C-bus specification.

By definition, a device that sends a signal is called a transmitter, and the device which receives the signal is called a receiver. The device which controls the signal is

called the master. The devices that are controlled by the master are called slaves.

Each byte is followed by one HIGH-level acknowledge bit asserted by the transmitter. The master generates an extra acknowledge related clock pulse. The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.

The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull-down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse.

Set-up and hold times must be taken into account.
A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master generation of the STOP condition.

See Chapter “Characteristics” for timing information.

DEVICE ADDRESSING

Each device has 2 different addresses, one for each card.

An application can use up to four devices in parallel by the use of address selection pins SAD0 and SAD1.
Pins SAD0 and SAD1 are externally hardwired to V_{DD} or GND; SAD0 specifies address bit A0, SAD1 specifies address bit A1; Address bit R/$\overline{W}$ specifies either read or write operation: logic 1 = Read, logic 0 = Write (see Tables 1 and 2).

Table 1 Proposed device address bit allocations

Device	Address bits							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDA8020HL	0	1	0	0	0/1	A1	A0	R/$\overline{W}$

Table 2 Proposed I^2C-bus addresses for 4 devices in parallel

PIN SAD1	PIN SAD0	CARD 1	CARD 2
LOW	LOW	40H	48H
LOW	HIGH	42H	4AH
HIGH	LOW	44H	4CH
HIGH	HIGH	46H	4EH

WRITE SEQUENCE

The write sequence is as follows:

1. START condition
2. Byte 1: ADDRESS plus write command
3. ACK: acknowledge
4. Byte 2: CONTROL byte; see Table 3
5. ACK: acknowledge
6. STOP condition.

Table 3 CONTROL byte bits (all bits cleared after power-on)

BIT	NAME	DESCRIPTION
0	START/$\overline{\text{STOP}}$	when set, initiates an activation and a cold reset procedure; when reset, initiates a deactivation sequence
1	WARM	when set, initiates a warm reset procedure; automatically reset by hardware when the card starts answering or when the card is declared mute (once the status has been read)
2	3 V / $\overline{5\ \text{V}}$	when set; V_{CC} = 3 V; when reset; V_{CC} = 5 V
3	PDOWN	when set, the configuration defined by bit CLKPD is applied to pin CLK, and the circuit enters the Power-down mode; when reset, the circuit goes back to normal (active) mode
4	CLKPD	when set, CLK is stopped HIGH during Power-down mode; when reset, CLK is stopped LOW in Power-down mode
5	CLKSEL1	determine the clock to the card in active mode:
6	CLKSEL2	00: CLKIN/8 01: CLKIN/4 10: CLKIN/2 11: CLKIN
7	I/OEN	when set, I/O data is transferred on pin I/OuC; when reset, pin I/OuC is high-impedance

All frequency changes are synchronous, thus ensuring that no pulse is shorter than 45% of the smallest period. For cards power reduction modes, CLKIN may be stopped after switching to stop LOW or stop HIGH. CLKIN should be restarted before leaving this mode and the selected frequency must not be changed during a CLK stop mode.

A correct duty factor can not be guaranteed in the CLKIN configuration, as it depends on the duty factor of the CLKIN signal.

READ STATUS SEQUENCE

The read status sequence is as follows:

1. START condition
2. Byte 1: ADDRESS plus read command
3. ACK: acknowledge
4. Byte 2: STATUS byte; see Table 4
5. ACK: acknowledge
6. STOP condition.

Table 4 STATUS byte bits (all bits cleared after power-on)

BIT	NAME	DESCRIPTION
0	PRES	set when the card is present; reset when the card is not present
1	PRESL	set when the card has been inserted or extracted; reset when the status has been read
2	I/O	set when I/O is HIGH; reset when I/O is LOW
3	SUPL	set when the supervisor has signalled a fault; reset when the status has been read
4	PROT	set when an overload or an overheating has occurred during a session; reset when the status has been read
5	MUTE	set during ATR when the selected card has not answered during the ISO 7816 time slots; reset when the status has been read
6	EARLY	set during ATR when the selected card has answered too early; reset when the status has been read
7	ACTIVE	set if the card is active; reset if the card is inactive

When one of the bits PRESL, MUTE, EARLY and PROT is set, then $\overline{IRQ}$ goes LOW until the status byte has been read. After power-on, bit SUPL is set until the status byte has been read, and $\overline{IRQ}$ is LOW until the supervisor becomes inactive.

Sequencers and clock counter

Two sequencers are used to ensure activation and deactivation sequences according to ISO 7816 and EMV 2000, even in the event of an emergency (card removal during transaction, supply drop-out and hardware problem).

The sequencers are clocked by the internal oscillator.

The activation of a card is initiated by setting the card select bit and the start bit within the control register. This is only possible if the card is present and if the voltage supervisor is not active.

During activation the DC-to-DC converter is initiated (except if another card is already powered up or if V_{DD} = 5 V and V_{CC} = 3 V). V_{CC} then goes high to the selected voltage (3 or 5 V), the I/O lines are then enabled and the clock is started with RST LOW.

DEVICE TYPE TDA8020HL/C1:

1. If a start bit is detected on the I/O during the first 200 CLK pulses, it is ignored and the count continues.
2. If a start bit is detected between 200 and 352 CLK pulses, bit EARLY is set in the status register.
3. If the card starts responding within 41950 CLK pulses, RST remains LOW.
4. If the card has not responded within 41950 CLK pulses, then RST goes HIGH.
5. If a start bit is detected within 352 CLK pulses, bit EARLY is set in the status register.
6. If the card does not respond within the next 41950 CLK pulses, bit MUTE is set within the status register. This initiates a warm reset command.
7. If the card responds within the correct window period, the CLK count is stopped and the system controller may send commands to the card.

Deactivation is initiated either by the system controller (reset bit START), or automatically in the event of a hardware problem or supply drop-out. With a supply drop-out both cards are deactivated at the same time.

During deactivation, RST goes LOW, the clock is stopped and the I/O lines go LOW. V_{CC} then goes low with a controlled slope and the DC-to-DC converter is stopped if no card is active.

Outside a session, cards contacts are forced low impedance to CGND.

DEVICE TYPE TDA8020HL/C2:

1. If a start bit is detected on the I/O during the first 200 CLK pulses, it is ignored and the count continues.
2. If a start bit is detected whilst RST is LOW (between 200 and 42100 CLK pulses), bits EARLY and MUTE are set in the status register; RST will remain LOW; the software decides whether to accept the card or not.
3. If no start bit has been detected until after 42100 CLK pulses, RST is set to logic 1.
4. If a start bit is detected within 370 CLK pulses, bit EARLY is set in the status register.
5. If the card does not respond within the next 42100 CLK pulses, bit MUTE is set within the status register. This initiates a warm reset command.
6. If the card responds within the correct window period, the CLK count is stopped and the system controller may send commands to the card.

Deactivation is initiated either by the system controller (reset bit START), or automatically in the event of a hardware problem or supply drop-out. With a supply drop-out both cards are deactivated at the same time.

During deactivation, RST goes LOW, the clock is stopped and the I/O lines go LOW. V_{CC} then goes low with a controlled slope and the DC-to-DC converter is stopped if no card is active.

Outside a session, cards contacts are forced low impedance to CGND.

Activation sequence

When the cards are inactive, V_{CC}, CLK, RST and I/O are LOW, with low impedance with respect to CGND. The DC-to-DC converter is stopped.

When everything is satisfactory (voltage supply, card present and no hardware problems), the system controller may initiate a card present activation sequence (see Fig.4):

1. The internal oscillator changes to its high frequency (t0).
2. The DC-to-DC converter is started (t1). If one card was already active, then the DC-to-DC converter was already on, and nothing more occurs at this step.
3. V_{CC} starts rising from 0 to 5 or 3 V with a controlled rise time of 0.14 V/µs typical (t2).
4. I/O rises to V_{CC} (t3); internal 14 kΩ pull-up resistors to V_{CC}.
5. CLK is sent to the card and RST is enabled ($t4 = t_{act}$).

If the card does not respond within the first 42100 CLK cycles, then RST is raised HIGH (t5).

The sequencer is clocked by $f_{int}/64$ which leads to a time interval T of 25 µs typical. Thus t1 = 0 to T/64; t2 = t1 + 3T/2; t3 = t1 + 7T/2 and t4 = t1 + 4T.

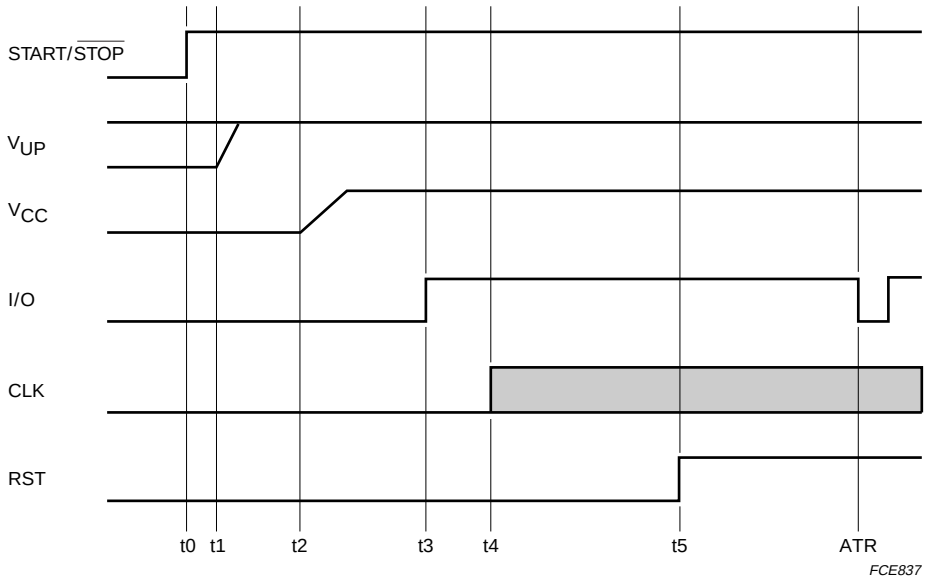


Fig.4 Activation sequence.

Deactivation sequence

When the session is completed, the microcontroller resets bit START/$\overline{\text{STOP}}$ to logic 0 (t10). The circuit then executes an automatic deactivation sequence (see Fig.5):

1. Card reset (RST falls LOW) (t11)
2. Clock is stopped (t12)
3. I/O falls to 0 V (t13)
4. V_{CC} falls to 0 V with a controlled slew rate (t14)
5. The DC-to-DC converter is stopped (if both cards are inactive) and CLK, RST, V_{CC} and I/O become low impedance to CGND (t15)
6. The internal oscillator changes to its low frequency if both cards are inactive (t15).

t11 = t10 + T/64; t12 = t11 + T/2; t13 = t11 + T; t14 = t11 + 3T/2; t15 = t11 + 7T/2.

The deactivation time t_{de} is the time that V_{CC} needs to drop below 0.4 V from START/$\overline{\text{STOP}}$ to logic 0 (t10).

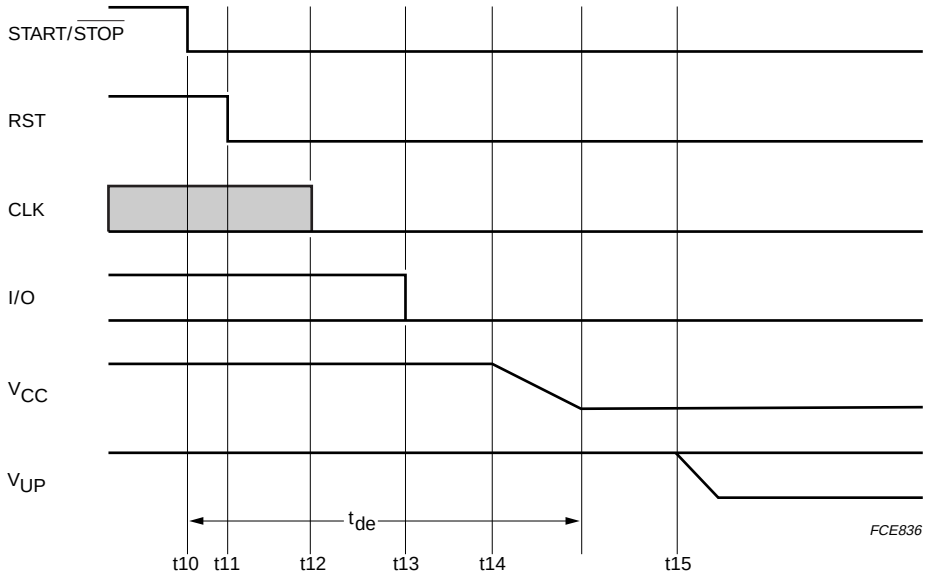


Fig.5 Deactivation sequence.

V_{CC} buffers

Each card is supplied by a separate V_{CC} buffer. Both buffers are supplied by the same multimode capacitive DC-to-DC converter.

In all modes (follower, doubler and tripler), the DC-to-DC converter is able to deliver 80 mA over the whole V_{DD} range (2.7 to 6.5 V) or 120 mA if V_{DD} > 3 V.

The current in each V_{CC} buffer is limited internally to around 90 mA. When one of the buffers reaches this limit, an automatic deactivation sequence is performed.

Each V_{CC} supply voltage should be decoupled by an ESR capacitor with a value of between 100 and 200 nF. If the card socket is not very close to the device, one capacitor should be connected close to the device, and a second one connected close to card contact C1.

Protections

The current on pin CLK is limited to within the range +70 mA and −70 mA.

The current on pin RST is limited to within the range +20 mA and −20 mA; if the current reaches this value with RST LOW, then an emergency deactivation sequence is performed, $\overline{IRQ}$ is pulled LOW and bit PROT is set in the status register.

The current on pins I/O is limited to within the range +15 mA and −15 mA.

The current on V_{CC} is limited to 90 mA; if I_{CC} reaches this value, then an emergency deactivation sequence is performed, $\overline{IRQ}$ is pulled LOW and bit PROT is set in the status register.

In the event of overcurrent on V_{CC}, card take-off during a session, overheating, or overcurrent on RST, then the TDA8020HL performs an automatic emergency deactivation sequence on the corresponding card, resets bit START/$\overline{STOP}$ and pulls pin $\overline{IRQ}$ LOW.

In the event of overheating or supply drop-out, or DC-to-DC converter out of specification, the TDA8020HL performs an automatic emergency deactivation sequence on both cards, resets both bits START/$\overline{STOP}$ and pulls pin $\overline{IRQ}$ LOW.

Clock inputs and data inputs/outputs to the system controller

CLKIN1 is the input clock for card 1, CLKIN2 for card 2. They may be driven separately from the system controller, or be tied together externally and driven by the same signal.

I/O1uC is the data signal to or from card 1, I/O2uC to or from card 2. They can be driven separately from the system controller, in which case both bits I/OEN may be set to logic 1. They can also be driven by the same signal, which requires them to be tied together externally, but each bit I/OEN has to be set or reset according to the addressed card.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
V_{DD}	supply voltage on pins V_{DD} and V_{DDA}		–0.5	+6.5	V
V_{DDI}	supply voltage for interface signals		–0.5	+6.5	V
V_n	input voltage				
	on pins SAP, SAM, SBP, SBM and V_{UP}		–0.5	+7.5	V
	on pins SDA and SCL		–0.5	+6.5	V
	on all other pins		–0.5	V_{DD} + 0.5	V
P_{tot}	total power dissipation	T_{amb} = –40 °C to +85 °C	–	500	mW
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–	125	°C
V_{esd}	electrostatic discharge voltage	HMB; note 1			
		all card contact pins within the typical application; note 2	–6	+6	kV
		pins V_{DDA} and V_{DDI}	–0.5	+0.5	kV
		all other pins	–2	+2	kV
		MM; note 3			
		all pins	–200	+200	V

Notes

1. HBM: EIA/JESD22-A 114-B; June 2000.
2. All card contacts are protected against any short-circuit with any other card contact.
3. MM: EIA/JESD22-A 115-A; October 1997.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	80	K/W

CHARACTERISTICS

V_{DD} = 3.3 V; V_{DDI} = 1.5 V; f_{CLKIN1} = f_{CLKIN2} = 10 MHz; GND = 0 V; T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Temperature						
T_{amb}	ambient temperature	TDA8020HL/C1	–30	–	+85	°C
		TDA8020HL/C2	–40	–	+85	°C
Supply						
V_{DD}	supply voltage on pins V_{DD} and V_{DDA}		2.7	–	6.5	V
I_{DD}	supply current (I_{DD} and I_{DDA})	inactive mode	–	–	150	µA
		Power-down mode; 2 cards activated; V_{CC1} = V_{CC2} = 5 V; I_{CC1} = I_{CC2} = 100 µA; CLK1 and CLK2 stopped	–	–	2.5	mA
		active mode; V_{CC1} = V_{CC2} = 5 V; I_{CC1} + I_{CC2} = 80 mA; CLK1 = CLK2 = 5 MHz	–	–	300	mA
		active mode; V_{CC1} = V_{CC2} = 3 V; I_{CC1} = I_{CC2} = 10 mA; CLK1 = CLK2 = 5 MHz	–	–	80	mA
V_{DDI}	supply voltage for interface signals		1.5	–	V_{DD}	V
I_{DDI}	supply current for interface signals		–	–	120	µA
V_{th1}	threshold voltage for supervisor on V_{DD}	falling	2.1	–	2.4	V
V_{hys1}	hysteresis on V_{th1}		50	–	100	mV
V_{th2}	threshold voltage on pin C_{DEL}		–	1.38	–	V
V_{CDEL}	voltage on pin C_{DEL}		–	–	V_{DD} + 0.3	V
I_{CDEL}	output current at pin C_{DEL}	pin grounded (charge)	–	–2	–	µA
		V_{CDEL} = V_{DD} (discharge)	–	5	–	mA
t_W	width of the internal ALARM pulse	C_{CDEL} = 22 nF	–	10	–	ms
DC-to-DC converter						
f_{int}	internal oscillator frequency		2	2.5	3.2	MHz
V_{UP}	voltage on pin V_{UP}	at least one 5 V card	–	5.5	–	V
		both 3 V cards	–	4	–	V
V_{dt}	detection voltage for doubler, tripler and follower selection		–	3.4	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Card supply voltages (pins V_{CC1} and V_{CC2}); note 1						
$V_{CC(inactive)}$	output voltage in inactive mode	no load	0	–	0.1	V
		$I_{inactive}$ = 1 mA	0	–	0.3	V
$I_{CC(inactive)}$	output current from V_{CC} when inactive	pin grounded	–	–	–1	mA
$V_{CC(active)}$	output voltage in active mode including ripple	I_{CC} < 60 mA; 5 V card; $I_{CC1} + I_{CC2}$ < 80 mA; 2.7 V < V_{DD} < 6.5 V	4.75	5	5.25	V
		I_{CC} < 55 mA; 3 V card; $I_{CC1} + I_{CC2}$ < 80 mA; 2.7 V < V_{DD} < 6.5 V	2.8	3	3.2	V
		current pulses of 40 nAs with I < 200 mA and t < 400 ns; f < 20 MHz; 5 V card	4.6	–	5.4	V
		current pulses of 24 nAs with I < 200 mA and t < 400 ns; f < 20 MHz; 3 V card	2.76	–	3.24	V
$V_{CC(load)}$	output voltage when both card interfaces fully loaded	active mode; V_{DD} > 3 V; I_{CC1} < 60 mA; I_{CC2} < 60 mA; 5 V cards	4.6	–	5.4	V
		active mode; V_{DD} > 3 V; I_{CC} < 55 mA; I_{CC2} < 55 mA; 3 V cards	2.76	–	3.24	V
$I_{CC(max)}$	maximum output current	from 0 to 5 V (5 V card); the other card at full load; V_{DD} > 3 V	–	–	–60	mA
		from 0 to 3 V (3 V card); the other card at full load; V_{DD} > 3 V	–	–	–55	mA
$I_{CC(sc)}$	short-circuit current	V_{CC} shorted to GND	–	–	–100	mA
$V_{ripple(p-p)}$	ripple voltage (peak-to-peak value)	from 20 kHz to 200 MHz	–	–	350	mV
SR	slew rate	up or down for 5 V card (maximum capacitance is 300 nF)	0.08	0.14	0.20	V/µs
		up or down for 3 V card (maximum capacitance is 300 nF)	0.05	0.09	0.13	V/µs
Reset output to the cards (pins RST1 and RST2)						
$V_{o(inactive)}$	output voltage in inactive mode	no load	0	–	0.1	V
		$I_{inactive}$ = 1 mA	0	–	0.3	V
$I_{o(inactive)}$	output current from pin RST when inactive	pin grounded	0	–	–1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 200 µA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} < –200 µA	V_{CC} – 0.5	–	V_{CC}	V
t_r	rise time	C_L = 30 pF	–	–	0.1	µs
t_f	fall time	C_L = 30 pF	–	–	0.1	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock output to the cards (pins CLK1 and CLK2)						
$V_{o(inactive)}$	output voltage in inactive mode	no load	0	–	0.1	V
		$I_{inactive}$ = 1 mA	0	–	0.3	V
$I_{o(inactive)}$	output current from pin CLK when inactive	pin grounded	0	–	–1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 200 μA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} < –200 μA	V_{CC} – 0.5	–	V_{CC}	V
t_r	rise time	C_L = 30 pF	–	–	8	ns
t_f	fall time	C_L = 30 pF	–	–	8	ns
f_{clk}	clock frequency	operational	0	–	10	MHz
δ	duty factor	C_L = 30 pF	45	–	55	%
SR	slew rate (rise and fall)	C_L = 30 pF	0.2	–	–	V/ns
Data lines (pins I/O1 and I/O2); note 2						
$V_{o(inactive)}$	output voltage in inactive mode	no load	0	–	0.1	V
		$I_{inactive}$ = 1 mA	–	–	0.3	V
$I_{o(inactive)}$	current from pin I/O when inactive	pin grounded	–	–	–1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	no DC load	$0.9V_{CC}$	–	V_{CC} + 0.1	V
		I_{OH} < –20 μA	$0.8V_{CC}$	–	V_{CC} + 0.1	V
		I_{OH} < –40 μA	$0.75V_{CC}$	–	V_{CC} + 0.1	V
I_{edge}	current from pins I/O1 and I/O2 when active pull-up	V_{OH} = 0.9 V_{CC}; C_L = 30 pF	–1	–	–	mA
$t_{d(edge)}$	delay between falling edge on pins I/O1, I/O2 and width of active pull-up pulse		–	500	650	ns
V_{IL}	LOW-level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH-level input voltage		1.5	–	V_{CC}	V
I_{IL}	LOW-level input current on pin I/O	V_{IL} = 0; V_{CC} = 5 V	–	–	600	μA
		V_{IL} = 0; V_{CC} = 3 V	–	–	500	μA
I_{LIH}	HIGH-level input leakage current on pin I/O	V_{IH} = V_{CC}	–	–	10	μA
$t_{i(r)}$, $t_{i(f)}$	input transition times	from $V_{IL(max)}$ to $V_{IH(min)}$	–	–	1.5	μs
$t_{o(r)}$, $t_{o(f)}$	output transition times	C_L < 30 pF; no DC load; 10% to 90% from 0 V to V_{CC1} and V_{CC2}	–	–	0.1	μs
C_i	input capacitance on pins I/O1 and I/O2		–	–	10	pF
$R_{pu(int)}$	internal pull-up resistance between pin I/O and V_{CC}		10	14	18	kΩ
f_{max}	maximum frequency on pins I/O1 and I/O2		–	–	500	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data lines (pins I/O1uC and I/O2uC); note 3						
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	–	0.4	V
V_{OH}	HIGH-level output voltage	no DC load	$0.9V_{DDI}$	–	V_{DDI} + 0.2	V
		I_{OH} < −10 µA	$0.75V_{DDI}$	–	V_{DDI} + 0.2	V
V_{IL}	LOW-level input voltage		−0.3	–	$+0.25V_{DDI}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDI}$	–	V_{DDI} + 0.3	V
I_{IL}	LOW-level input current	V_{IL} = 0	–	–	600	µA
I_{LIH}	HIGH-level input leakage current	$V_{IH} = V_{DDI}$	–	–	10	µA
$t_{i(r)}$, $t_{i(f)}$	input transition times	from $V_{IL(max)}$ to $V_{IH(min)}$	–	–	1	µs
$t_{o(r)}$, $t_{o(f)}$	output transition times	C_L < 30 pF; 10% to 90% from 0 V to V_{DDI}	–	–	0.1	µs
$R_{pu(int)}$	internal pull-up resistance	between I/O1uC, I/O2uC and V_{DDI}	7	11	15	kΩ
Timing						
t_{act}	activation sequence duration		–	–	135	µs
t_{de}	deactivation sequence duration		–	–	110	µs
Protections and limitations						
$I_{CC(sd)}$	shutdown and limitation current at V_{CC1} and V_{CC2}	normal mode	–	−90	–	mA
		Power-down mode	–	−12	–	mA
$I_{I/O(lim)}$	limitation current on pins I/O1 and I/O2		−15	–	+15	mA
$I_{CLK(lim)}$	limitation current on pins CLK1 and CLK2		−70	–	+70	mA
$I_{RST(sd)}$	shutdown and limitation current on pins RST1 and RST2		−20	–	+20	mA
$T_{j(sd)}$	shutdown die temperature		–	150	–	°C
Card presence inputs (pins PRES1 and PRES2)						
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	–	V
I_{LIL}	LOW-level input leakage current	V_I = 0 V	–	–	±20	µA
I_{LIH}	HIGH-level input leakage current	$V_I = V_{DD}$	–	–	±20	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock inputs (pins CLKIN1 and CLKIN2)						
f_{ext}	external frequency applied on CLKIN1 and CLKIN2		0	–	25	MHz
V_{IL}	LOW-level input voltage	$V_{DDI} > 2$ V	0	–	$0.3V_{DDI}$	V
		1.5 V < V_{DDI} < 2 V	0	–	$0.15V_{DDI}$	V
V_{IH}	HIGH-level input voltage	$V_{DDI} > 2$ V	$0.7V_{DDI}$	–	V_{DDI} + 0.3	V
		1.5 V < V_{DDI} < 2 V	$0.85V_{DDI}$	–	V_{DDI} + 0.3	V
$t_{i(r)}$, $t_{i(f)}$	input transition times		–	–	$0.1/f_{CLKIN}$	ns
Logic inputs (pins SAD0 and SAD1)						
V_{IL}	LOW-level input voltage		–0.3	–	$+0.3V_{DDI}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDI}$	–	V_{DDI} + 0.3	V
I_{LIL}	LOW-level input leakage current		–	–	±20	µA
I_{LIH}	HIGH-level input leakage current		–	–	±20	µA
C_i	input capacitance		–	–	10	pF
Interrupt line (pin $\overline{IRQ}$; open-drain; active LOW output)						
V_{OL}	LOW-level output voltage	I_o = 2 mA	–	–	0.3	V
I_{LH}	HIGH-level leakage current		–	–	10	µA
Serial data input/output (pin SDA; open-drain)						
V_{IL}	LOW-level input voltage		–0.3	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	6.5	V
I_{LH}	HIGH-level leakage current		–	–	1	µA
I_{IL}	LOW-level input current	depends on the pull-up resistance	–	–	–	
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	–	–	0.3	V
Serial clock input (pin SCL; open-drain)						
V_{IL}	LOW-level input voltage		–0.3	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	6.5	V
I_{LH}	HIGH-level leakage current		–	–	1	µA
I_{IL}	LOW-level input current	depends on the pull-up resistance	–	–	–	
I^2C-bus timings; see Figures 6 and 7						
f_{SCL}	clock frequency		0	–	400	kHz
t_{BUF}	bus free time between a STOP and START condition		1.3	–	–	µs
$t_{HD;STA}$	START condition hold time after which first clock pulse is generated		0.6	–	–	µs
t_{LOW}	SCL LOW time		1.3	–	–	µs
t_{HIGH}	SCL HIGH time		0.6	–	–	µs
$t_{SU;STA}$	set-up time START condition	repeated start	0.6	–	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{HD;DAT}$	data hold time	note 4	0	–	–	ns
$t_{SU;DAT}$	data set-up time		100	–	–	ns
t_r	rise time SDA and SCL		–	–	300	ns
t_f	fall time SDA and SCL		–	–	300	ns
$t_{SU;STO}$	set-up time STOP condition		0.6	–	–	µs

Notes

1. Two ceramic multilayer capacitors of minimum 100 nF with low ESR should be used in order to meet these specifications.
2. Pin I/O1 has an internal 14 kΩ pull-up resistor to V_{CC1} and pin I/O2 has an internal 14 kΩ pull-up resistor to V_{CC2}.
3. Pins I/O1uC and I/O2uC have an internal 11 kΩ pull-up resistor to V_{DDI}.
4. The hold time required (not greater than 300 ns) to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter.

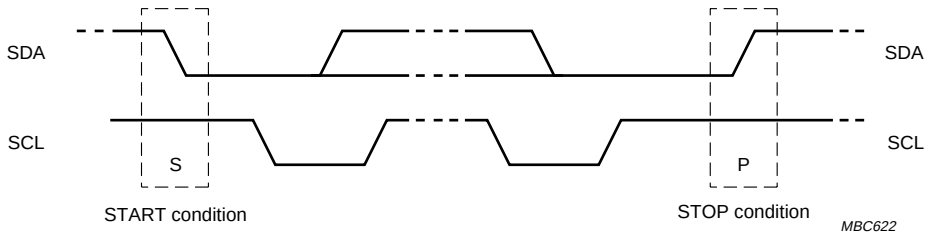


Fig.6 START and STOP conditions.

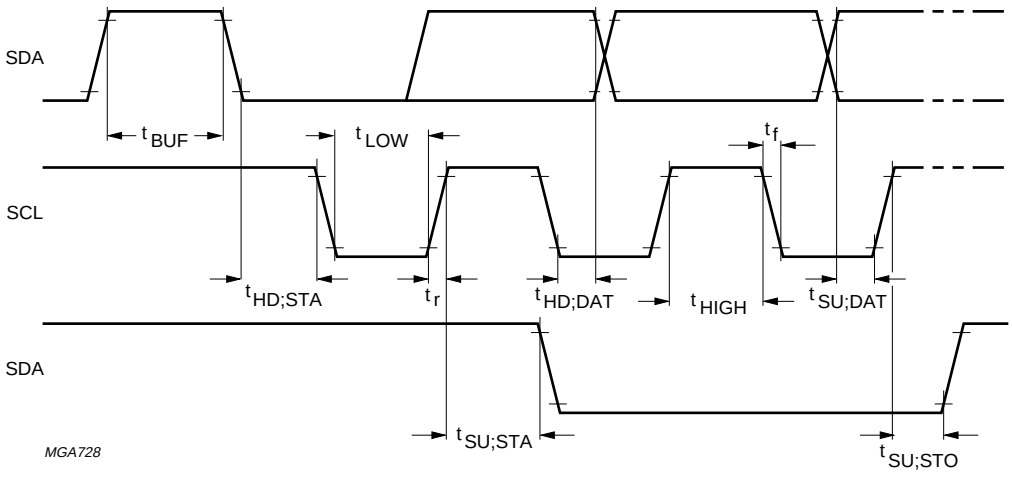


Fig.7 I^2C-bus timing waveforms.

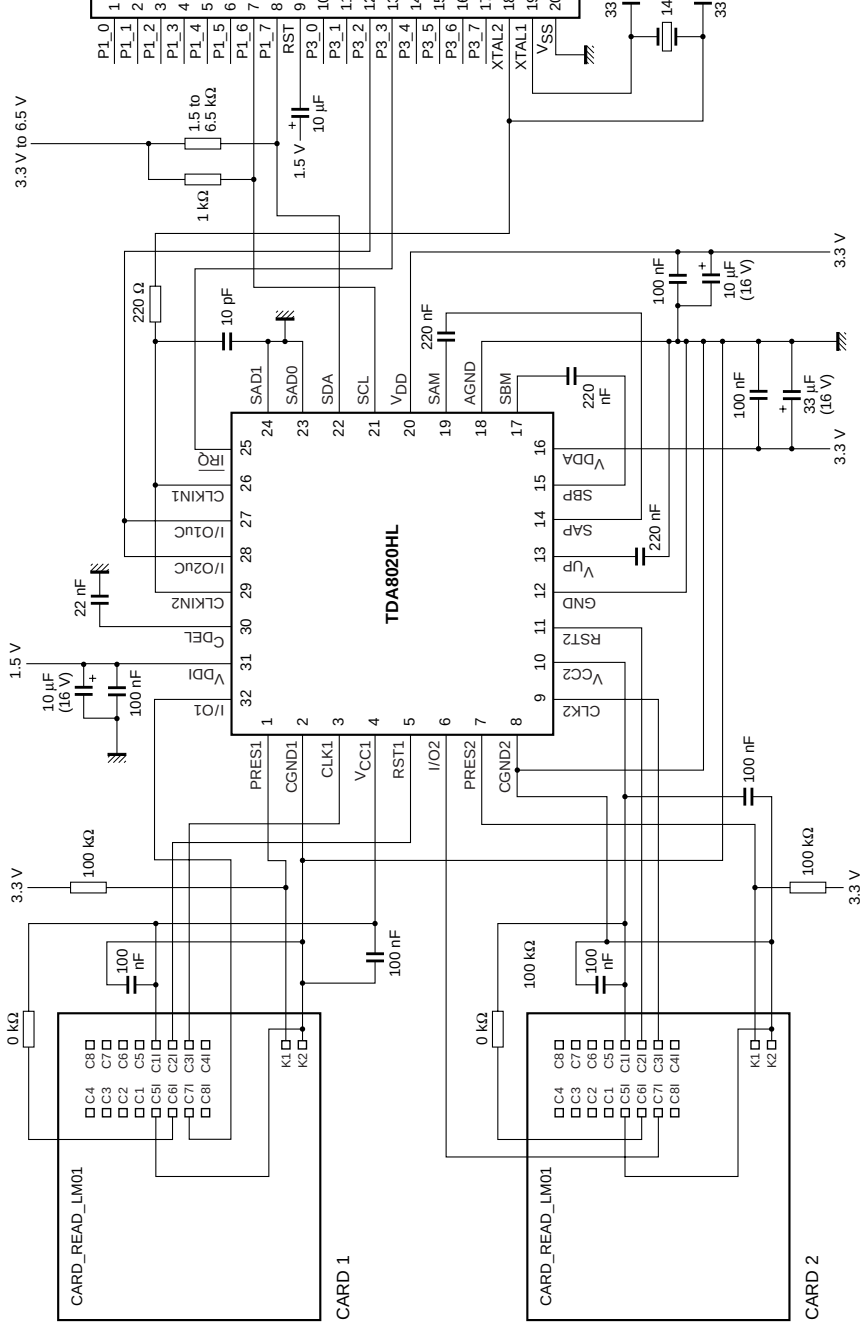
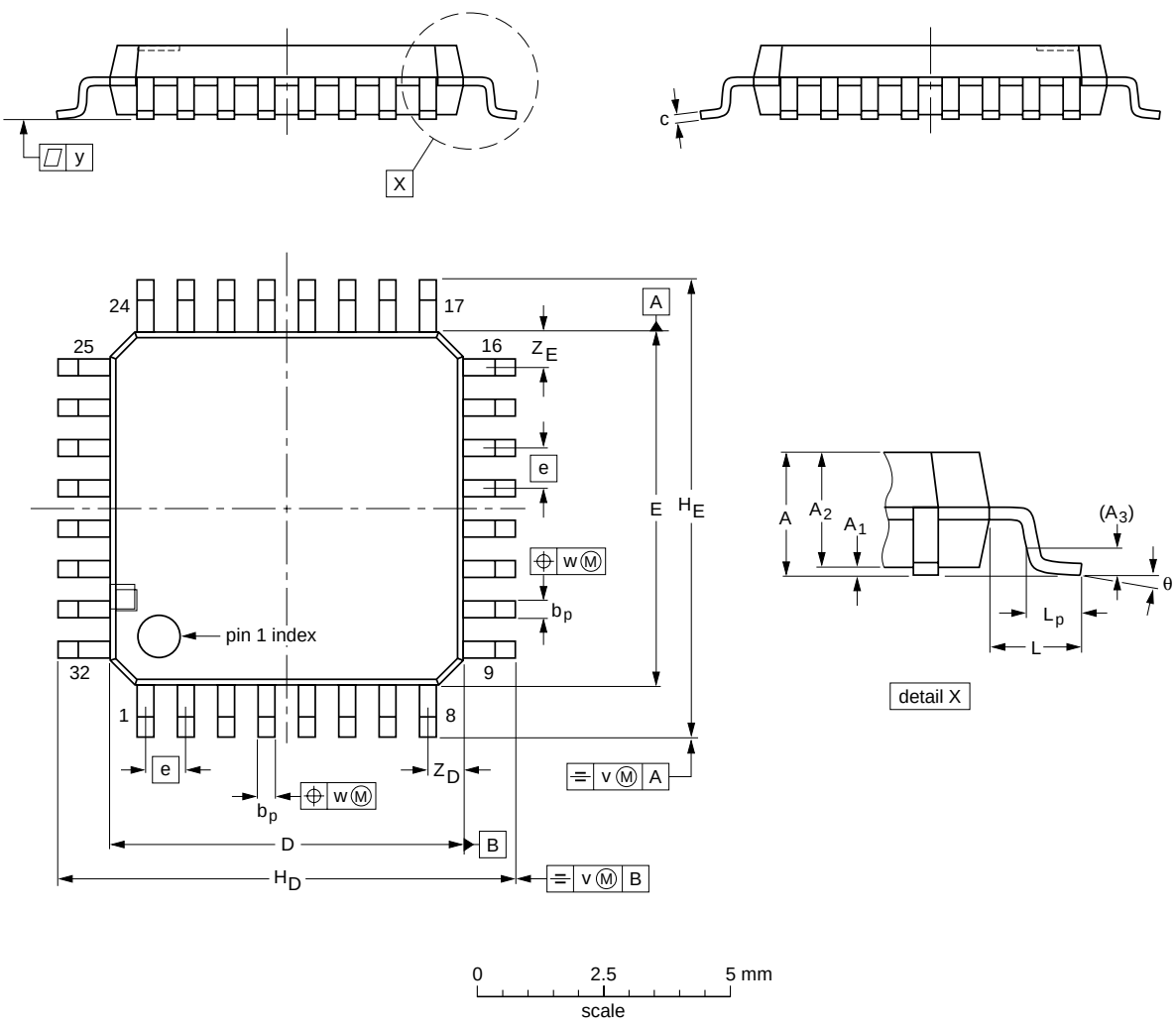


Fig.8 Application diagram.

PACKAGE OUTLINE

LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm **SOT358-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.4 0.3	0.18 0.12	7.1 6.9	7.1 6.9	0.8	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.25	0.1	0.9 0.5	0.9 0.5	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT358 -1	136E03	MS-026				~~00-01-19~~ 03-02-25

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON-T and SSOP-T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, HTSSON-T[3], LBGA, LFBGA, SQFP, SSOP-T[3], TFBGA, USON, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
PMFP[8]	not suitable	not suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
4. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
5. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
6. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
7. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
8. Hot bar or manual soldering is suitable for PMFP packages.

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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