TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7MBL3253CFT, TC7MBL3253CFK

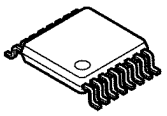
Dual 1-of-4 FET Multiplexer/Demultiplexer

The TC7MBL3253C is a Low Voltage/Low Capacitance CMOS 2bit 1-of-4 Multiplexer/Demultiplexer. The low on-resistance of the switch allows connections to be made with minimal propagation delay time.

This device consists of two individual four-inputs multiplexer/demultiplexer with common select input (S1, S0) and output enable ($\overline{OE}$). The A input is connected to the B1 to B4 outputs as determined by the combination of both the select input (S1, S0) and output enable ($\overline{OE}$). When the output enable ($\overline{OE}$) input is held at “H” level, the switches are open regardless of the state of the select inputs, and a high-impedance state exists between the switches.

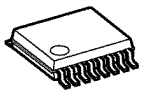
All inputs are equipped with protection circuits against static discharge.

TC7MBL3253CFT



TSSOP16-P-0044-0.65A

TC7MBL3253CFK



VSSOP16-P-0030-0.50

Weight

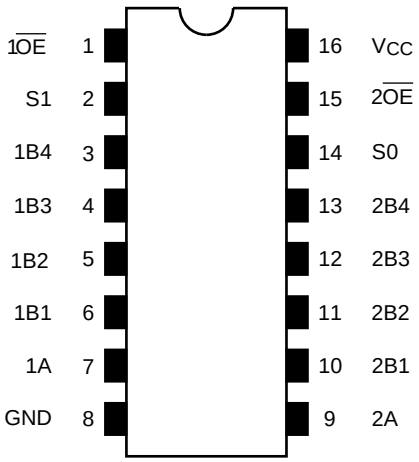
TSSOP16-P-0044-0.65A:	0.06 g (typ.)
VSSOP16-P-0030-0.50:	0.02 g (typ.)

Features

- Operating voltage: V_{CC} = 1.65 to 3.6 V
- On-capacitance: $C_{I/O}$ = 13 pF Switch On (typ.) @ V_{CC} = 3 V
- On-resistance: R_{ON} = 9 Ω (typ.) @ V_{CC} = 3 V, $V_{I/O}$ = 0 V
- ESD performance: Machine model ≥ ±200 V
  Human body model ≥ ±2000 V
- Power-down protection for inputs ($\overline{OE}$, S1, S0 and I/O)
- Package: TSSOP16, VSSOP16 (US16)

Pin Assignment (top view)

FT (TSSOP16-P-0044-0.65A)
FK (VSSOP16-P-0030-0.50)



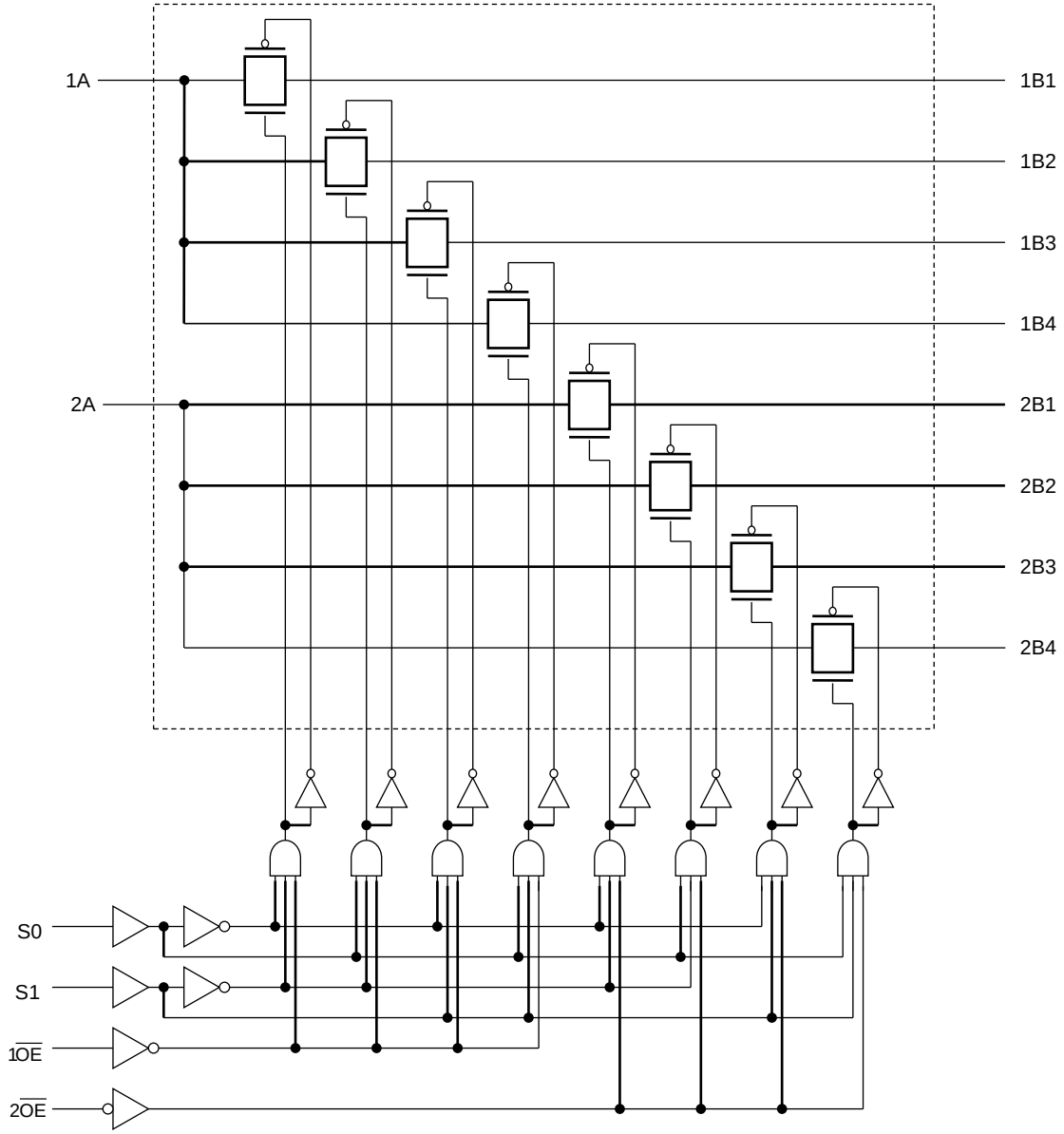
Start of commercial production
2008-06

Truth Table

Inputs			Function
$\overline{OE}$	S1	S0	
L	L	L	A port = B1 port
L	L	H	A port = B2 port
L	H	L	A port = B3 port
L	H	H	A port = B4 port
H	X	X	Disconnect

X: Don’t care

System Diagram



Absolute Maximum Ratings (Note)

Characteristics		Symbol	Rating	Unit
Power supply range		V_{CC}	−0.5 to 4.6	V
Control pin input voltage ($\overline{OE}$, S1, S0)		V_{IN}	-0.5 to 4.6	V
Switch terminal I/O voltage	V_{CC} = 0 V or Switch = Off	V_S	-0.5 to 4.6	V
	Switch = On	V_S	-0.5 to V_{CC}+0.5	
Clamp diode current		I_{IK}	-50	mA
Switch I/O current		I_S	50	mA
Power dissipation		P_D	180	mW
DC V_{CC}/GND current		I_{CC}/I_{GND}	±100	mA
Storage temperature		T_{stg}	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics		Symbol	Rating	Unit
Power supply voltage		V_{CC}	1.65 to 3.6	V
Control pin input voltage ($\overline{OE}$, S1, S0)		V_{IN}	0 to 3.6	V
Switch terminal I/O voltage	V_{CC} = 0 V or Switch = Off	V_S	0 to 3.6	V
	Switch = On	V_S	0 to V_{CC}	
Operating temperature		T_{opr}	-40 to 85	°C
Input rise and fall time		dt/dv	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics (Ta = -40 to 85°C)

Characteristics		Symbol	Test Condition	V_{CC} (V)	Min	Typ.	Max	Unit
Input voltage ($\overline{OE}$, S1, S0)	"H" level	V_{IH}	—	1.65 to 3.6	0.7 × V_{CC}	—	—	V
	"L" level	V_{IL}	—	1.65 to 3.6	—	—	0.3 × V_{CC}	
Input leakage current ($\overline{OE}$, S1, S0)		I_{IN}	V_{IN} = 0 to 3.6 V	1.65 to 3.6	—	—	±1.0	μA
Power-off leakage current		I_{OFF}	$\overline{OE}$, S, A, B = 0 to 3.6 V	0	—	—	10	μA
Off-state leakage current (switch off)		I_{SZ}	A, B = 0 to V_{CC}, $\overline{OE}$ = V_{CC}	1.65 to 3.6	—	—	±1.0	μA
On resistance (Note 1)(Note2)		R_{ON}	V_{IS} = 0 V, I_{IS} = 30 mA	3.0	—	9	13	Ω
			V_{IS} = 3.0 V, I_{IS} = 30 mA	3.0	—	18	24	
			V_{IS} = 2.4 V, I_{IS} = 15 mA	3.0	—	20	28	
			V_{IS} = 0 V, I_{IS} = 24 mA	2.3	—	10	15	
			V_{IS} = 2.3 V, I_{IS} = 24 mA	2.3	—	23	32	
			V_{IS} = 2.0 V, I_{IS} = 15 mA	2.3	—	25	35	
			V_{IS} = 0 V, I_{IS} = 4 mA	1.65	—	12	18	
			V_{IS} = 1.65 V, I_{IS} = 4 mA	1.65	—	29	40	
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND, I_{OUT} = 0 A	3.6	—	—	10	μA

Note1: All typical values are at Ta = 25°C.

Note2: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins

AC Characteristics (Ta = -40 to 85°C)

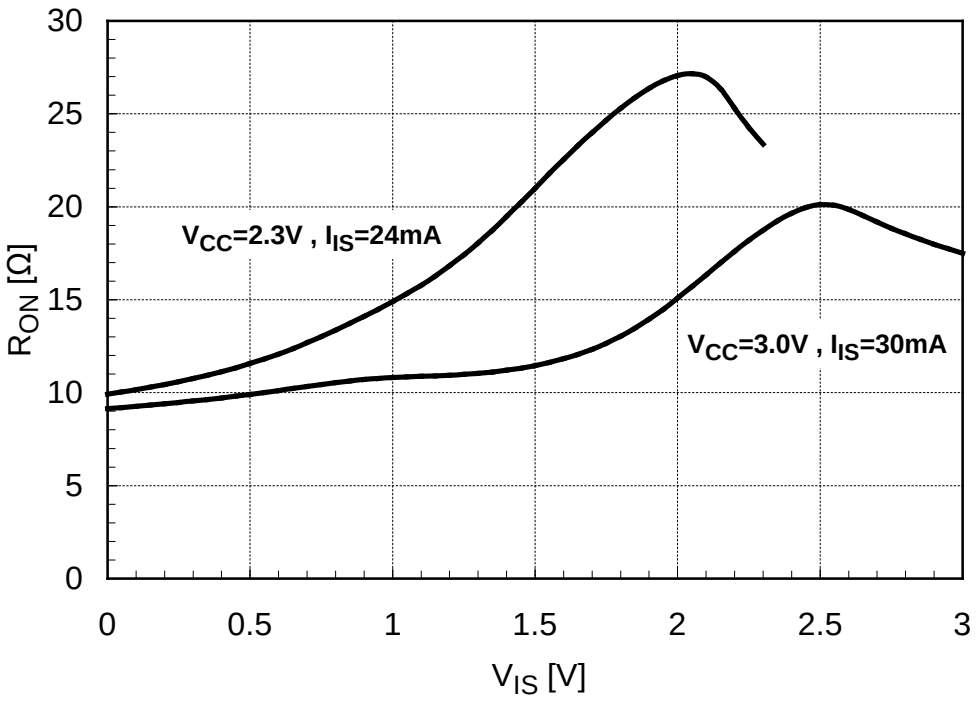
Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit
Output enable time ($\overline{OE}$ to bus)	t_{pZL} t_{pZH}	Figure 1, Figure 2	3.3 ± 0.3	—	6	ns
			2.5 ± 0.2	—	7	
			1.8 ± 0.15	—	11	
Output enable time (S1, S0 to bus)	t_{pZL} t_{pZH}	Figure 1, Figure 2	3.3 ± 0.3	—	6	ns
			2.5 ± 0.2	—	7	
			1.8 ± 0.15	—	11	
Output disable time ($\overline{OE}$ to bus)	t_{pLZ} t_{pHZ}	Figure 1, Figure 2	3.3 ± 0.3	—	6	ns
			2.5 ± 0.2	—	7	
			1.8 ± 0.15	—	11	
Output disable time (S1, S0 to bus)	t_{pLZ} t_{pHZ}	Figure 1, Figure 2	3.3 ± 0.3	—	6	ns
			2.5 ± 0.2	—	7	
			1.8 ± 0.15	—	11	

Capacitive Characteristics (Note) (Ta = 25°C)

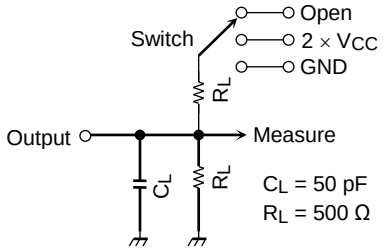
Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Control pin input capacitance ($\overline{OE}$, S1, S0)	C_{IN}	V_{IN} = 0 V	3.0	5	pF
Switch terminal capacitance (Bn) (Switch Off)	$C_{I/O}$	$\overline{OE}$ = V_{CC}, V_{IS} = 0 V	3.0	4	pF
Switch terminal capacitance (A) (Switch Off)	$C_{I/O}$	$\overline{OE}$ = V_{CC}, V_{IS} = 0 V	3.0	9	pF
Switch terminal capacitance (Bn) (Switch On)	$C_{I/O}$	$\overline{OE}$ = GND, V_{IS} = 0 V	3.0	13	pF
Switch terminal capacitance (A) (Switch On)	$C_{I/O}$	$\overline{OE}$ = GND, V_{IS} = 0 V	3.0	13	pF

Note: This parameter is guaranteed by design.

RON - VIS Characteristic (typ.) Ta=25°C



AC Test Circuit



Characteristics	Switch
t_{pLZ}, t_{pZL}	2 × V_{CC}
t_{pHZ}, t_{pZH}	GND

Figure 1 AC Test Circuit

AC Waveform

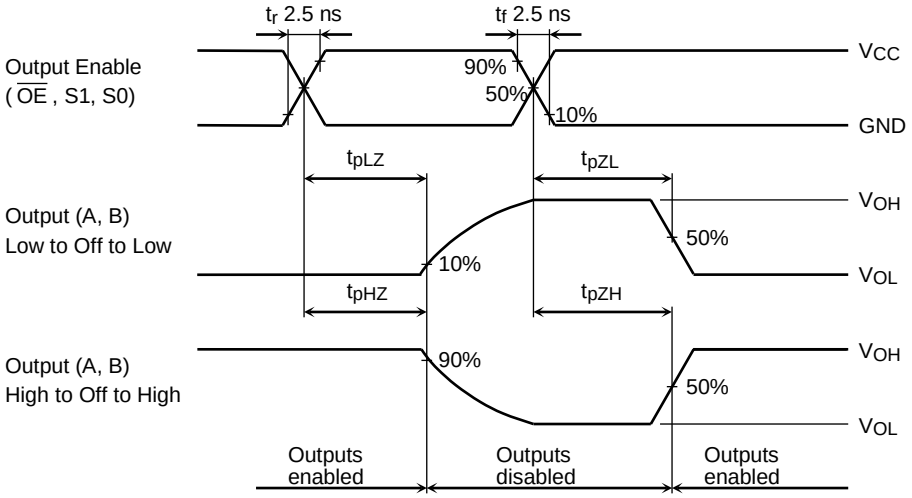


Figure 2 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

Rise and Fall Time (tr / tf) of the TC7MBL3253C I/O Signals

The tr(out) and tf(out) values of the output signals are affected by the CR time constant of the input, which consists of the switch terminal capacitance ($C_{I/O}$) and the on-resistance (R_{ON}) of the input.

In practice, the tr(out) and tf(out) values are also affected by the circuit's capacitance and resistance components other than those of the TC7MBL3253C.

The tr(out) / tf(out) values can be approximated as follows. (Figure 3 shows the test circuit.)

$$tr(out) / tf(out) (approx) = - (C_{I/O} + C_L) \cdot (R_{DRIVE} + R_{ON}) \cdot \ln (((V_{OH} - V_{OL}) - V_M) / (V_{OH} - V_{OL}))$$

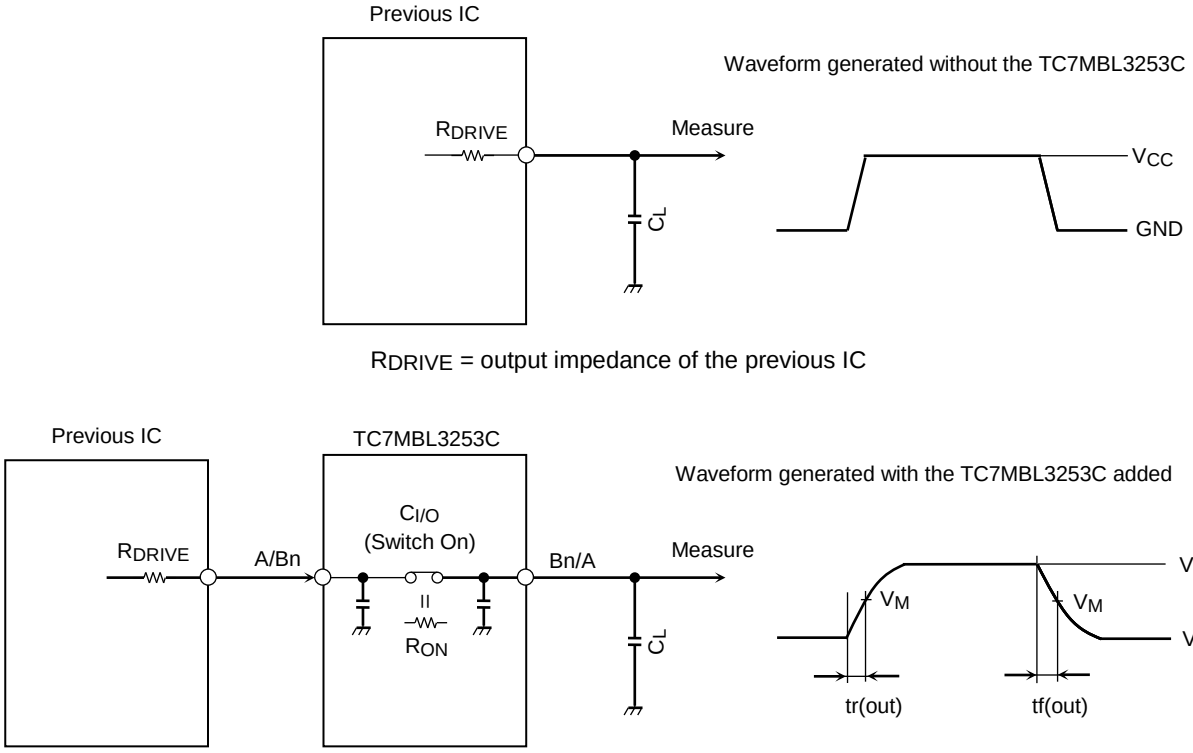
where, R_{DRIVE} is the output impedance of the previous-stage circuit.

Calculation example:

$$tr(out) (approx) = - (13 + 15)E-12 \cdot (120 + 9) \cdot \ln (((3.0 - 0) - 1.5) / (3.0 - 0))$$
$$\approx 2.5 \text{ ns}$$

Calculation conditions:

V_{CC} = 3.0 V, C_L = 15 pF, R_{DRIVE} = 120 Ω (output impedance of the previous IC), V_M = 1.5 V (V_{CC} / 2)
Output of the previous IC = digital (i.e., high-level voltage = V_{CC}; low-level voltage = GND)

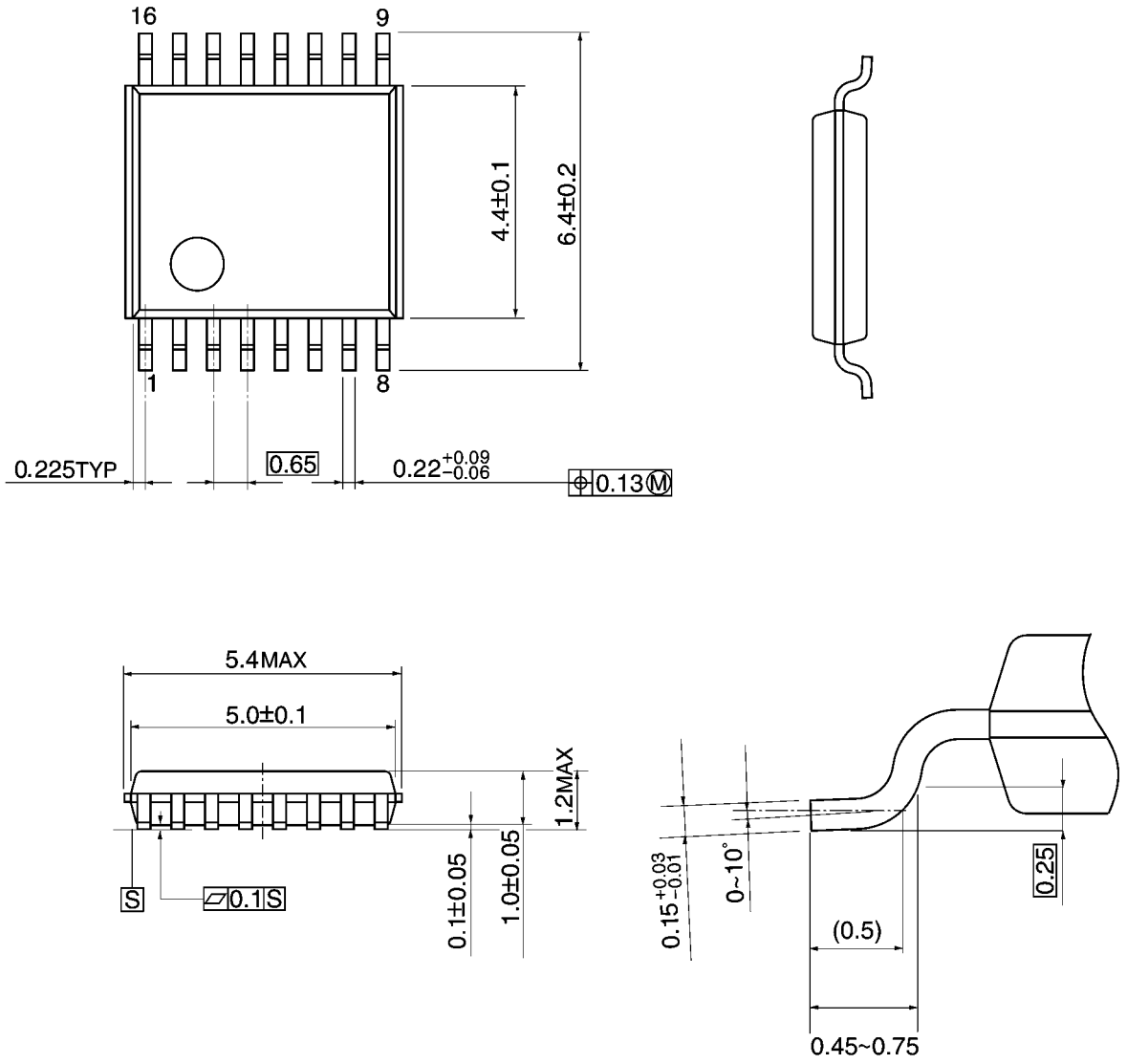


Characteristics	V_{CC}		
	3.3 ± 0.3 V	2.5 ± 0.2 V	1.8 ± 0.15 V
V_M	V_{CC} / 2	V_{CC} / 2	V_{CC} / 2

Figure 3 Test Circuit

Package Dimensions

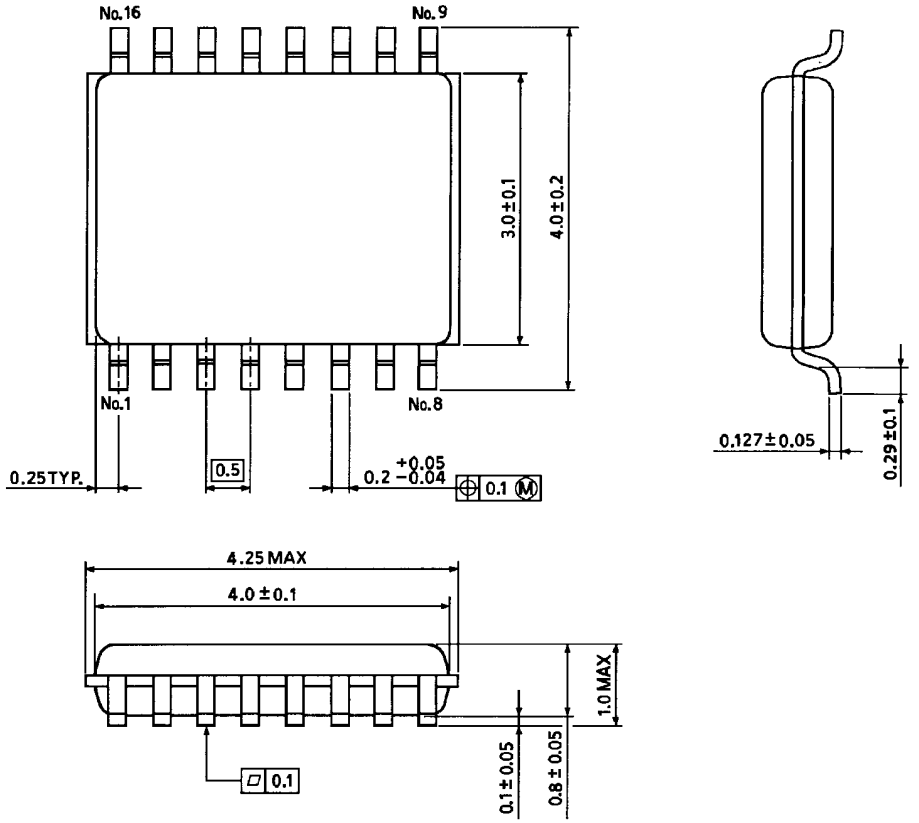
TSSOP16-P-0044-0.65A Unit: mm



Weight: 0.06 g (typ.)

Package Dimensions

VSSOP16-P-0030-0.50 Unit : mm



Weight: 0.02 g (typ.)

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