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74VHCT74A

Dual D-Type Flip-Flop with Preset and Clear

Features

- n High speed: $f_{MAX} = 160\text{MHz}$ (Typ.) at $T_A = 25^\circ\text{C}$
- n High noise immunity: $V_{IH} = 2.0\text{V}$, $V_{IL} = 0.8\text{V}$
- n Power down protection is provided on all inputs and outputs
- n Low power dissipation: $I_{CC} = 2\mu\text{A}$ (Max.) at $T_A = 25^\circ\text{C}$
- n Pin and function compatible with 74HCT74

General Description


The VHCT74A is an advanced high speed CMOS Dual D-Type Flip-Flop fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The signal level applied to the D INPUT is transferred to the Q OUTPUT during the positive going transition of the CK pulse. CLR and PR are independent of the CK and are accomplished by setting the appropriate input LOW.

Protection circuits ensure that 0V to 7V can be applied to the input pins without regard to the supply voltage and to the output pins with $V_{CC} = 0\text{V}$. These circuits prevent device destruction due to mismatched supply and input/output voltages. This device can be used to interface 3V to 5V systems and two supply systems such as battery backup.

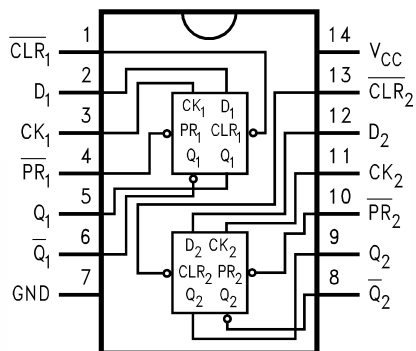
Ordering Information

| Order Number | Package Number | Package Description |
|--------------|----------------|--|
| 74VHCT74AM | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| 74VHCT74ASJ | M14D | 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74VHCT74AMTC | MTC14 | 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |

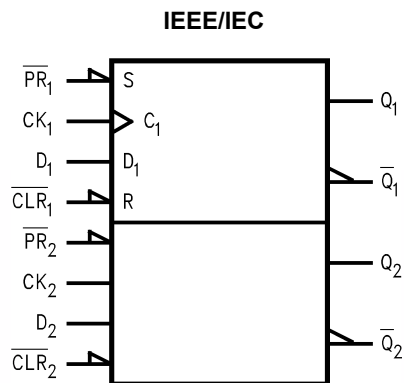
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



Logic Symbol



Pin Description

| Pin Names | Description |
|---|----------------------|
| D ₁ , D ₂ | Data Inputs |
| CK ₁ , CK ₂ | Clock Pulse Inputs |
| CLR ₁ , CLR ₂ | Direct Clear Inputs |
| PR ₁ , PR ₂ | Direct Preset Inputs |
| Q ₁ , Q ₁ [̄] , Q ₂ , Q ₂ [̄] | Outputs |

Truth Table

| Inputs | | | | Outputs | | Function |
|--------|----|---|----|----------------|----------------|-----------|
| CLR | PR | D | CK | Q | Q [̄] | |
| L | H | X | X | L | H | Clear |
| H | L | X | X | H | L | Preset |
| L | L | X | X | H | H | |
| H | H | L | ↗ | L | H | |
| H | H | H | ↘ | H | L | |
| H | H | X | ~ | Q _n | Q _n | No Change |

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Rating |
|-----------|--|---|
| V_{CC} | Supply Voltage | -0.5V to +7.0V |
| V_{IN} | DC Input Voltage | -0.5V to +7.0V |
| V_{OUT} | DC Output Voltage Note 1 Note 2 | -0.5V to $V_{CC} + 0.5V$ -0.5V to 7.0V |
| I_{IK} | Input Diode Current | -20mA |
| I_{OK} | Output Diode Current ⁽³⁾ | $\pm 20mA$ |
| I_{OUT} | DC Output Current | $\pm 25mA$ |
| I_{CC} | DC V_{CC} /GND Current | $\pm 50mA$ |
| T_{STG} | Storage Temperature | -65°C to +150°C |
| T_L | Lead Temperature (Soldering, 10 seconds) | 260°C |

Recommended Operating Conditions⁽⁴⁾

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Rating |
|------------|--|------------------------------|
| V_{CC} | Supply Voltage | 4.5V to +5.5V |
| V_{IN} | Input Voltage | 0V to +5.5V |
| V_{OUT} | Output Voltage Note 1 Note 2 | 0V to V_{CC} 0V to 5.5V |
| T_{OPR} | Operating Temperature | -40°C to +85°C |
| t_r, t_f | Input Rise and Fall Time $V_{CC} = 5.0V \pm 0.5V$ | 0ns/V ~ 20ns/V |

Notes:

1. HIGH or LOW state. I_{OUT} absolute maximum rating must be observed.
2. $V_{CC} = 0V$.
3. $V_{OUT} < GND$, $V_{OUT} > V_{CC}$ (Outputs Active).
4. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = 25°C | | | T _A = -40°C to +85°C | | Units | |
|--------------------|---|---------------------|---|-------------------------|------|------|---------------------------------|------|-------|----|
| | | | | Min. | Typ. | Max. | Min. | Max. | | |
| V _{IH} | HIGH Level Input Voltage | 4.5 | | 2.0 | | | 2.0 | | V | |
| | | 5.5 | | 2.0 | | | 2.0 | | | |
| V _{IL} | LOW Level Input Voltage | 4.5 | | | | 0.8 | | 0.8 | V | |
| | | 5.5 | | | | 0.8 | | 0.8 | | |
| V _{OH} | HIGH Level Output Voltage | 4.5 | V _{IN} = V _{IH} or V _{IL} | I _{OH} = -50μA | 4.40 | 4.50 | | 4.40 | V | |
| | | 4.5 | | I _{OH} = -8mA | 3.94 | | | 3.80 | | |
| V _{OL} | LOW Level Output Voltage | 4.5 | V _{IN} = V _{IH} or V _{IL} | I _{OL} = 50μA | | 0.0 | 0.1 | | 0.1 | V |
| | | 4.5 | | I _{OL} = 8mA | | | 0.36 | | 0.44 | |
| I _{IN} | Input Leakage Current | 0-5.5 | V _{IN} = 5.5V or GND | | | | ±0.1 | | ±1.0 | μA |
| I _{CC} | Quiescent Supply Current | 5.5 | V _{IN} = V _{CC} or GND | | | | 2.0 | | 20.0 | μA |
| I _{CC(T)} | Maximum I _{CC} /Input | 5.5 | V _{IN} = 3.4V, Other Inputs = V _{CC} or GND | | | | 1.35 | | 1.50 | mA |
| I _{OFF} | Output Leakage Current (Power Down State) | 0.0 | V _{OUT} = 5.5V | | | | +0.5 | | +5.0 | μA |

AC Electrical Characteristics

| Symbol | Parameter | V _{CC} (V) ⁽⁵⁾ | Conditions | T _A = 25°C | | | T _A = -40°C to +85°C | | Units |
|-------------------------------------|---------------------------------------|------------------------------------|------------------------|-----------------------|------|------|---------------------------------|------|-------|
| | | | | Min. | Typ. | Max. | Min. | Max. | |
| f _{MAX} | Maximum Clock Frequency | 5.0 | C _L = 15pF | 100 | 160 | | 80 | | MHz |
| | | 5.0 | C _L = 50pF | 80 | 140 | | 65 | | |
| t _{PLH} , t _{PHL} | Propagation Delay Time (CK-Q, Q) | 5.0 | C _L = 15pF | | 5.8 | 7.8 | 1.0 | 9.0 | ns |
| | | 5.0 | C _L = 50pF | | 6.3 | 8.8 | 1.0 | 10.0 | |
| t _{PLH} , t _{PHL} | Propagation Delay Time (CLR, PR-Q, Q) | 5.0 | C _L = 15pF | | 7.6 | 10.4 | 1.0 | 12.0 | ns |
| | | 5.0 | C _L = 50pF | | 8.1 | 11.4 | 1.0 | 13.0 | |
| C _{IN} | Input Capacitance | | V _{CC} = Open | | 4 | 10 | | 10 | pF |
| C _{PD} | Power Dissipation Capacitance | | ⁽⁶⁾ | | 24 | | | | pF |

Notes:

5. V_{CC} is 5.0 ± 0.5V

6. C_{PD} is defined as the value of internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

$$I_{CC}(\text{Opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2 \text{ (per flip-flop).}$$

AC Operating Requirements

| Symbol | Parameter | V _{CC} (V) | T _A = 25°C | | T _A = -40°C to +85°C | Units |
|---------------------------------------|--|---------------------|-----------------------|--------------------|------------------------------------|-------|
| | | | Typ. | Guaranteed Minimum | | |
| t _{W(L)} , t _{W(H)} | Minimum Pulse Width (CK) | 5.0 ± 0.5 | | 5.0 | 5.0 | ns |
| t _{W(L)} | Minimum Pulse Width ($\overline{\text{CLR}}$, $\overline{\text{PR}}$) | 5.0 ± 0.5 | | 5.0 | 5.0 | ns |
| t _S | Minimum Setup Time | 5.0 ± 0.5 | | 5.0 | 5.0 | ns |
| t _H | Minimum Hold Time | 5.0 ± 0.5 | | 0 | 0 | ns |
| t _{REM} | Minimum Removal Time (CLR, PR) | 5.0 ± 0.5 | | 3.5 | 3.5 | ns |



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 2009.
- E. LANDPATTERN STANDARD: SOP65P640X110-14M.
- F. DRAWING FILE NAME: MKT-MTC14rev7.





NOTES:

- A. CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C
- B. ALL DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
- D. LAND PATTERN STANDARD: SOIC127P600X145-14M
- E. CONFORMS TO ASME Y14.5M, 2009
- D. DRAWING FILENAME: MKT-M14Arev14



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