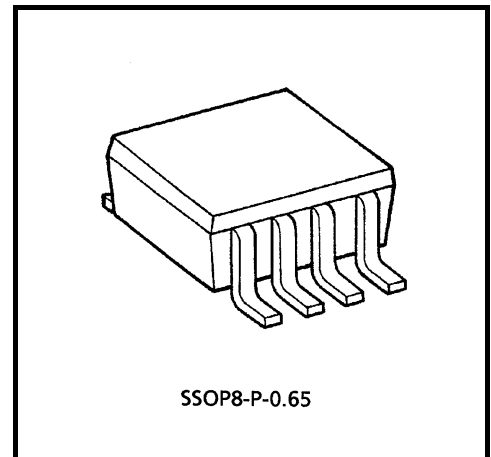


# TA75W01FU

## Dual Operational Amplifier

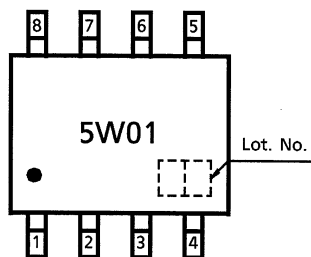
### Features

- In the linear mode the input common mode voltage range includes ground.
- The internally compensated operational amplifier is small package.
- Low power dissipation and power drain suitable for battery operation.
- Differential input voltage range equal to the power supply voltage.
- Large output voltage swing : 0V<sub>DC</sub> to 3.4V<sub>DC</sub> (V<sub>CC</sub> = 5V<sub>DC</sub>)
- Wide power supply voltage range and single power supply is possible.
- Single supply 3V<sub>DC</sub> to 12V<sub>DC</sub> or dual supplies ± 1.5V<sub>DC</sub> to ± 6V<sub>DC</sub>.

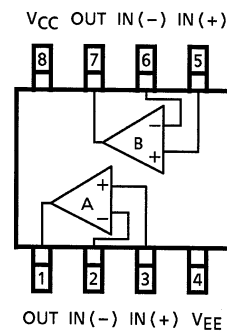


Weight: 0.021g (typ.)

### Marking (Top View)

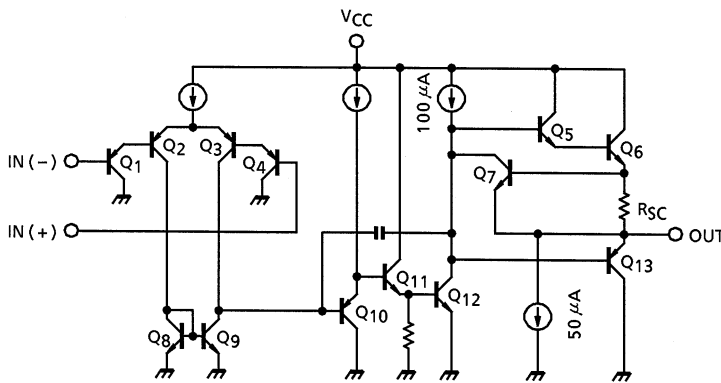


### Pin Connection (Top View)



Start of commercial production  
1991-07

**Equivalent Circuit**



**Absolute Maximum Ratings (Ta = 25°C)**

Characteristic	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub> , V <sub>EE</sub>	±6 or 12	V
Differential input voltage	DV <sub>IN</sub>	±12	V
Input voltage	V <sub>IN</sub>	-0.3 to V <sub>CC</sub>	V
Power dissipation	P <sub>D</sub>	250	mW
Operating temperature	T <sub>opr</sub>	-40 to 85	°C
Storage temperature	T <sub>stg</sub>	-55 to 125	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

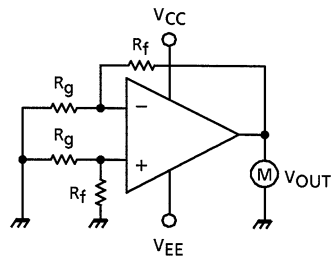
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

**Electrical Characteristics (V<sub>CC</sub> = 5V, V<sub>EE</sub> = GND, Ta = 25°C)**

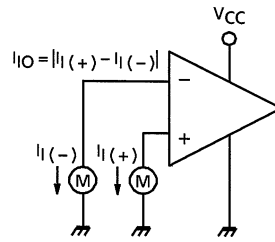
Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input offset voltage	V <sub>IO</sub>	1	R <sub>g</sub> ≤ 10kΩ	—	2	7	mV
Input offset current	I <sub>IO</sub>	2	—	—	5	50	nA
Input bias current	I <sub>I</sub>	2	—	—	45	250	nA
Common mode input voltage	CMV <sub>IN</sub>	3	—	0	—	V <sub>CC</sub> -1.5	V
Supply current	I <sub>CC</sub>	4	—	—	0.7	1.2	mA
Voltage gain	G <sub>V</sub>	—	R <sub>L</sub> ≥ 2kΩ	86	100	—	dB
Maximum output voltage swing	V <sub>op-p</sub>	5	R <sub>L</sub> = 2kΩ	0	—	3.4	V
Common mode rejection ratio	CMRR	3	—	65	85	—	dB
Supply voltage rejection ratio	SVRR	—	R <sub>g</sub> = 10kΩ	65	100	—	dB
Source current	I <sub>source</sub>	6	IN (-) = 0V, IN (+) = 1V	20	40	—	mA
Sink current	I <sub>sink</sub>	7	IN (-) = 1V, IN (+) = 0V	10	20	—	mA
Unity gain cross frequency	f <sub>T</sub>	—	—	—	0.3	—	MHz

**Test Circuit**

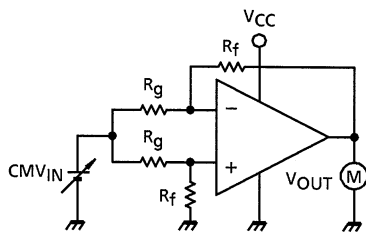
**(1)  $V_{IO}$**



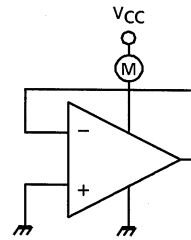
**(2)  $I_I, I_{IO}$**



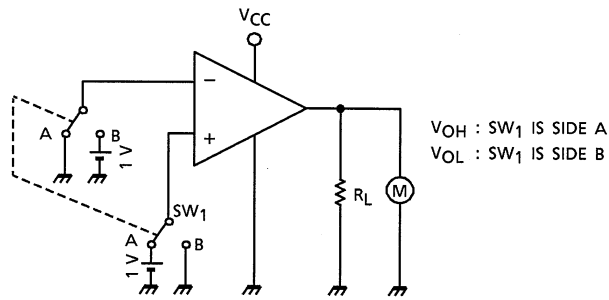
**(3)  $CMV_{IN}, CMRR$**



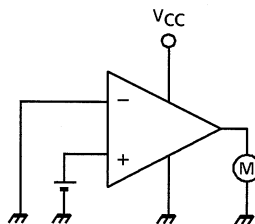
**(4)  $I_{CC}$**



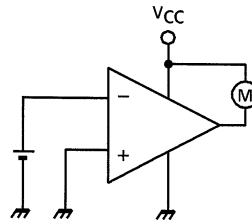
**(5)  $V_{OP-P}$**

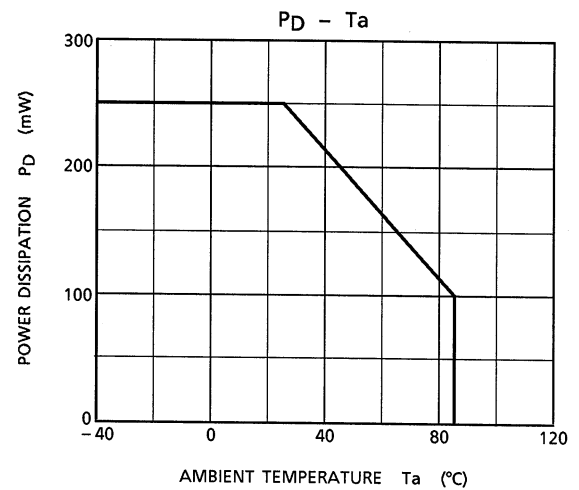
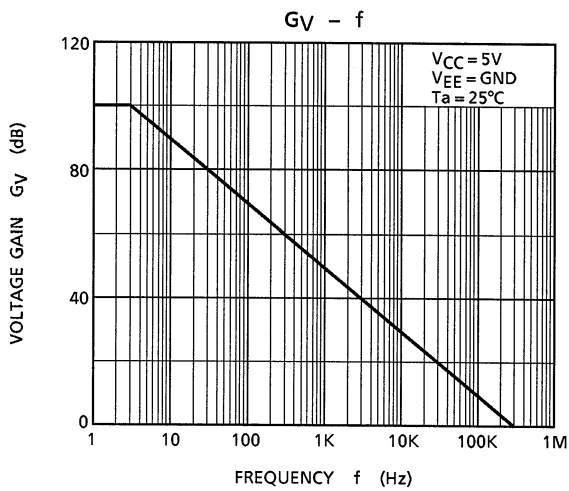
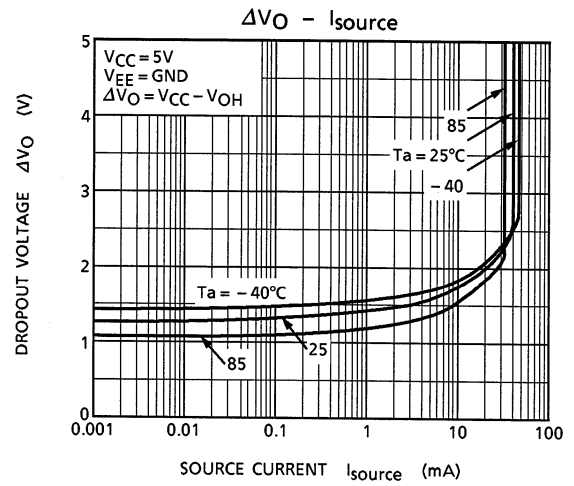
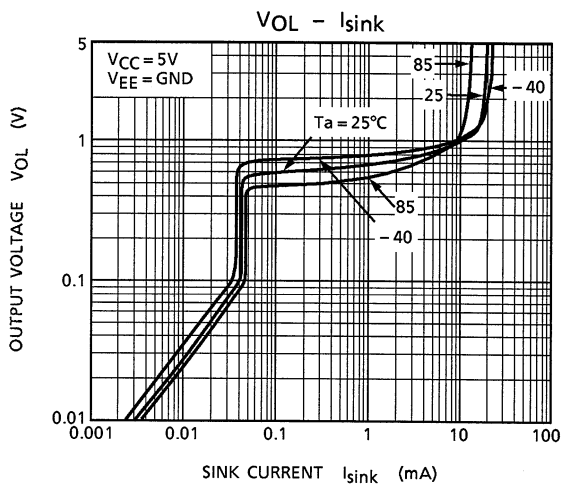
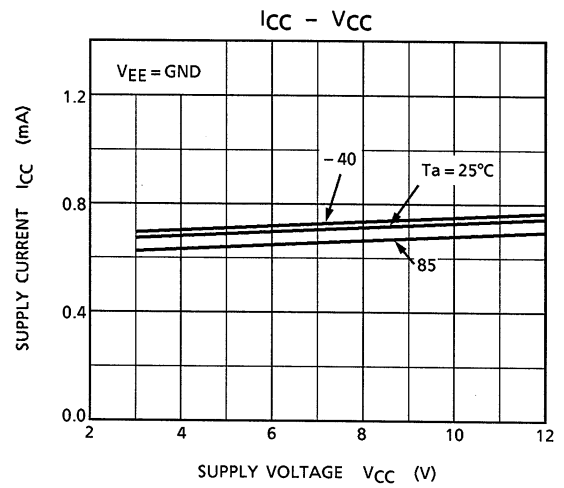
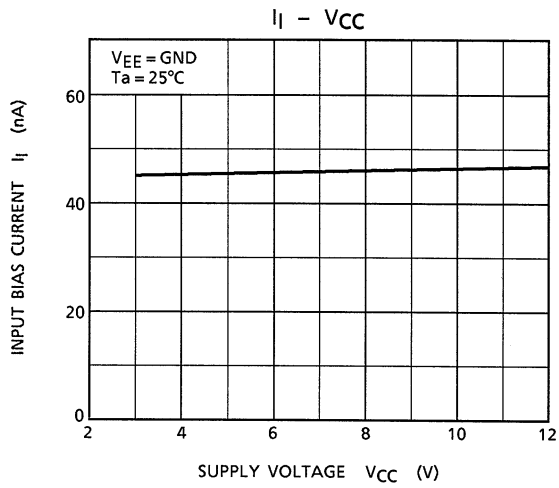


**(6)  $I_{source}$**



**(7)  $I_{sink}$**







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