WINSOURCE ELECTRONICS

THE DATASHEET OF

74SSTUB32865AZJBR

28-BIT TO 56-BIT REGISTERED BUFFER WITH ADDRESS-PARITY TEST

FEATURES

- **Member of the Texas Instruments Widebus+™ Family**
- **Pinout Optimizes DDR2 RDIMM PCB Layout**
- **1-to-2 Outputs Supports Stacked DDR2 RDIMMs**
- **High driver strength for heavily loaded DIMMs**
- **Chip-Select Inputs Gate the Data Outputs from Changing State and Minimizes System Power Consumption**
- **Output Edge-Control Circuitry Minimizes Switching Noise in an Unterminated Line**
- **Supports SSTL_18 Data Inputs**
- **Differential Clock (CK and $\overline{CK}$) Inputs**
- **Supports LVCMOS Switching Levels on the Chip-Select Gate-Enable and $\overline{RESET}$ Inputs**
- **Checks Parity on DIMM-Independent Data Inputs**
- **$\overline{RESET}$ Input Disables Differential Input Receivers, Resets All Registers, and Forces All Outputs Low, Except $\overline{PTYERR}$**
- **Supports industrial temperature range (-40°C to 85°C)**

DESCRIPTION

This 28-bit 1:2 configurable registered buffer is designed for 1.7-V to 1.9-V V_{CC} operation. One device per DIMM is required to drive up to stacked 18 SDRAM loads or two devices per DIMM are required to drive up to 36 stacked SDRAM loads.

All inputs are SSTL_18, except the chip-select gate-enable (CSGateEN) and reset ($\overline{RESET}$) inputs, which are LVCMOS. All outputs are edge-controlled circuits optimized for unterminated DIMM loads, and meet SSTL_18 specifications, except the open-drain error ($\overline{PTYERR}$) output.

The 74SSTUB32865A operates from a differential clock (CK and $\overline{CK}$). Data are registered at the crossing of CK going high and $\overline{CK}$ going low.

The 74SSTUB32865A accepts a parity bit from the memory controller on the parity bit (PARIN) input, compares it with the data received on the DIMM-independent D-inputs (D0-D21) and indicates whether a parity error has occurred on the open-drain $\overline{PTYERR}$ pin (active low). The convention is even parity, i.e., valid parity is defined as an even number of ones across the DIMM-independent data inputs combined with the parity input bit. To calculate parity, all DIMM-independent D-inputs must be tied to a known logic state.

The 74SSTUB32865A includes a parity checking function. Parity, which arrives one cycle after the data input to which it applies, is checked on the PARIN input of the device. Two clock cycles after the data are registered, the corresponding $\overline{PTYERR}$ signal is generated.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	TFBGA-ZJB	Tape and reel	74SSTUB32865AZJBR	SB865A

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

DESCRIPTION (CONTINUED)

If an error occurs and the $\overline{\text{PTYERR}}$ output is driven low, it stays latched low for a minimum of two clock cycles or until $\overline{\text{RESET}}$ is driven low. If two or more consecutive parity errors occur, the $\overline{\text{PTYERR}}$ output is driven low and latched low for a clock duration equal to the parity error duration or until $\overline{\text{RESET}}$ is driven low. If a parity error occurs on the clock cycle before the device enters the low-power mode (LPM) and the $\overline{\text{PTYERR}}$ output is driven low, it stays latched low for the LPM duration plus two clock cycles or until $\overline{\text{RESET}}$ is driven low. The DIMM-dependent signals (DCKE0, DCKE1, DODT0, DODT1, $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$) are not included in the parity check computation.

In a typical DDR2 RDIMM application, $\overline{\text{RESET}}$ is completely asynchronous with respect to CK and $\overline{\text{CK}}$. Therefore, no timing relationship can be ensured between the two. When entering reset, the register is cleared and the data outputs are quickly driven low, relative to the time to disable the differential input receivers. However, when coming out of reset, the register quickly becomes active, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of $\overline{\text{RESET}}$ until the input receivers are fully enabled, the 74SSTUB32865A outputs remain low, thus preventing glitches on the output.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

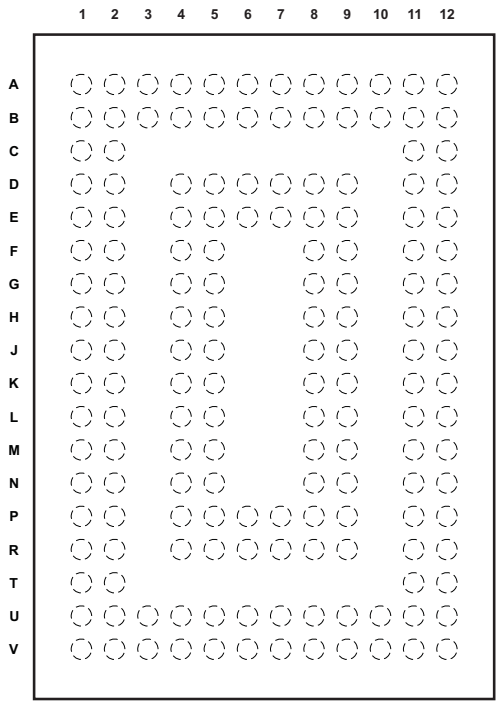
The device supports low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (VREF) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low, all registers are reset and all outputs are forced low except $\overline{\text{PTYERR}}$. The LVCMOS $\overline{\text{RESET}}$ input must always be held at a valid logic high or low level.

The device also supports low-power active operation by monitoring both system chip select (DCS0 and DCS1) and CSGateEN inputs. It gates the Qn outputs from changing states when the CSGateEN, $\overline{\text{DCS0}}$, and $\overline{\text{DCS1}}$ inputs are high. If the CSGateEN, $\overline{\text{DCS0}}$ or $\overline{\text{DCS1}}$ input is low, the Qn outputs function normally. Also, if both DCS0 and DCS1 inputs are high, the device gates the $\overline{\text{PTYERR}}$ output from changing states. If either $\overline{\text{DCS0}}$ or $\overline{\text{DCS1}}$ is low, the $\overline{\text{PTYERR}}$ output functions normally. The $\overline{\text{RESET}}$ input has priority over the $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ control, and when driven low forces the Qn outputs low, and the $\overline{\text{PTYERR}}$ output high. If the chip-select control functionality is not desired, then the CSGateEN input can be hardwired to ground, in which case, the setup-time requirement for $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ would be the same as for the other D data inputs. To control the low-power mode with $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ only, then the CSGateEN input should be pulled up to V_{CC} through a pullup resistor.

The two V_{REF} pins (A1 and V1) are connected together internally by a resistance of approximately 150 Ω. However, it is necessary to connect only one of the two V_{REF} pins to the external V_{REF} power supply. An unused V_{REF} pin should be terminated with a V_{REF} coupling capacitor.

PINOUT

ZJB PACKAGE
(TOP VIEW)

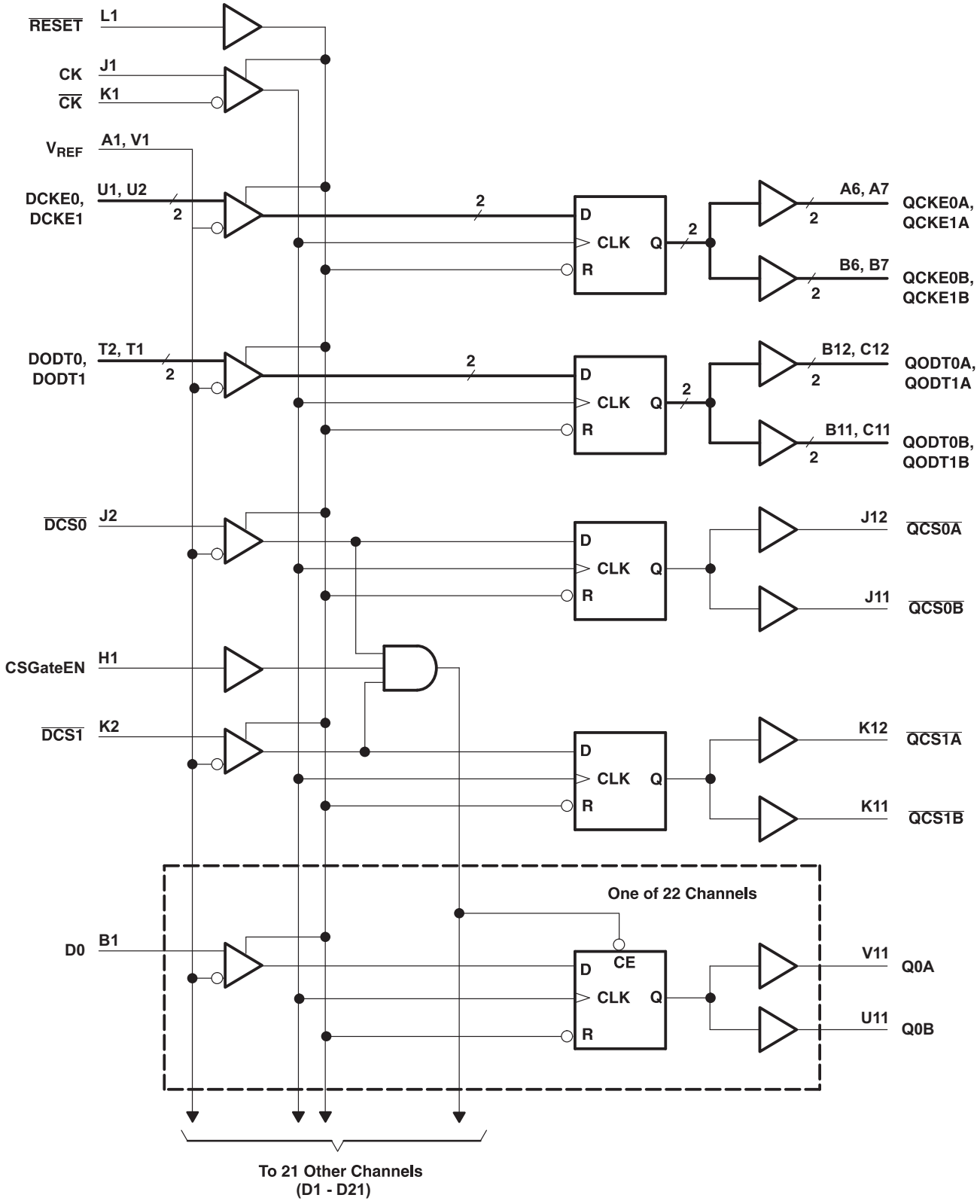


TERMINAL ASSIGNMENTS

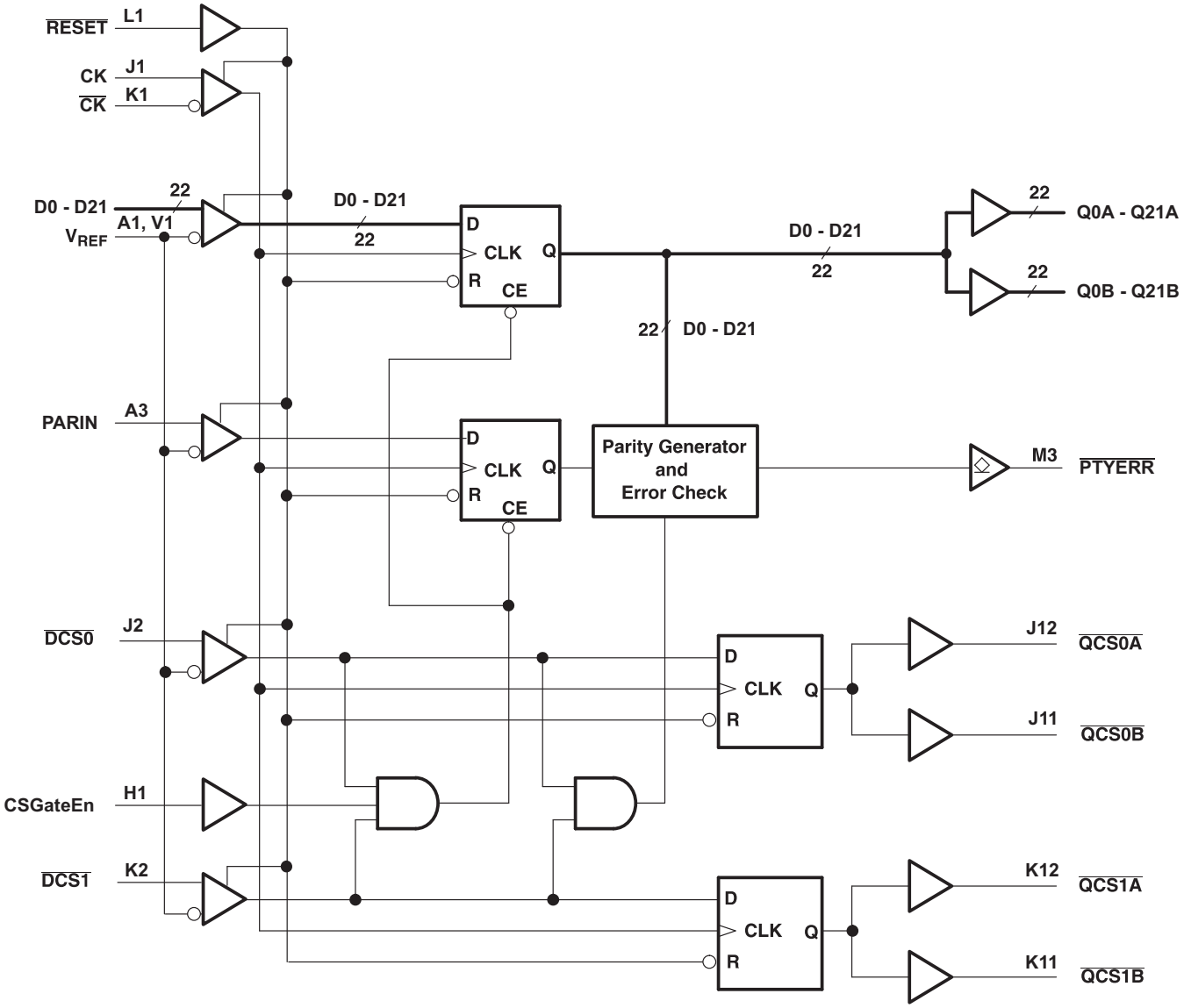
	1	2	3	4	5	6	7	8	9	10	11	12
A	VREF	NC(1)	PARIN	NC	NC	QCKE1A	QCKE0A	Q21A	Q19A	Q18A	Q17B	Q17A
B	D1	D2	NC	NC	NC	QCKE1B	QCKE0B	Q21B	Q19B	Q18B	QODT0B	QODT0A
C	D3	D4									QODT1B	QODT1A
D	D6	D5		VCC	GND	NC	NC	GND	GND		Q20B	Q20A
E	D7	D8		VCC	GND	VCC	VCC	GND	GND		Q16B	Q16A
F	D11	D9		VCC	GND			VCC	VCC		Q1B	Q1A
G	D18	D12		VCC	GND			VCC	VCC		Q2B	Q2A
H	CSGateEN	D15		VCC	GND			GND	GND		Q5B	Q5A
J	CK	$\overline{DCS0}$		GND	GND			VCC	VCC		$\overline{QCS0B}$	QCS0A
K	$\overline{CK}$	$\overline{DCS1}$		VCC	VCC			GD	GND		$\overline{QCS1B}$	QCS1A
L	$\overline{RESET}$	D14		GND	GND			VCC	VCC		Q6B	Q6A
M	D0	D10		GND	GND			GND	GND		Q10B	Q10A
N	D17	D16		VCC	VCC			VCC	VCC		Q9B	Q9A
P	D19	D21		GND	VCC	VCC	VCC	VCC	GND		Q11B	Q11A
R	D13	D20		GND	VCC	VCC	GND	GND	GND		Q15B	Q15A
T	DODT1	DODT0									Q14B	Q14A
U	DCKE0	DCKE1	MCL(2)	$\overline{PTYERR}$	MCH(3)	Q3B	Q12B	Q7B	Q4A	Q13A	Q0B	Q8B
V	VREF	MCL	MCL	NC	MCH	Q3A	Q12A	Q7A	Q4B	Q13B	Q0A	Q8A

(1) NC denotes pins that have no internal connection
(2) MCL denotes pins that must be connected LOW
(3) MCH denotes pins that must be connected HIGH

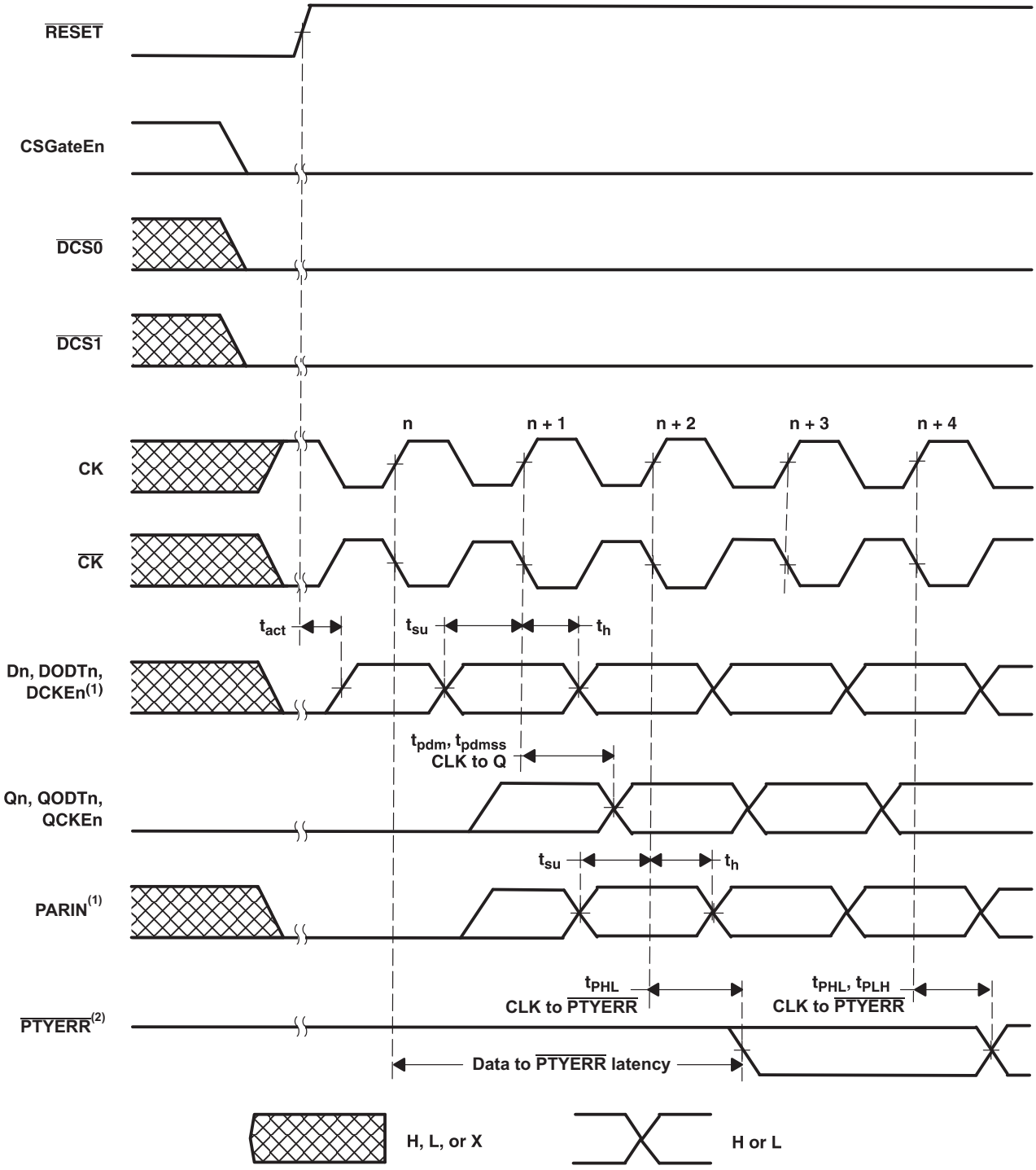
LOGIC DIAGRAM



PARITYLOGIC DIAGRAM



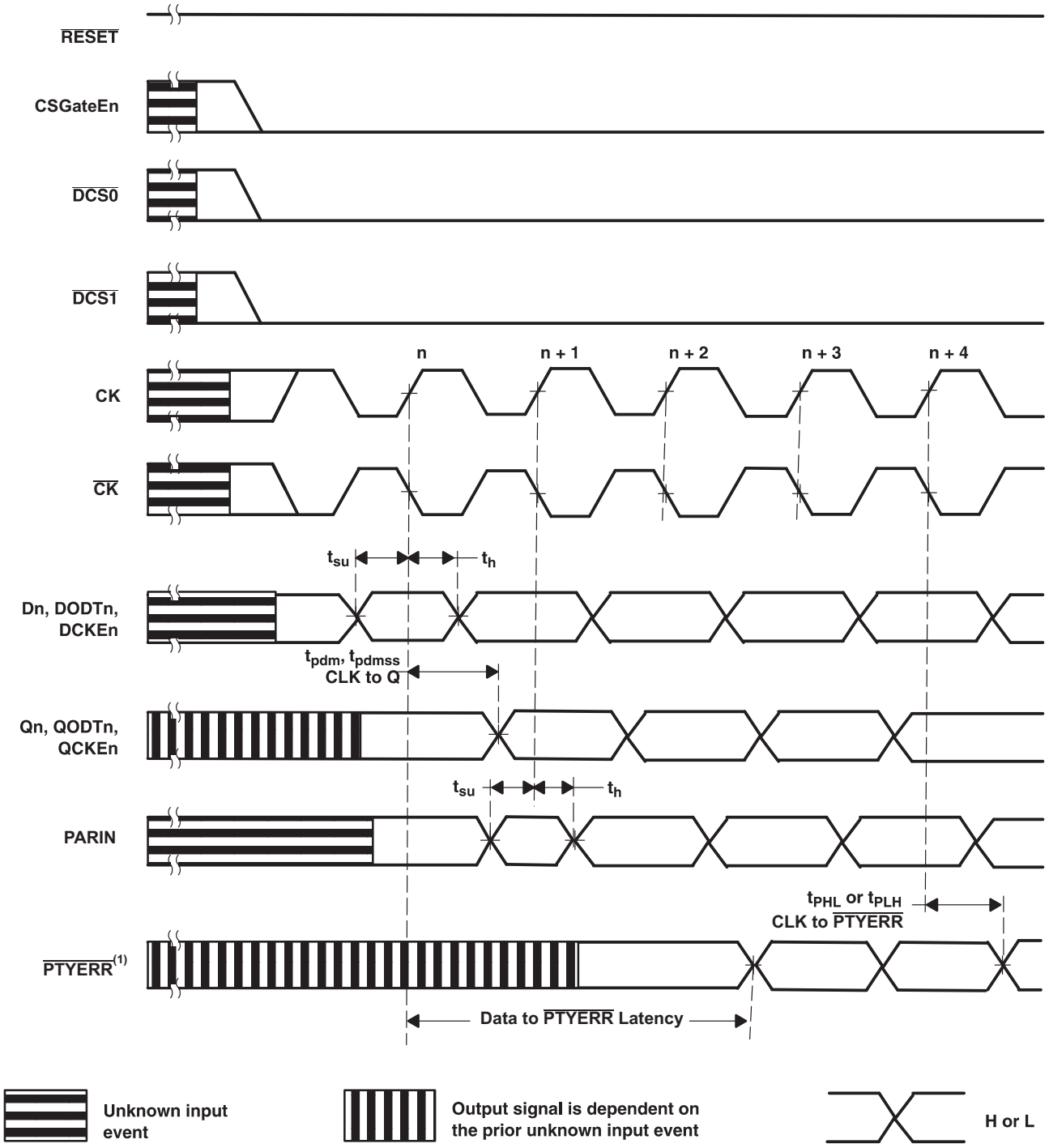
TIMING DIAGRAM for 74SSTUB32865A DURING START-UP ($\overline{\text{RESET}}$ switches from L to H)



(1) After $\overline{\text{RESET}}$ is switched from low to high, all data and PARIN input signals must be set and held low for a minimum time of t_{act} max, to avoid false error.

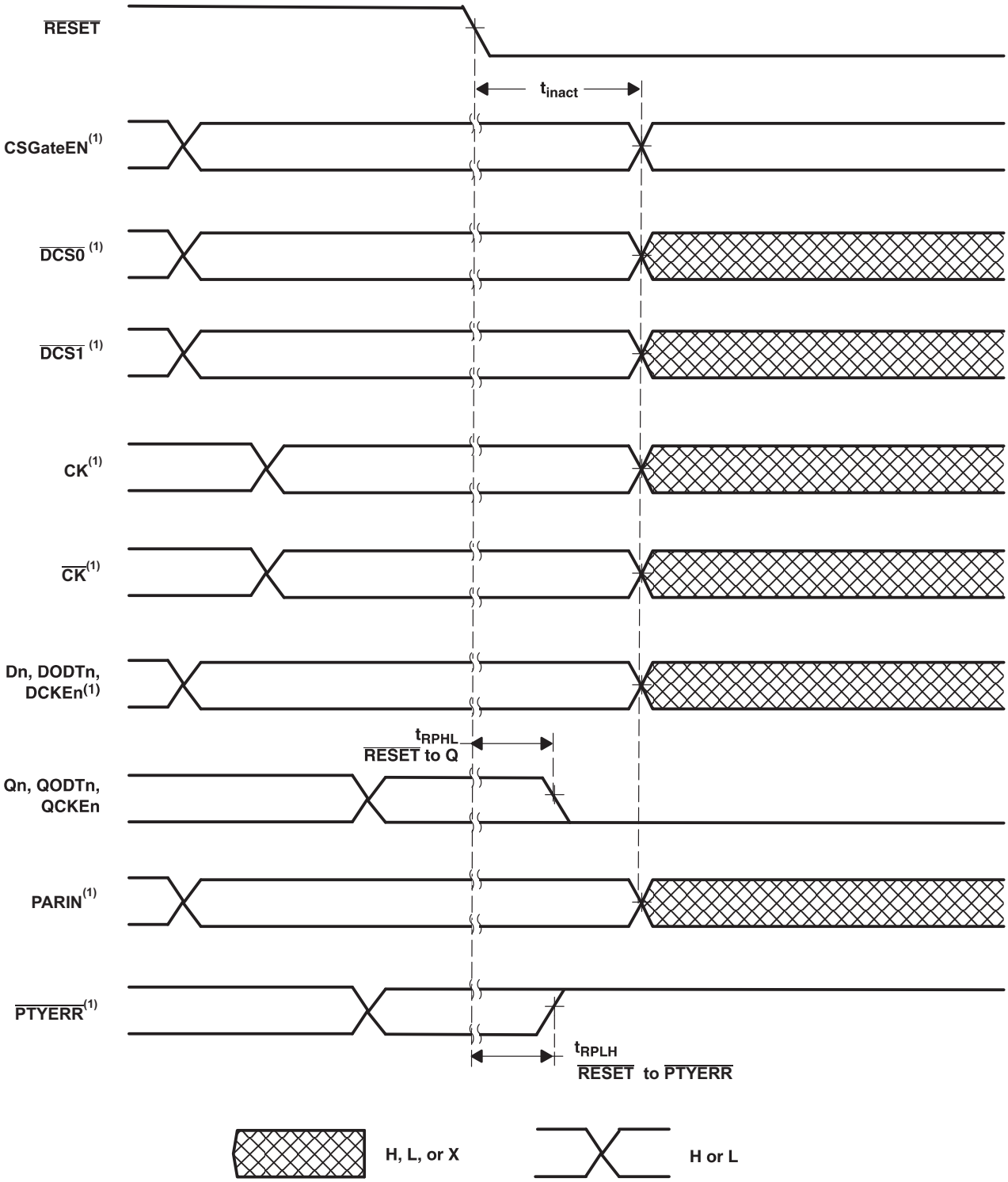
(2) If the data is clocked in on the n clock pulse, the $\overline{\text{PTYERR}}$ output signal will be generated on the n + 2 clock pulse and it will be valid on the n + 3 clock pulse.

TIMING DIAGRAM for 74SSTUB32865A DURING NORMAL OPERATION (RESET = H)



(1) If the data is clocked in on the n clock pulse, the $\overline{\text{PTYERR}}$ output signal is generated on the n + 2 clock pulse and is valid on the n + 3 clock pulse. If an error occurs and the $\overline{\text{PTYERR}}$ output is driven low, it stays latched low for a minimum of two clock cycles or until $\overline{\text{RESET}}$ is driven low.

TIMING DIAGRAM for 74SSTUB32865A DURING SHUT-DOWN ($\overline{\text{RESET}}$ switches from H to L)



(1) After $\overline{\text{RESET}}$ is switched from high to low, all data and clock input signals must be held at valid logic levels (not floating) for a minimum time of t_{inact} max.

TERMINAL FUNCTIONS

TERMINAL NAME	DESCRIPTION	ELECTRICAL CHARACTERISTICS
GND	Ground	Ground input
V_{CC}	Power supply voltage	1.8 V nominal
VREF	Input reference voltage	0.9 V nominal
CK	Positive master clock input	Differential input
$\overline{CK}$	Negative master clock input	Differential input
$\overline{RESET}$	Asynchronous reset input – resets registers and disables V_{REF}, data and clock differential-input receivers. When $\overline{RESET}$ is low, all the Q outputs are forced low and the $\overline{PTYERR}$ output is forced high.	LVCMOS input
CSGateEN	Chip select gate enable – When high, D0-D21 inputs will be latched only when at least one chip select input is low during the rising edge of the clock. When low, the D0-D21 inputs will be latched and redriven on every rising edge of the clock.	LVCMOS input
D0-D21	Data input – clocked in on the crossing of the rising edge of CK and the falling edge of $\overline{CK}$	SSTL_18 inputs
$\overline{DCS0}$, $\overline{DCS1}$	Chip select inputs – These pins initiate DRAM address/command decodes, and as such at least one will be low when a valid address/command is present. The Register can be programmed to redrive all D inputs (CSGateEN high) only when at least one chip select input is low. If CSGateEN, $\overline{DCS0}$, and $\overline{DCS1}$ inputs are high, D1-D28(1) inputs will be disabled.	SSTL_18 inputs
$\overline{DODT0}$, $\overline{DODT1}$	The outputs of this register bit will not be suspended by the $\overline{DCS0}$ and $\overline{DCS1}$ control.	SSTL_18 input
$\overline{DCKE0}$, $\overline{DCKE1}$	The outputs of this register bit will not be suspended by the $\overline{DCS0}$ and $\overline{DCS1}$ control.	SSTL_18 input
PARIN	Parity input – arrives one clock cycle after the corresponding data input	SSTL_18 input
Q0A-Q21A, Q0B-Q21B	Data outputs that are suspended by the $\overline{DCS0}$ and $\overline{DCS1}$ control.	1.8 V CMOS outputs
$\overline{QCS0A}$, $\overline{QCS1A}$, $\overline{QCS0B}$, $\overline{QCS1B}$	Data output that are not suspended by the $\overline{DCS0}$ and $\overline{DCS1}$ control.	1.8 V CMOS output
QODT0A, QODT1A, QODT0B, QODT1B	Data output that are not suspended by the $\overline{DCS0}$ and $\overline{DCS1}$ control.	1.8 V CMOS output
QCKE0A, QCKE1A, QCKE0B, QCKE0B	Data output that are not suspended by the $\overline{DCS0}$ and $\overline{DCS1}$ control.	1.8 V CMOS output
$\overline{PTYERR}$	Output error bit – generated two clock cycles after the corresponding data is registered.	Open-drain output
MCL	Must be connected to logic LOW	
MCH	Must be connected to logic HIGH	
NC	No internal connection	

FUNCTION TABLE

INPUTS							OUTPUTS			
$\overline{RESET}$	$\overline{DCS0}$	$\overline{DCS1}$	CSGateEN	CK	$\overline{CK}$	Dn, DODTn, DCKEn	Qn	$\overline{QCS0}$	$\overline{QCS1}$	QODT, QCKE
H	L	L	X	↑	↓	L	L	L	L	L
H	L	L	X	↑	↓	H	H	L	L	H
H	L	L	X	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	L	H	X	↑	↓	L	L	L	H	L
H	L	H	X	↑	↓	H	H	L	H	H
H	L	H	X	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	H	L	X	↑	↓	L	L	H	L	L
H	H	L	X	↑	↓	H	H	H	L	H
H	H	L	X	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	H	H	L	↑	↓	L	L	H	H	L
H	H	H	L	↑	↓	H	H	H	H	H

FUNCTION TABLE (continued)

INPUTS							OUTPUTS			
$\overline{\text{RESET}}$	$\overline{\text{DCS0}}$	$\overline{\text{DCS1}}$	CSGateEN	CK	$\overline{\text{CK}}$	Dn, DODTn, DCKEn	Qn	$\overline{\text{QCS0}}$	$\overline{\text{QCS1}}$	QODT, QCKE
H	H	H	L	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	H	H	H	↑	↓	L	Q_0	H	H	L
H	H	H	H	↑	↓	H	Q_0	H	H	H
H	H	H	H	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
L	X or floating	X or floating	X or floating	X or floating	X or floating	X or floating	L	L	L	L

PARITY AND STANDBY FUNCTION

INPUTS							OUTPUT
$\overline{\text{RESET}}$	CK	$\overline{\text{CK}}$	$\overline{\text{DCS0}}$	$\overline{\text{DCS1}}$	Σ OF INPUTS = H D1–D22	PARIN(1)	PTYERR(2)
H	↑	↓	L	X	Even	L	H
H	↑	↓	L	X	Odd	L	L
H	↑	↓	L	X	Even	H	L
H	↑	↓	L	X	Odd	H	H
H	↑	↓	X	L	Even	L	H
H	↑	↓	X	L	Odd	L	L
H	↑		X	L	Even	H	L
H	↑	↓	X	L	Odd	H	H
H	↑	↓	H	H	X	X	$\overline{\text{PTYERR}}_0$ (3)
H	L or H	L or H	X	X	X	X	$\overline{\text{PTYERR}}_0$
L	X or floating	X or floating	X or floating	X or floating	X	X or floating	

(1) PARIN arrives one clock cycle after the data to which it applies.
(2) This transition assumes that $\overline{\text{PTYERR}}$ is high at the crossing of $\overline{\text{CK}}$ going high and CK going low. If PTYERR goes low, it stays latched low for a minimum of two clock cycles or until $\overline{\text{RESET}}$ is driven low. If two or more consecutive errors occur, the $\overline{\text{PTYERR}}$ output is driven low and latched low for a clock duration equal to the parity error duration or until $\overline{\text{RESET}}$ is driven low. For $\overline{\text{PTYERR}}$ computation CSGateEN is a *don't care*.
(3) If $\overline{\text{DCS0}}$, $\overline{\text{DCS1}}$ and CSGateEN are driven high, the device is placed in a low-power mode (LPM). If a parity error occurs on the clock cycle before the device enters the LPM and the $\overline{\text{PTYERR}}$ output is driven low, it stays latched low for the LPM duration plus two clock cycles or until $\overline{\text{RESET}}$ is driven low.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

			VALUE	UNIT
V_{CC}	Supply voltage range		–0.5 to 2.5	V
V_I	Input voltage range (2) (3)		–0.5 to V_{CC} + 0.5	V
V_O	Output voltage range (2) (3)		–0.5 to V_{CC} + 0.5	V
I_{IK}	Input clamp curren t(V_I < 0 or V_I > V_{CC})		±50	mA
I_{OK}	Output clamp current (V_O < 0 or V_O > V_{CC})		±50	mA
I_O	Continuous output current (V_O = 0 to V_{CC})		±50	mA
I_{CC}	Continuous current through each V_{CC} or GND		±100	mA
θ_{JA}	Thermal resistance, junction to ambient(4)	No Airflow	51.2	°C/W
		Airflow 200 ft/min	47.2	
θ_{JC}	Thermal resistance, junction to case(4)	No Airflow	29.7	
T_{stg}	Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This value is limited to 2.5 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		1.7		1.9	V
V_{REF}	Reference voltage		0.49 × V_{CC}	0.5 × V_{CC}	0.51 × V_{CC}	V
V_{TT}	Termination voltage		V_{REF}–40 mV	V_{REF}	V_{REF}+40mV	V
V_I	Input voltage		0		V_{CC}	V
V_{IH}	AC high-level input voltage	Data inputs, $\overline{DCSn}$, PARIN	V_{REF}+250 mV			V
V_{IL}	AC low-level input voltage	Data inputs, $\overline{DCSn}$, PARIN			V_{REF}–250 mV	V
V_{IH}	DC high-level input voltage	Data inputs, $\overline{DCSn}$, PARIN	V_{REF}+125 mV			V
V_{IL}	DC low-level input voltage	Data inputs, $\overline{DCSn}$, PARIN			V_{REF}–125 mV	V
V_{IH}	High-level input voltage	$\overline{RESET}$, CSGateEN, C	0.65 × V_{CC}			V
V_{IL}	Low-level input voltage	$\overline{RESET}$, CSGateEN, C			0.35 × V_{CC}	V
V_{ICR}	Common-mode input voltage range	CK, $\overline{CK}$	0.675		1.125	V
$V_{I(PP)}$	Peak-to-peak input voltage	CK, $\overline{CK}$	600			mV
I_{OH}	High-level output current	Q outputs			–12	mA
I_{OL}	Low-level output current	Q outputs			12	mA
		$\overline{PTYERR}$ output	30			
T_A	Operating free-air temperature		-40		85	°C

(1) The $\overline{RESET}$ and Cn inputs of the device must be held at valid logic voltage levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless $\overline{RESET}$ is low. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}	Q outputs	I_{OH} = –100 µA	1.7 V to 1.9 V	V_{CC} –0.2			V
		I_{OH} = –8 mA	1.7 V	1.2			

(1) All typical values are at V_{CC} = 1.8 V, T_A = 25°C.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OL}	Q ouputs	I_{OL} = 100 µA		1.7 V to 1.9 V			0.2	V
		I_{OL} = 8mA		1.7 V			0.5	
	$\overline{PTYERR}$ output	I_{OL} = 25mA		1.7 V			0.5	
I_I	PARIN	V_I = GND		1.9 V			-5	µA
		V_I = V_{CC}					+25	
	All other inputs(2)	V_I = V_{CC} or GND					±5	
I_{OZ}	$\overline{PTYERR}$ output	V_O = V_{CC} or GND		1.9 V			±10	µA
I_{CC}	Static standby(3)	$\overline{RESET}$ = GND	I_O = 0	1.9 V			200	µA
	Static operating	$\overline{RESET}$ = V_{CC}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$					80	mA
I_{CCD}	Dynamic operating – clock only	$\overline{RESET}$ = V_{CC}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CK and $\overline{CK}$ switching 50% duty cycle	I_O = 0	1.8 V		64		µA/MHz
	Dynamic operating – per each data input	$\overline{RESET}$ = V_{CC}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CK and $\overline{CK}$ switching 50% duty cycle, One data input switching at one half clock frequency, 50% duty cycle				37		µA/clock MHz/D input
I_{CCDLP}	Chip-select-enabled low-power active mode – clock only	$\overline{RESET}$ = V_{CC}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CK and $\overline{CK}$ switching 50% duty cycle	I_O = 0	1.8 V		68		µA/MHz
	Chip-select-enabled low-power active model	$\overline{RESET}$ = V_{CC}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CK and $\overline{CK}$ switching 50% duty cycle, One data input switching at one half clock frequency, 50% duty cyclel				2.7		µA/clock MHz/D input
C_i(4)	Input Capacitance, Data inputs	V_I=V_{REF}±250mV		1.8V	2.5		3.5	pF
	input Capacitance, CK and $\overline{CK}$	V_{ICR}=0.9V, $V_{I(PP)}$=600mV			2		3	
	Input Capacitance, $\overline{RESET}$	V_I=V_{CC} or GND				4		

(2) Each V_{REF} pin (A1 or V1) should be tested independently, with the other (untested) pin open.
(3) The maximum static standby current I_{CC} is 100 µA if the device is exposed only to standard temperature range (0°C to 70°C). For industrial temperature range (-40°C to 85°C) the maximum static I_{CC} is 200 µA.
(4) Measured using TDR method and adjusted from substrate transmission line effects.

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2 and Note (1))

			V_{CC} = 1.85 V ± 0.15 V		UNIT
			MIN	MAX	
f_{clock}	Clock frequency			410	MHz
t_w	Pulse duration, CK, $\overline{CK}$ high or low		1		ns
t_{act}	Differential inputs active time(2)			10	ns
t_{inact}	Differential inputs inactive time(3)			15	ns
t_{su}	Setup time	$\overline{DCSn}$ before CK↑, $\overline{CK}$↓, CSGateEN high	0.6		ns
		$\overline{DCSn}$ before CK↑, $\overline{CK}$↓, CSGateEN low	0.5		
		DODTn, DCKEn, and Data before CK↑, $\overline{CK}$↓	0.5		
		PARIN before CK↑, $\overline{CK}$↓	0.5		
t_h	Hold time	$\overline{DCSn}$, DODTn, DCKEn, and Data after CK↑, $\overline{CK}$↓	0.4		ns
		PARIN after CK↑, $\overline{CK}$↓	0.4		

(1) All inputs slew rate is 1 V/ns ±20%.
(2) V_{REF} must be held at a valid input level and data inputs must be held low for a minimum time of $_{tact}$ max, after $\overline{RESET}$ is taken high.
(3) V_{REF}, data, and clock inputs must be held at valid voltage levels (not floating) for a minimum time of tinact max, after $\overline{RESET}$ is taken low.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.85 V ± 0.15 V		UNIT
			MIN	MAX	
f_{max} (see Figure 2)			410		MHz
t_{pdm} (1) (production test, see Figure 1)	CK and $\overline{CK}$	Q	0.5	1.1	ns
t_{PLH} (see Figure 4)	CK and $\overline{CK}$	$\overline{PTYERR}$	1.2	3	ns
t_{PHL} (see Figure 4)			1	2.4	ns
t_{RPHL} (2) (see Figure 2)	$\overline{RESET}$	Q		3	ns
t_{RPLH} (see Figure 4)	RESET	$\overline{PTYERR}$		3	ns

(1) The typical difference between min and max does not exceed 400ps.
(2) Includes 350ps test-load transmission line delay

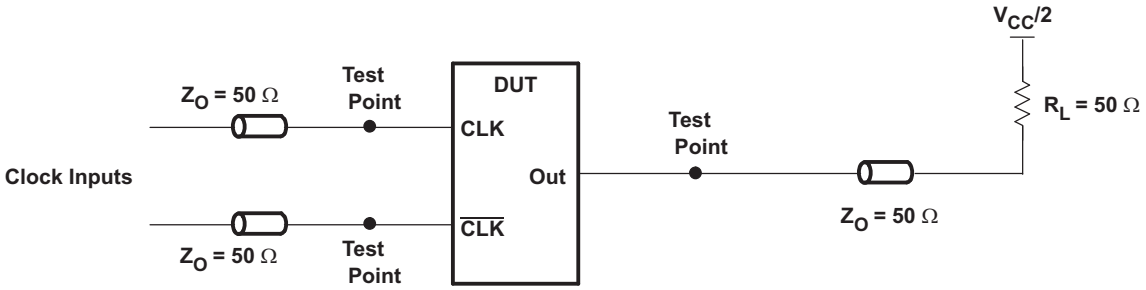
OUTPUT SLEW RATES

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

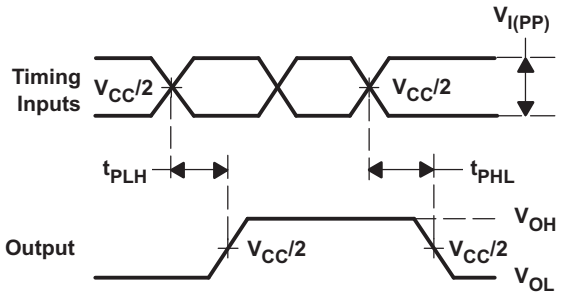
PARAMETER	FROM	TO	V_{CC} = 1.85 V ± 0.15 V		UNIT
			MIN	MAX	
dV/dt_r	20%	80%	1	5	V/ns
dV/dt_f	80%	20%	1	5	V/ns
dV/dt_Δ (1)	20% or 80%	80% or 20%		1	V/ns

(1) Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate).

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

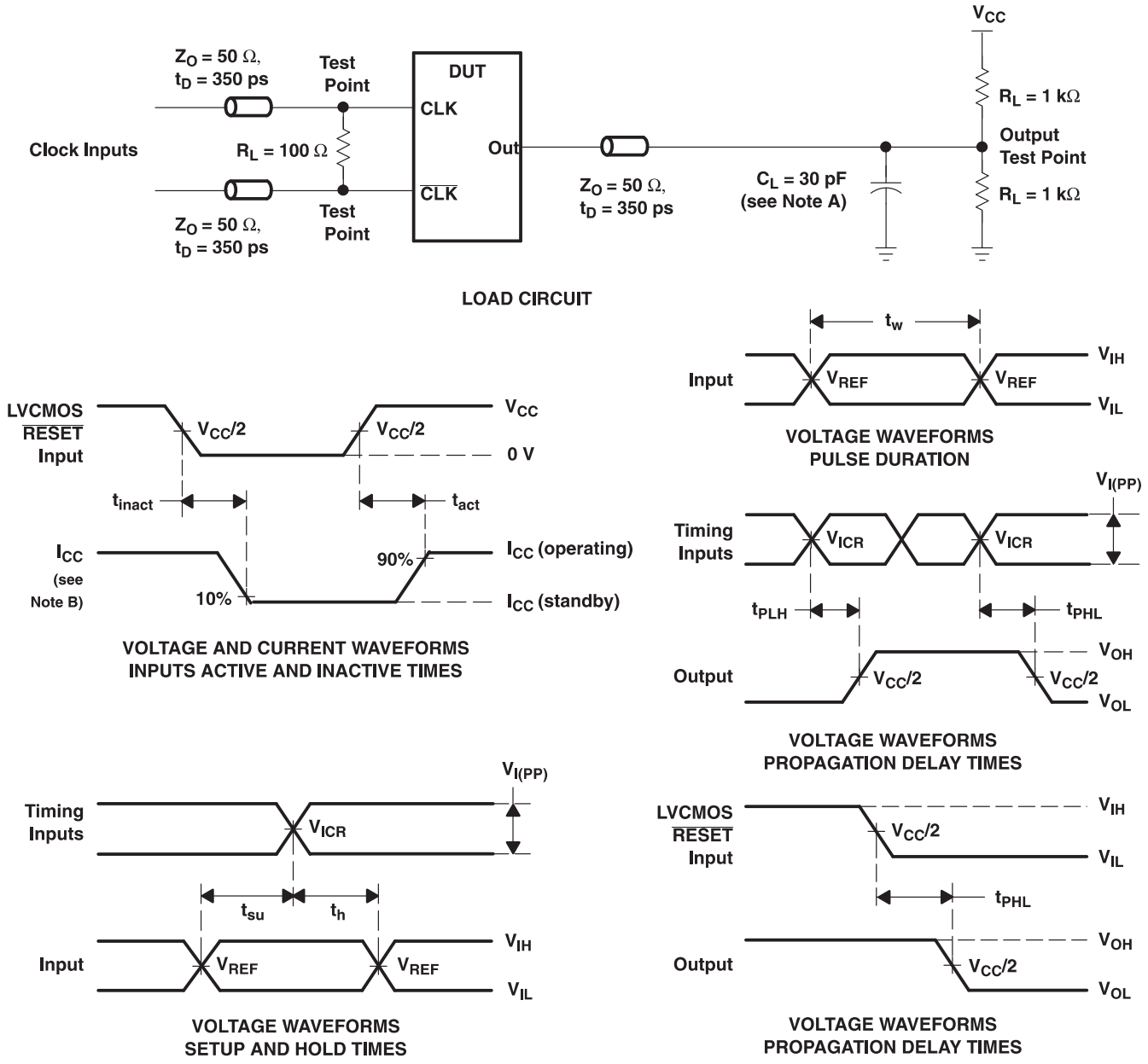
Figure 1. Output Load Circuit for Production Test

PARAMETER MEASUREMENT INFORMATION (continued)

Propagation Delay (Design Goal as per JEDEC Specification)

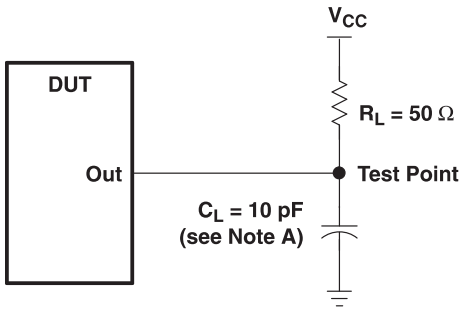
			V_{CC} = 1.8 V ±0.1 V		
PARAMETER	**FROM (INPUT)**	**TO (OUTPUT)**	**MIN**	**MAX**	**UNIT**
t_{pdm} (1)	CLK and $\overline{CLK}$	Q	1.1	1.5	ns
t_{pdmss} (1)	CLK and $\overline{CLK}$	Q		1.6	ns

(1) Includes 350-ps test-load transmission line delay.

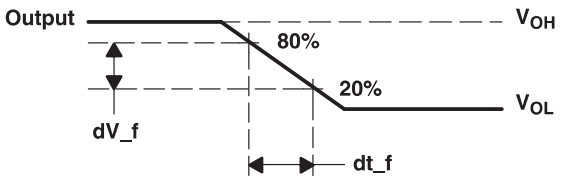


NOTES:
A. C_L includes probe and jig capacitance.
B. I_{CC} tested with clock and data inputs held at V_{CC} or GND, and I_O = 0 mA.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, input slew rate = 1 V/ns ±20% (unless otherwise noted).
D. The outputs are measured one at a time with one transition per measurement.
E. $V_{REF} = V_{CC}/2$
F. $V_{IH} = V_{REF}$ + 250 mV (ac voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVCMOS input.
G. $V_{IL} = V_{REF}$ – 250 mV (ac voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
H. $V_{I(PP)}$ = 600 mV
I. t_{PLH} and t_{PHL} are the same as t_{pd}.

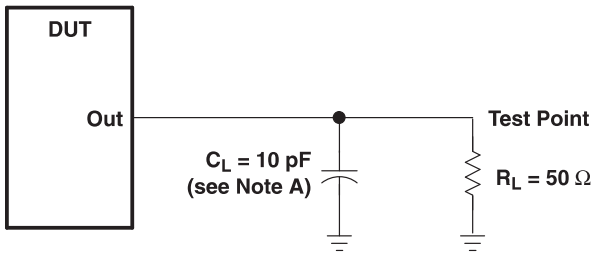
Figure 2. Data Output Load Circuit and Voltage Waveforms



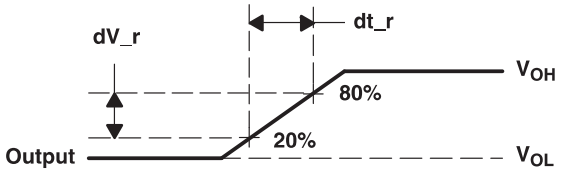
LOAD CIRCUIT
HIGH-TO-LOW SLEW-RATE MEASUREMENT



VOLTAGE WAVEFORMS
HIGH-TO-LOW SLEW-RATE MEASUREMENT



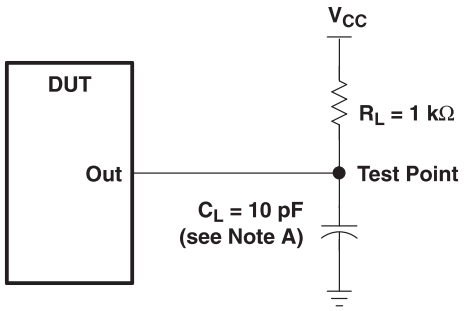
LOAD CIRCUIT
LOW-TO-HIGH SLEW-RATE MEASUREMENT



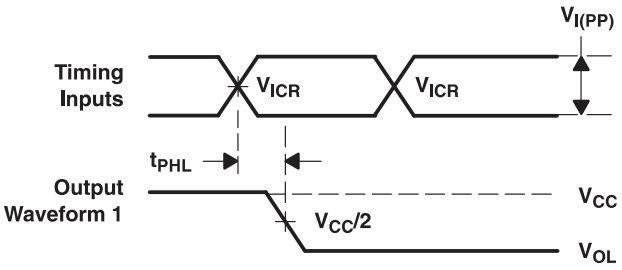
VOLTAGE WAVEFORMS
LOW-TO-HIGH SLEW-RATE MEASUREMENT

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics:
PRR ≤ 10 MHz, Z_O = 50 Ω, input slew rate = 1 V/ns ± 20% (unless otherwise specified).

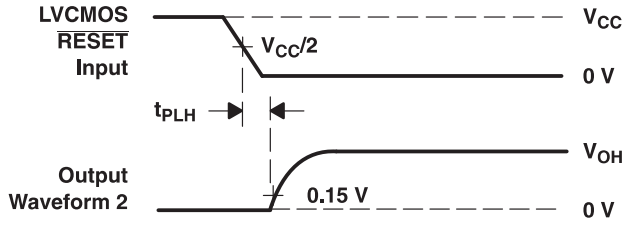
Figure 3. Data Output Slew-Rate Measurement Information



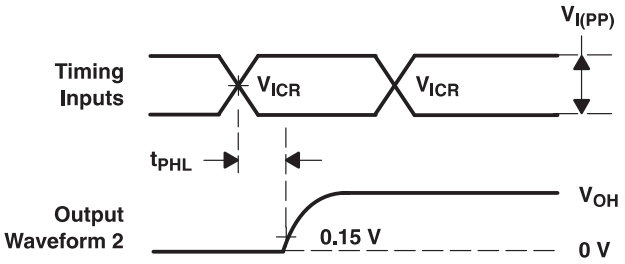
LOAD CIRCUIT



VOLTAGE WAVEFORMS
OPEN-DRAIN OUTPUT TRANSITION TIME
(HIGH-TO-LOW)



VOLTAGE WAVEFORMS
OPEN-DRAIN OUTPUT TRANSITION TIME
(LOW-TO-HIGH)



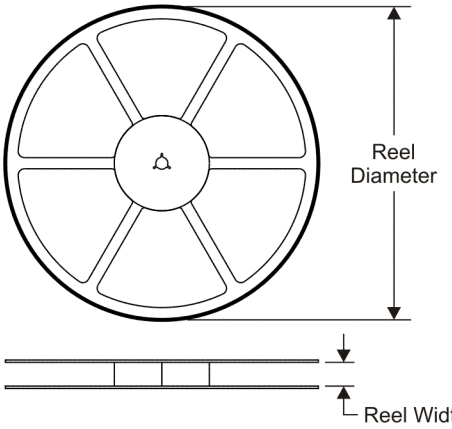
VOLTAGE WAVEFORMS
OPEN-DRAIN OUTPUT TRANSITION TIME
(LOW-TO-HIGH)

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, input slew rate = 1 V/ns ±20% (unless otherwise noted).
C. t_{PLH} and t_{PHL} are the same as t_{pd}.

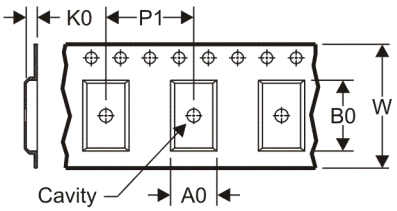
Figure 4. Error Output Load Circuit and Voltage Waveforms

TAPE AND REEL INFORMATION

REEL DIMENSIONS

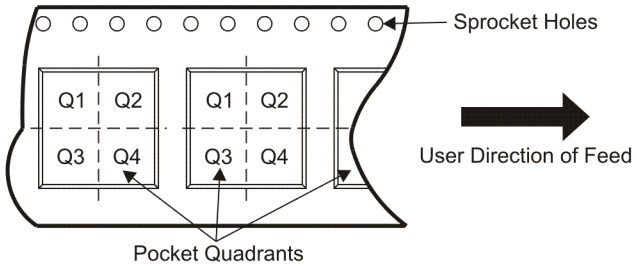


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

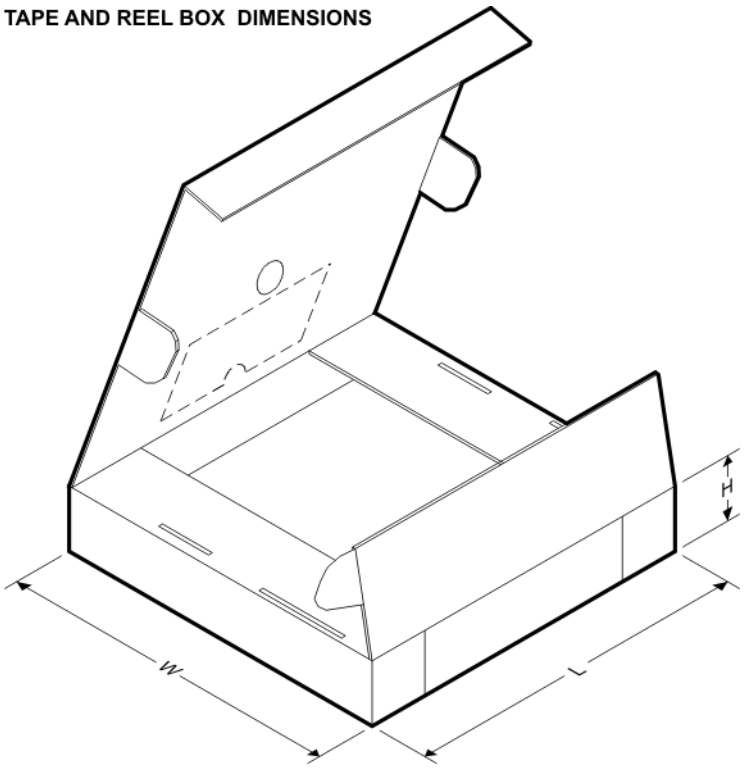
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74SSTUB32865AZJBR	NFBGA	ZJB	160	1000	330.0	24.4	9.3	13.3	1.9	12.0	24.0	Q1

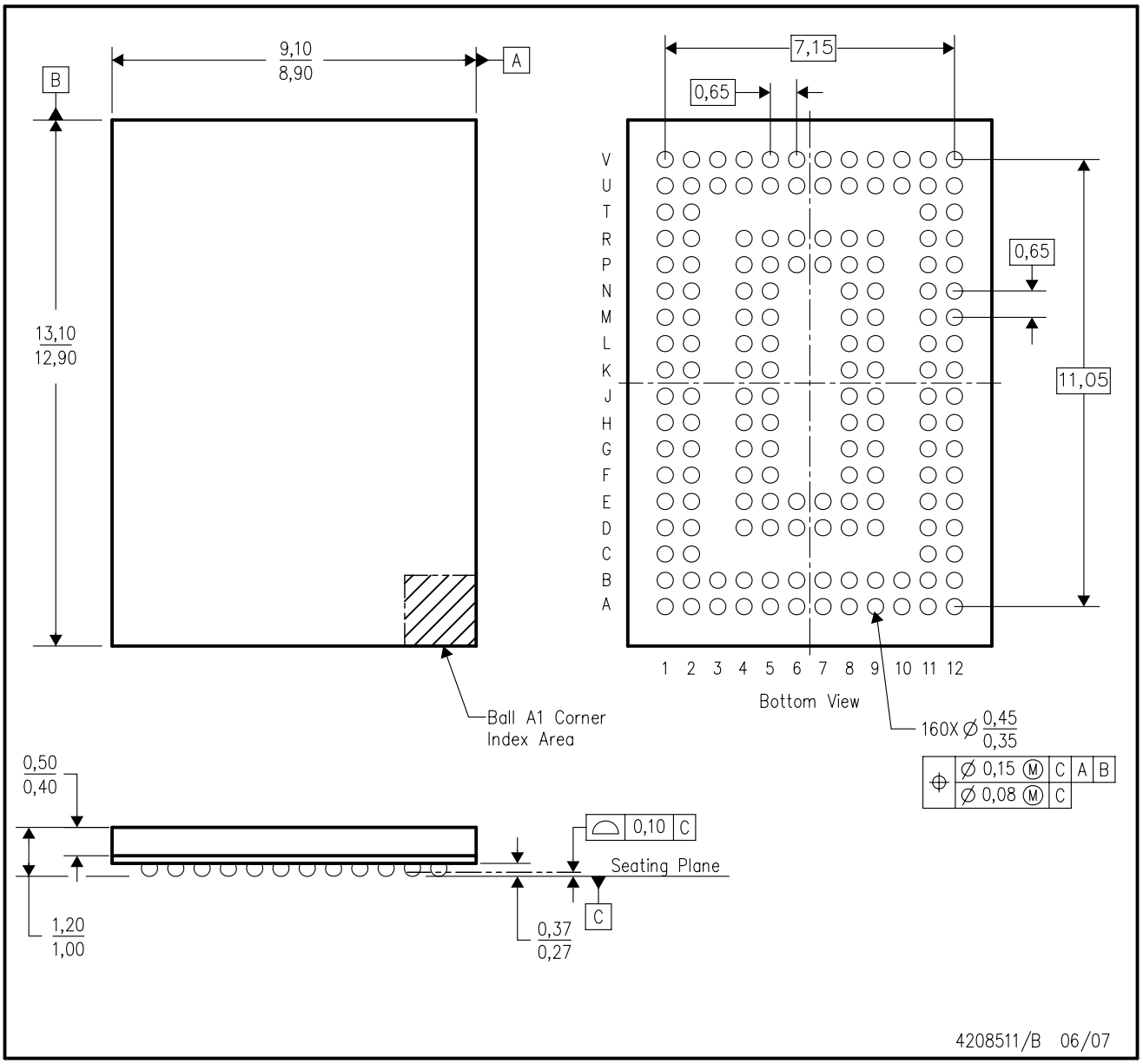
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74SSTUB32865AZJBR	NFBGA	ZJB	160	1000	333.2	345.9	31.8

ZJB (R–PBGA–N160) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a lead–free solder ball design.
D. Falls within Jedec MO 246

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