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74LVX273 Low Voltage Octal D-Type Flip-Flop

General Description

The LVX273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (\overline{MR}) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the \overline{MR} input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

Features

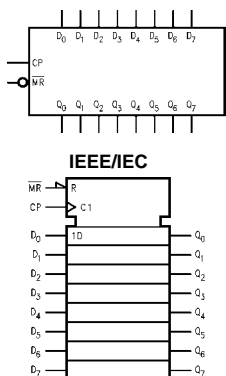
- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Ordering Code:

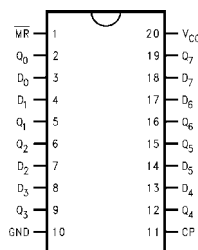
| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| 74LVX273M | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74LVX273SJ | M20D | Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74LVX273MTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |

Devices also available in Tape and Reel. Specify by appending letter suffix "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Logic Symbols



Connection Diagram



Pin Descriptions

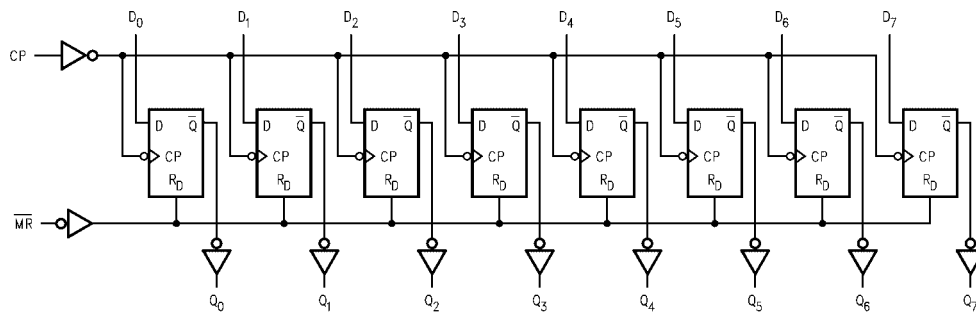
| Pin Names | Description |
|--------------------------------|-------------------|
| D ₀ -D ₇ | Data Inputs |
| \overline{MR} | Master Reset |
| CP | Clock Pulse Input |
| Q ₀ -Q ₇ | Data Outputs |

Truth Table

| Operating Mode | Inputs | | | Outputs |
|----------------|-----------------|----|----------------|----------------|
| | \overline{MR} | CP | D _n | Q _n |
| Reset (Clear) | L | X | X | L |
| Load '1' | H | ↗ | H | H |
| Load '0' | H | ↗ | L | L |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

| | |
|--------------------------------------|--------------------------|
| Supply Voltage (V_{CC}) | -0.5V to +7.0V |
| DC Input Diode Current (I_{IK}) | |
| $V_I = -0.5V$ | -20 mA |
| DC Input Voltage (V_I) | -0.5V to 7V |
| DC Output Diode Current (I_{OK}) | |
| $V_O = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | +20 mA |
| DC Output Voltage (V_O) | -0.5V to $V_{CC} + 0.5V$ |
| DC Output Source | |
| or Sink Current (I_O) | ± 25 mA |
| DC V_{CC} or Ground Current | |
| (I_{CC} or I_{GND}) | ± 75 mA |
| Storage Temperature (T_{STG}) | -65°C to +150°C |
| Power Dissipation | 180 mW |

Recommended Operating Conditions (Note 2)

| | |
|--|--------------------|
| Supply Voltage (V_{CC}) | 2.0V to 3.6V |
| Input Voltage (V_I) | 0V to 5.5V |
| Output Voltage (V_O) | 0V to V_{CC} |
| Operating Temperature (T_A) | -40°C to +85°C |
| Input Rise and Fall Time ($\Delta t/\Delta V$) | 0 ns/V to 100 ns/V |

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

| Symbol | Parameter | V_{CC} | $T_A = +25^\circ\text{C}$ | | | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ | | Units | Conditions |
|----------|-------------------------------------|----------|---------------------------|-----|------------|---|-----------|---------------|--|
| | | | Min | Typ | Max | Min | Max | | |
| V_{IH} | HIGH Level Input Voltage | 2.0 | 1.5 | | | 1.5 | | V | |
| | | 3.0 | 2.0 | | | 2.0 | | | |
| | | 3.6 | 2.4 | | | 2.4 | | | |
| V_{IL} | LOW Level Input Voltage | 2.0 | | | 0.5 | | 0.5 | V | |
| | | 3.0 | | | 0.8 | | 0.8 | | |
| | | 3.6 | | | 0.8 | | 0.8 | | |
| V_{OH} | HIGH Level Output Voltage | 2.0 | 1.9 | 2.0 | | 1.9 | | V | $V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50 \mu\text{A}$ $I_{OH} = -50 \mu\text{A}$ $I_{OH} = -4 \text{mA}$ |
| | | 3.0 | 2.9 | 3.0 | | 2.9 | | | |
| | | 3.0 | 2.58 | | | 2.48 | | | |
| V_{OL} | LOW Level Output Voltage | 2.0 | | 0.0 | 0.1 | | 0.1 | V | $V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50 \mu\text{A}$ $I_{OL} = 50 \mu\text{A}$ $I_{OL} = 4 \text{mA}$ |
| | | 3.0 | | 0.0 | 0.1 | | 0.1 | | |
| | | 3.0 | | | 0.36 | | 0.44 | | |
| I_{OZ} | 3-STATE Output Off-State Current | 3.6 | | | ± 0.25 | | ± 2.5 | μA | $V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND |
| I_{IN} | Input Leakage Current | 3.6 | | | ± 0.1 | | ± 1.0 | μA | $V_{IN} = 5.5V$ or GND |
| I_{CC} | Quiescent Supply Current | 3.6 | | | 4.0 | | 40.0 | μA | $V_{IN} = V_{CC}$ or GND |

Noise Characteristics (Note 3)

| Symbol | Parameter | V_{CC} (V) | $T_A = 25^\circ\text{C}$ | | Units | C_L (pF) |
|-----------|--|-----------------|--------------------------|-------|-------|------------|
| | | | Typ | Limit | | |
| V_{OLP} | Quiet Output Maximum Dynamic V_{OL} | 3.3 | 0.5 | 0.8 | V | 50 |
| V_{OLV} | Quiet Output Minimum Dynamic V_{OL} | 3.3 | -0.5 | -0.8 | V | 50 |
| V_{IHD} | Minimum HIGH Level Dynamic Input Voltage | 3.3 | | 2.0 | V | 50 |
| V_{ILD} | Maximum LOW Level Dynamic Input Voltage | 3.3 | | 0.8 | V | 50 |

Note 3: Input $t_r = t_f = 3\text{ns}$

AC Electrical Characteristics

| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | | T _A = -40°C to +85°C | | Units | C _L (pF) |
|-------------------|--|------------------------|------------------------|------|------|---------------------------------|------|-------|---------------------|
| | | | Min | Typ | Max | Min | Max | | |
| t _{PLH} | Propagation Delay Time | 2.7 | | 9.0 | 16.9 | 1.0 | 20.5 | ns | 15 |
| t _{PHL} | CP to Q _n | | | 11.5 | 20.0 | 1.0 | 24.0 | | 50 |
| | | 3.3 ± 0.3 | | 7.1 | 11.0 | 1.0 | 13.0 | | 15 |
| | | | | 9.6 | 14.5 | 1.0 | 16.5 | | 50 |
| t _{PHL} | Propagation Delay MR to Q _n | 2.7 | | 9.3 | 17.8 | 1.0 | 20.5 | ns | 15 |
| | | | | 11.8 | 21.1 | 1.0 | 24.0 | | 50 |
| | | 3.3 ± 0.3 | | 7.3 | 11.5 | 1.0 | 13.5 | | 15 |
| | | | | 9.8 | 15.0 | 1.0 | 17.0 | | 50 |
| t _S | Setup Time D _n to CP | 2.7 | 8.0 | | | 9.5 | | ns | |
| | | 3.3 ± 0.3 | 5.5 | | | 6.5 | | | |
| t _H | Hold Time D _n to CP | 2.7 | 1.0 | | | 1.0 | | ns | |
| | | 3.3 ± 0.3 | 1.0 | | | 1.0 | | | |
| t _{REC} | Removal Time MR to CP | 2.7 | 4.0 | | | 4.0 | | ns | |
| | | 3.3 ± 0.3 | 2.5 | | | 2.5 | | | |
| t _W | Clock Pulse Width | 2.7 | 8.0 | | | 9.5 | | ns | |
| | | 3.3 ± 0.3 | 5.5 | | | 6.5 | | | |
| t _W | MR Pulse Width | 2.7 | 7.5 | | | 8.5 | | ns | |
| | | 3.3 ± 0.3 | 5.0 | | | 6.0 | | | |
| f _{MAX} | Maximum Clock Frequency | 2.7 | 55 | 110 | | 45 | | MHz | 15 |
| | | | 45 | 60 | | 40 | | | 50 |
| | | 3.3 ± 0.3 | 95 | 150 | | 80 | | | 15 |
| | | | 60 | 90 | | 50 | | | 50 |
| t _{OSLH} | Output to Output Skew (Note 4) | 2.7 | | | 1.5 | | 1.5 | ns | 50 |
| t _{OSHL} | | 3.3 | | | 1.5 | | 1.5 | | |

Note 4: Parameter guaranteed by design. t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|

Capacitance

| Symbol | Parameter | T _A = +25°C | | | T _A = -40°C to +85°C | | Units |
|------------------|--|------------------------|-----|-----|---------------------------------|-----|-------|
| | | Min | Typ | Max | Min | Max | |
| C _{IN} | Input Capacitance | | 4 | 10 | | 10 | pF |
| C _{OUT} | Output Capacitance | | 6 | | | | pF |
| C _{PD} | Power Dissipation Capacitance (Note 5) | | 31 | | | | pF |

Note 5: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

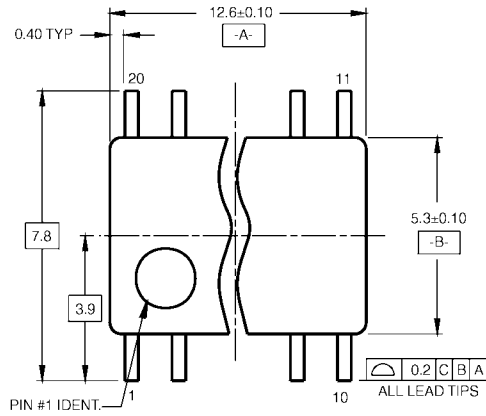
$$\text{Average operating current can be obtained by the equation: } I_{CC(\text{opr.})} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{8 \text{ (per F/F)}}$$

Physical Dimensions inches (millimeters) unless otherwise noted

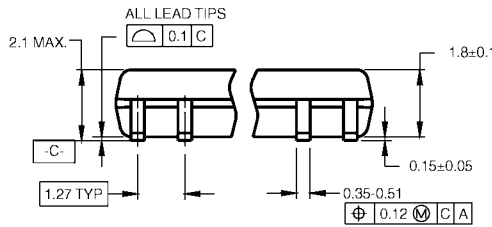


**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



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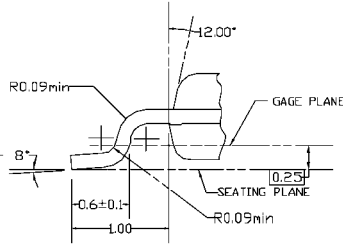
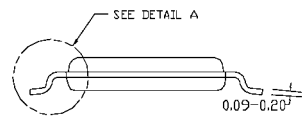
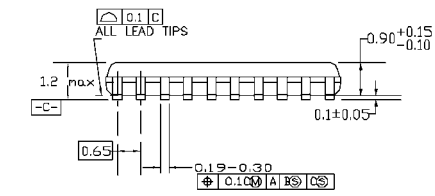
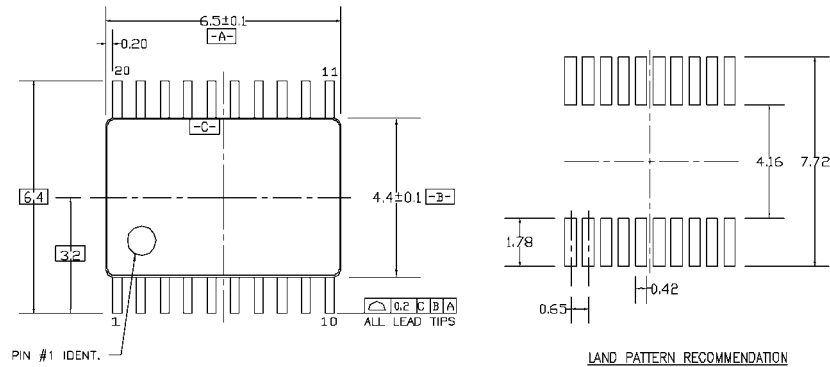
DETAIL A

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M20DRevB1

Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

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MTC20REVD1

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20

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