

# DATA SHEET

## **74LVT32374**

**3.3 V 32-bit edge-triggered D-type  
flip-flop; 3-state**

Product specification  
Supersedes data of 2002 Mar 20

2004 Oct 15

### 3.3 V 32-bit edge-triggered D-type flip-flop; 3-state

## 74LVT32374

#### FEATURES

- 32-bit edge-triggered flip-flop
- 3-state buffers
- Output capability: +64 mA/-32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- Latch-up protection exceeds 500 mA in accordance with JEDEC std 17
- ESD protection exceeds 2000 V in accordance with MIL STD 883 method 3015 and 200 V in accordance with machine model.

#### DESCRIPTION

The 74LVT32374 is a high-performance BICMOS product designed for  $V_{CC}$  operation at 3.3 V.

The 74LVT32374 is a 32-bit edge-triggered D-type flip-flop featuring non-inverting 3-state outputs. The device can be used as four 8-bit flip-flops, or two 16-bit flip-flops or one 32-bit flip-flop. On the positive transition of the clock (CP), the Q outputs of the flip-flop take on the logic levels set-up at the D inputs.

#### QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f \leq 2.5\text{ ns}$ .

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	propagation delay nCP to nQ <sub>n</sub>	$C_L = 50\text{ pF}$ ; $V_{CC} = 3.3\text{ V}$	2.9	ns
$C_I$	input capacitance	$V_I = 0\text{ V}$ or $3.0\text{ V}$	3	pF
$C_O$	output capacitance	outputs disabled; $V_O = 0\text{ V}$ or $3.0\text{ V}$	9	pF
$I_{CCZ}$	total supply current	output disabled; $V_{CC} = 3.6\text{ V}$	140	$\mu\text{A}$

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#### FUNCTION TABLE

See note 1.

OPERATING MODE	INPUT			INTERNAL REGISTER	OUTPUT
	$\overline{\text{nOE}}$	nCP	nD <sub>n</sub>		nQ <sub>n</sub>
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Hold	L	↑ +	X	NC	NC
Disable outputs	H	↑ +	X	NC	Z
	H	↑	nD <sub>n</sub>	nD <sub>n</sub>	Z

#### Note

- H = HIGH voltage level;  
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW OE transition;  
L = LOW voltage level;  
l = LOW voltage level one set-up time prior to the HIGH-to-LOW OE transition;  
NC = not connected;  
X = don't care;  
Z = high-impedance OFF-state;  
↑ = LOW-to-HIGH CP transition;  
↑  
+ = not a LOW-to-HIGH CP transition.

#### ORDERING INFORMATION

TYPE NUMBER	TEMPERATURE RANGE	PACKAGE			
		PINS	PACKAGE	MATERIAL	CODE
74LVT32374EC	-40 °C to +85 °C	96	LFPGA96	plastic	SOT536-1

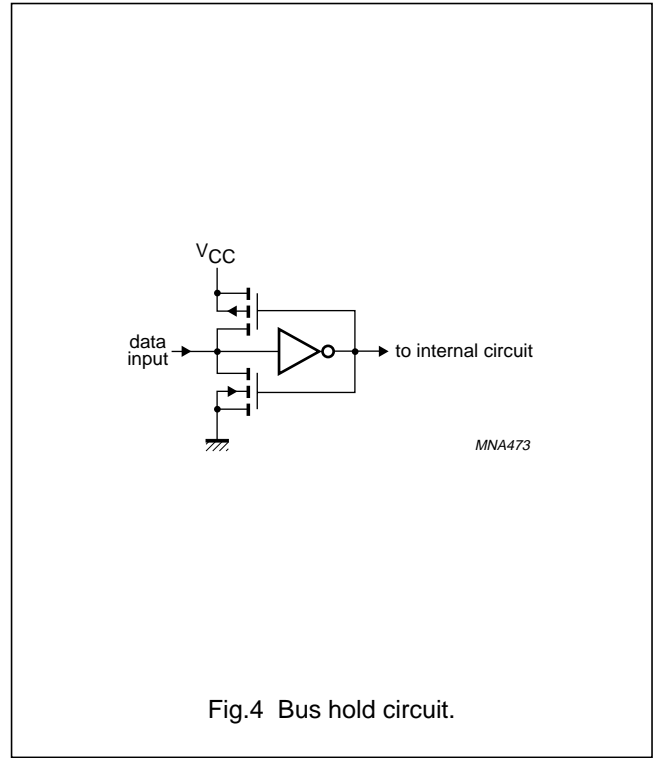
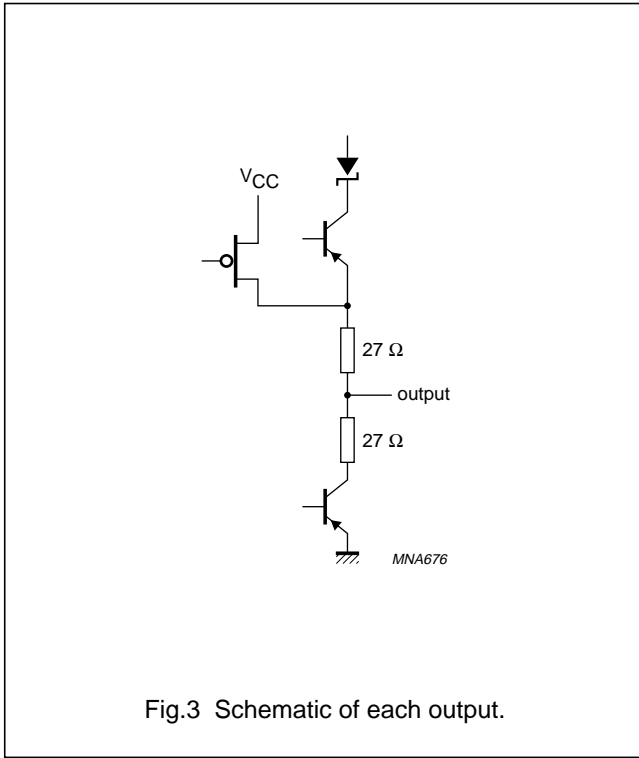
#### PINNING

SYMBOL	DESCRIPTION
nD <sub>n</sub>	data input
nCP	clock input
nQ <sub>n</sub>	flip-flop output
GND	ground (0 V)
$\overline{\text{nOE}}$	output enable input (active LOW)
V <sub>CC</sub>	supply voltage



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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage		2.7	+3.6	V
V <sub>I</sub>	input voltage	note 1	0	5.5	V
V <sub>IH</sub>	HIGH-level input voltage		2.0	–	V
V <sub>IL</sub>	LOW-level input voltage		–	0.8	V
I <sub>OH</sub>	HIGH-level output current		–	–32	mA
I <sub>OL</sub>	LOW-level output current		–	32	mA
		current duty cycle ≤ 50 %; f ≥ 1 kHz	–	64	mA
Δt/ΔV	input transition rise or fall times	outputs enabled	–	10	ns/V
T <sub>amb</sub>	ambient temperature		–40	+85	°C
P <sub>tot</sub>	power dissipation per package	note 2	–	1000	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 70 °C the value of P<sub>tot</sub> derates linearly with 1.8 mW/K.

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#### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CC}$	supply voltage		-0.5	-	+4.6	V
$I_{IK}$	input diode current	$V_I < 0$ V	-	-50	-	mA
$V_I$	input voltage	note 2	-0.5	-	+7.0	V
$I_{OK}$	output diode current		-	-50	-	mA
$V_O$	output voltage	output in OFF or HIGH state; note 2	-0.5	-	+7.0	V
$I_O$	output current	output in LOW state	-	128	-	mA
		output in HIGH state	-	-64	-	mA
$T_{stg}$	storage temperature		-65	-	+150	°C

#### Notes

1. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
2. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

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#### DC CHARACTERISTICS

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>							
V <sub>IK</sub>	input clamp voltage	I <sub>IK</sub> = -18 mA	2.7	-	-0.85	-1.2	V
V <sub>OH</sub>	HIGH-level output voltage	I <sub>OH</sub> = -32 mA	3.0	2.0	2.3	-	V
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 64 mA	3.0	-	0.4	0.55	V
V <sub>RST</sub>	power-up output LOW voltage	I <sub>O</sub> = -1 mA; V <sub>I</sub> = GND or V <sub>CC</sub> ; note 2	3.6	-	0.1	0.55	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; control pins	3.6	-	0.1	±1	μA
		V <sub>I</sub> = 5.5 V	0 or 3.6	-	0.4	10	μA
		V <sub>I</sub> = V <sub>CC</sub> ; data pins; note 3	3.6	-	0.1	1	μA
		V <sub>I</sub> = 0 V; data pins; note 3	3.6	-	-0.4	-5	μA
I <sub>off</sub>	output OFF current	V <sub>I</sub> or V <sub>O</sub> = 0 V to 4.5 V	0	-	0.1	±100	μA
I <sub>hold</sub>	bus hold current D inputs	V <sub>I</sub> = 0.8 V; note 4	3.0	75	135	-	μA
		V <sub>I</sub> = 2.0 V; note 4	3.0	-75	-135	-	μA
		V <sub>CC</sub> = 3.6 V; note 4	0 to 3.6	±500	-	-	μA
I <sub>EX</sub>	current into an output in the HIGH state when V <sub>O</sub> > V <sub>CC</sub>	V <sub>O</sub> = 5.5 V	3.0	-	50	125	μA
I <sub>pu/pd</sub>	power-up/down 3-state output current	V <sub>O</sub> = 5.5 V to V <sub>CC</sub> ; V <sub>I</sub> = GND or V <sub>CC</sub> ; V <sub>OE</sub> = don't care; note 5	≤ 1.2 V	-	1	±100	μA
I <sub>OZH</sub>	3-state output HIGH current	V <sub>O</sub> = 3.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	3.6	-	0.5	5	μA
I <sub>OZL</sub>	3-state output LOW current	V <sub>O</sub> = 0.5 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	3.6	-	+0.5	-5	μA
I <sub>CCH</sub>	quiescent supply current	outputs HIGH; I <sub>O</sub> = 0 A; V <sub>I</sub> = GND or V <sub>CC</sub>	3.6	-	0.14	0.24	mA
I <sub>CCL</sub>	quiescent supply current	outputs LOW; I <sub>O</sub> = 0 A; V <sub>I</sub> = GND or V <sub>CC</sub>	3.6	-	8	12	mA
I <sub>CCZ</sub>	quiescent supply current	outputs disabled; I <sub>O</sub> = 0 A; V <sub>I</sub> = GND or V <sub>CC</sub> ; note 6	3.6	-	0.14	0.24	mA
ΔI <sub>CC</sub>	additional supply current per input pin	one input at V <sub>CC</sub> - 0.6 V; other inputs at GND or V <sub>CC</sub> ; note 7	3.0 to 3.6	-	0.1	0.2	μA

#### Notes

- All typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
- Unused pins at V<sub>CC</sub> or GND.
- This is the bus hold overdrive current required to force the input to the opposite logic state.
- This parameter is valid for any V<sub>CC</sub> between 0 V and 1.2 V with a transition time of up to 10 ms. From V<sub>CC</sub> = 1.2 V to V<sub>CC</sub> = 3.3 V ± 0.3 V a transition time of 100 μs is permitted. This parameter is valid for T<sub>amb</sub> = 25 °C only.
- I<sub>CCZ</sub> is measured with outputs pulled to V<sub>CC</sub> or GND.
- This is the increase in supply current for each input at the specified voltage level other than V<sub>CC</sub> or GND.

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**AC CHARACTERISTICS**GND = 0 V;  $t_r = t_f \leq 2.5$  ns;  $C_L = 50$  pF;  $R_L = 500$   $\Omega$ .

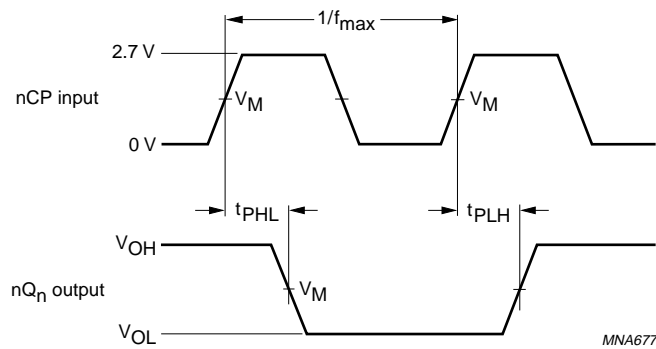
SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>							
t <sub>PLH</sub>	propagation delay nCP to nQ <sub>n</sub>	see Fig.5	2.7	–	–	6.2	ns
			3.0 to 3.6	1.5	3.0	5.3	ns
t <sub>PHL</sub>	propagation delay nCP to nQ <sub>n</sub>	see Fig.5	2.7	–	–	5.1	ns
			3.0 to 3.6	1.5	3.0	4.9	ns
t <sub>PZH</sub>	output enable time to HIGH level	see Figs 7 and 8	2.7	–	–	6.9	ns
			3.0 to 3.6	1.5	3.5	5.6	ns
t <sub>PZL</sub>	output enable time to LOW level	see Figs 7 and 8	2.7	–	–	6.0	ns
			3.0 to 3.6	1.5	3.2	4.9	ns
t <sub>PHZ</sub>	output disable time from HIGH level	see Figs 7 and 8	2.7	–	–	5.7	ns
			3.0 to 3.6	1.5	3.5	5.4	ns
t <sub>PLZ</sub>	output disable time from LOW level	see Figs 7 and 8	2.7	1.5	3.2	5.1	ns
			3.0 to 3.6	1.5	3.2	5.0	ns
t <sub>suH</sub>	set-up time nD <sub>n</sub> HIGH to nCP	see Fig.6	2.7	2.0	–	–	ns
			3.0 to 3.6	2.0	0.7	–	ns
t <sub>suL</sub>	set-up time nD <sub>n</sub> LOW to nCP	see Fig.6	2.7	2.0	–	–	ns
			3.0 to 3.6	2.0	0.7	–	ns
t <sub>hH</sub>	hold time nD <sub>n</sub> HIGH to nCP	see Fig.6	2.7	0.1	–	–	ns
			3.0 to 3.6	0.8	0	–	ns
t <sub>hL</sub>	hold time nD <sub>n</sub> LOW to nCP	see Fig.6	2.7	0.1	–	–	ns
			3.0 to 3.6	0.8	0	–	ns
t <sub>WH</sub>	nCP HIGH pulse width	see Fig.6	2.7	1.5	–	–	ns
			3.0 to 3.6	1.5	0.6	–	ns
t <sub>WL</sub>	nCP LOW pulse width	see Fig.6	2.7	3.0	–	–	ns
			3.0 to 3.6	3.0	1.6	–	ns
f <sub>max</sub>	maximum clock pulse frequency	see Fig.5	3.0 to 3.6	150	–	–	MHz

**Note**1. All typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

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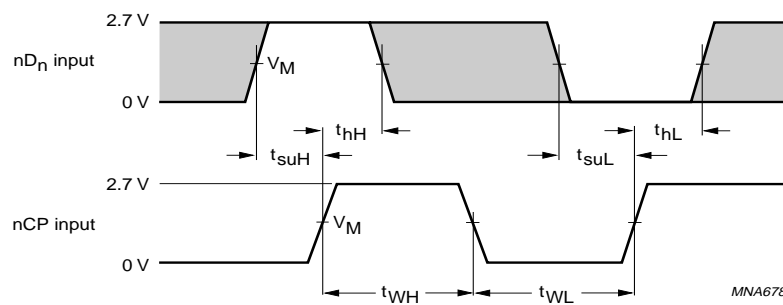
AC WAVEFORMS



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$V_M = 1.5\text{ V};$   
 $V_M = \text{GND to } 3.0\text{ V}.$

Fig.5 Clock (nCP) to output (nQ<sub>n</sub>) propagation delays, the clock pulse width and the maximum clock pulse frequency.



MNA678

The shaded areas indicate when the input is permitted to change for predicable output performance.

Fig.6 Set-up and hold times for inputs (nD<sub>n</sub>) to inputs (nCP).

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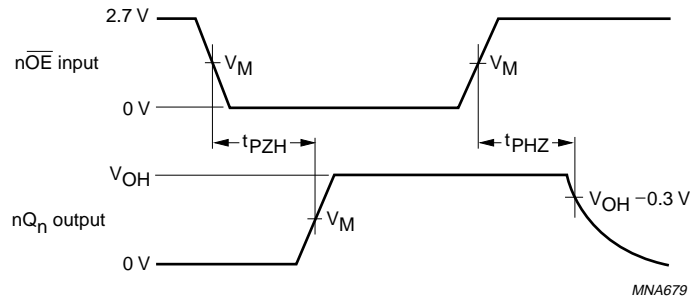


Fig.7 3-state output enable time to HIGH level and output disable time from HIGH level.

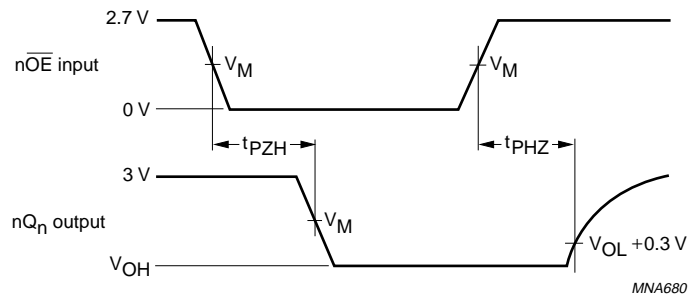
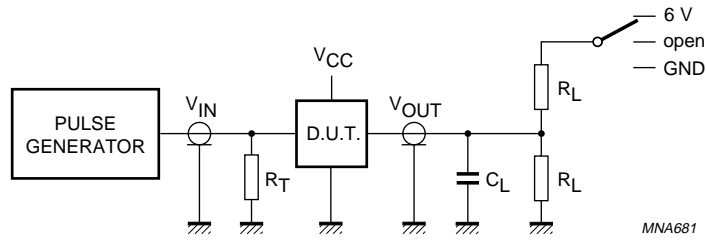


Fig.8 3-state output enable time to LOW level and output disable time from LOW level.

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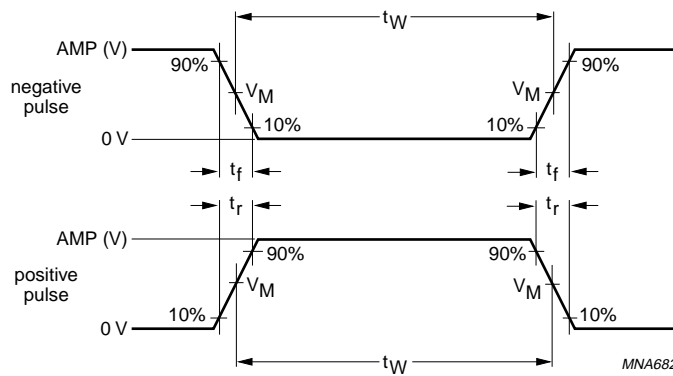
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TEST	SWITCH
$t_{PLH}/t_{PHL}$	open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND

Definitions for test circuit:  
 $R_L$  = Load resistor.  
 $C_L$  = Load capacitance including jig and probe capacitance.  
 $R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

Fig.9 Load circuitry for switching times.



INPUT PULSE REQUIREMENTS				
AMPLITUDE	PULSE RATE	$t_w$	$t_r$	$t_f$
2.7 V	$\leq 10$ MHz	500 ns	$\leq 2.5$ ns	$\leq 2.5$ ns

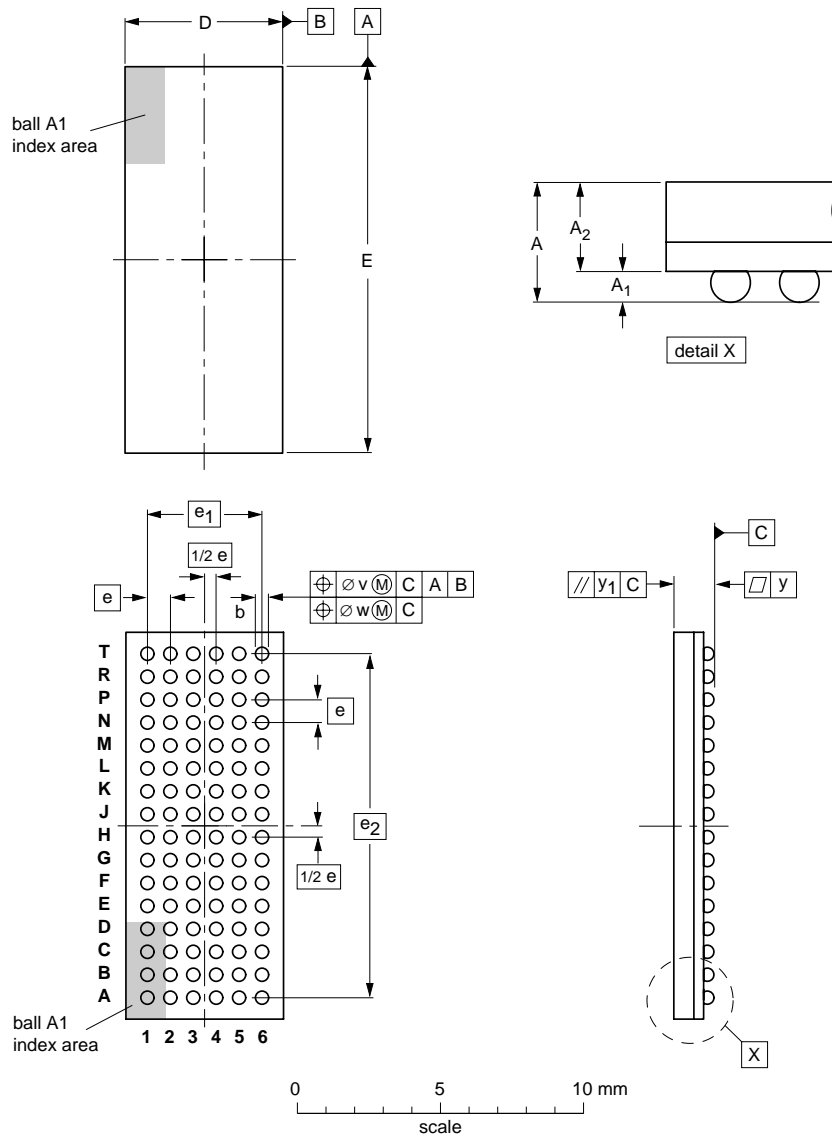
Fig.10 Input pulse definition.

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PACKAGE OUTLINE

LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	b	D	E	e	e <sub>1</sub>	e <sub>2</sub>	v	w	y	y <sub>1</sub>
mm	1.5	0.41 0.31	1.2 0.9	0.51 0.41	5.6 5.4	13.6 13.4	0.8	4	12	0.15	0.1	0.1	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT536-1						00-03-04 03-02-05

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#### DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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