



**THE DATASHEET OF
74LVT244APW,118**



74LVT244A; 74LVTH244A

3.3 V octal buffer/line driver; 3-state

Rev. 5 — 16 August 2017

Product data sheet

1 General description

The 74LVT244A; 74LVTH244A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

This device is an octal buffer that is ideal for driving bus lines. The device features two output enables ($1\overline{OE}$, $2\overline{OE}$), each controlling four of the 3-state outputs.

2 Features and benefits

- Octal bus interface
- 3-state buffers
- Output capability: +64 mA and -32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- Latch-up protection
 - JESD78 Class II exceeds 500 mA
- ESD protection:
 - HBM JESD22-A114E exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V

3 Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVT244AD	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVTH244AD				
74LVT244ADB	-40 °C to +85 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74LVTH244ADB				
74LVT244APW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74LVTH244APW				
74LVT244ABQ	-40 °C to +85 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1
74LVTH244ABQ				

4 Functional diagram

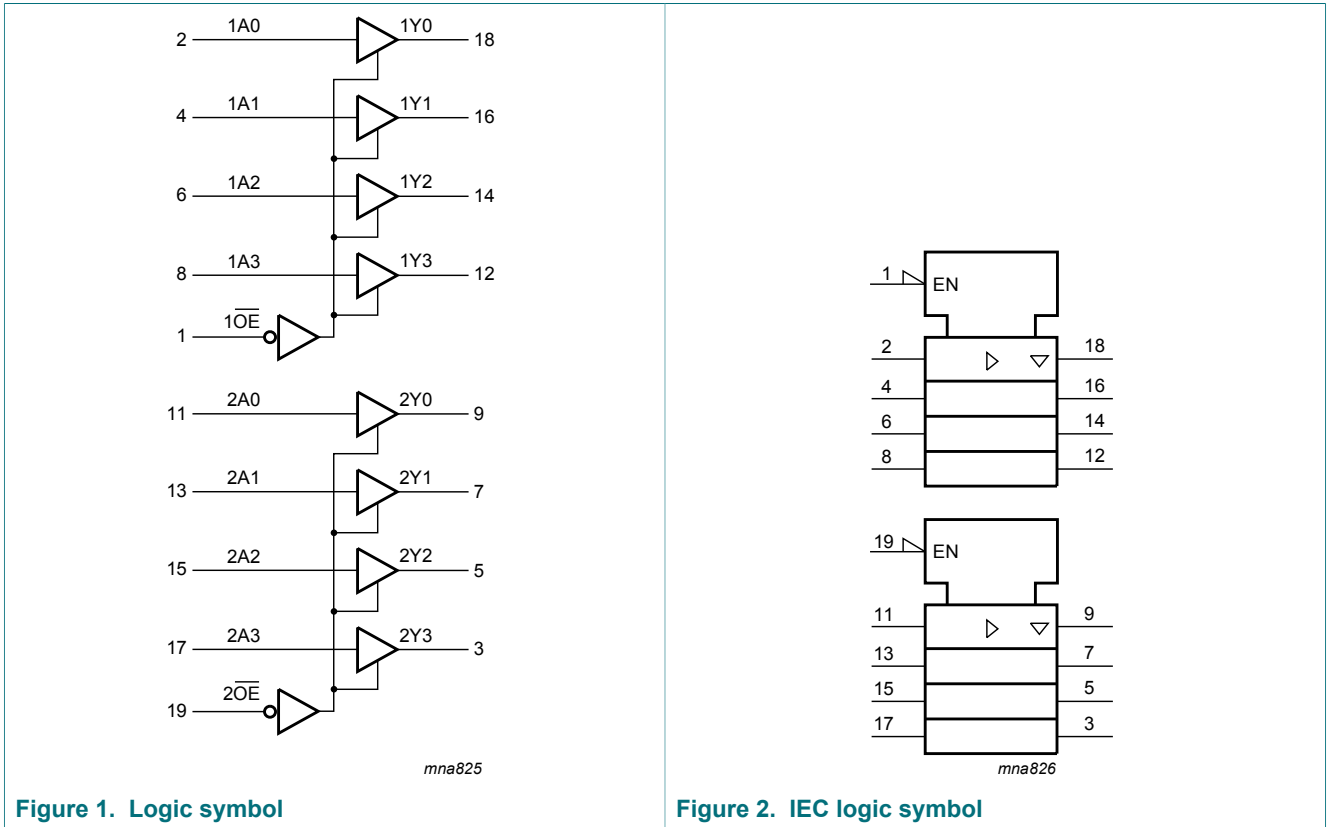


Figure 1. Logic symbol

Figure 2. IEC logic symbol

5 Pinning information

5.1 Pinning

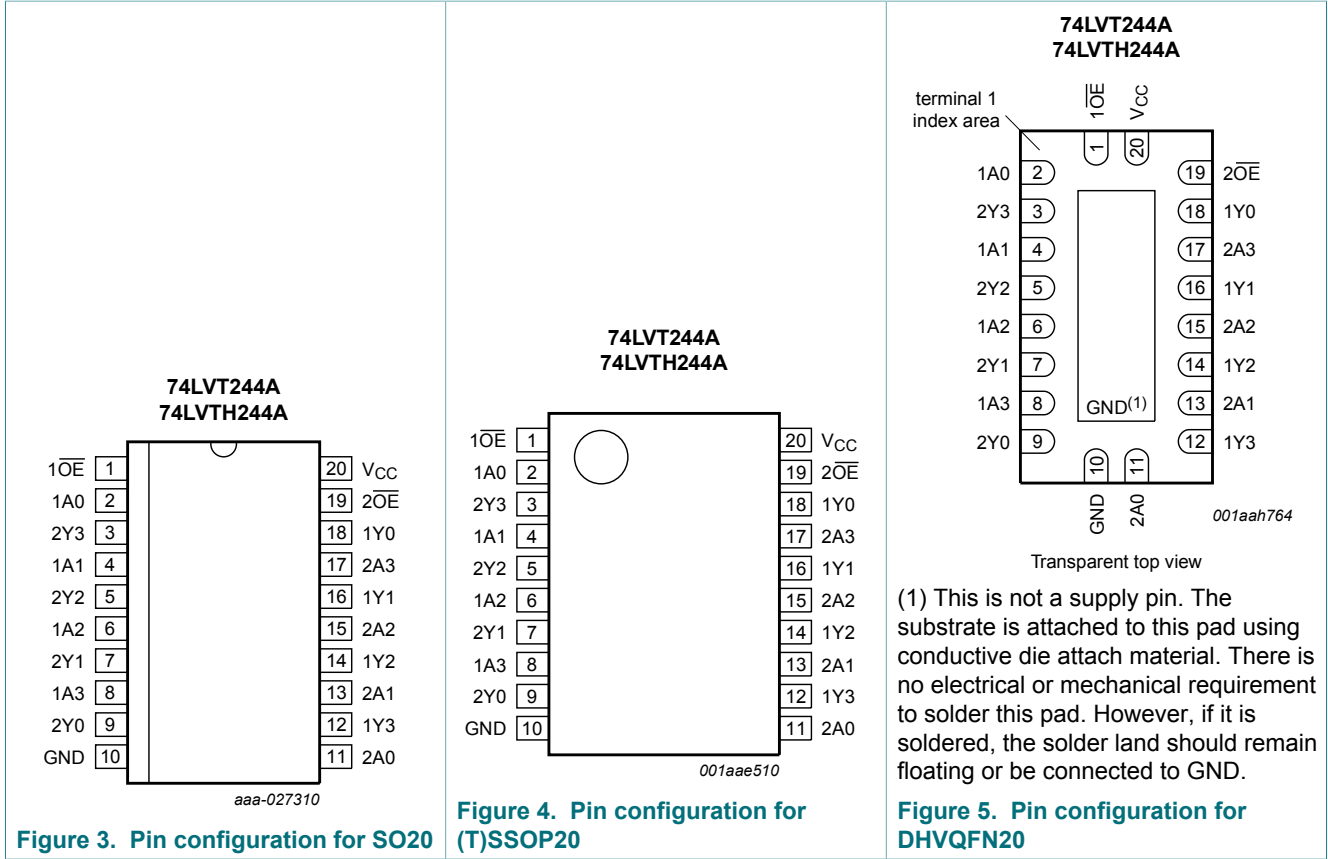


Figure 3. Pin configuration for SO20

Figure 4. Pin configuration for (T)SSOP20

Figure 5. Pin configuration for DHVQFN20

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 19	output enable input (active low)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
2Y0, 2Y1, 2Y2, 2Y3	9, 7, 5, 3	data output
GND	10	ground (0 V)
2A0, 2A1, 2A2, 2A3	11, 13, 15, 17	data input
1Y0, 1Y1, 1Y2, 1Y3	18, 16, 14, 12	data output
VCC	20	supply voltage

6 Functional description

Table 3. Function table ^[1]

Control	Input	Output
nOE	nAn	nYn
L	L	L
L	H	H
H	X	Z

- [1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care;
 Z = high-impedance OFF-state.

7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage		-0.5	+7.0	V
V _O	output voltage	output in OFF-state or HIGH-state	-0.5	+7.0	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
I _O	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-64	-	mA
T _{stg}	storage temperature		-65	+150	°C
T _j	junction temperature		-	150	°C
P _{tot}	total power dissipation	T _{amb} = -40 to +85 °C	-	500	mW

- [1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
 [2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.
 [3] For SO20 packages: above 70 °C derate linearly with 8 mW/K.
 For SSOP20 and TSSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.
 For DHVQFN20 packages: above 60 °C derate linearly with 4.5 mW/K.

8 Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.7	-	3.6	V
V_I	input voltage		0	-	5.5	V
I_{OH}	HIGH-level output current		-32	-	-	mA
I_{OL}	LOW-level output current	none	-	-	32	mA
		current duty cycle $\leq 50\%$; $f_i \geq 1$ kHz	-	-	64	mA
T_{amb}	ambient temperature	in free-air	-40	-	+85	$^{\circ}\text{C}$
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

9 Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$						
V_{IK}	input clamping voltage	$V_{CC} = 2.7\text{ V}$; $I_{IK} = -18\text{ mA}$	-1.2	-0.9	-	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_{CC} = 2.7\text{ V}$ to 3.6 V ; $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$	$V_{CC} - 0.1$	-	V
		$V_{CC} = 2.7\text{ V}$ to 3.6 V ; $I_{OH} = -8\text{ mA}$	2.4	2.5	-	V
		$V_{CC} = 3.0\text{ V}$; $I_{OH} = -32\text{ mA}$	2.0	2.2	-	V
V_{OL}	LOW-level output voltage	$V_{CC} = 2.7\text{ V}$; $I_{OL} = 100\text{ }\mu\text{A}$	-	0.1	0.2	V
		$V_{CC} = 2.7\text{ V}$; $I_{OL} = 24\text{ mA}$	-	0.3	0.5	V
		$V_{CC} = 3.0\text{ V}$; $I_{OL} = 16\text{ mA}$	-	0.25	0.4	V
		$V_{CC} = 3.0\text{ V}$; $I_{OL} = 32\text{ mA}$	-	0.3	0.5	V
		$V_{CC} = 3.0\text{ V}$; $I_{OL} = 64\text{ mA}$	-	0.4	0.55	V
I_I	input leakage current	all input pins				
		$V_{CC} = 0\text{ V}$ or 3.6 V ; $V_I = 5.5\text{ V}$	-	0.1	10	μA
		control pins				
		$V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$ or GND	-	± 0.1	± 1	μA
		data pins ^[2]				
	$V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$	-	0.1	1	μA	
	$V_{CC} = 3.6\text{ V}$; $V_I = 0\text{ V}$	-5	-1	-	μA	
I_{OFF}	power-off leakage current	$V_{CC} = 0\text{ V}$; V_I or $V_O = 0\text{ V}$ to 4.5 V	-	1	± 100	μA
I_{BHL}	bus hold LOW current	$V_{CC} = 3\text{ V}$; $V_I = 0.8\text{ V}$	75	150	-	μA
I_{BHH}	bus hold HIGH current	$V_{CC} = 3\text{ V}$; $V_I = 2.0\text{ V}$	-	-150	-75	μA

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
I_{BHLO}	bus hold LOW overdrive current	nAn input; $V_{CC} = 3.6\text{ V}$; $V_I = 0\text{ V to }3.6\text{ V}$ ^[3]	500	-	-	μA
I_{BHHO}	bus hold HIGH overdrive current	nAn input; $V_{CC} = 3.6\text{ V}$; $V_I = 0\text{ V to }3.6\text{ V}$ ^[3]	-	-	-500	μA
I_{EX}	external current	nYn output in HIGH-state when $V_O > V_{CC}$; $V_O = 5.5\text{ V}$; $V_{CC} = 3.0\text{ V}$	-	60	125	μA
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} \leq 1.2\text{ V}$; $V_O = 0.5\text{ V to }V_{CC}$; $V_I = \text{GND or }V_{CC}$; n \overline{OE} = don't care ^[4]	-	± 1	± 100	μA
I_{OZ}	OFF-state output current	$V_{CC} = 3.6\text{ V}$; $V_I = V_{IH}$ or V_{IL}				
		$V_O = 3.0\text{ V}$	-	1	5	μA
		$V_O = 0.5\text{ V}$	-5	-1	-	μA
I_{CC}	supply current	$V_{CC} = 3.6\text{ V}$; $V_I = \text{GND or }V_{CC}$; $I_O = 0\text{ A}$				
		output HIGH	-	0.13	0.19	mA
		output LOW	-	3	12	mA
		outputs disabled ^[5]	-	0.13	0.19	mA
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 3.0\text{ V to }3.6\text{ V}$; one input at $V_{CC} - 0.6\text{ V}$ and other inputs at V_{CC} or GND ^[6]	-	0.1	0.2	mA
C_I	input capacitance	$V_I = 0\text{ V or }3.0\text{ V}$	-	4	-	pF
C_O	output capacitance	outputs disabled; $V_O = 0\text{ V or }3.0\text{ V}$	-	8	-	pF

[1] All typical values are measured at $T_{amb} = 25\text{ }^\circ\text{C}$.

[2] Unused pins at V_{CC} or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From $V_{CC} = 1.2\text{ V}$ to $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ a transition time of 100 μs is permitted. This parameter is valid for $T_{amb} = 25\text{ }^\circ\text{C}$ only.

[5] I_{CC} is measured with outputs pulled to V_{CC} or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10 Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
$T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$						
t_{PLH}	LOW to HIGH propagation delay	nAn to nYn; see Figure 6				
		$V_{CC} = 2.7\text{ V}$	-	-	5.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1	2.5	4.1	ns
t_{PHL}	HIGH to LOW propagation delay	nAn to nYn; see Figure 6				
		$V_{CC} = 2.7\text{ V}$	-	-	5.1	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1	2.6	4.1	ns
t_{PZH}	OFF-state to HIGH propagation delay	n $\overline{O}E$ to nYn; see Figure 7				
		$V_{CC} = 2.7\text{ V}$	-	-	6.3	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1	3.2	5.2	ns
t_{PZL}	OFF-state to LOW propagation delay	n $\overline{O}E$ to nYn; see Figure 7				
		$V_{CC} = 2.7\text{ V}$	-	-	6.7	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.1	3.1	5.2	ns
t_{PHZ}	HIGH to OFF-state propagation delay	n $\overline{O}E$ to nYn; see Figure 7				
		$V_{CC} = 2.7\text{ V}$	-	-	6.3	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.9	3.3	5.6	ns
t_{PLZ}	LOW to OFF-state propagation delay	n $\overline{O}E$ to nYn; see Figure 7				
		$V_{CC} = 2.7\text{ V}$	-	-	5.6	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.8	3.3	5.1	ns

[1] All typical values are at $V_{CC} = 3.3\text{ V}$ and $T_{amb} = 25\text{ }^{\circ}\text{C}$.

10.1 Waveforms and test circuit

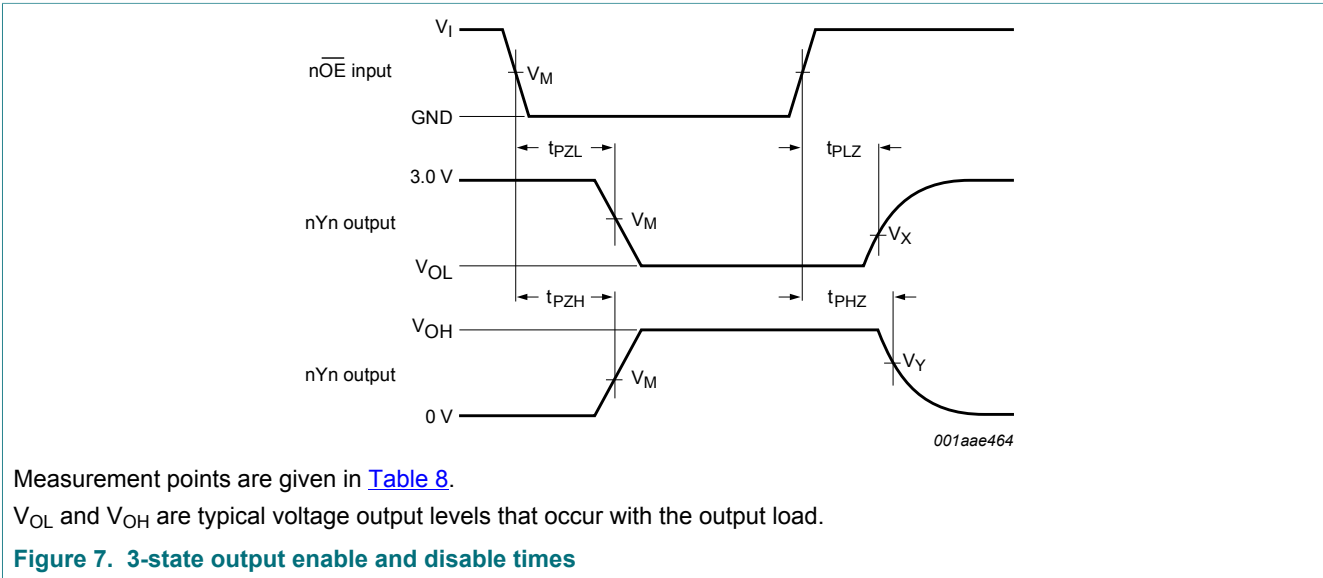
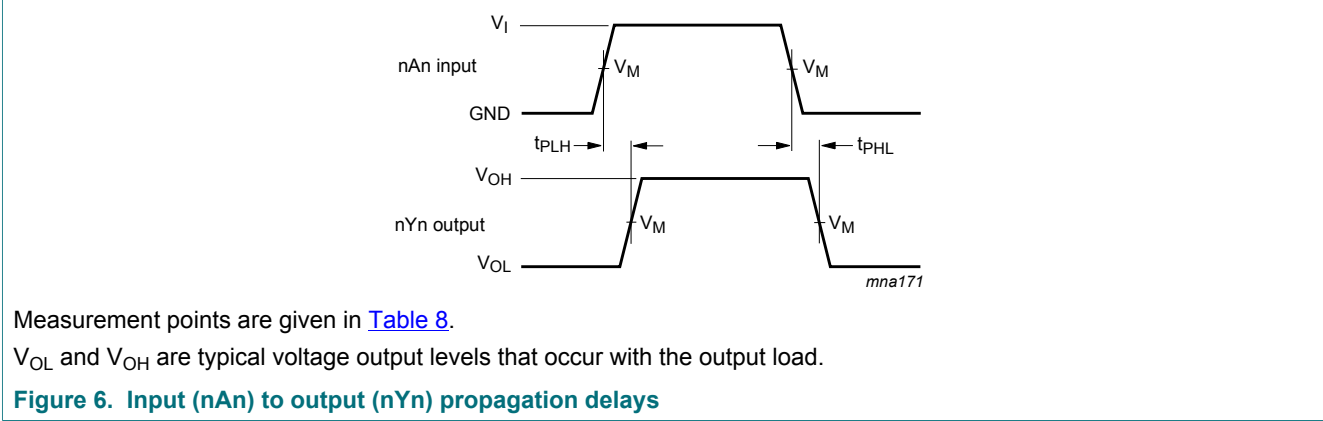
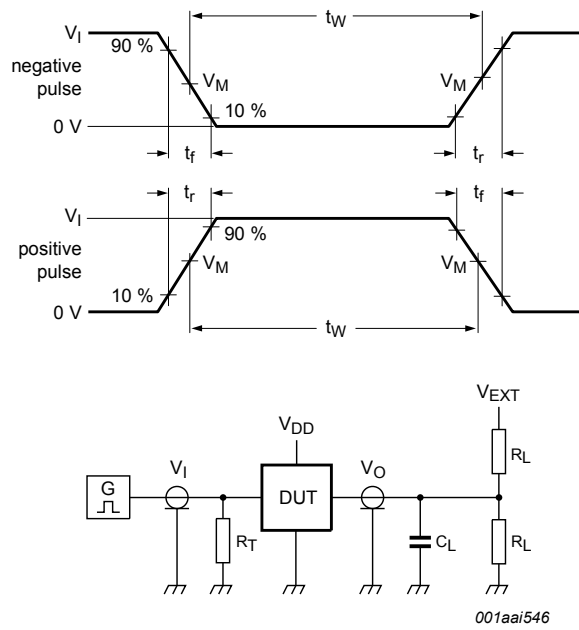


Table 8. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$



Test data is given in [Table 9](#).

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

Figure 8. Test circuit for measuring switching times

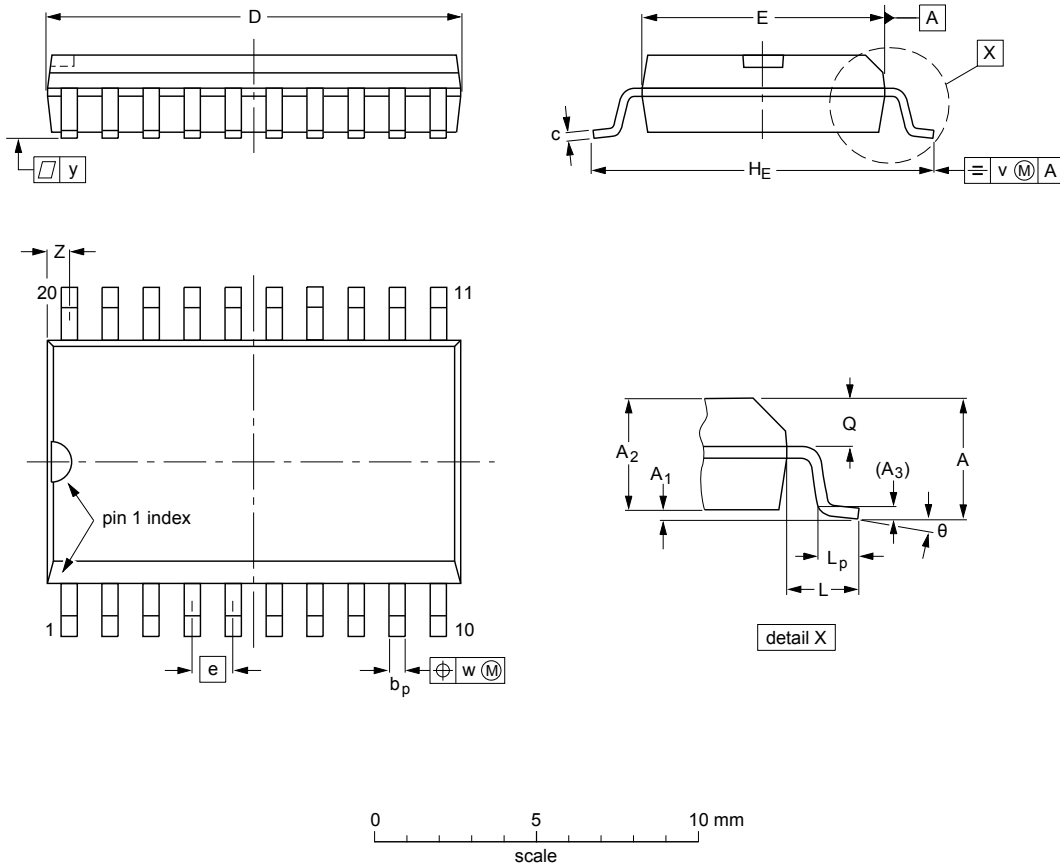
Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	GND	6 V	open

11 Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

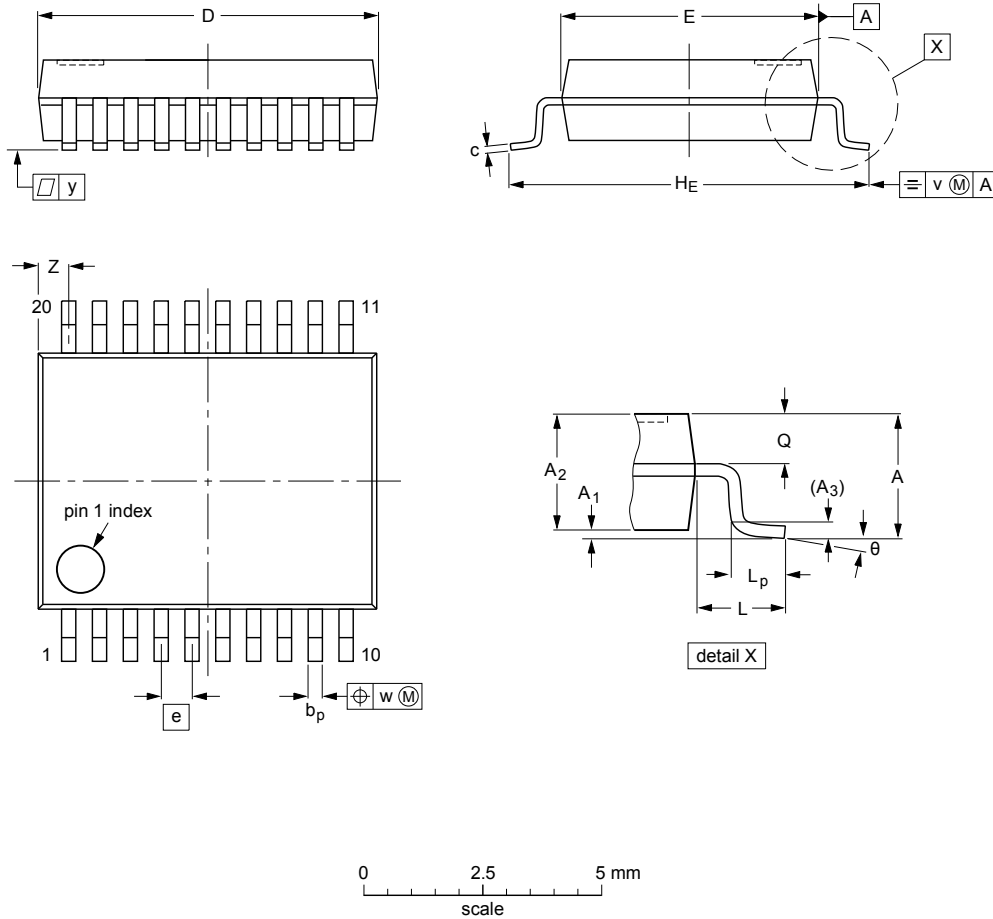
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT163-1	075E04	MS-013			99-12-27 03-02-19

Figure 9. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



DIMENSIONS (mm are the original dimensions)

UNIT	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

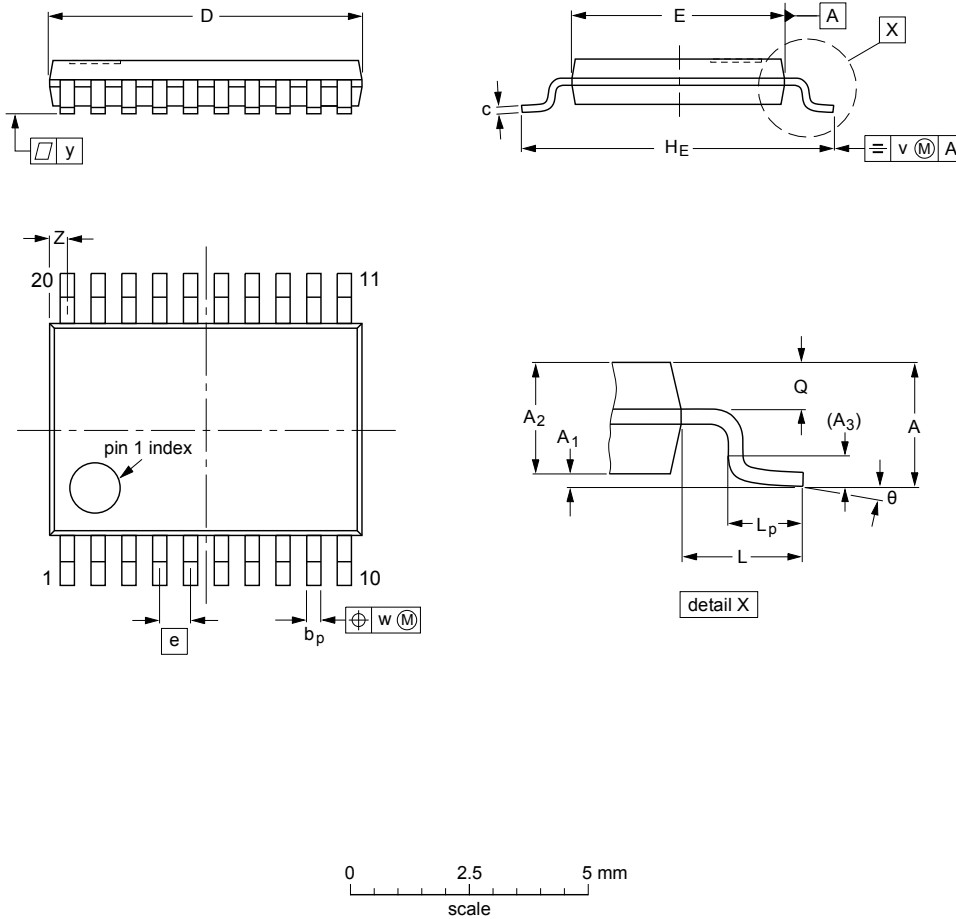
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				99-12-27 03-02-19

Figure 10. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				-99-12-27 03-02-19

Figure 11. Package outline SOT360-1 (TSSOP20)

12 Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT_LVTH244A v.5	20170816	Product data sheet	-	74LVT_LVTH244A v.4
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 			
74LVT_LVTH244A v.4	20080903	Product data sheet	-	74LVT_LVTH244A v.3
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Section 3 and Section 11 DHVQFN20 package added. 			
74LVT_LVTH244A v.3	20060315	Product specification	-	74LVT244A v.2
74LVT244A v.2	19980219	Product specification	-	74LVT244A v.1

14 Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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