



**THE DATASHEET OF
74LVT16646ADL,512**



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Team Nexperia

74LVT16646A

3.3 V 16-bit bus transceiver; 3-state

Rev. 03 — 12 January 2005

Product data sheet

1. General description

The 74LVT16646A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V. This device is a 16-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an output enable (\overline{OE}) input for easy cascading and a direction (DIR) input for direction control.

Data on bus A or bus B is clocked into the registers on the LOW-to-HIGH transition of the appropriate clock (CPAB or CPBA). The select control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode data).

2. Features

- 16-bit universal bus interface
- 3-state buffers
- Output capability: from +64 mA to -32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- No bus-current loading when output is tied to 5 V bus
- Power-up reset
- Power-up 3-state
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection:
 - ◆ MIL STD 883 Method 3 015: exceeds 2000 V
 - ◆ Machine model: exceeds 200 V

PHILIPS

3. Quick reference data

Table 1: Quick reference data

$T_{amb} = 25\text{ }^{\circ}\text{C}$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------|--|---|-----|-----|-----|---------------|
| t_{PLH} , t_{PHL} | propagation delay nAx to nBx or nBx to nAx | $C_L = 50\text{ pF}$; $V_{CC} = 3.3\text{ V}$ | - | 1.9 | - | ns |
| C_I | input capacitance | $V_I = 0\text{ V}$ or 3.0 V | - | 3 | - | pF |
| $C_{I/O}$ | I/O pin capacitance | $V_{I/O} = 0\text{ V}$ or 3.0 V ; outputs disabled | - | 9 | - | pF |
| I_{CC} | quiescent supply current | $V_{CC} = 3.6\text{ V}$; outputs disabled | - | 70 | - | μA |

4. Ordering information

Table 2: Ordering information

| Type number | Package | | | |
|----------------|-------------------|---------|--|----------|
| | Temperature range | Name | Description | Version |
| 74LVT16646ADGG | -40 °C to +85 °C | TSSOP56 | plastic thin shrink small outline package; 56 leads; body width 6.1 mm | SOT364-1 |
| 74LVT16646ADL | -40 °C to +85 °C | SSOP56 | plastic shrink small outline package; 56 leads; body width 7.5 mm | SOT371-1 |

5. Functional diagram

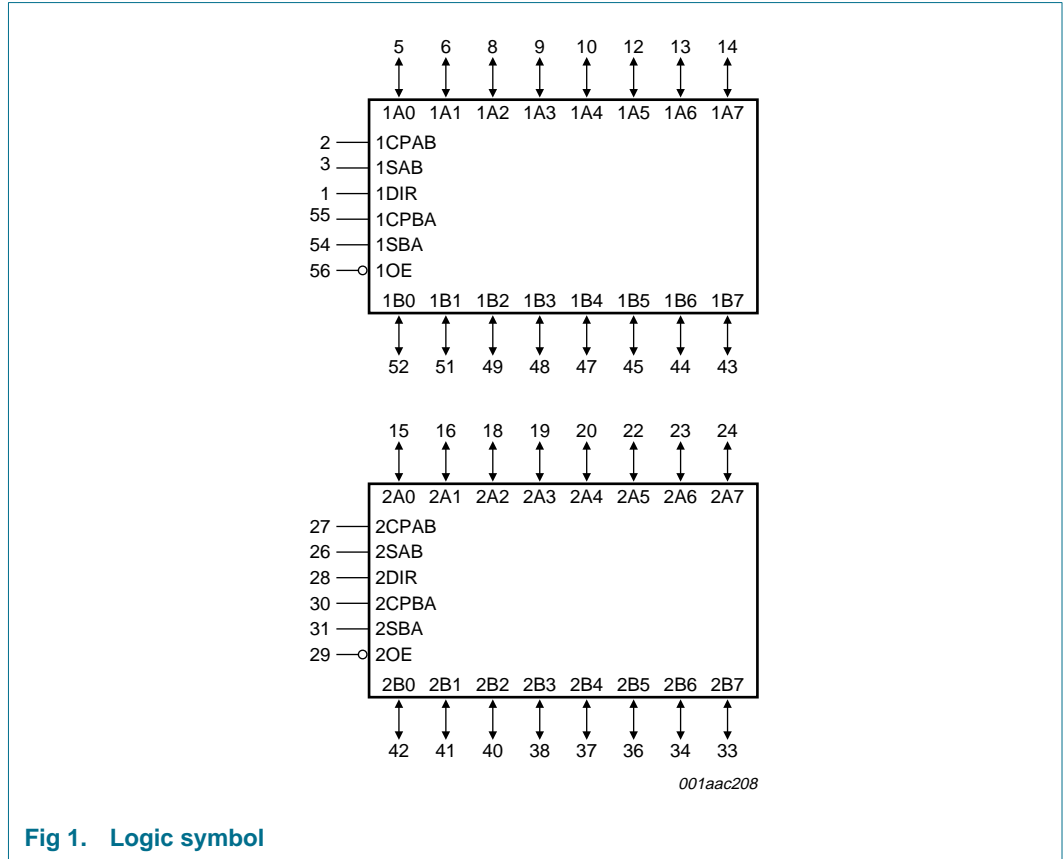


Fig 1. Logic symbol

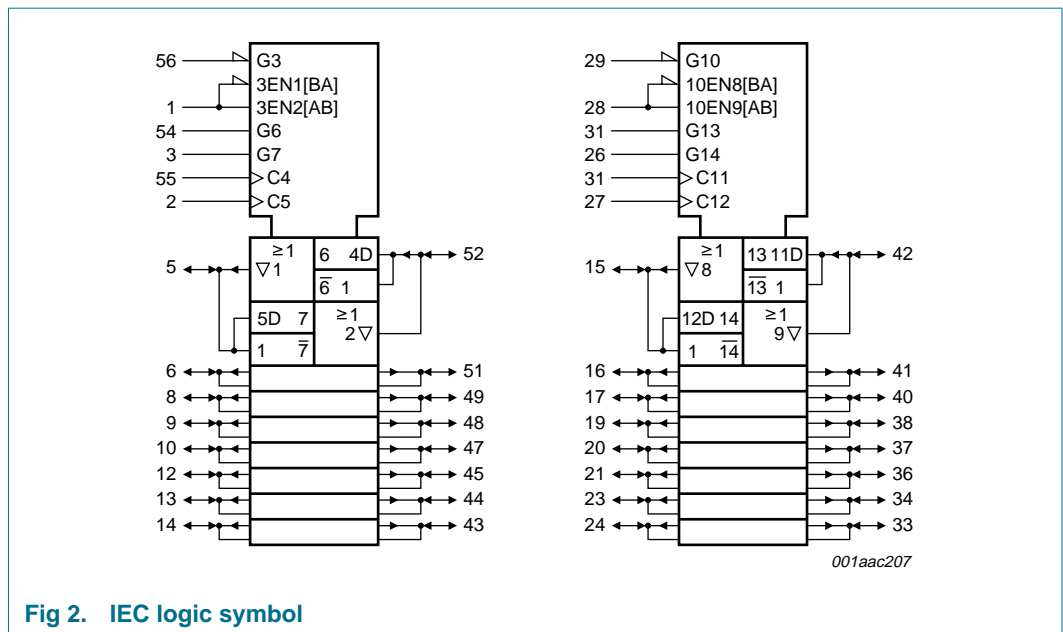


Fig 2. IEC logic symbol

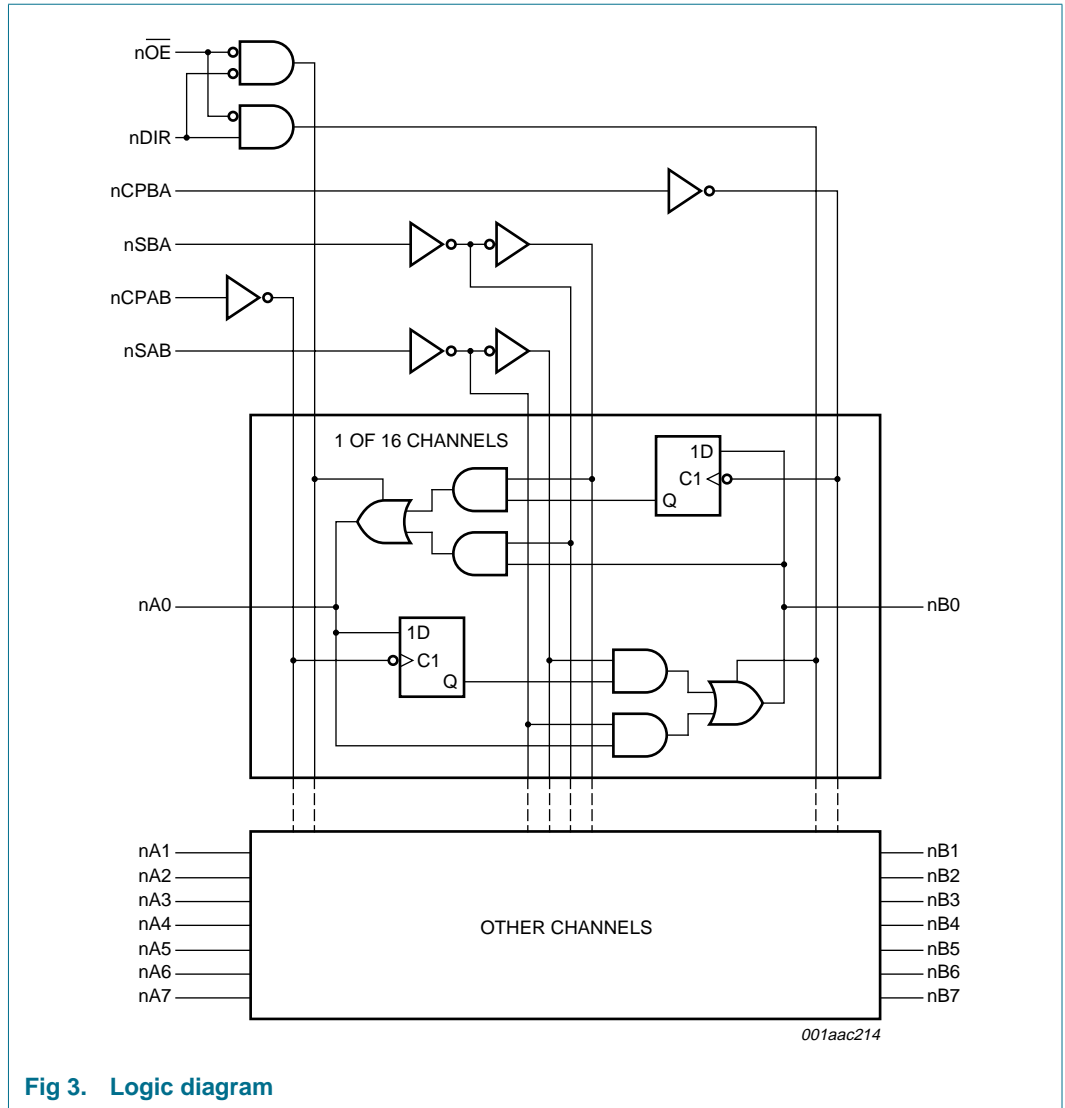
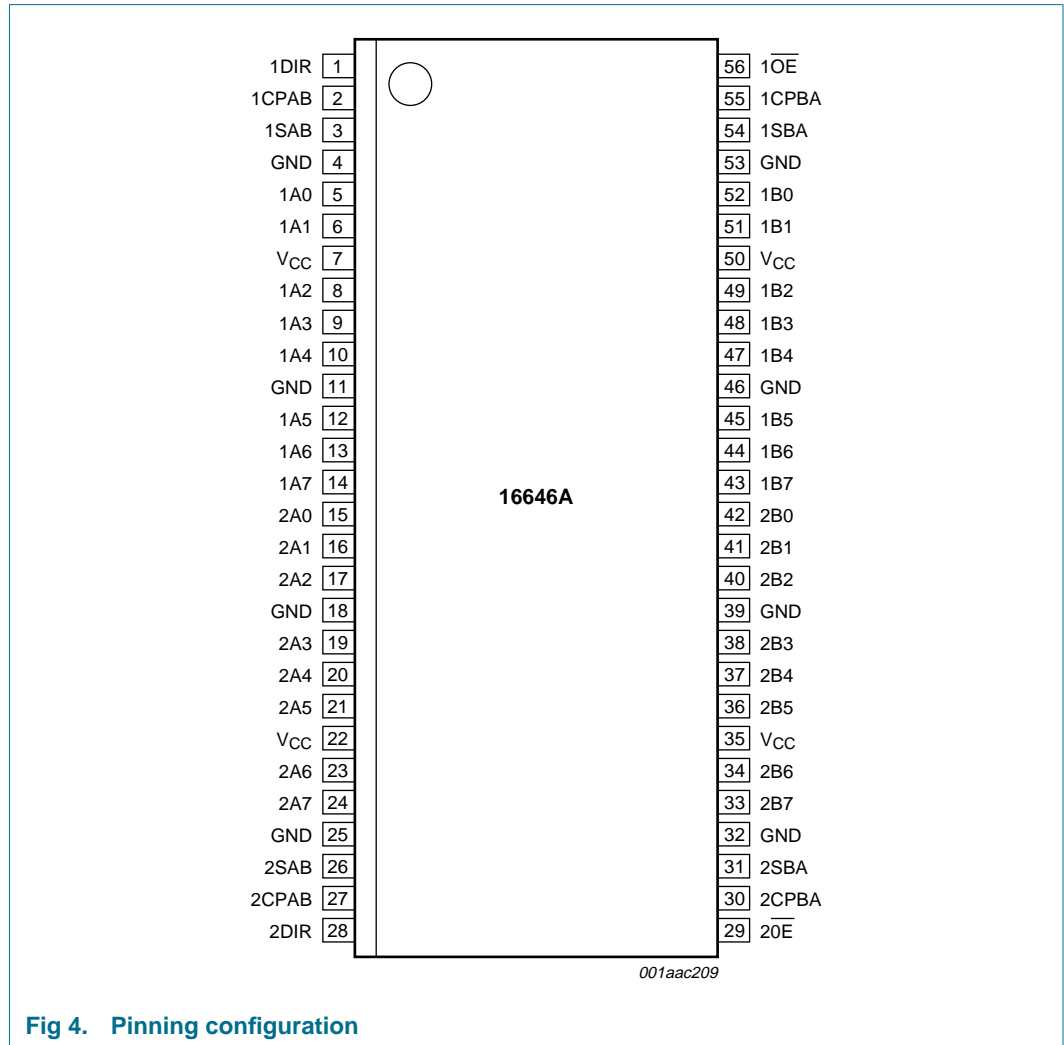


Fig 3. Logic diagram

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3: Pin description

| Symbol | Pin | Description |
|-----------------|-----|-----------------------------------|
| 1DIR | 1 | direction control inputs 0 to 7 |
| 1CPAB | 2 | clock inputs 0 to 7; A to B side |
| 1SAB | 3 | select inputs 0 to 7; A to B side |
| GND | 4 | ground (0V) |
| 1A0 | 5 | data input or output 0; A side |
| 1A1 | 6 | data input or output 1; A side |
| V _{CC} | 7 | positive supply voltage |
| 1A2 | 8 | data input or output 2; A side |

Table 3: Pin description ...continued

| Symbol | Pin | Description |
|-------------------|-----|------------------------------------|
| 1A3 | 9 | data input or output 3; A side |
| 1A4 | 10 | data input or output 4; A side |
| GND | 11 | ground (0V) |
| 1A5 | 12 | data input or output 5; A side |
| 1A6 | 13 | data input or output 6; A side |
| 1A7 | 14 | data input or output 7; A side |
| 2A0 | 15 | data input or output 8; A side |
| 2A1 | 16 | data input or output 9; A side |
| 2A2 | 17 | data input or output 10; A side |
| GND | 18 | ground (0V) |
| 2A3 | 19 | data input or output 11; A side |
| 2A4 | 20 | data input or output 12; A side |
| 2A5 | 21 | data input or output 13; A side |
| V _{CC} | 22 | positive supply voltage |
| 2A6 | 23 | data input or output 14; A side |
| 2A7 | 24 | data input or output 15; A side |
| GND | 25 | ground (0V) |
| 2SAB | 26 | select inputs 8 to 15; A to B side |
| 2CPAB | 27 | clock inputs 8 to 15; A to B side |
| 2DIR | 28 | direction control inputs 8 to 15 |
| 2 \overline{OE} | 29 | output enable inputs 8 to 15 |
| 2CPBA | 30 | clock inputs 8 to 15; B to A side |
| 2SBA | 31 | select inputs 8 to 15; B to A side |
| GND | 32 | ground (0V) |
| 2B7 | 33 | data input or output 15; B side |
| 2B6 | 34 | data input or output 14; B side |
| V _{CC} | 35 | positive supply voltage |
| 2B5 | 36 | data input or output 13; B side |
| 2B4 | 37 | data input or output 12; B side |
| 2B3 | 38 | data input or output 11; B side |
| GND | 39 | ground (0V) |
| 2B2 | 40 | data input or output 10; B side |
| 2B1 | 41 | data input or output 9; B side |
| 2B0 | 42 | data input or output 8; B side |
| 1B7 | 43 | data input or output 7; B side |
| 1B6 | 44 | data input or output 6; B side |
| 1B5 | 45 | data input or output 5; B side |
| GND | 46 | ground (0V) |
| 1B4 | 47 | data input or output 4; B side |
| 1B3 | 48 | data input or output 3; B side |
| 1B2 | 49 | data input or output 2; B side |

Table 3: Pin description ...continued

| Symbol | Pin | Description |
|-------------------|-----|-----------------------------------|
| V _{CC} | 50 | positive supply voltage |
| 1B1 | 51 | data input or output 1; B side |
| 1B0 | 52 | data input or output 0; B side |
| GND | 53 | ground (0V) |
| 1SBA | 54 | select inputs 0 to 7; B to A side |
| 1CPBA | 55 | clock inputs 0 to 7; B to A side |
| 1 \overline{OE} | 56 | output enable inputs 0 to 7 |

7. Functional description

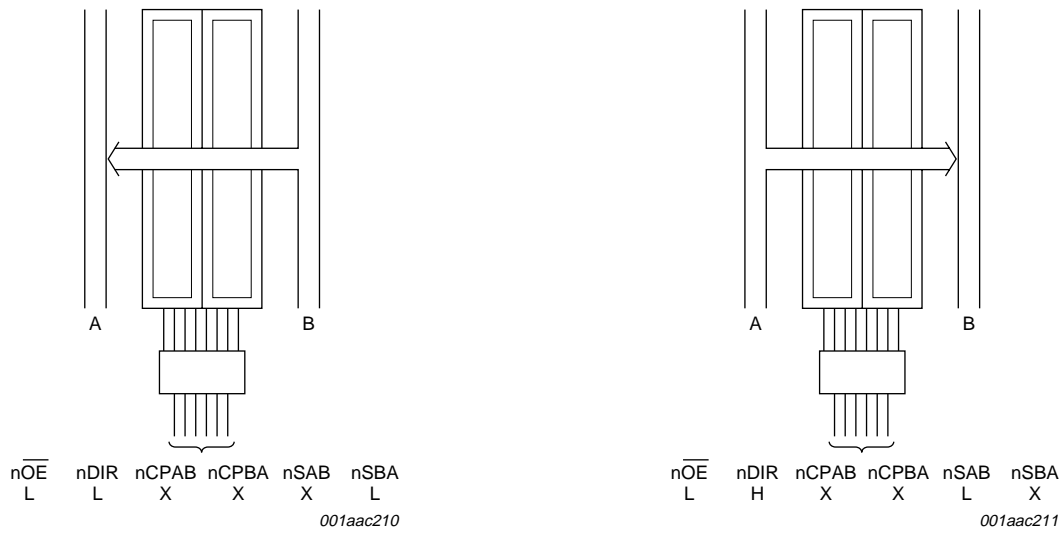
7.1 Function table

Table 4: Function table [1]

| Operating mode | Inputs | | | | | | Data I/O | | reference |
|---------------------------|-------------------|------|--------|--------|------|------|------------------------|------------------------|---------------------------|
| | n \overline{OE} | nDIR | nCPAB | nCPBA | nSAB | nSBA | nAx | nBx | |
| Store A (B unspecified) | X | X | ↑ | X | X | X | input | unspecified output [2] | Figure 5c |
| Store B (A unspecified) | X | X | X | ↑ | X | X | unspecified output [2] | input | Figure 5c |
| Store A and B data | H | X | ↑ | ↑ | X | X | input | input | Figure 5c |
| Isolation, hold storage | H | X | H or L | H or L | X | X | input | input | - |
| Real time B data to A bus | L | L | X | X | X | L | output | input | Figure 5a |
| Stored B data to A bus | L | L | X | H or L | X | H | output | input | Figure 5d |
| Real time A data to B bus | L | H | X | X | L | X | input | output | Figure 5b |
| Stored A data to B bus | L | H | H or L | X | H | X | input | output | Figure 5d |

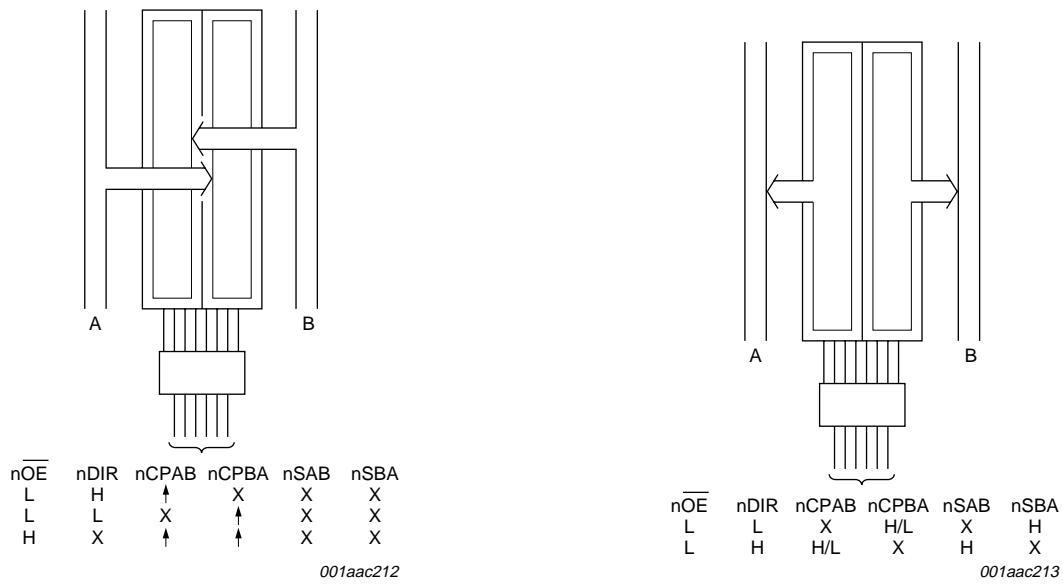
[1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care;
 ↑ = LOW-to-HIGH clock transition.

[2] The data output function may be enabled or disabled by various signals at the n \overline{OE} input. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition of the clock.



a. Real time bus transfer bus B to bus A

b. Real time bus transfer bus A to bus B



c. Storage from bus A, bus B or bus A and bus B

d. Transfer stored data to bus A or bus B

Fig 5. Examples of bus-management functions

8. Limiting values

Table 5: Limiting values

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-----------------------|-----------------------------------|----------|------|------|
| V_{CC} | supply voltage | | -0.5 | +4.6 | V |
| V_I | input voltage | | [1] -0.5 | +7.0 | V |
| V_O | output voltage | output in off-state or HIGH state | [1] -0.5 | +7.0 | V |
| I_{IK} | input diode current | $V_I < 0$ V | -50 | - | mA |
| I_{OK} | output diode current | $V_O < 0$ V | -50 | - | mA |
| I_O | output source current | output in LOW state | - | 128 | mA |
| | | output in HIGH state | -64 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| T_j | junction temperature | | [2] - | 150 | °C |

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

9. Recommended operating conditions

Table 6: Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|------------------------------------|---|-----|-----|-----|------|
| V_{CC} | supply voltage | | 2.7 | - | 3.6 | V |
| V_I | input voltage | | 0 | - | 5.5 | V |
| V_{IH} | HIGH-level input voltage | | 2.0 | - | - | V |
| V_{IL} | LOW-level input voltage | | - | - | 0.8 | V |
| I_{OH} | HIGH-level output current | | - | - | -32 | mA |
| I_{OL} | LOW-level output current | none | - | - | 32 | mA |
| | | duty cycle ≤ 50 %; $f \geq 1$ kHz | - | - | 64 | mA |
| $\Delta t/\Delta V$ | input transition rise or fall rate | outputs enabled | - | - | 10 | ns/V |
| T_{amb} | ambient temperature | | -40 | - | +85 | °C |

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|---|--|---|--|-----------------|------|------|----|
| T_{amb} = -40 °C to +85 °C [1] | | | | | | | |
| V _{IK} | input clamp voltage | V _{CC} = 2.7 V; I _{IK} = -18 mA | - | -0.85 | -1.2 | V | |
| V _{OH} | HIGH-level output voltage | V _{CC} = 2.7 V to 3.6 V; I _{OH} = 100 μA | V _{CC} - 0.2 | V _{CC} | - | V | |
| | | V _{CC} = 2.7 V; I _{OH} = -8 mA | 2.4 | 2.5 | - | V | |
| | | V _{CC} = 3.0 V; I _{OH} = -32 mA | 2.0 | 2.3 | - | V | |
| V _{OL} | LOW-level output voltage | V _{CC} = 2.7 V | | | | | |
| | | I _{OL} = 100 μA | - | 0.07 | 0.2 | V | |
| | | I _{OL} = 24 mA | - | 0.03 | 0.5 | V | |
| | | V _{CC} = 3.0 V | | | | | |
| | | I _{OL} = 16 mA | - | 0.25 | 0.4 | V | |
| | | I _{OL} = 32 mA | - | 0.3 | 0.5 | V | |
| V _{RST} | power-up LOW output voltage | V _{CC} = 3.6 V; I _O = 1 mA; V _I = GND or V _{CC} | [2] - | - | 0.55 | V | |
| | | input leakage current of control pins | V _{CC} = 3.6 V; V _I = V _{CC} or GND | - | 0.1 | ±1 | μA |
| | | | V _{CC} = 0 V or 3.6 V; V _I = 5.5 V | - | 0.1 | 10 | μA |
| I _{LI} | input leakage current of I/O data pins | V _{CC} = 3.6 V; V _I = 5.5 V | [3] - | 0.1 | 20 | μA | |
| | | V _{CC} = 3.6 V; V _I = V _{CC} | [3] - | 0.5 | 10 | μA | |
| | | V _{CC} = 3.6 V; V _I = 0 V | [3] - | +0.1 | -5 | μA | |
| I _{OFF} | output off current | V _{CC} = 0 V; V _I or V _O = 0 V to 4.5 V | - | 0.1 | ±100 | μA | |
| I _{HOLD} | bus hold current A or B outputs | V _{CC} = 3 V; V _I = 0.8 V | [4] 75 | 130 | - | μA | |
| | | V _{CC} = 3 V; V _I = 2.0 V | [4] -75 | -140 | - | μA | |
| | | V _{CC} = 0 V to 3.6 V; V _I = 3.6 V | [4] ±500 | - | - | μA | |
| I _{EX} | current into an output in HIGH state when V _O > V _{CC} | V _O = 5.5 V; V _{CC} = 3.0 V | - | 50 | 125 | μA | |
| I _{PU} , I _{PD} | power-up and power-down 3-state output current | V _{CC} ≤ 1.2 V; V _O = 0.5 V to V _{CC} ; V _I = GND or V _{CC} ; pin nDIR and nOE are don't care | [5] - | 35 | ±100 | μA | |
| I _{CC} | quiescent supply current | V _{CC} = 3.6 V; I _O = 0 A; V _I = GND or V _{CC} | | | | | |
| | | outputs HIGH | - | 0.07 | 0.12 | mA | |
| | | outputs LOW | - | 4.9 | 6 | mA | |
| | outputs disabled | [6] - | 0.07 | 0.12 | mA | | |

Table 7: Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|---|--|-------|-----|-----|------|
| ΔI_{CC} | additional supply current per input pin | $V_{CC} = 3\text{ V to }3.6\text{ V}$; one input at $V_{CC} - 0.6\text{ V}$, other inputs at V_{CC} or GND | [7] - | 0.1 | 0.2 | mA |
| C_I | input capacitance | $V_I = 0\text{ V or }3.0\text{ V}$ | - | 3 | - | pF |
| $C_{I/O}$ | I/O pin capacitance | $V_{I/O} = 0\text{ V or }3.0\text{ V}$; outputs disabled | - | 9 | - | pF |

- [1] All typical values are measured at $V_{CC} = 3.3\text{ V}$ and $T_{amb} = 25\text{ }^\circ\text{C}$.
- [2] For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
- [3] Unused pins at V_{CC} or GND.
- [4] This is the bus hold overdrive current required to force the input to the opposite logic state.
- [5] This parameter is valid for $V_{CC} = 0\text{ V to }1.2\text{ V}$ with a transition time of up to 10 ms. From $V_{CC} = 1.2\text{ V to }3.3\text{ V} \pm 0.3\text{ V}$. A transition time of 100 μs is permitted. This parameter is valid for $T_{amb} = 25\text{ }^\circ\text{C}$ only.
- [6] I_{CC} is measured with outputs pulled to V_{CC} or GND.
- [7] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

11. Dynamic characteristics

Table 8: Dynamic characteristics

$GND = 0\text{ V}$; $t_r = t_f = 2.5\text{ ns}$; $C_L = 50\text{ pF}$; $R_L = 500\text{ }\Omega$; for input definitions see [Figure 13](#); for test circuit see [Figure 14](#).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|--|---|-----|-----|-----|------|
| $T_{amb} = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ [1] | | | | | | |
| f_{max} | maximum clock frequency | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; see Figure 6 | 150 | - | - | MHz |
| t_{PLH} | propagation delay nAx to nBx or nBx to nAx | see Figure 8 | | | | |
| | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 0.5 | 1.9 | 3.7 | ns |
| | | $V_{CC} = 2.7\text{ V}$ | - | - | 4.3 | ns |
| propagation delay nCPAB to nBx or nCPBA to nAx | see Figure 6 | | | | | |
| | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 1.5 | 2.7 | 4.5 | ns | |
| | $V_{CC} = 2.7\text{ V}$ | - | - | 5.3 | ns | |
| propagation delay nSAB to nBx or nSBA to nAx | see Figure 7 | | | | | |
| | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 1.0 | 2.5 | 4.6 | ns | |
| | $V_{CC} = 2.7\text{ V}$ | - | - | 5.4 | ns | |
| t_{PHL} | propagation delay nAx to nBx or nBx to nAx | see Figure 8 | | | | |
| | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 0.5 | 1.9 | 3.7 | ns |
| | | $V_{CC} = 2.7\text{ V}$ | - | - | 4.4 | ns |
| propagation delay nCPAB to nBx or nCPBA to nAx | see Figure 6 | | | | | |
| | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 1.5 | 2.4 | 4.5 | ns | |
| | $V_{CC} = 2.7\text{ V}$ | - | - | 5.2 | ns | |
| propagation delay nSAB to nBx or nSBA to nAx | see Figure 7 | | | | | |
| | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 1.0 | 2.8 | 4.8 | ns | |
| | | $V_{CC} = 2.7\text{ V}$ | - | - | 5.6 | ns |

Table 8: Dynamic characteristics ...continued

$GND = 0\text{ V}$; $t_r = t_f = 2.5\text{ ns}$; $C_L = 50\text{ pF}$; $R_L = 500\ \Omega$; for input definitions see [Figure 13](#); for test circuit see [Figure 14](#).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|--|--|-----|-----|-----|------|
| t_{PZH} | output enable time $n\overline{OE}$ to nAx or nBx | see Figure 11 | | | | |
| | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 1.0 | 2.7 | 4.7 | ns |
| | | $V_{CC} = 2.7\text{ V}$ | - | - | 5.4 | ns |
| | output enable time $nDIR$ to nAx or nBx | see Figure 11 | | | | |
| $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | 1.0 | 2.9 | 4.8 | ns | |
| | $V_{CC} = 2.7\text{ V}$ | - | - | 5.4 | ns | |
| t_{PZL} | output enable time $n\overline{OE}$ to nAx or nBx | see Figure 12 | | | | |
| | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 1.0 | 2.5 | 4.9 | ns |
| | | $V_{CC} = 2.7\text{ V}$ | - | - | 5.7 | ns |
| | output enable time $nDIR$ to nAx or nBx | see Figure 12 | | | | |
| $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | 1.0 | 2.8 | 4.9 | ns | |
| | $V_{CC} = 2.7\text{ V}$ | - | - | 5.6 | ns | |
| t_{PHZ} | output disable time $n\overline{OE}$ to nAx or nBx | see Figure 11 | | | | |
| | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 1.5 | 3.2 | 5.2 | ns |
| | | $V_{CC} = 2.7\text{ V}$ | - | - | 5.5 | ns |
| | output disable time $nDIR$ to nAx or nBx | see Figure 11 | | | | |
| $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | 1.0 | 3.1 | 5.7 | ns | |
| | $V_{CC} = 2.7\text{ V}$ | - | - | 6.6 | ns | |
| t_{PLZ} | output disable time $n\overline{OE}$ to nAx or nBx | see Figure 12 | | | | |
| | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 1.5 | 2.9 | 4.6 | ns |
| | | $V_{CC} = 2.7\text{ V}$ | - | - | 4.7 | ns |
| | output disable time $nDIR$ to nAx or nBx | see Figure 12 | | | | |
| $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | 1.0 | 2.9 | 5.2 | ns | |
| | $V_{CC} = 2.7\text{ V}$ | - | - | 5.7 | ns | |

[1] All typical values are measured at $V_{CC} = 3.3\text{ V}$ and $T_{amb} = 25\text{ }^\circ\text{C}$.

Table 9: Dynamic characteristics setup requirements

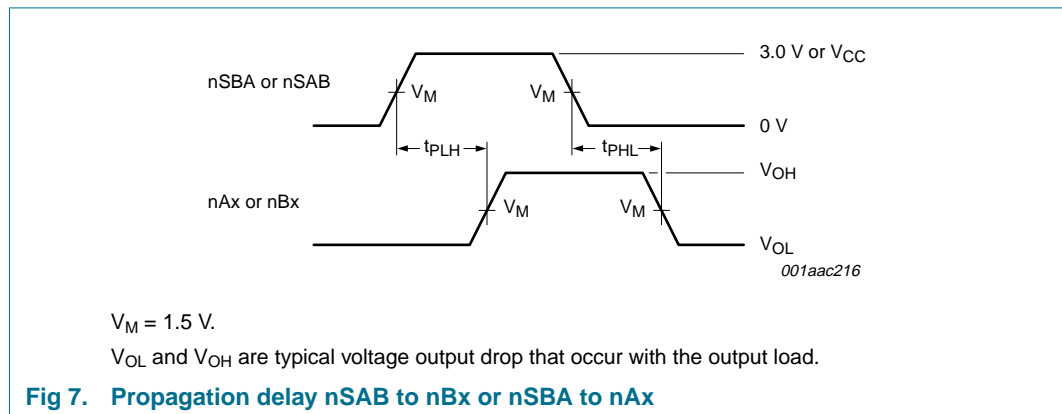
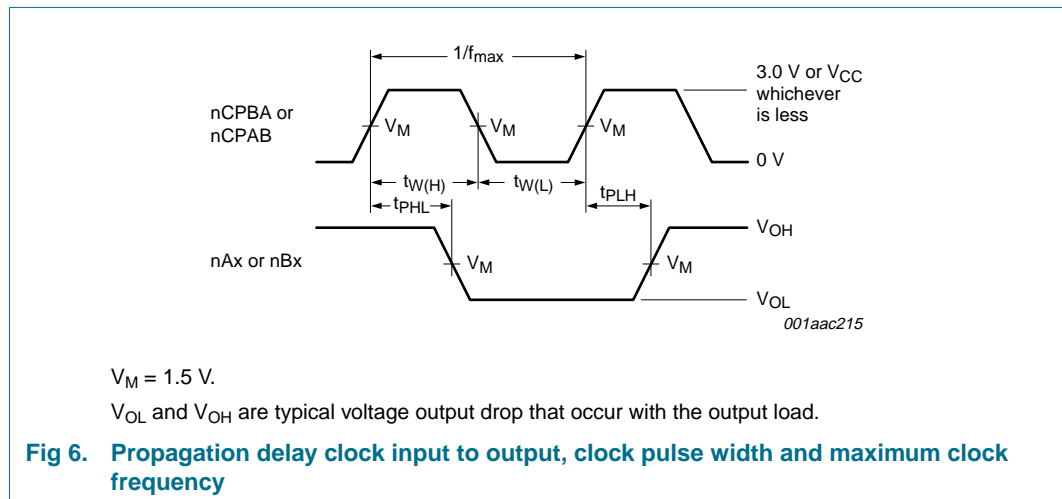
$GND = 0\text{ V}$; $t_r = t_f = 2.5\text{ ns}$; $C_L = 50\text{ pF}$; $R_L = 500\ \Omega$.

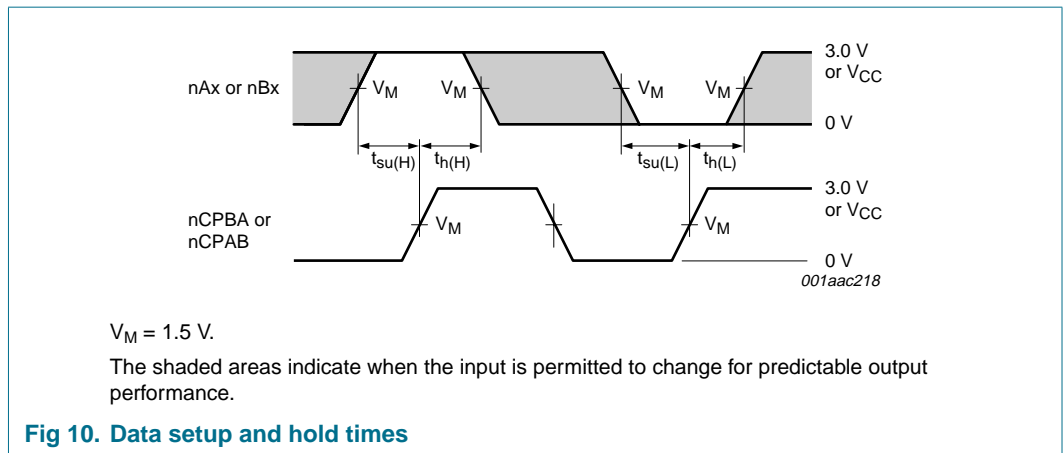
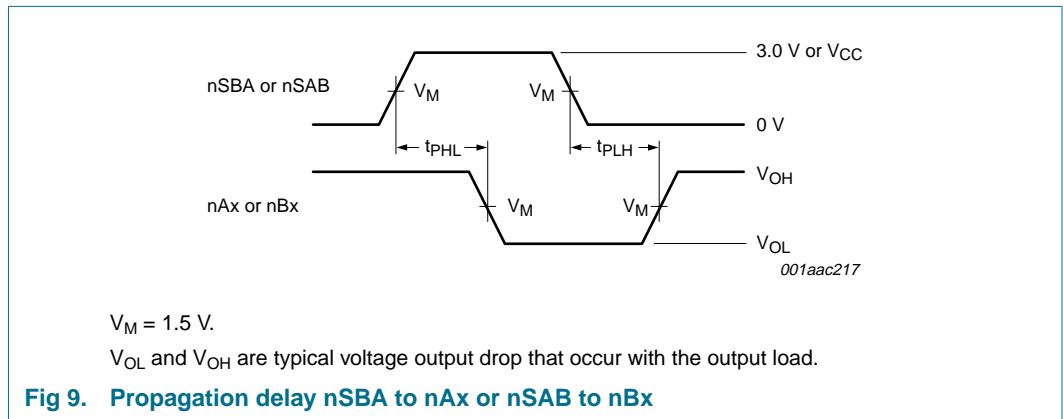
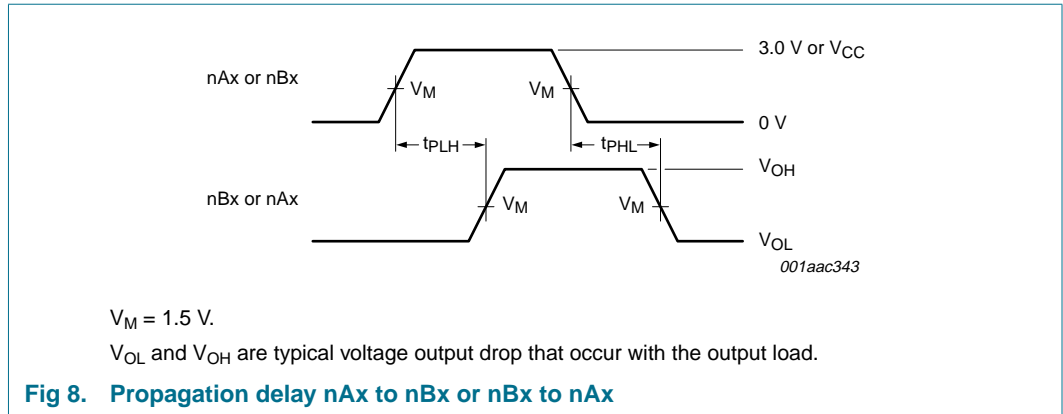
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|--|-----|-----|-----|------|
| $T_{amb} = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$ | | | | | | |
| $t_{su(H)}$ | set-up time HIGH nAx to $nCPAB$ or nBx to $nCPBA$ | see Figure 10 | | | | |
| | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 1.0 | 0.6 | - | ns |
| | | $V_{CC} = 2.7\text{ V}$ | 1.1 | - | - | ns |
| $t_{su(L)}$ | set-up time LOW nAx to $nCPAB$ or nBx to $nCPBA$ | see Figure 10 | | | | |
| | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 1.9 | 0.4 | - | ns |
| | | $V_{CC} = 2.7\text{ V}$ | 2.4 | - | - | ns |
| $t_{h(H)}$ | hold time HIGH nAx to $nCPAB$ or nBx to $nCPBA$ | see Figure 10 | | | | |
| | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 1.0 | 0.4 | - | ns |
| | | $V_{CC} = 2.7\text{ V}$ | 1.0 | - | - | ns |

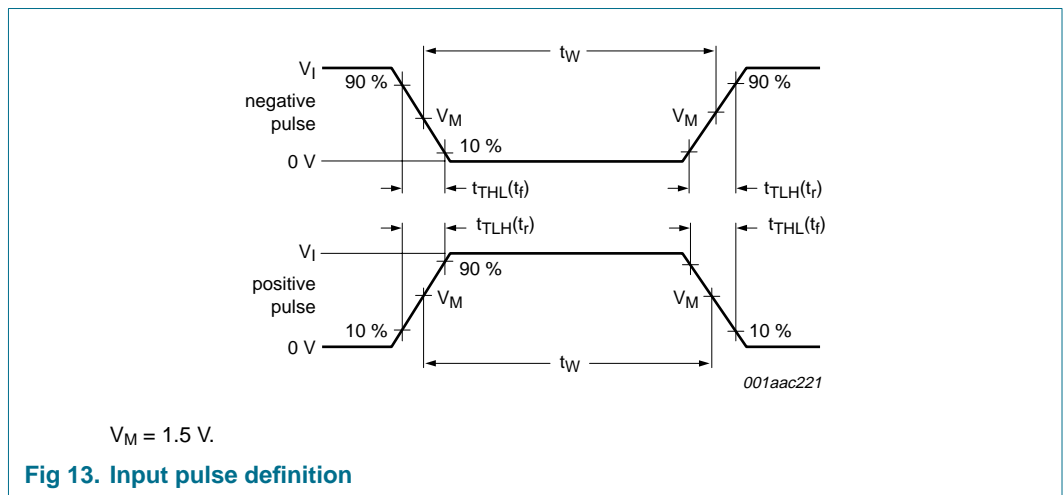
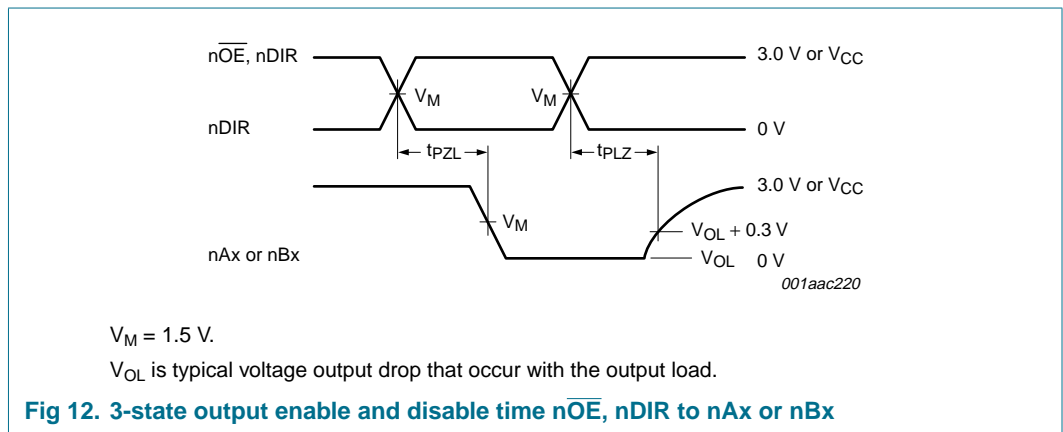
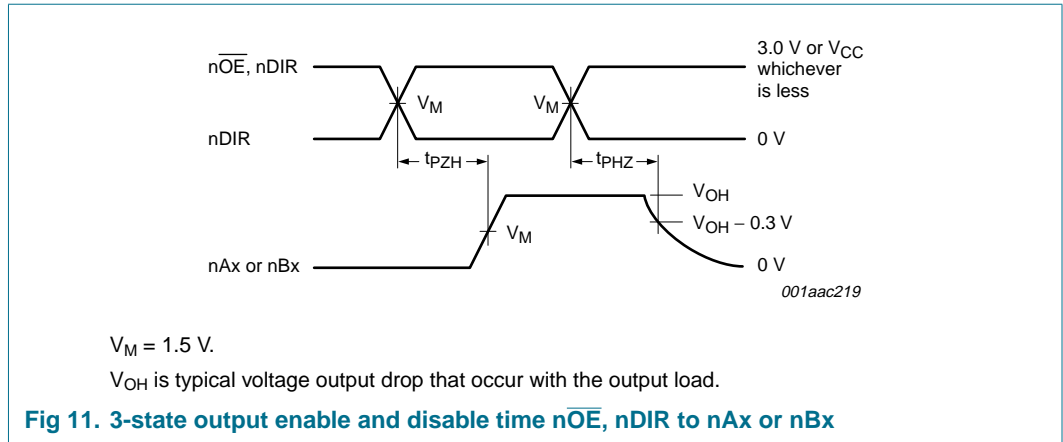
Table 9: Dynamic characteristics setup requirements ...continued
GND = 0 V; $t_r = t_f = 2.5$ ns; $C_L = 50$ pF; $R_L = 500$ Ω .

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------|--|-------------------------------|-----|-----|-----|------|
| $t_{h(L)}$ | hold time LOW nAx to nCPAB or nBx to nCPBA | see Figure 10 | | | | |
| | | $V_{CC} = 3.3$ V \pm 0.3 V | 1.0 | 0.5 | - | ns |
| | | $V_{CC} = 2.7$ V | 1.0 | - | - | ns |
| $t_{W(H)}$ | pulse width HIGH nCPAB or nCPBA | see Figure 6 | | | | |
| | | $V_{CC} = 3.3$ V \pm 0.3 V | 2.6 | 2.2 | - | ns |
| | | $V_{CC} = 2.7$ V | 2.6 | - | - | ns |
| $t_{W(L)}$ | pulse width HIGH nCPAB or nCPBA | see Figure 6 | | | | |
| | | $V_{CC} = 3.3$ V \pm 0.3 V | 2.8 | 2.4 | - | ns |
| | | $V_{CC} = 2.7$ V | 2.8 | - | - | ns |

12. Waveforms







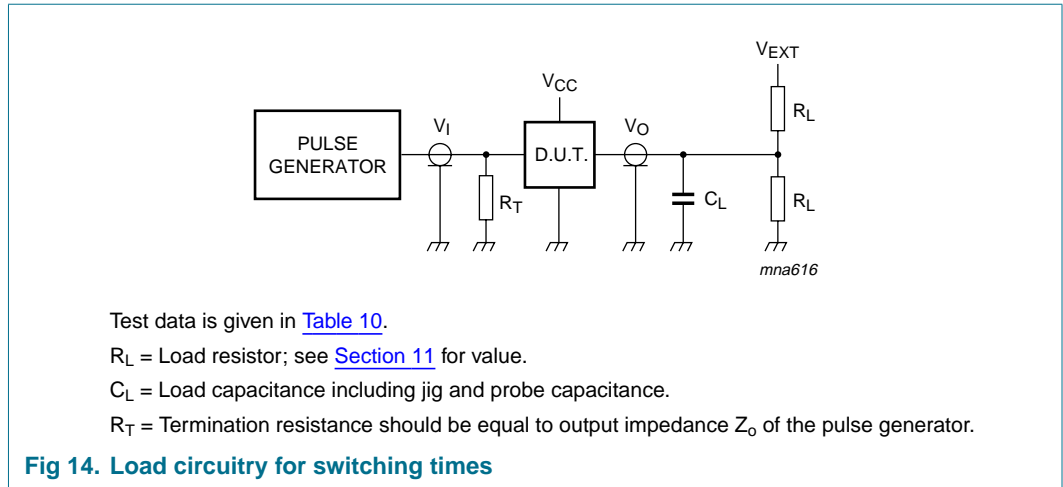


Table 10: Test data

| V_I | Repetition rate | t_w | t_r | t_f | C_L | R_L | V_{EXT} | | |
|-------|-----------------|--------|---------------|---------------|-------|--------------|--------------------|--------------------|--------------------|
| | | | | | | | t_{PHZ}, t_{PZH} | t_{PLZ}, t_{PZL} | t_{PLH}, t_{PHL} |
| 2.7 V | ≤ 10 MHz | 500 ns | ≤ 2.5 ns | ≤ 2.5 ns | 50 pF | 500 Ω | GND | 6 V | open |

13. Package outline

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1

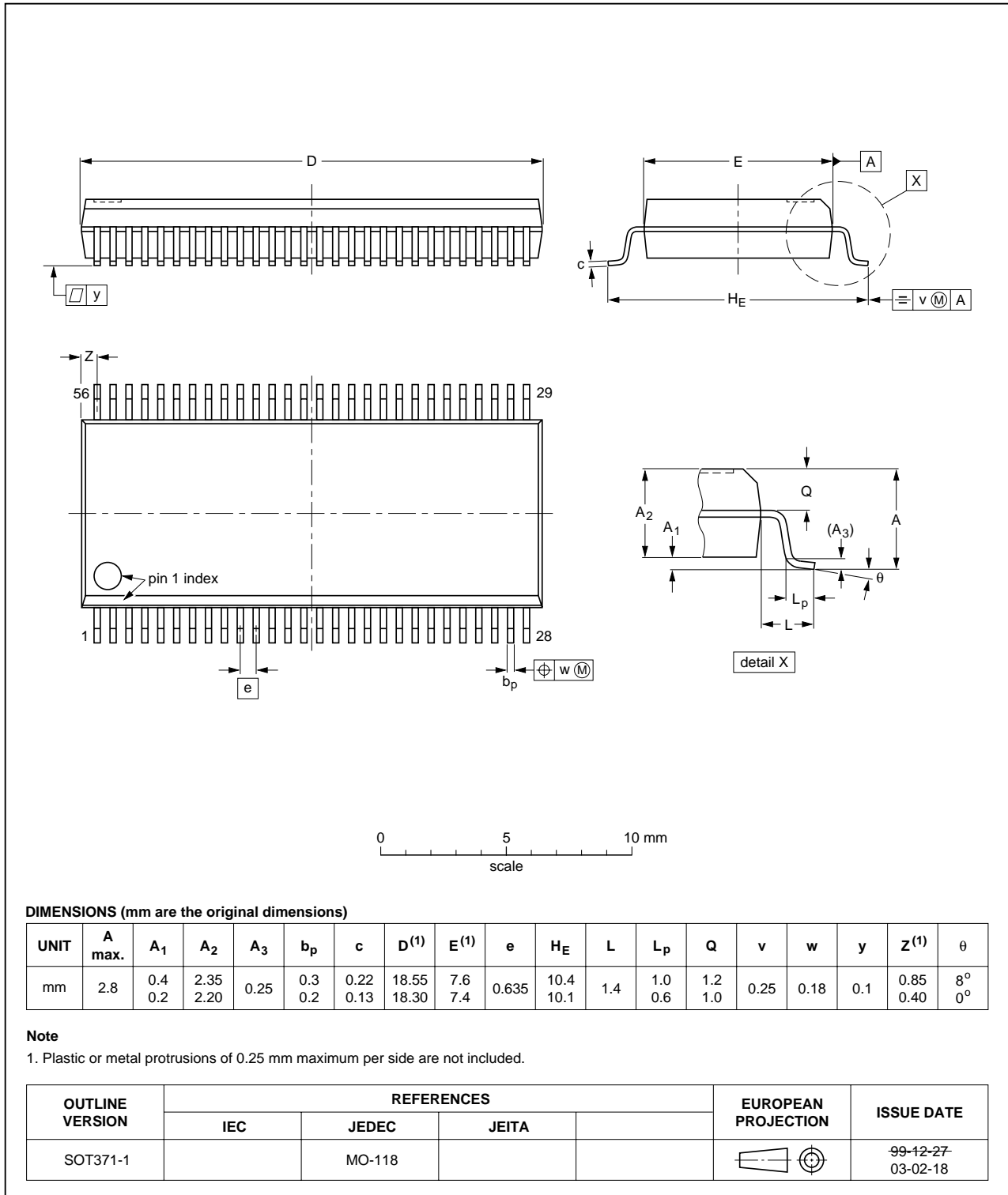


Fig 15. Package outline SOT371-1 (SSOP56)

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1

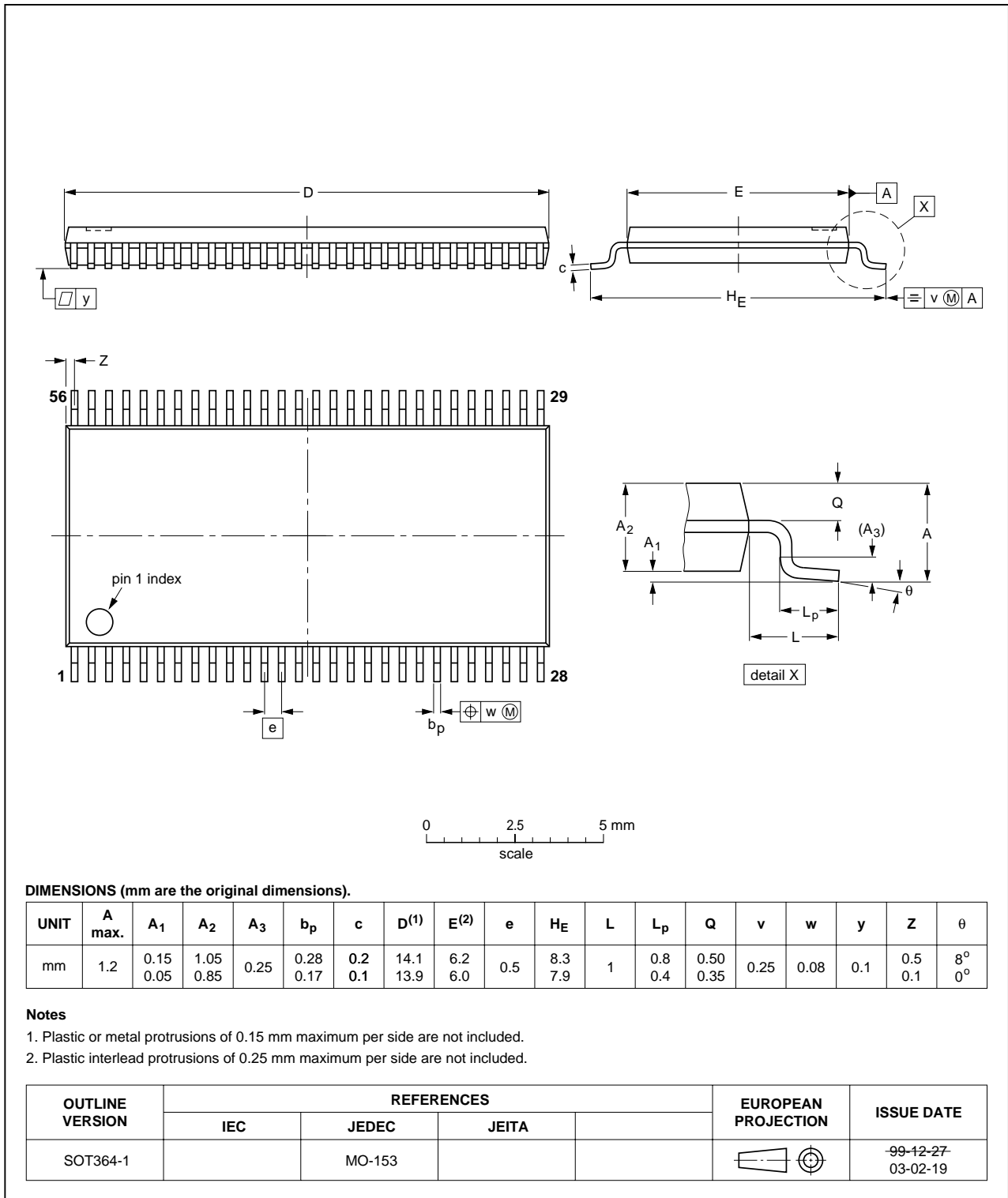


Fig 16. Package outline SOT364-1 (TSSOP56)

14. Revision history

Table 11: Revision history

| Document ID | Release date | Data sheet status | Change notice | Doc. number | Supersedes |
|----------------|--------------|-----------------------|---|----------------|---------------|
| 74LVT16646A_3 | 20050112 | Product data sheet | - | 9397 750 14326 | 74LVT16646A_2 |
| Modifications: | | | | | |
| | | | <ul style="list-style-type: none">• The format of this data sheet is redesigned to comply with the current presentation and information standard of Philips Semiconductors.• Data sheet title changed from “3.3 V ABT 16-bit bus transceiver (3-state)” to “3.3 V 16-bit bus transceiver; 3-state”• Table 8: updated parameter descriptions and values. | | |
| 74LVT16646A_2 | 19980219 | Product specification | - | 9397 750 03559 | 74LVT16646A_1 |
| 74LVT16646A_1 | 19940725 | - | - | - | - |

15. Data sheet status

| Level | Data sheet status ^[1] | Product status ^{[2] [3]} | Definition |
|-------|----------------------------------|-----------------------------------|--|
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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