



**THE DATASHEET OF  
74LVT125D,118**



# 74LVT125; 74LVTH125

3.3 V quad buffer; 3-state

Rev. 7 — 31 May 2016

Product data sheet

## 1. General description

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The 74LVT125; 74LVTH125 is a high-performance BiCMOS product designed for  $V_{CC}$  operation at 3.3 V.

This device combines low static and dynamic power dissipation with high speed and high output drive. The 74LVT125; 74LVTH125 device is a quad buffer that is ideal for driving bus lines. The device features four output enable inputs ( $\overline{1OE}$ ,  $\overline{2OE}$ ,  $\overline{3OE}$  and  $\overline{4OE}$ ), each controlling one of the 3-state outputs.

## 2. Features and benefits

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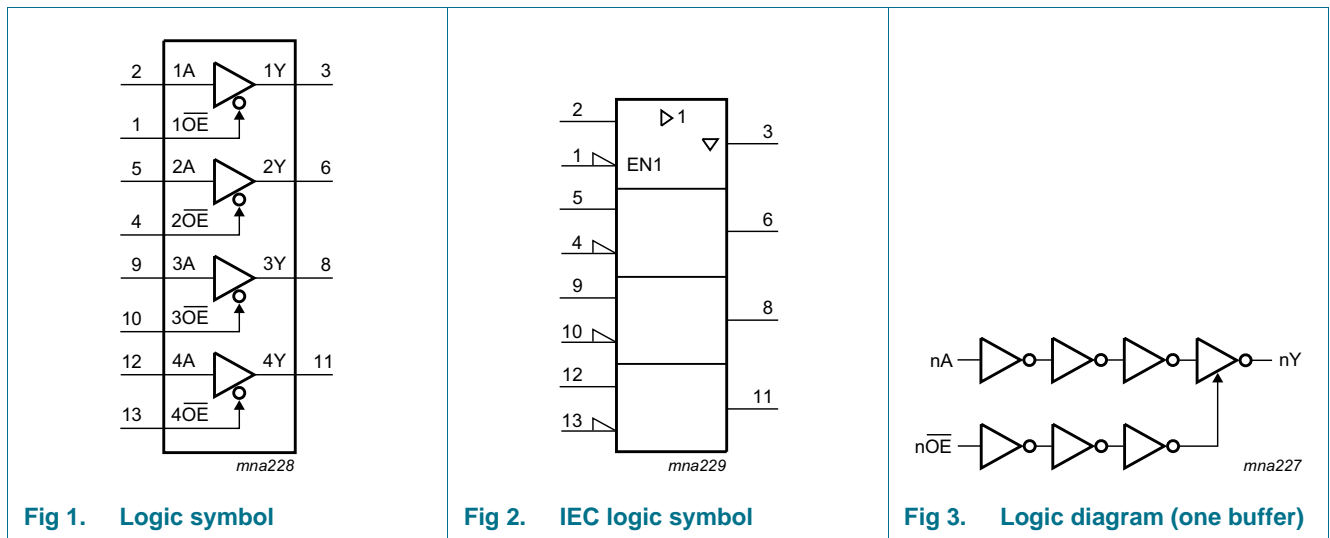
- Quad bus interface
- 3-state buffers
- Output capability: +64 mA and -32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- No bus current loading when output is tied to 5 V bus
- Power-up 3-state
- Latch-up protection:
  - ◆ JESD78: exceeds 500 mA
- ESD protection:
  - ◆ MIL STD 883 method 3015: exceeds 2000 V
  - ◆ Machine model: exceeds 200 V

## 3. Ordering information

Table 1. Ordering information

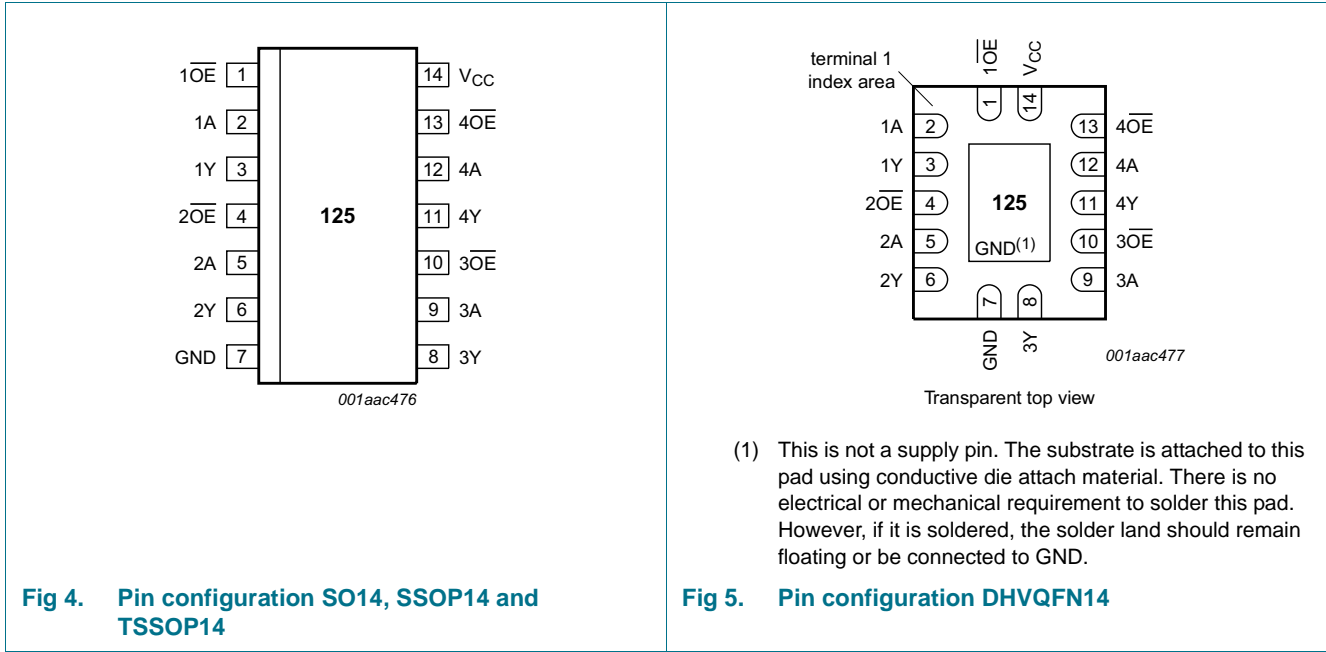
Type number	Package			Version
	Temperature range	Name	Description	
74LVT125D 74LVTH125D	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVT125DB 74LVTH125DB				
74LVT125PW 74LVTH125PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVT125BQ 74LVTH125BQ				
	-40 °C to +85 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

## 4. Functional diagram



5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE	1	1 output enable input (active LOW)
1A	2	1 data input
1Y	3	1 data output
2OE	4	2 output enable input (active LOW)
2A	5	2 data input
2Y	6	2 data output
GND	7	ground (0 V)
3Y	8	3 data output
3A	9	3 data input
3OE	10	3 output enable input (active LOW)
4Y	11	4 data output
4A	12	4 data input
4OE	13	4 output enable input (active LOW)
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

### 6.1 Function table

Table 3. Function table<sup>[1]</sup>

Control	Input	Output
nOE	nA	nY
L	L	L
L	H	H
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+4.6	V
V <sub>I</sub>	input voltage		-0.5	+7.0	V
V <sub>O</sub>	output voltage	output in OFF-state or HIGH-state	-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-	-50	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-	-50	mA
I <sub>O</sub>	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-	-64	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>j</sub>	junction temperature		-	150	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage		2.7	-	3.6	V
V <sub>I</sub>	input voltage		0	-	5.5	V
V <sub>IH</sub>	HIGH-level input voltage		2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage		-	-	0.8	V
I <sub>OH</sub>	HIGH-level output current		-	-	-32	mA
I <sub>OL</sub>	LOW-level output current	none	-	-	32	mA
		current duty cycle ≤ 50 %; f ≥ 1 kHz	-	-	64	mA
Δt/ΔV	input transition rise and fall rate		0	-	10	ns/V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+85	°C

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +85 °C<sup>[1]</sup></b>						
V <sub>IK</sub>	input clamping voltage	I <sub>IK</sub> = -18 mA; V <sub>CC</sub> = 2.7 V	-	-0.9	-1.2	V
V <sub>OH</sub>	HIGH-level output voltage	I <sub>OH</sub> = -100 μA; V <sub>CC</sub> = 2.7 V to 3.6 V	V <sub>CC</sub> - 0.2	V <sub>CC</sub> - 0.1	-	V
		I <sub>OH</sub> = -8 mA; V <sub>CC</sub> = 2.7 V	2.4	2.5	-	V
		I <sub>OH</sub> = -32 mA; V <sub>CC</sub> = 3.0 V	2.0	2.2	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>CC</sub> = 2.7 V				
		I <sub>OL</sub> = 100 μA	-	0.1	0.2	V
		I <sub>OL</sub> = 24 mA	-	0.3	0.5	V
		V <sub>CC</sub> = 3.0 V				
		I <sub>OL</sub> = 16 mA	-	0.25	0.4	V
		I <sub>OL</sub> = 32 mA	-	0.3	0.5	V
I <sub>I</sub>	input leakage current	all input pins				
		V <sub>CC</sub> = 0 V or 3.6 V; V <sub>I</sub> = 5.5 V	-	1	10	μA
		control pins				
		V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND	-	±0.1	±1	μA
		data pins <sup>[2]</sup>				
		V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub>	-	0.1	1	μA
I <sub>OFF</sub>	power-off leakage current	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 0 V to 4.5 V	-	1	±100	μA
		V <sub>CC</sub> = 3 V; V <sub>I</sub> = 0.8 V <sup>[3]</sup>	75	150	-	μA
I <sub>BHL</sub>	bus hold LOW current	V <sub>CC</sub> = 3 V; V <sub>I</sub> = 0.8 V <sup>[3]</sup>	75	150	-	μA
I <sub>BHH</sub>	bus hold HIGH current	V <sub>CC</sub> = 3 V; V <sub>I</sub> = 2.0 V	-	-150	-75	μA
I <sub>BHLO</sub>	bus hold LOW overdrive current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 0 V to 3.6 V	500	-	-	μA
I <sub>BHHO</sub>	bus hold HIGH overdrive current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 0 V to 3.6 V	-	-	-500	μA
I <sub>LO</sub>	output leakage current	output in HIGH-state when V <sub>O</sub> > V <sub>CC</sub> ; V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 3.0 V	-	60	125	μA
I <sub>O(pu/pd)</sub>	power-up/power-down output current	V <sub>CC</sub> ≤ 1.2 V; V <sub>O</sub> = 0.5 V to V <sub>CC</sub> ; V <sub>I</sub> = GND or V <sub>CC</sub> ; nOE = don't care <sup>[4]</sup>	-	±1	±100	μA
I <sub>OZ</sub>	OFF-state output current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		output HIGH: V <sub>O</sub> = 3.0 V	-	1	5	μA
		output LOW: V <sub>O</sub> = 0.5 V	-	-1	-5	μA

**Table 6.** Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = GND or V <sub>CC</sub> ; I <sub>O</sub> = 0 A				
		outputs HIGH	-	0.13	0.19	mA
		outputs LOW	-	2	7	mA
		outputs disabled [5]	-	0.13	0.19	mA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 3 V to 3.6 V; one input at V <sub>CC</sub> - 0.6 V and other inputs at V <sub>CC</sub> or GND [6]	-	0.1	0.2	mA
C <sub>I</sub>	input capacitance	V <sub>I</sub> = 0 V or 3.0 V	-	4	-	pF
C <sub>O</sub>	output capacitance	outputs disabled; V <sub>O</sub> = 0 V or 3.0 V	-	8	-	pF

[1] Typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.[2] Unused pins at V<sub>CC</sub> or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V<sub>CC</sub> between 0 V and 1.2 V with a transition time of up to 10 ms. From V<sub>CC</sub> = 1.2 V to V<sub>CC</sub> = 3.0 V to 3.6 V a transition time of 100 μs is permitted. This parameter is valid for T<sub>amb</sub> = 25 °C only.[5] I<sub>CC</sub> is measured with outputs pulled to V<sub>CC</sub> or GND.[6] This is the increase in supply current for each input at the specified voltage level other than V<sub>CC</sub> or GND.

## 10. Dynamic characteristics

**Table 7.** Dynamic characteristicsVoltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T <sub>amb</sub> = -40 °C to +85 °C [1]						
t <sub>PLH</sub>	LOW to HIGH propagation delay	nAn to nY; see <a href="#">Figure 6</a>				
		V <sub>CC</sub> = 2.7 V	-	-	4.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.7	4.0	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	nAn to nY; see <a href="#">Figure 6</a>				
		V <sub>CC</sub> = 2.7 V	-	-	4.9	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.9	3.9	ns
t <sub>PZH</sub>	OFF-state to HIGH propagation delay	nOE to nY; see <a href="#">Figure 7</a>				
		V <sub>CC</sub> = 2.7 V	-	-	6.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	3.4	4.7	ns
t <sub>PZL</sub>	OFF-state to LOW propagation delay	nOE to nY; see <a href="#">Figure 7</a>				
		V <sub>CC</sub> = 2.7 V	-	-	6.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.1	3.4	4.7	ns
t <sub>PHZ</sub>	HIGH to OFF-state propagation delay	nOE to nY; see <a href="#">Figure 7</a>				
		V <sub>CC</sub> = 2.7 V	-	-	5.7	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.8	3.7	5.1	ns

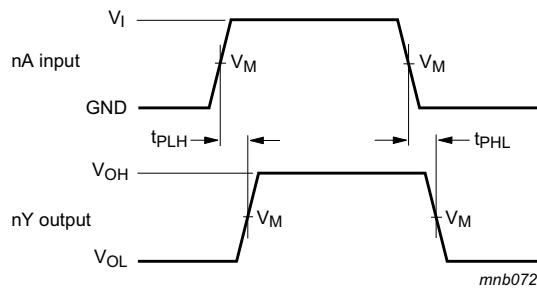
**Table 7. Dynamic characteristics ...continued**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	n $\overline{\text{OE}}$ to nY; see <a href="#">Figure 7</a>				
		V <sub>CC</sub> = 2.7 V	-	-	4.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.3	2.6	4.5	ns

[1] Typical values are at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

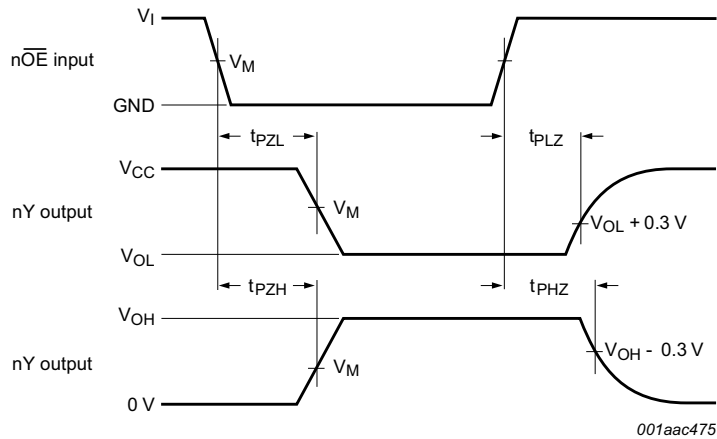
## 11. Waveforms



V<sub>M</sub> = 1.5 V.

V<sub>OL</sub> and V<sub>OH</sub> are typical voltage output levels that occur with the output load.

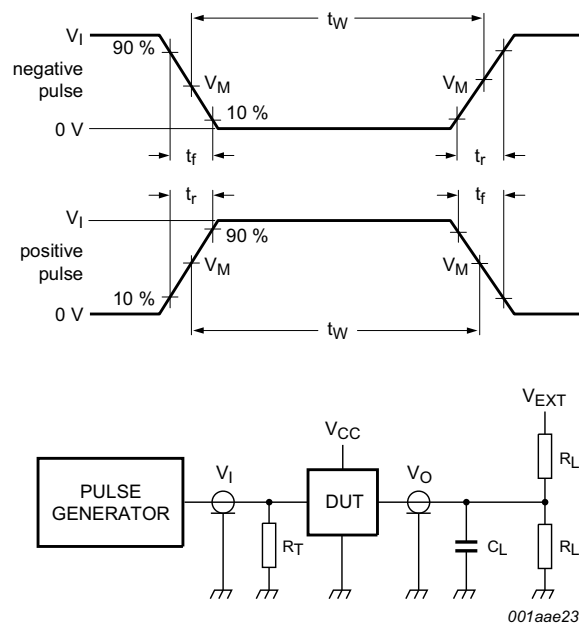
**Fig 6. Propagation delay input (nA) to output (nY)**



V<sub>M</sub> = 1.5 V.

V<sub>OL</sub> and V<sub>OH</sub> are typical voltage output levels that occur with the output load.

**Fig 7. Enable and disable times of 3-state outputs**



Test data is given in [Table 8](#).

Definitions test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = Test voltage for switching times.

**Fig 8. Test circuit for measuring switching times**

**Table 8. Test data**

Input				Load		$V_{EXT}$		
$V_I$	$f_i$	$t_W$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHZ}, t_{PZH}$	$t_{PLZ}, t_{PZL}$	$t_{PLH}, t_{PHL}$
2.7 V	$\leq 10$ MHz	500 ns	$\leq 2.5$ ns	50 pF	500 $\Omega$	GND	6 V	open

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

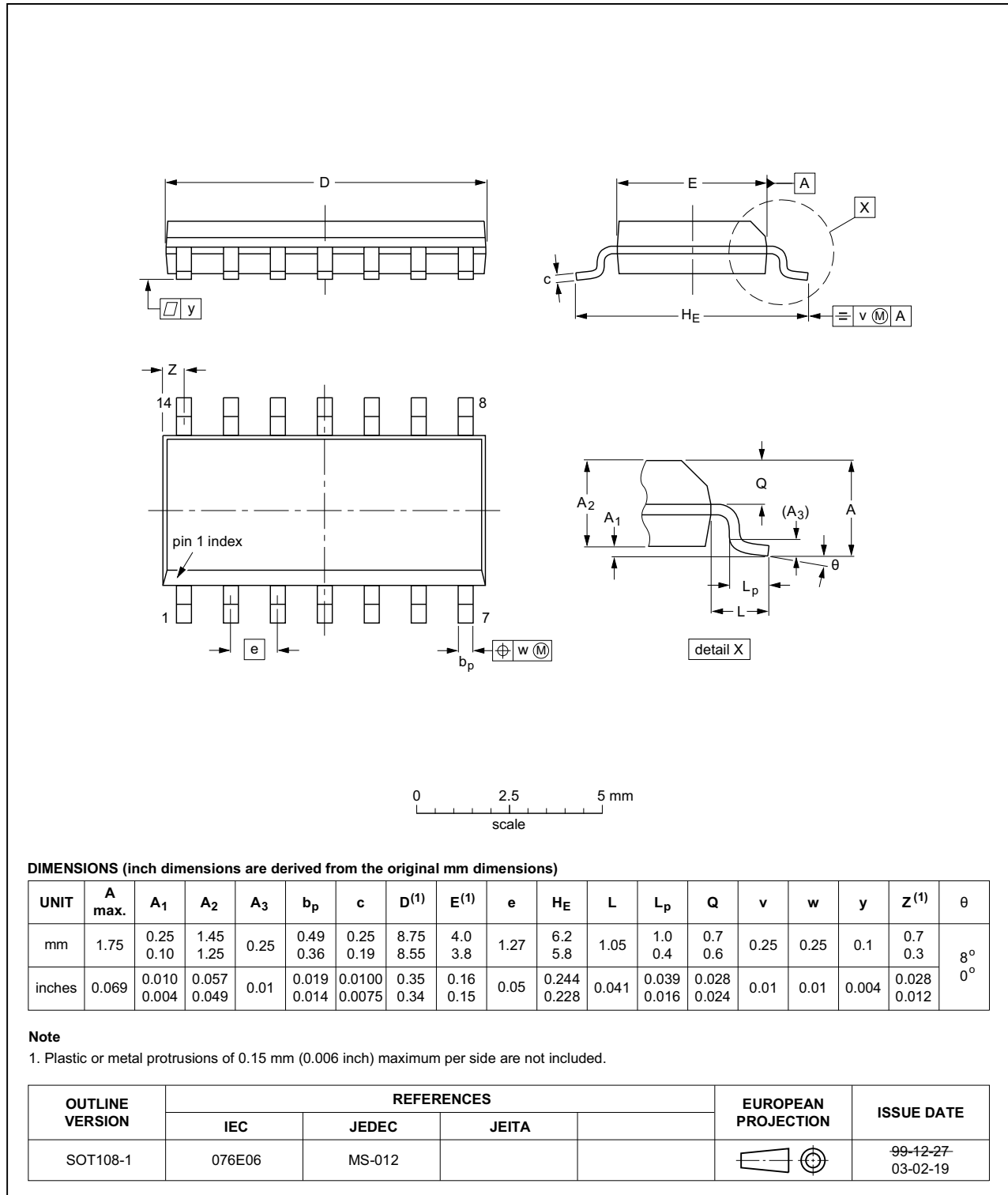


Fig 9. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



Fig 10. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



Fig 11. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

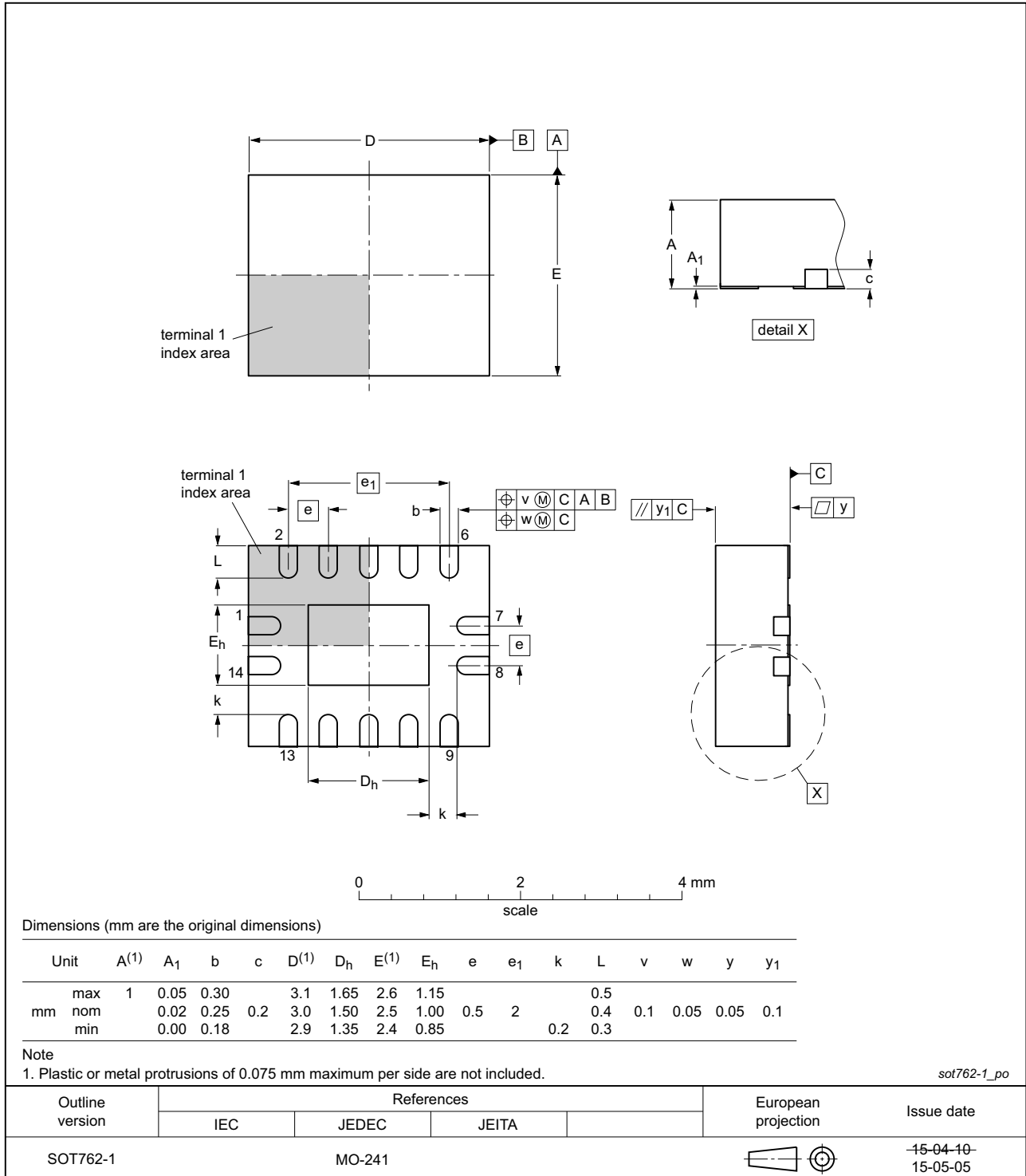


Fig 12. Package outline SOT762-1 (DHVQFN14)

## 13. Abbreviations

Table 9. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT_LVTH125 v.7	20160531	Product data sheet	-	74LVT125 v.6
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74LVT_LVTH125 v.6	20060306	Product data sheet	-	74LVT125 v.5
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 3</a>: Added type numbers 74LVTH125D, 74LVTH125DB, 74LVTH125PW and 74LVTH125BQ.</li> </ul>			
74LVT125 v.5	20050210	Product data sheet	-	74LVT125 v.4
74LVT125 v.4	20050207	Product data sheet	-	74LVT125 v.3
74LVT125 v.3	20040624	Product data sheet	-	74LVT125 v.2
74LVT125 v.2	19980219	Product specification	-	74LVT125 v.1
74LVT125 v.1	-	-	-	-

## 15. Legal information

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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