THE DATASHEET OF

STW81103AT

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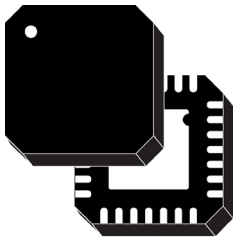
STW81103

Multi-band RF frequency synthesizer with integrated VCOs

Features

- Integer-N frequency synthesizer
- Dual differential integrated VCOs with automatic center frequency calibration:
  - 2500 - 3050 MHz (direct output)
  - 4350 - 5000 MHz (direct output)
  - 1250 - 1525 MHz (internal divider by 2)
  - 2175 - 2500 MHz (internal divider by 2)
  - 625 - 762.5 MHz (internal divider by 4)
  - 1087.5 - 1250 MHz (internal divider by 4)
- Excellent integrated phase noise
- Fast lock time: 150µs
- Dual modulus programmable prescaler (16/17 or 19/20)
- 2 programmable counters to achieve a feedback division ratio from 256 to 65551 (prescaler 16/17) and from 361 to 77836 (prescaler 19/20).
- Programmable reference frequency divider (10 bits)
- Phase frequency comparator and charge pump
- Programmable charge pump current
- Digital lock detector
- Dual digital bus interface: SPI and I^2C bus (fast mode) with 3 bit programmable address ($1100A_2A_1A_0$)
- 3.3 V power supply
- Power down mode (hardware and software)
- Small size exposed pad VFQFPN28 package 5 mm x 5 mm x 1.0 mm
- Process: BICMOS 0.35 µm SiGe



VFQFPN28

Applications

- 2.5G and 3G Cellular infrastructure equipment
- CATV equipment
- Instrumentation and test equipment
- Other wireless communication systems

Description

The STMicroelectronics STW81103 is an integrated RF synthesizer with voltage controlled oscillators (VCOs). Showing high performance, high integration, low power, and multi-band performances, STW81103 is a low cost one chip alternative to discrete PLL and VCOs solutions.

STW81103 includes an Integer-N frequency synthesizer and two fully integrated VCOs featuring low phase noise performance and a noise floor of -155dBc/Hz. The combination of wide frequency range VCOs (thanks to center-frequency calibration over 32 sub-bands) and multiple output options (direct output, divided by 2 or divided by 4) allows to cover the 625 MHz-762.5 MHz, the 1087.5 MHz-1525 MHz, the 2175 MHz-3050 MHz and the 4350 MHz-5000 MHz bands.

The STW81103 is designed with STMicroelectronics advanced 0.35 µm SiGe process.

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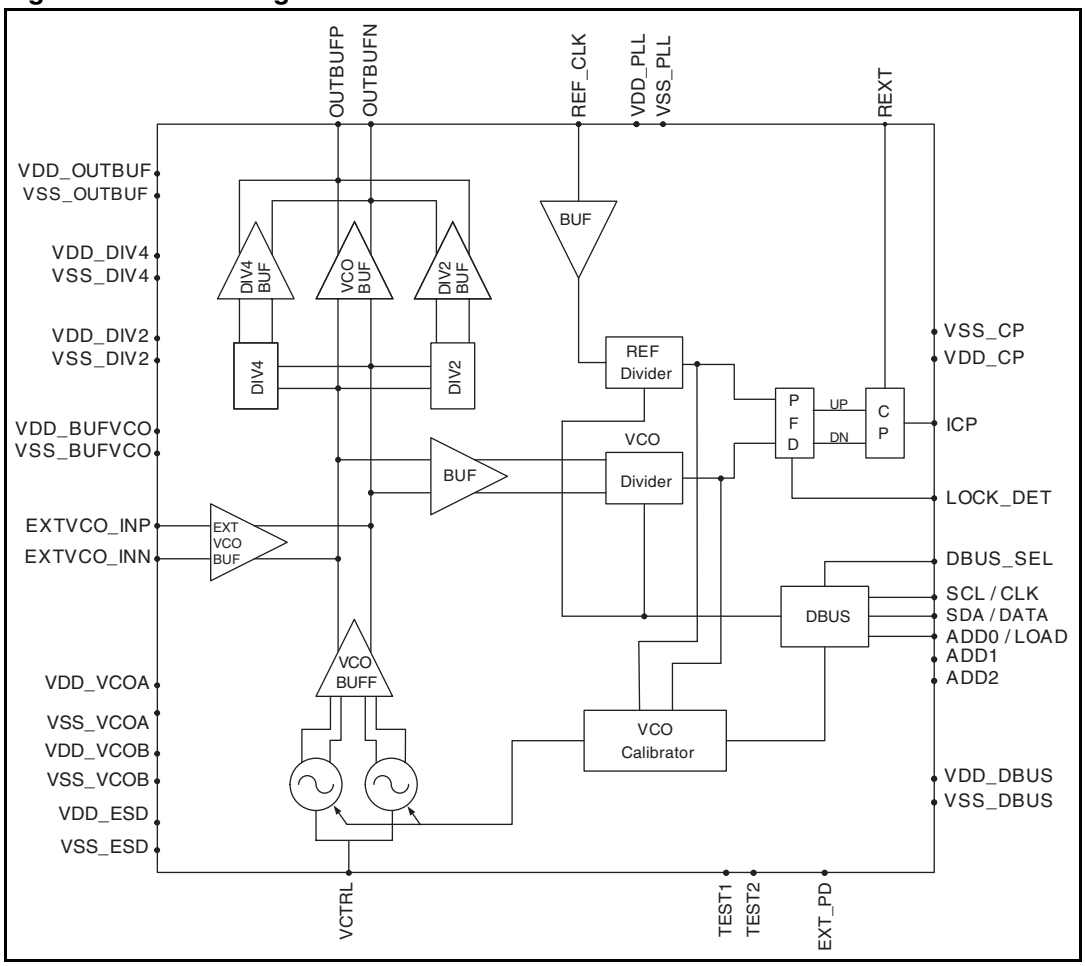
1 Block diagram and pin configuration

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin configuration

Figure 2. Pin connection (top view)

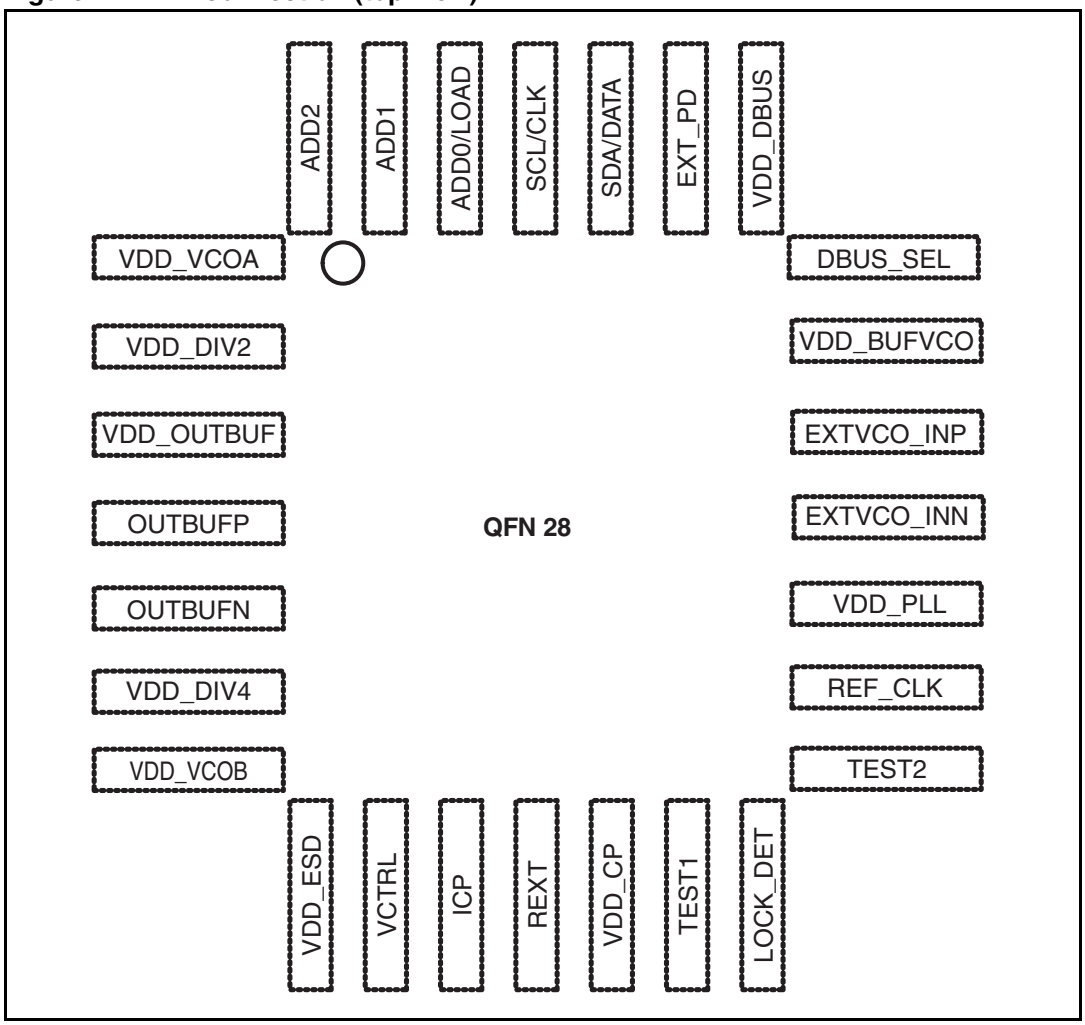


Table 1. Pin description

Pin No	Name	Description	Observation
1	VDD_VCOA	VCO A power supply	
2	VDD_DIV2	Divider by 2 power supply	
3	VDD_OUTBUF	Output buffer power supply	
4	OUTBUFP	LO buffer positive output	Open collector
5	OUTBUFN	LO buffer negative output	Open collector
6	VDD_DIV4	Divider by 4 power supply	
7	VDD_VCOB	VCO B power supply	
8	VDD_ESD	ESD positive rail power supply	
9	VCTRL	VCO control voltage	

Table 1. Pin description (continued)

Pin No	Name	Description	Observation
10	ICP	PLL charge pump output	
11	REXT	External resistance connection for PLL charge pump	
12	VDD_CP	Power supply for charge pump	
13	TEST1	Test input 1	For test purposes only; must be connected to GND
14	LOCK_DET	Lock detector	CMOS output (I_{OUT}=4mA)
15	TEST2	Test input 2	For test purposes only; must be connected to GND
16	REF_CLK	Reference clock input	
17	VDD_PLL	PLL digital power supply	
18	EXTVCO_INN	External VCO negative input	For test purposes only; must be connected to GND
19	EXTVCO_INP	External VCO positive input	For test purposes only; must be connected to GND
20	VDD_BUFVCO	VCO buffer power supply	
21	DBUS_SEL	Digital Bus Interface select	CMOS input
22	VDD_DBUS	SPI and I^2C bus power supply	
23	EXT_PD	Power down hardware ‘0’ device ON; ‘1’ device OFF	CMOS input
24	SDA/DATA	I2CBUS/SPI data line	CMOS Bidir Schmitt triggered (I_{OUT}=4mA)
25	SCL/CLK	I2CBUS/SPI clock line	CMOS input Schmitt triggered
26	ADD0/LOAD	I2CBUS address select pin/ SPI load line	CMOS input
27	ADD1	I2CBUS address select pin	CMOS input; must be connected to GND in SPI mode
28	ADD2	I2CBUS address select pin	CMOS input; must be connected to GND in SPI mode

2 Electrical specifications

2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Values	Unit
AV_{CC}	Analog supply voltage	0 to 4.6	V
DV_{CC}	Digital supply voltage	0 to 4.6	V
T_{stg}	Storage temperature	+150	°C
ESD	Electrical static discharge - HBM(1) - CDM-JEDEC standard - MM	 4 1.5 0.2	kV

1. The maximum rating of the ESD protection circuitry on pin 4 and pin 5 is 800 V.

2.2 Operating conditions

Table 3. Operating conditions (1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		3.0	3.3	3.6	V
DV_{CC}	Digital supply voltage		3.0	3.3	3.6	V
I_{VDD1}	V_{DD1} current consumption			90		mA
I_{VDD2}	V_{DD2} current consumption			12		mA
T_{amb}	Operating ambient temperature		-40		85	°C
T_j	Maximum junction temperature				125	°C
$R_{th\ j\text{-}a}$	Junction to ambient package thermal resistance	Multilayer JEDEC board		44		°C/W
$R_{th\ j\text{-}b}$	Junction to board package thermal resistance	Multilayer JEDEC board		26.3		°C/W
$R_{th\ j\text{-}c}$	Junction to case package thermal resistance	Multilayer JEDEC board		6.3		°C/W

1. Refer to *Figure 36: Typical application diagram*.

2.3 Digital logic levels

Table 4. Digital logic levels

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units
V_{il}	Low-level input voltage				0.2*Vdd	V
V_{ih}	High-level input voltage		0.8*Vdd			V
V_{hyst}	Schmitt trigger hysteresis		0.8			V
V_{ol}	Low-level output voltage				0.4	V
V_{oh}	High-level output voltage		0.85*Vdd			V

2.4 Electrical specifications

All electrical specifications are intended for a 3.3 V supply voltage.

Table 5. Electrical specifications

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Output frequency range						
F_{OUTA}	Output frequency range with VCOA	Direct output	2500		3050	MHz
		Divider by 2	1250		1525	MHz
		Divider by 4	625		762.5	MHz
F_{OUTB}	Output frequency range with VCOB	Direct output	4350		5000	MHz
		Divider by 2	2175		2500	MHz
		Divider by 4	1087.5		1250	MHz
VCO dividers						
N	VCO divider ratio	Prescaler 16/17	256		65551	
		Prescaler 19/20	361		77836	
Reference clock and phase frequency detector						
F_{ref}	Reference input frequency		10		200	MHz
	Reference input sensitivity(1)		0.35	1	1.5	Vpeak
R	Reference divider ratio		2		1023	
F_{PFD}	PFD input frequency				16	MHz
F_{STEP}	Frequency step(2)	Prescaler 16/17	F_{OUT}/ 65551		F_{OUT}/ 256	Hz
		Prescaler 19/20	F_{OUT}/ 77836		F_{OUT}/ 361	Hz

Table 5. Electrical specifications (continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Charge pump						
I_{CP}	ICP sink/source(3)	3-bit programmable			5	mA
V_{OCP}	Output voltage compliance range		0.4		V_{dd}-0.3	V
	Spurious(4)	Direct output (F_{PFD}=200 kHz)		-76		dBc
		Divider by 2 (F_{PFD}=400 kHz)		-82		dBc
		Divider by 4 (F_{PFD}=800 kHz)		-88		dBc
VCOs						
K_{VCOA}	VCOA sensitivity(5)	Lower frequency range	45	65	85	MHz/V
		Intermediate frequency range	60	80	105	MHz/V
		Higher frequency range	85	105	145	MHz/V
K_{VCOB}	VCOB sensitivity(5)	Lower frequency range	45	65	85	MHz/V
		Intermediate frequency range	60	80	100	MHz/V
		Higher frequency range	85	100	130	MHz/V
ΔT_{LK}	Maximum temperature variation for continuous lock(5) (6)	VCO A	125			°C
		VCO B	95			°C
	VCOA pushing(5)			4	7	MHz/V
	VCOB pushing(5)			15	21	MHz/V
V_{CTRL}	VCO control voltage(5)		0.4		3	V
	LO harmonic spurious(5)				-20	dBc
I_{VCOA}	VCOA current consumption	F_{VCO}=2.8 GHz; amplitude[11]		30		mA
		F_{VCO}=2.8 GHz; amplitude[00]		16		mA
I_{VCOB}	VCOB current consumption	F_{VCO}=4.7 GHz; amplitude[11]		24		mA
		F_{VCO}=4.7 GHz; amplitude[00]		13		mA
I_{VCOBUF}	VCO buffer consumption			15		mA
I_{DIV2}	Divider by 2 consumption			17		mA
I_{DIV4}	Divider by 4 consumption			14		mA
LO output buffer						
P_{LO}	Output level			0		dBm
R_L	Return loss	Matched to 50 ohms		15		dB
I_{OUTBUF}	Current consumption	DIV4 Buff		26		mA
		DIV2 Buff		23		mA
		Direct output		39		mA

Table 5. Electrical specifications (continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
External VCO						
	Frequency range		0.625		5.0	GHz
	Input level		-10		+6	dBm
	Current consumption	VCO internal buffer		28		mA
PLL miscellaneous						
I_{PLL}	Current consumption	Input buffer, prescaler, digital dividers, misc.		12		mA
t_{lock}	Lockup time(5) (7)	25 kHz PLL bandwidth; within 1 ppm of frequency error		150		µs

1. In order to achieve best phase noise performance 1 V peak level is suggested.
2. The frequency step is related to the PFD input frequency as follows:
   - $F_{step} = F_{PFD}$ for direct output
   - $F_{step} = F_{PFD}/2$ for divided by 2 output
   - $F_{step} = F_{PFD}/4$ for divided by 4 output
3. See relationship between ICP and REXT in *Section 5.7: Charge pump*.
4. The level of the spurs may change depending on PFD frequency, charge pump current, selected channel and PLL loop BW.
5. Guaranteed by design and specification.
6. When setting a specified output frequency, the VCO calibration procedure must be run in order to select the best sub-range for the VCO covering the desired frequency. Once programmed at the initial temperature T_0 inside the operating temperature range (-40 °C to +85 °C), the synthesizer is able to maintain the lock status only if the temperature drift (in either direction) is within the limit specified by ΔT_{LK}, provided that the final temperature T_1 is still inside the nominal range. If higher ΔT are required the **"VCO calibration auto-restart"** feature can be enabled, thus allowing to re-start the VCO calibration procedure automatically when the part loose the lock condition (trigger on lock detector signal).
7. Frequency jump from 2250 to 2400 MHz; it includes the time required by the VCO calibration procedure (7 F_{PFD} cycles with F_{PFD}=400 kHz).

2.5 Phase noise specification

Table 6. Phase noise specification (1)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
In-band phase noise floor – closed loop(2)					
Normalized inband phase noise floor	ICP=4 mA, PLL BW=50 kHz; including reference clock contribution		-222		dBc/Hz
Inband phase noise floor direct output			-222+20log(N)+10log(F_{PFD})		dBc/Hz
Inband phase noise floor divider by 2			-228+20log(N)+10log(F_{PFD})		dBc/Hz
Inband phase noise floor divider by 4			-234+20log(N)+10log(F_{PFD})		dBc/Hz
PLL integrated phase noise – direct output					
Integrated phase noise 100 Hz to 40 MHz	F_{OUT}=4.675 GHz, F_{PFD}=200 kHz, F_{STEP}=200 kHz, PLL BW = 15 kHz, ICP=3 mA		-34.6		dBc
			1.5		° rms
PLL integrated phase noise – divider by 2					
Integrated phase noise 100 Hz to 40 MHz	F_{OUT}=2.3376 GHz, F_{PFD}=400 kHz, F_{STEP}=200 kHz, PLL BW=25 kHz, ICP=2 mA		-42.6		dBc
			0.6		° rms
PLL integrated phase noise – divider by 4					
Integrated phase noise 100 Hz to 40 MHz	F_{OUT}=1.1688 GHz, F_{PFD}=800 kHz, F_{STEP}=200 kHz, PLL BW=35 kHz, ICP=1.5 mA		-49.5		dBc
			0.27		° rms
VCO A direct (2500 MHz-3050 MHz) – open loop(3)					
Phase noise @ 1 kHz			-59		dBc/Hz
Phase noise @ 10 kHz			-87		dBc/Hz
Phase noise @ 100 kHz			-109		dBc/Hz
Phase noise @ 1 MHz			-131		dBc/Hz
Phase noise @ 10 MHz			-151		dBc/Hz
Phase noise @ 40 MHz			-161		dBc/Hz
VCO B direct (4350 MHz-5000 MHz) – open loop(3)					
Phase noise @ 1 kHz			-54		dBc/Hz
Phase noise @ 10 kHz			-82		dBc/Hz
Phase noise @ 100 kHz			-105		dBc/Hz
Phase noise @ 1 MHz			-127		dBc/Hz
Phase noise @ 10 MHz			-147		dBc/Hz
Phase noise @ 40 MHz			-157		dBc/Hz

Table 6. Phase noise specification (1) (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
VCO A with divider by 2 (1250 MHz-1525 MHz) – open loop(3)					
Phase noise @ 1 kHz			-65		dBc/Hz
Phase noise @ 10 kHz			-93		dBc/Hz
Phase noise @ 100 kHz			-115		dBc/Hz
Phase noise @ 1 MHz			-137		dBc/Hz
Phase noise @ 10 MHz			-153		dBc/Hz
Phase noise floor @ 40 MHz			-155		dBc/Hz
VCO B with divider by 2 (2175 MHz-2500 MHz) – open loop(3)					
Phase noise @ 1 kHz			-60		dBc/Hz
Phase noise @ 10 kHz			-88		dBc/Hz
Phase noise @ 100 kHz			-111		dBc/Hz
Phase noise @ 1 MHz			-132		dBc/Hz
Phase noise @ 10 MHz			-150		dBc/Hz
Phase noise floor @ 40 MHz			-154		dBc/Hz
VCO A with divider by 4 (625 MHz-762.5 MHz) – open loop(3)					
Phase noise @ 1 kHz			-71		dBc/Hz
Phase noise @ 10 kHz			-99		dBc/Hz
Phase noise @ 100 kHz			-121		dBc/Hz
Phase noise @ 1 MHz			-142		dBc/Hz
Phase noise @ 10 MHz			-154		dBc/Hz
Phase noise floor @ 40 MHz			-155		dBc/Hz
VCO B with divider by 4 (1087.5 MHz-1250 MHz) – open loop(3)					
Phase noise @ 1 kHz			-66		dBc/Hz
Phase noise @ 10 kHz			-94		dBc/Hz
Phase noise @ 100 kHz			-117		dBc/Hz
Phase noise @ 1 MHz			-138		dBc/Hz
Phase noise @ 10 MHz			-153		dBc/Hz
Phase noise floor @ 40 MHz			-154		dBc/Hz

1. Phase Noise SSB. VCO amplitude setting to value [11]. All closed-loop performances are specified using a reference clock signal at 76.8 MHz with a phase noise of -135 dBc/Hz @1 kHz offset, -145dBc/Hz @10kHz offset and -149.5 dBc/Hz of noise floor.
2. Normalized PN = Measured PN – 20log(N) – 10log(F_{PFD}), where N is the VCO divider ratio (N=B*P+A) and F_{PFD} is the comparison frequency at the PFD input.
3. Typical phase noise at centre band frequency.

An evaluation kit is available upon request, including a powerful simulation tool (STWPLLSim) that allows a very accurate estimation of the device's phase noise according to the desired project parameters (VCO frequency, selected output stage, reference clock, frequency step, and so on); refer to *Section 8: Application information* for more details.

3 Typical performance characteristics

Phase noise is measured with the Agilent E5052A Signal Source Analyzer. All closed-loop measurements are done with F_{STEP}=200 kHz, with the F_{PFD} and charge pump current properly set. The loop filter configuration is depicted in *Figure 36: Typical application diagram*, and the reference clock signal is at 76.8 MHz with a phase noise of -135 dBc/Hz @1 kHz offset, -145 dBc/Hz @10 kHz offset and -149.5 dBc/Hz of noise floor.

Figure 3. VCO A (direct output) open loop phase noise

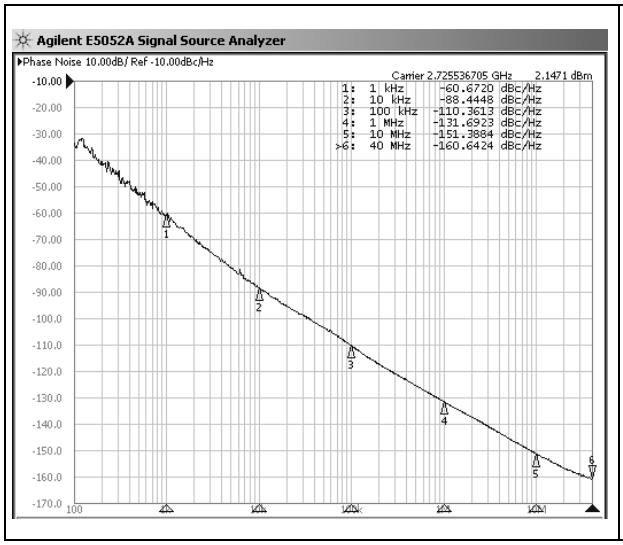


Figure 4. VCO B (direct output) open loop phase noise

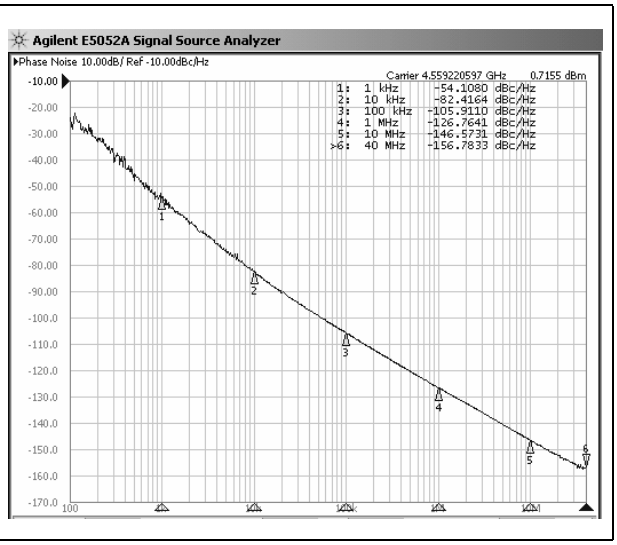


Figure 5. VCO A (direct output) closed loop phase noise at 2.775 GHz (F_{STEP}=200 kHz; F_{PFD}=200 kHz; I_{CP}=2 mA)

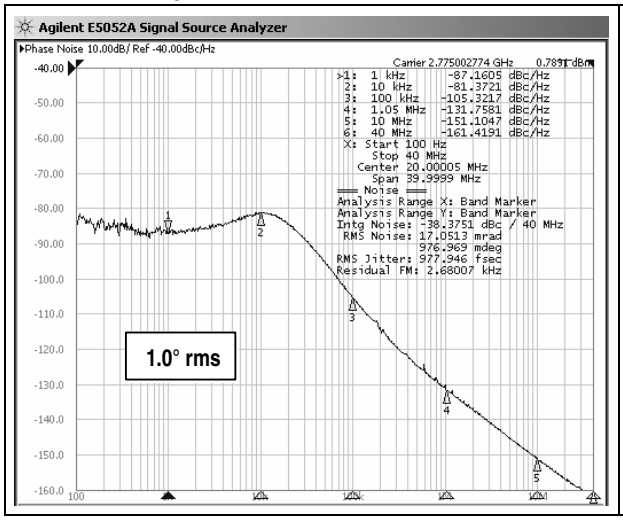


Figure 6. VCO B (direct output) closed loop phase noise at 4.675 GHz (F_{STEP}=200 kHz; F_{PFD}=200 kHz; I_{CP}=3 mA)

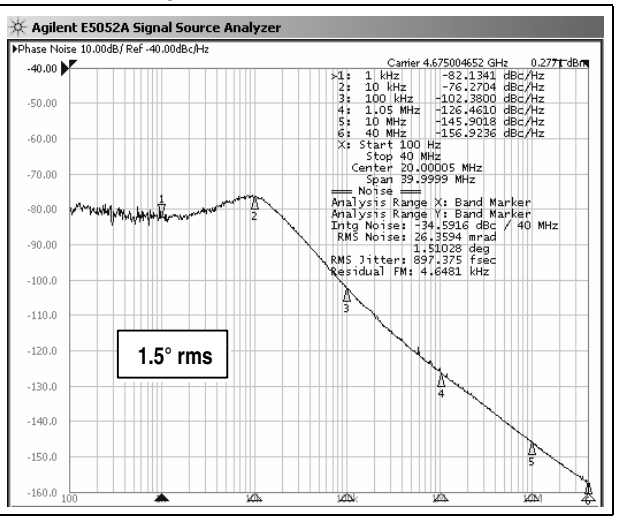


Figure 7. VCO A (div. by 2 output) closed loop phase noise at 1.3876 GHz (F_{STEP}=200 kHz; F_{PFD}=400 kHz; I_{CP}=1.5 mA)

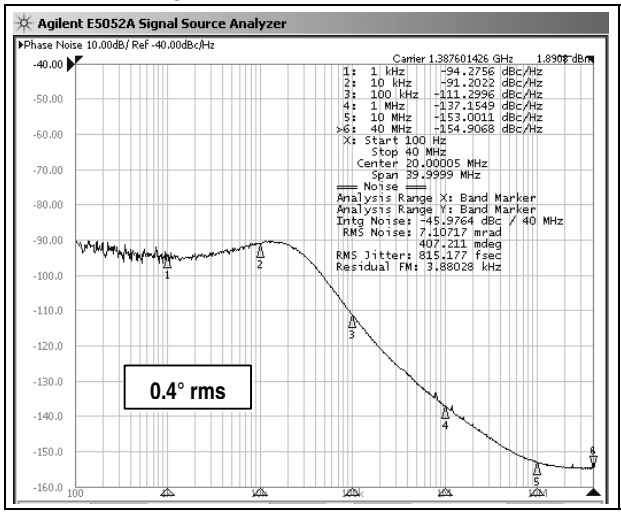


Figure 8. VCO B (div. by 2 output) closed loop phase noise at 2.3376 GHz (F_{STEP}=200 kHz; F_{PFD}=400 kHz; I_{CP}=2 mA)

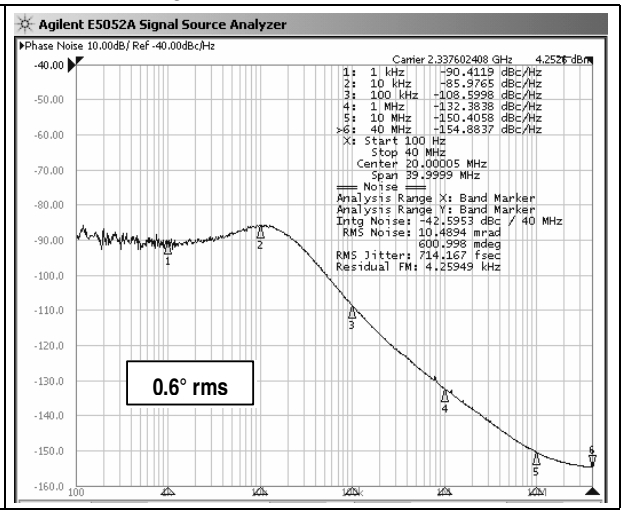


Figure 9. VCO A (div. by 4 output) closed loop phase noise at 693.8 MHz (F_{STEP}=200 kHz; F_{PFD}=800 kHz; I_{CP}=1 mA)

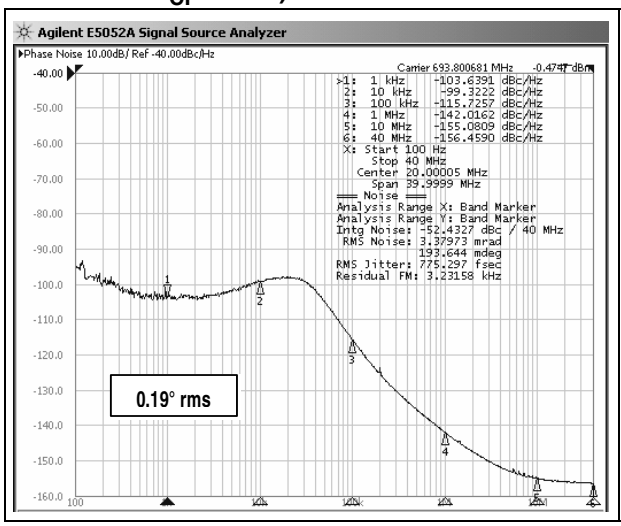


Figure 10. VCO B (div. by 4 output) closed loop phase noise at 1168.8 MHz (F_{STEP}=200 kHz; F_{PFD}=800 kHz; I_{CP}=1.5 mA)

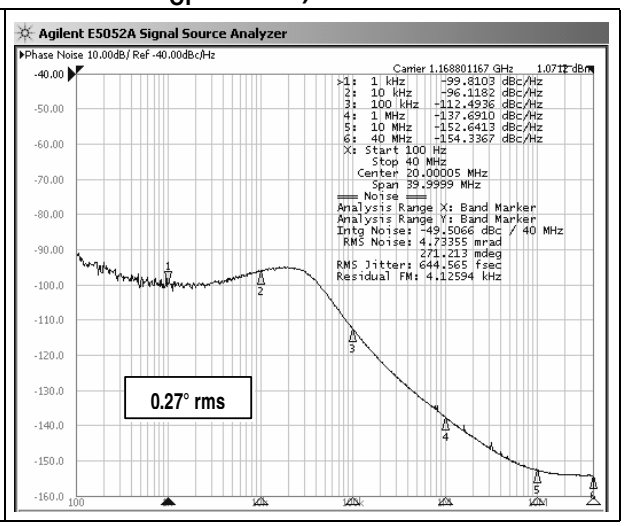


Figure 11. PFD frequency spurs (direct output; F_{PFD}=200 kHz)

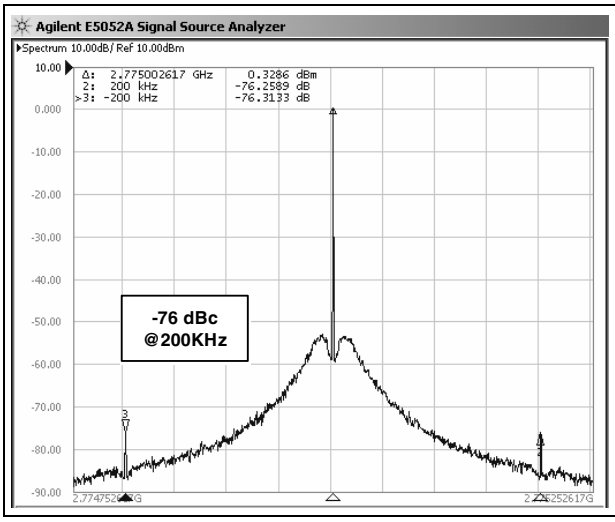


Figure 12. PFD frequency spurs (div. by 2 output; F_{PFD}=400 kHz)

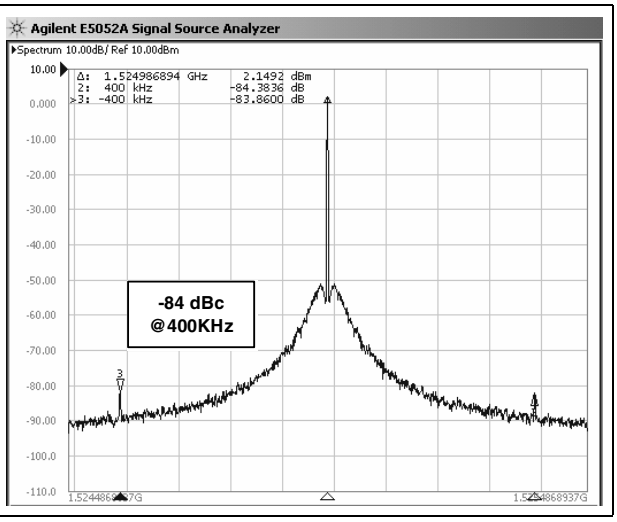


Figure 13. PFD frequency spurs (div. by 4 output; F_{PFD}=800 kHz)

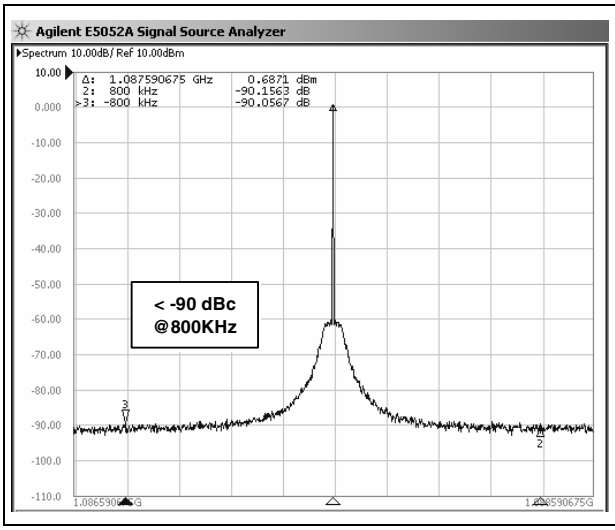
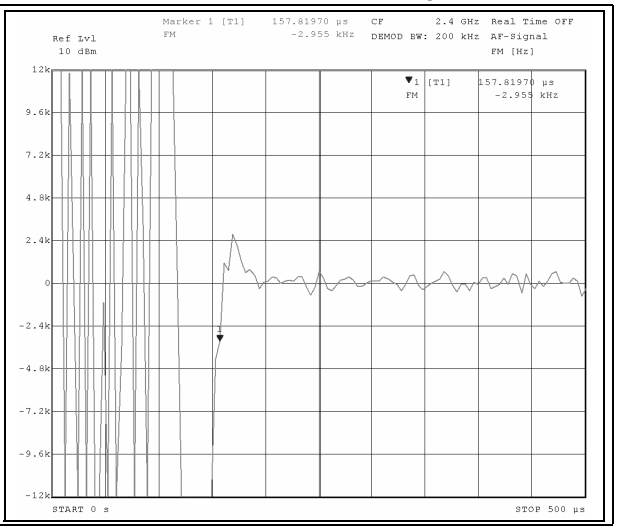


Figure 14. Settling time (final frequency=2.4 GHz; F_{PFD}=400 kHz; I_{CP}=2.5 mA)



4 General description

Figure 1: Block diagram shows the separate blocks that, when integrated, form an Integer-N PLL frequency synthesizer.

The STW81103 consists of two internal low-noise VCOs with buffer blocks, a divider by 2, a divider by 4, a low-noise PFD (phase frequency detector), a precise charge pump, a 10-bit programmable reference divider, two programmable counters and a programmable dual-modulus prescaler. The 5-bit A-counter and 12-bit B-counter, in conjunction with the dual-modulus prescaler P/P+1 (16/17 or 19/20), implement an N integer divider, where N = B*P +A. The division ratio of both reference and VCO dividers is controlled through the selected digital interface (I^2C bus or SPI).

The digital interface type is selected through the proper hardware connection of pin DBUS_SEL (0 V for I^2C bus, 3.3 V for SPI).

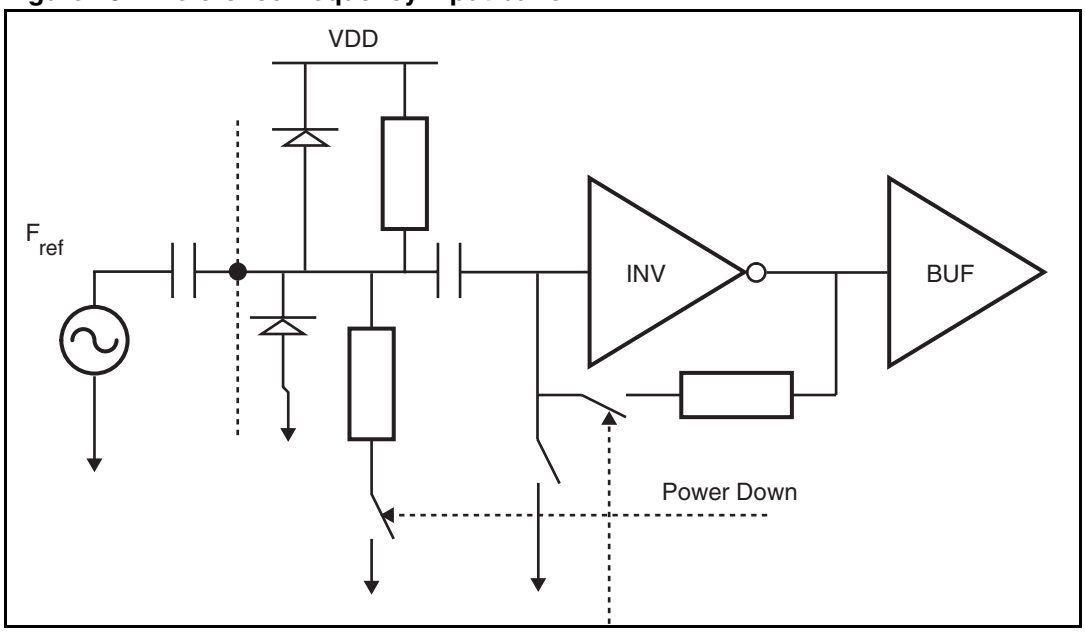
All devices operate with a power supply of 3.3 V, and can be powered down when not in use.

5 Circuit description

5.1 Reference input stage

The reference input stage is shown in *Figure 15*. The resistor network feeds a DC bias at the F_{ref} input, while the inverter used as the frequency reference buffer is AC coupled.

Figure 15. Reference frequency input buffer



5.2 Reference divider

The 10-bit programmable reference counter allows division of the input reference frequency to produce the input clock to the PFD. The division ratio is programmed through the digital interface.

5.3 Prescaler

The dual-modulus prescaler P/P+1 takes the CML clock from the VCO buffer and divides it down to a manageable frequency for the CMOS A and B counters. The modulus P is programmable and can be set to 16 or 19. The prescaler is based on a synchronous 4/5 core whose division ratio depends on the state of the modulus input.

5.4 A and B counters

The 5-bit A-counter and 12-bit B-counter, in conjunction with the selected dual modulus (16/17 or 19/20) prescaler, allow the generation of output frequencies that are spaced only by the reference frequency divided by the reference division ratio. The division ratio and the VCO output frequency are given by the following formulas:

$N = B \times P + A$

$$F_{VCO} = \frac{(B \times P + A)}{R} \times F_{ref}$$

where

F_{VCO}: output frequency of VCO

P: modulus of dual modulus prescaler (16 or 19 selected through the digital interface)

B: division ratio of the main counter

A: division ratio of the swallow counter

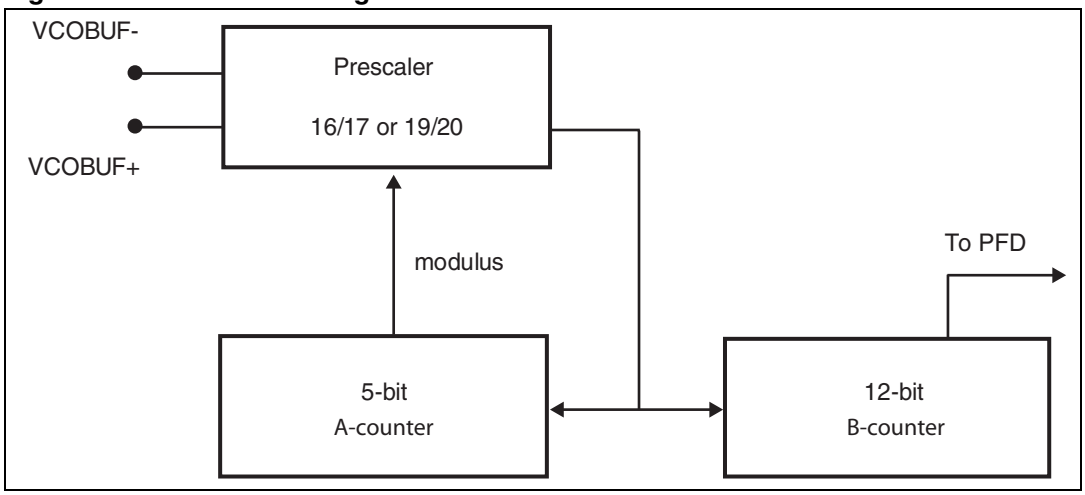
F_{ref}: input reference frequency

R: division ratio of the reference counter

N: division ratio of the PLL

For the VCO divider to work correctly, B absolutely must be greater than A, which can take any value ranging from 0 to 31. The value range of N is either from 256 to 65551 (if P=16) or from 361 to 77836 (P=19).

Figure 16. VCO divider diagram

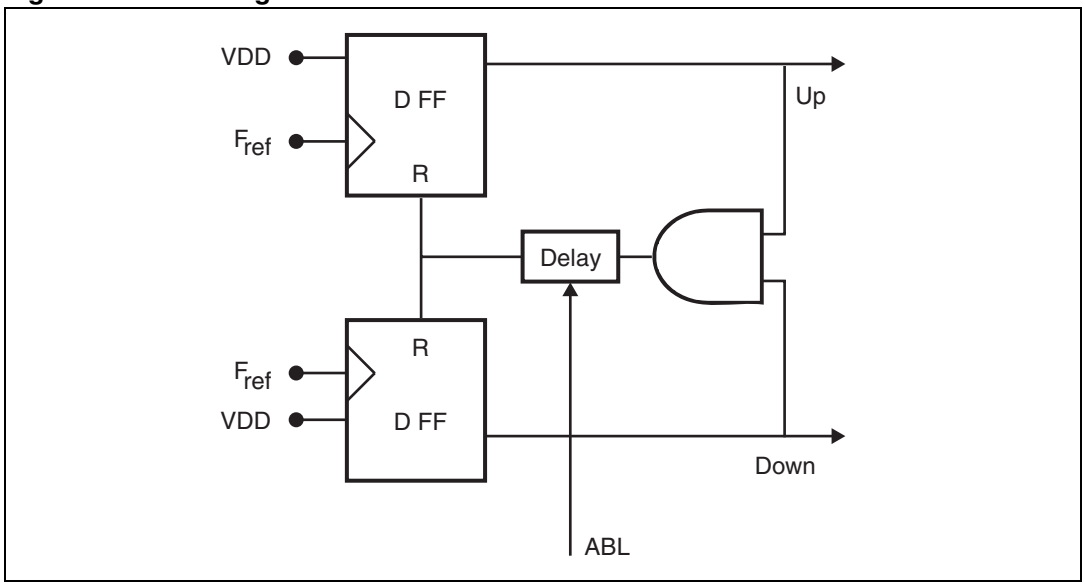


5.5 Phase frequency detector (PFD)

The PFD takes inputs from the reference and the VCO dividers and produces an output proportional to the phase error. The PFD includes a delay gate that controls the width of the anti-backlash pulse. This pulse ensures that there is no dead zone in the PFD transfer function.

Figure 17 is a simplified schematic of the PFD.

Figure 17. PFD diagram



5.6 Lock detect

This signal indicates that the difference between rising edges of both UP and DOWN PFD signals is found to be shorter than the fixed delay (roughly 5 ns). The Lock Detect signal is high when the PLL is locked and low when the PLL is unlocked. Lock Detect consumes current only during PLL transients.

5.7 Charge pump

This block drives two matched current sources, I_{UP} and I_{DOWN}, which are controlled respectively by UP and DOWN PFD outputs. The nominal value of the output current is controlled by an external resistor (connected to the REXT input pin) and a 3-bit word that allows selection among 8 different values.

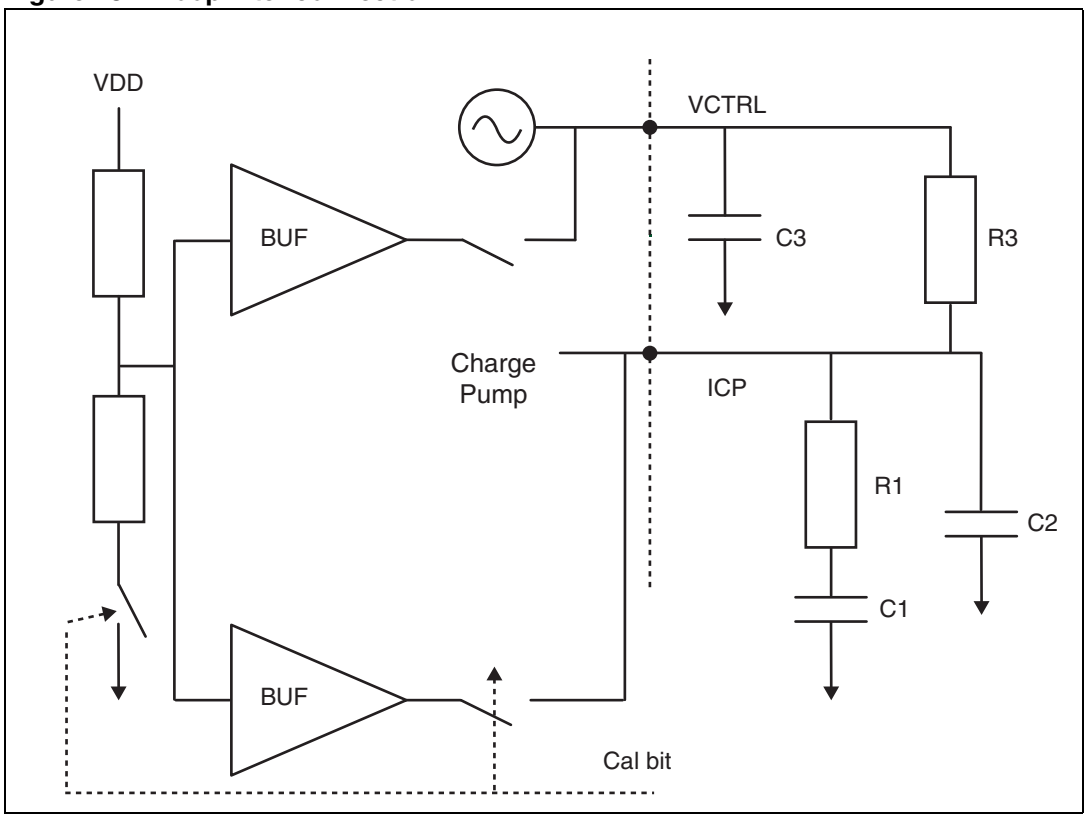
The minimum value of the output current is: I_{MIN} = 2*VBG/REXT (VBG~1.17 V)

Table 7. Current value vs. selection

CPSEL2	CPSEL1	CPSEL0	Current	Value for REXT=4.7 KΩ
0	0	0	I_{MIN}	0.5 mA
0	0	1	$2*I_{MIN}$	1.0 mA
0	1	0	$3*I_{MIN}$	1.5 mA
0	1	1	$4*I_{MIN}$	2.0 mA
1	0	0	$5*I_{MIN}$	2.5 mA
1	0	1	$6*I_{MIN}$	3.0 mA
1	1	0	$7*I_{MIN}$	3.5 mA
1	1	1	$8*I_{MIN}$	4.0 mA

Note: The current is output on pin ICP. During VCO auto-calibration, the ICP and VCTRL pins are forced to VDD/2.

Figure 18. Loop filter connection



5.8 Voltage controlled oscillators

5.8.1 VCO selection

The STW81103 integrates two low-noise VCOs to cover a wide band from:

- 2500 MHz to 3050 MHz and from 4350 MHz to 5000 MHz (direct output)
- 1250 MHz to 1525 MHz and from 2175 MHz to 2500 MHz (selecting divider by 2)
- 625 MHz to 762.5 MHz and from 1087.5 MHz to 1250 MHz (selecting divider by 4)

The frequency range is 2500 MHz-3050 MHz for VCO A, and 4350 MHz-5000 MHz for VCO B.

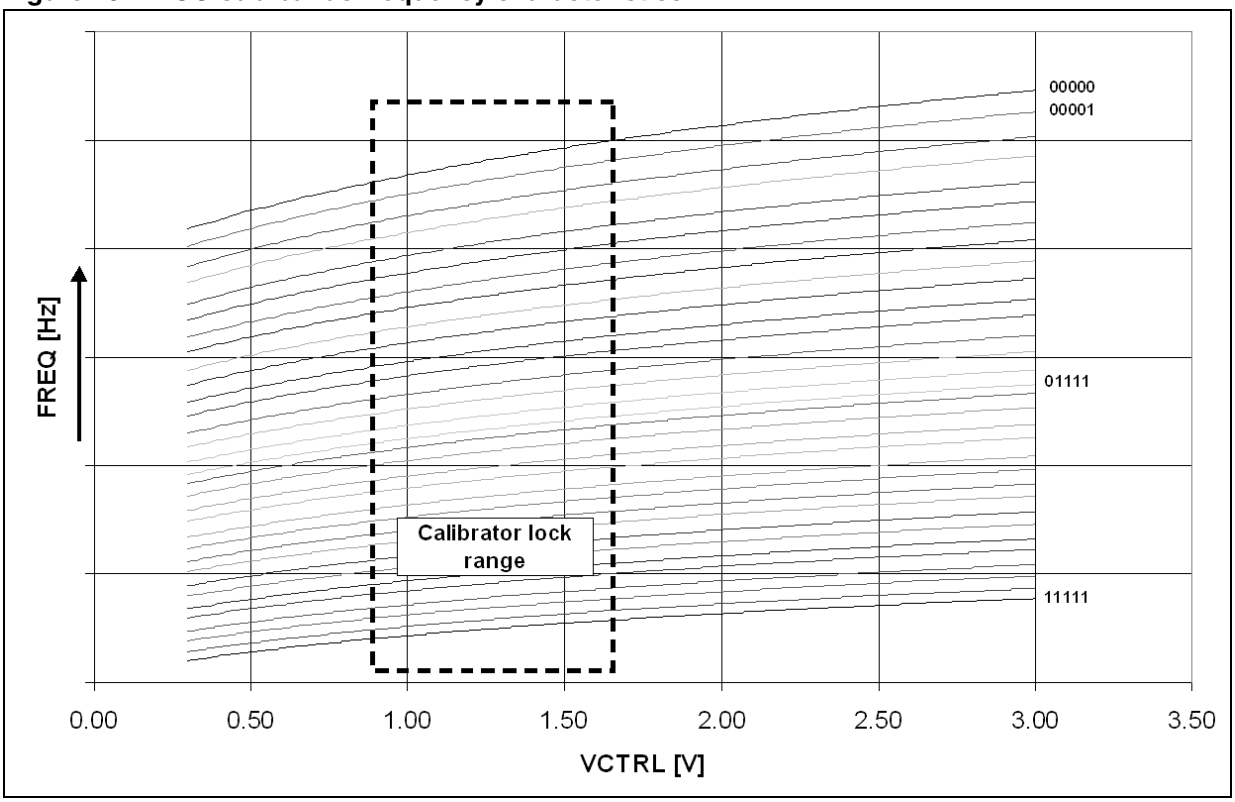
5.8.2 VCO frequency calibration

Both VCOs can operate on 32 frequency ranges that are selected by adding or subtracting capacitors from the resonator. These frequency ranges are intended to cover the wide band of operation and compensate for process variation on the VCO center frequency.

The range is automatically selected when the SERCAL bit is set to 1. The charge pump is inhibited, and the ICP and VCTRL pins are at VDD/2 volts. The ranges are then tested with this VCO input voltage to select the one nearest to the desired output frequency ($F_{OUT} = N*F_{ref}/R$).

After this selection, the SERCAL bit is automatically reset to 0 and the charge pump is once again enabled. To enable a fast settle, the PLL needs only to perform fine adjustments around VDD/2 on the loop filter to reach F_{OUT}.

Figure 19. VCO sub-bands frequency characteristics



The SERCAL bit should be set to “1” at each division ratio change. The VCO calibration procedure takes approximately 7 periods of the PFD frequency.

The maximum allowed F_{PFD} to perform the calibration process is 1 MHz. When using a higher F_{PFD}, follow the steps below:

1. Calibrate the VCO at the desired frequency with an F_{PFD} less than 1 MHz.
2. Set the ratio of the A, B and R dividers for the desired F_{PFD}.

VCO calibration auto-restart feature

The VCO calibration auto-restart feature, once activated, allows to restart the calibration procedure when the lock detector reports that the PLL has moved to an unlock condition (trigger on ‘1’ to ‘0’ transition of lock detector signal).

This situation could happen if the device experiences a significant temperature variation. Once programmed at the initial temperature T_0 inside the operating temperature range (-40 °C to +85 °C), the synthesizer is able to maintain the lock status only if the temperature drift (in either direction) is within the limit specified by the ΔT_{LK} parameter, provided that the final temperature T_1 is still inside the nominal range.

Each VCO featured by STW81103 has its specific ΔT_{LK} parameter reported in *Table 5*, that is typically lower than the maximum allowable drift (ΔT_{MAX}=125; from -40 °C to +85 °C and vice versa).

By enabling the VCO calibration auto-restart feature (through the CAL_AUTOSTART_EN bit), the part will be able to select again the proper VCO frequency sub-range if the temperature drift exceeds the ΔT_{LK} limit, without any external user command.

5.8.3 VCO voltage amplitude control

The voltage swing of the VCOs can be adjusted over four levels by means of two dedicated programming bits (PLL_A1 and PLL_A0). Higher amplitudes provide best phase noise, whereas lower amplitudes save power.

Table 8 gives the voltage swing level expected on the resonator nodes, the current consumption, and the phase noise at 1 MHz.

Table 8. VCO A performances versus amplitude setting (Freq = 2.8 GHz)

PLL_A[1:0]	Differential voltage swing (Vp)	Current consumption (mA)	PN @1 MHz (dBc/Hz)
00	1.1	16	-126
01	1.3	19	-127
10	1.9	27	-130
11	2.1	30	-131

Table 9. VCO B performances vs. amplitude setting (Freq = 4.7 GHz)

PLL_A[1:0]	Differential voltage swing (Vp)	Current consumption (mA)	PN at 1 MHz (dBc/Hz)
00	1.1	13	-121
01	1.3	15	-122
10	1.9	22	-126
11	2.1	24	-127

5.9 Output stage

The differential output signal of the synthesizer can be selected by software among three different signal paths (direct, divider by 2 and divider by 4) providing multi-band capability.

The selection of the output stage is done by programming properly the PD[4:0] bits.

The output stage is an open-collector structure which is able to meet different requirements over the desired output frequency range by proper connections on the PCB. Refer to *Section 8: Application information* for more details on PCB connections.

5.9.1 Output buffer control mode

This control mode allows to enable/disable the output stage by a hardware control pin (EXT_PD, pin#23) while the PLL stays locked at the desired frequency; in such a way a very fast switching time is achieved.

This feature can be useful in designing a ping-pong architecture saving the cost of an external RF switch.

The function of pin#23 (EXT_PD) is set with the OUTBUF_CTRL_EN bit as shown in *Table 10.*

Table 10. EXT_PD pin function setting

OUTBUF_CTRL_EN	Function of the EXT_PD pin	EXT_PD pin settings
0	Device hardware power down	EXT_PD = 0 V ➔ Device ON
		EXT_PD = 3.3 V ➔ Device OFF
1	Output Buffer control	EXT_PD = 0 V ➔ Output Stage ON
		EXT_PD = 3.3 V ➔ Output Stage OFF

5.10 External VCO buffer

Although the main benefits of the STW81103 are the two wideband and low-noise VCOs, the capability to use an external VCO is also provided.

The external VCO buffer is able to manage a signal coming from an external VCO in order to build a synthesizer using the STW81103 only as PLL IC. The output signal of the synthesizer can also be taken from the output section of the STW81103 (direct, divided by 2 or divided by 4 by) by properly setting the PD[4:0] bits, thus providing additional flexibility.

The external VCO signal can range from 625 MHz up to 5 GHz and its minimum power level must be -10 dBm.

6 I²C bus interface

The I²C bus interface is selected by hardware connection of pin #21 (DBUS_SEL) to 0 V.

Data is transmitted from microprocessor to the STW81103 through the 2-wire (SDA and SCL) I²C bus interface. The STW81103 is always a slave device.

The I²C bus protocol defines any device that sends data on the bus as a transmitter, and any device that reads the data as a receiver. The device controlling the data transfer is the master, and the others are slaves. The master always initiates the transfer and provides the serial clock for synchronization.

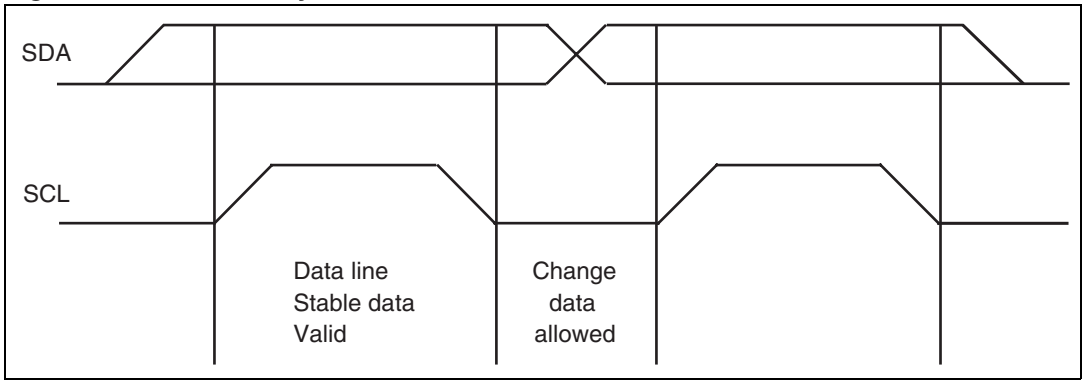
The STW81103 I²C bus supports Fast Mode operation (clock frequency up to 1MHz).

6.1 General features

6.1.1 Data validity

Data changes on the SDA line must only occur when the SCL is low. SDA transitions while the clock is high are used to identify a START or STOP condition.

Figure 20. Data validity



6.1.2 START and STOP conditions

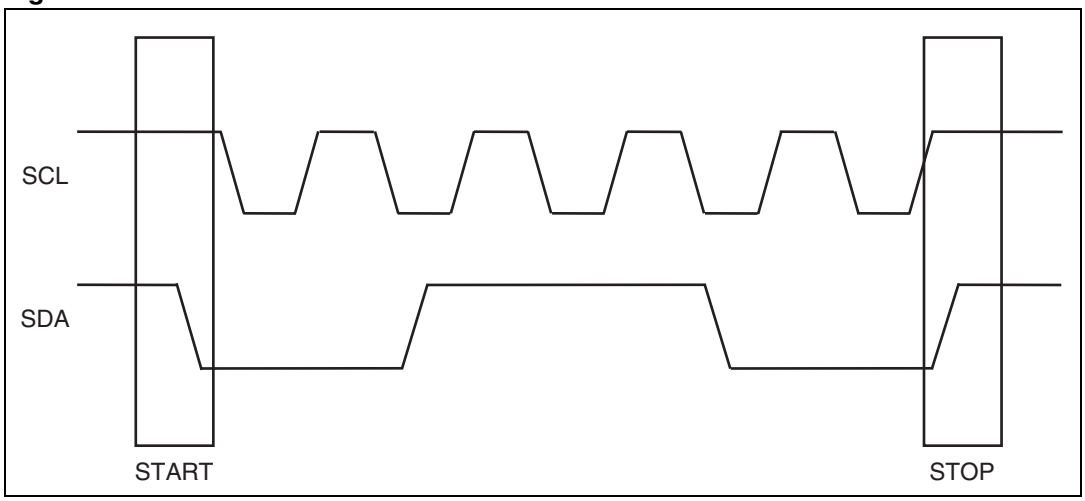
START condition

A START condition is identified by a transition of the data bus SDA from high to low while the clock signal SCL is stable in the high state. A START condition must precede any data transfer command.

STOP condition

A STOP condition is identified by a transition of the data bus SDA from low to high while the clock signal SCL is stable in the high state. A STOP condition terminates communications between the STW81103 and the bus master.

Figure 21. START and STOP conditions

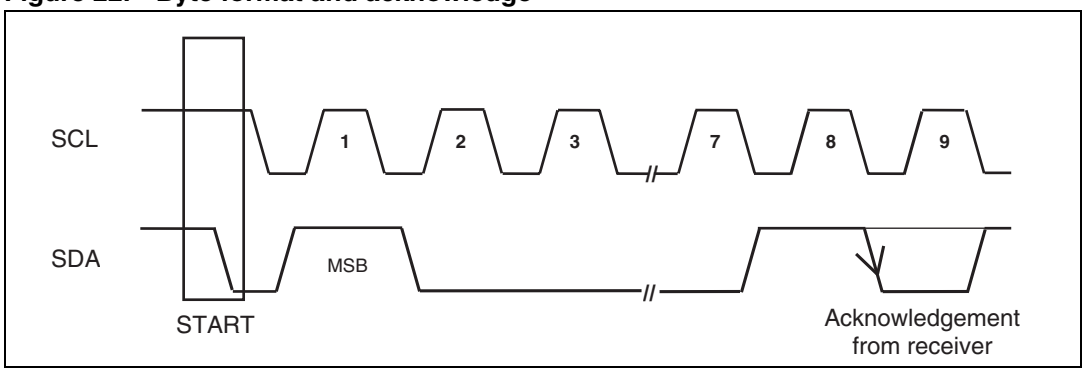


6.1.3 Byte format and acknowledge

Every byte put on the SDA line must be 8 bits long, starting with the most significant bit (MSB), and be followed by an acknowledge bit to indicate a successful data transfer.

The transmitter releases the SDA line after sending 8 bits of data. During the 9th clock pulse, the receiver pulls the SDA line low to acknowledge the receipt of 8 bits of data.

Figure 22. Byte format and acknowledge



6.1.4 Device addressing

The master must first initiate with a START condition to communicate with the STW81103, and then send 8 bits (MSB first) on the SDA line which correspond to the device select address and the read or write mode.

The first seven MSBs are the device address identifier, which corresponds to the I²C bus definition. For the STW81103, the address is set at "1100$A_2A_1A_0$", 3 bits programmable. The 8th bit (LSB) is the read or write (RW) operation bit, which is set to 1 in read mode and to 0 in write mode.

Following a START condition, the STW81103 identifies the device address on the bus and, if matched, acknowledges the identification on the SDA bus during the 9th clock pulse.

6.1.5 Single-byte write mode

Following a START condition, the master sends a device select code with the RW bit set to 0. The STW81103 sends an acknowledge and waits for the 1-byte internal sub-address that provides access to the internal registers.

After receiving the sub-address internal byte, the STW81103 again responds with an acknowledge. A single-byte write to sub-address 00H changes the FUNCTIONAL_MODE register, a single-byte write with sub-address 04H changes the CONTROL register, and so on.

Table 11. Single-byte write mode

S	$1100A_2A_1A_0$	0	ack	sub-address byte	ack	DATA IN	ack	P

6.1.6 Multi-byte write mode

The multi-byte write mode can start from any internal address. The master sends the data bytes, and each one is acknowledged. The master terminates the transfer by generating a STOP condition.

The sub-address decides the starting byte. For example, a multi-byte with sub-address 01H and 2 DATA_IN bytes changes the B_COUNTER and A_COUNTER registers (01H,02H), and a multi-byte with sub-address 00H and 6 DATA_IN bytes changes all the STW81103 registers.

Table 12. Multi-byte write mode

S	$1100A_2A_1A_0$	0	ack	sub-address byte	ack	DATA IN	ack	…….	DATA IN	ack	P

6.1.7 Current byte address read mode

In the current byte address read mode, following a START condition, the master sends the device address with the RW bit set to 1. Note that no sub-address is needed since there is only one read register. The STW81103 acknowledges this and outputs the data byte. The master does not acknowledge the received byte, and terminates the transfer with a STOP condition.

Table 13. Current byte address read mode

S	$1100A_2A_1A_0$	1	ack	DATA OUT	No ack	P

6.2 Timing specification

Figure 23. Data and clock

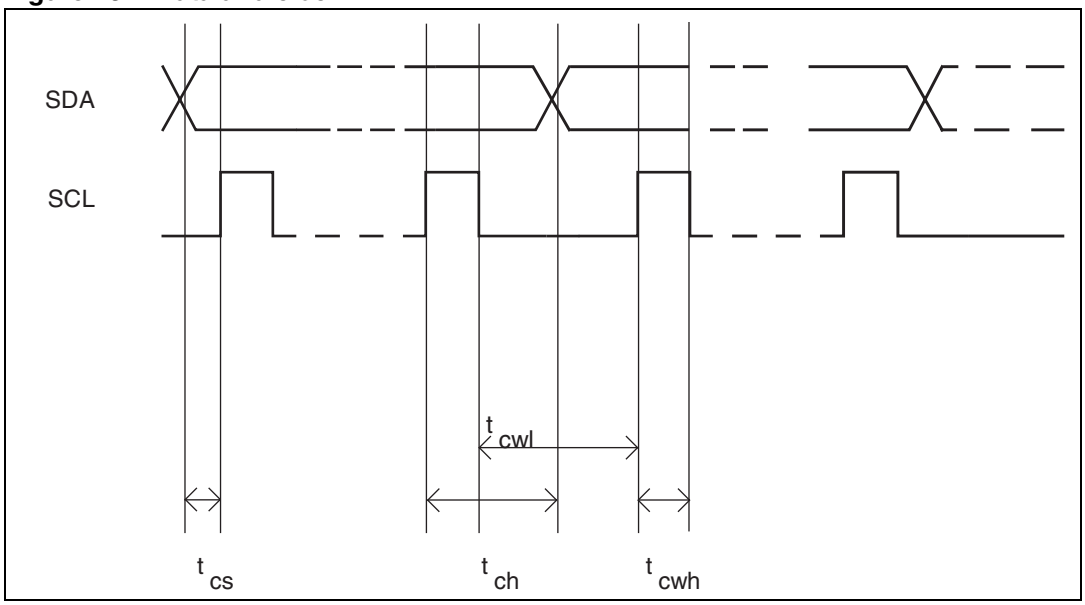


Table 14. Data and clock timing specifications

Symbol	Parameter	Minimum time	Units
t_{cs}	Data to clock setup time	2	ns
t_{ch}	Data to clock hold time	2	ns
t_{cwh}	Clock pulse width high	10	ns
t_{cwl}	Clock pulse width low	5	ns

Figure 24. Start and stop

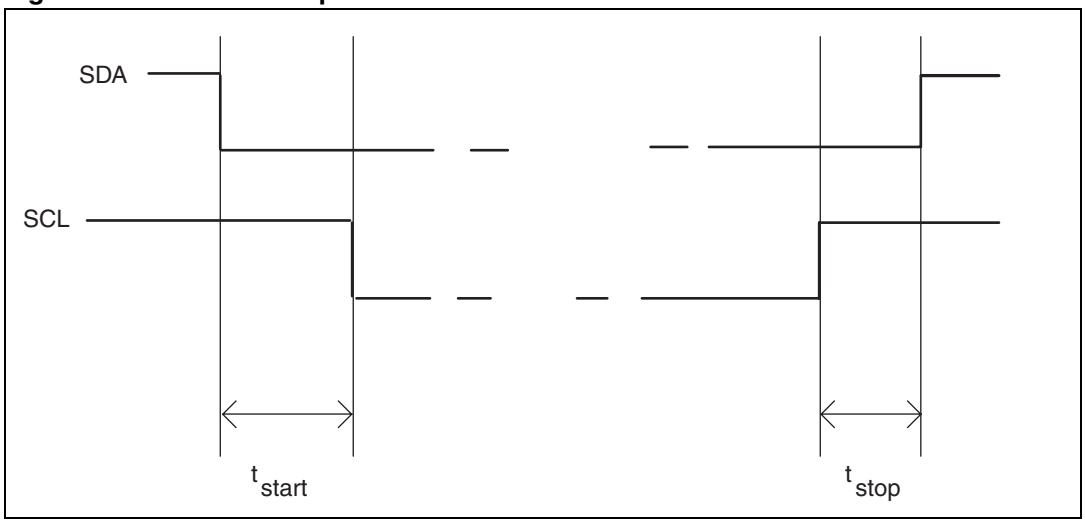


Table 15. Start and stop timing specifications

Symbol	Parameter	Minimum time	Units
t_{start}	Clock to data start time	2	ns
t_{stop}	Data to clock down stop time	2	ns

Figure 25. Ack

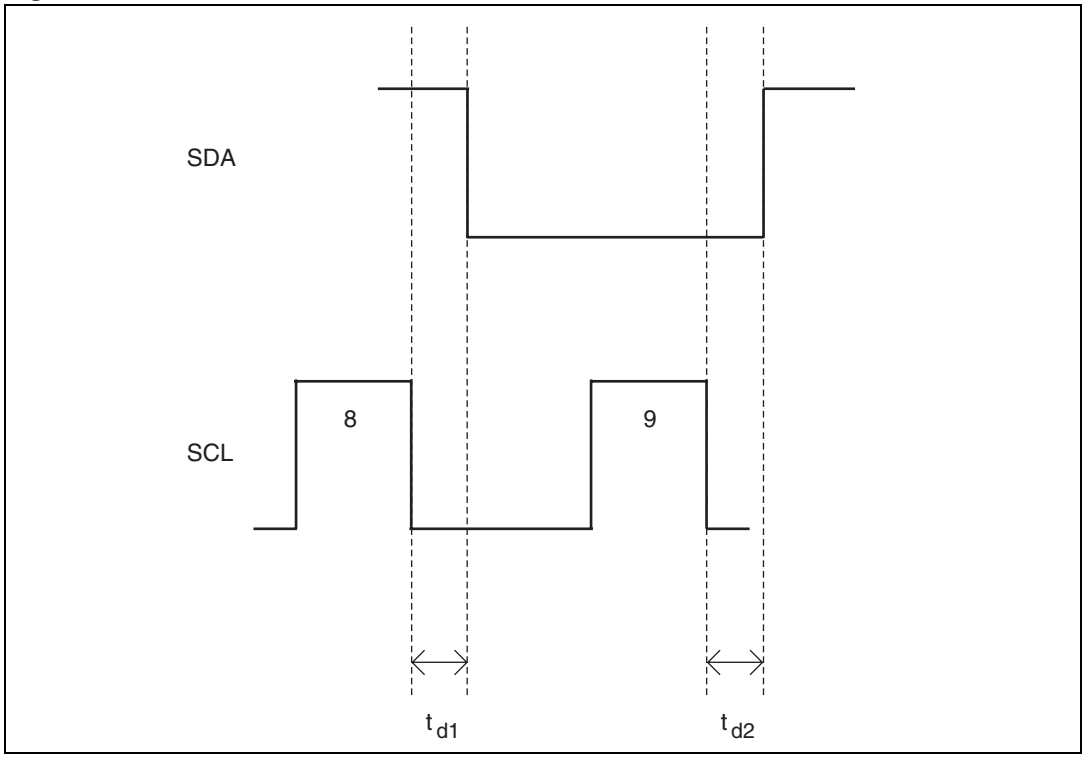


Table 16. Ack timing specifications

Symbol	Parameter	Minimum time	Units
t_{d1}	Ack begin delay	2	ns
t_{d2}	Ack end delay	2	ns

6.3 I²C registers

The STW81103 has 6 write-only registers and 1 read-only register.

6.3.1 Write-only registers

Table 17 gives a short description of the write-only registers.

Table 17. Write-only registers

HEX code	DEC code	Description
0x00	0	FUNCTIONAL_MODE
0x01	1	B_COUNTER
0x02	2	A_COUNTER
0x03	3	REF_DIVIDER
0x04	4	CONTROL
0x05	5	CALIBRATION

FUNCTIONAL_MODE

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
OUTBUF_CTRL_EN	CAL_AUTOSTART_EN	PD4	PD3	PD2	PD1	PD0	B11

OUTBUF_CTRL_EN: Output buffer control mode enable (0 = Off; 1 = ON)

CAL_AUTOSTART_EN: VCO calibration auto-restart enable (0 = Off; 1 = ON)

The bits PD[4:0] allow to select different functional modes for the STW81103 synthesizer according to the *Table 18*.

Table 18. Functional modes

Decimal value PD[6:0]	Description
0	Power down mode
1	Enable VCO A, output frequency divided by 2
2	Enable VCO B, output frequency divided by 2
3	Enable external VCO, output frequency divided by 2
4	Enable VCO A, output frequency divided by 4
5	Enable VCO B, output frequency divided by 4
6	Enable external VCO, output frequency divided by 4
7	Enable VCO A, direct output
8	Enable VCO B, direct output
9	Enable external VCO, direct output

B_COUNTER

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
B10	B9	B8	B7	B6	B5	B4	B3

B[10:3]. B counter value (bit B11 in the previous register, bits B[2:0] in the next register)

A_COUNTER

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
B2	B1	B0	A4	A3	A2	A1	A0

Bits B[2:0] for B_COUNTER, A_COUNTER values.

REF_DIVIDER

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
R9	R8	R7	R6	R5	R4	R3	R2

Reference clock divider ratio R[9:1] (bits R1, R0 in the next register).

CONTROL

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
R1	R0	PLL_A1	PLL_A0	CPSEL2	CPSEL1	CPSEL0	PSC_SEL

The CONTROL register is used to set the charge pump current, the VCO output voltage amplitude and the prescaler modulus:

PLL_A[1:0]: VCO amplitude

CPSEL[2:0]: charge pump output current

PSC_SEL: prescaler modulus select ('0' for P=16, '1' for P=19)

The LO output frequency is programmed by setting the proper values for A, B and R according to the following formula:

$$F_{OUT} = D_R \times (B \times P + A) \times \frac{F_{REF-CLK}}{R}$$

where D_R equals

$$\begin{cases} 1 & \text{for direct output} \\ 0.5 & \text{for output divided by 2} \\ 0.25 & \text{for output divided by 4} \end{cases}$$

and P is the selected prescaler modulus.

CALIBRATION

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
INITCAL	SERCAL	SELEXTCAL	CAL4	CAL3	CAL2	CAL1	CAL0

This register controls the VCO calibrator using the following values:

INITCAL: for test purposes only, must be set to 0

SERCAL: at 1 starts the VCO auto-calibration (automatically reset to 0 at the end of calibration)

SELEXTCAL: for test purposes only; must be set to 0

CAL[4:0]: for test purposes only; must be set to 0

6.3.2 Read-only register

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
DEV_ID1	DEV_ID0	LOCK_DET	INTCAL4	INTCAL3	INTCAL2	INTCAL1	INTCAL0

This register is automatically addressed in the ‘current byte address read mode’, using the following values:

DEV_ID[1:0]: device identifier bits; returns ‘10’

LOCK_DET: 1 when PLL is locked

INTCAL[4:0]: internal value of the VCO control word

6.3.3 Default configuration

At power on, all the bits are set to '0'. Consequently the part starts in power down mode.

6.4 VCO calibration procedure

Calibration of the VCO center frequency is activated when the SERCAL bit (CALIBRATION register bit[6]) is set to 1.

To program the device properly while ensuring VCO calibration, perform the following steps before every channel change:

1. Program all the registers using a multi-byte write sequence with the desired settings (functional mode, B and A counters, R counter, VCO amplitude, charge pump, prescaler modulus), and all the bits of the CALIBRATION register (05H) set to 0.
2. Program the CALIBRATION register using a single-byte write sequence (subaddress 05H) with the SERCAL bit set to 1.

The maximum allowed PFD frequency (F_{PFD}) during calibration is 1 MHz; if you want a F_{PFD} higher than 1 MHz, perform the following additional steps:

- Perform all the steps of the calibration procedure, making sure to program the desired VCO frequency with proper settings for the R, B and A counters so that F_{PFD} is ≤1 MHz.
- Program the device with the desired VCO and PFD frequency settings according to step 1) above.

6.4.1 VCO calibration auto-restart feature

The VCO calibration auto-restart feature can be enabled in two steps:

1. set the desired frequency ensuring VCO calibration as described above (section 6.4)
2. program the FUNCTIONAL_MODE register (sub-address 00H) using a single-byte write sequence with the CAL_AUTOSTART_EN bit set to '1' while keeping unchanged the others.

7 SPI digital interface

7.1 General features

The SPI digital interface is selected by hardware connection of pin #21 (DBUS_SEL) to 3.3 V.

The STW81103 IC is programmed by means of a high-speed serial-to-parallel interface with write option only. The 3-wire bus can be clocked at a frequency as high as 100 MHz to allow fast programming of the registers containing the data for RF IC configuration.

The chip is programmed through serial words with a full length of 26 bits. The first 2 MSBs represent the address of the registers, and the 24 LSBs represent the value of the registers.

Each data bit is stored in the internal shift register on the **rising edge** of the CLOCK signal.

The outputs of the selected register are sent to the device on the **rising edge** of the LOAD signal.

Figure 26. SPI input and output bit order

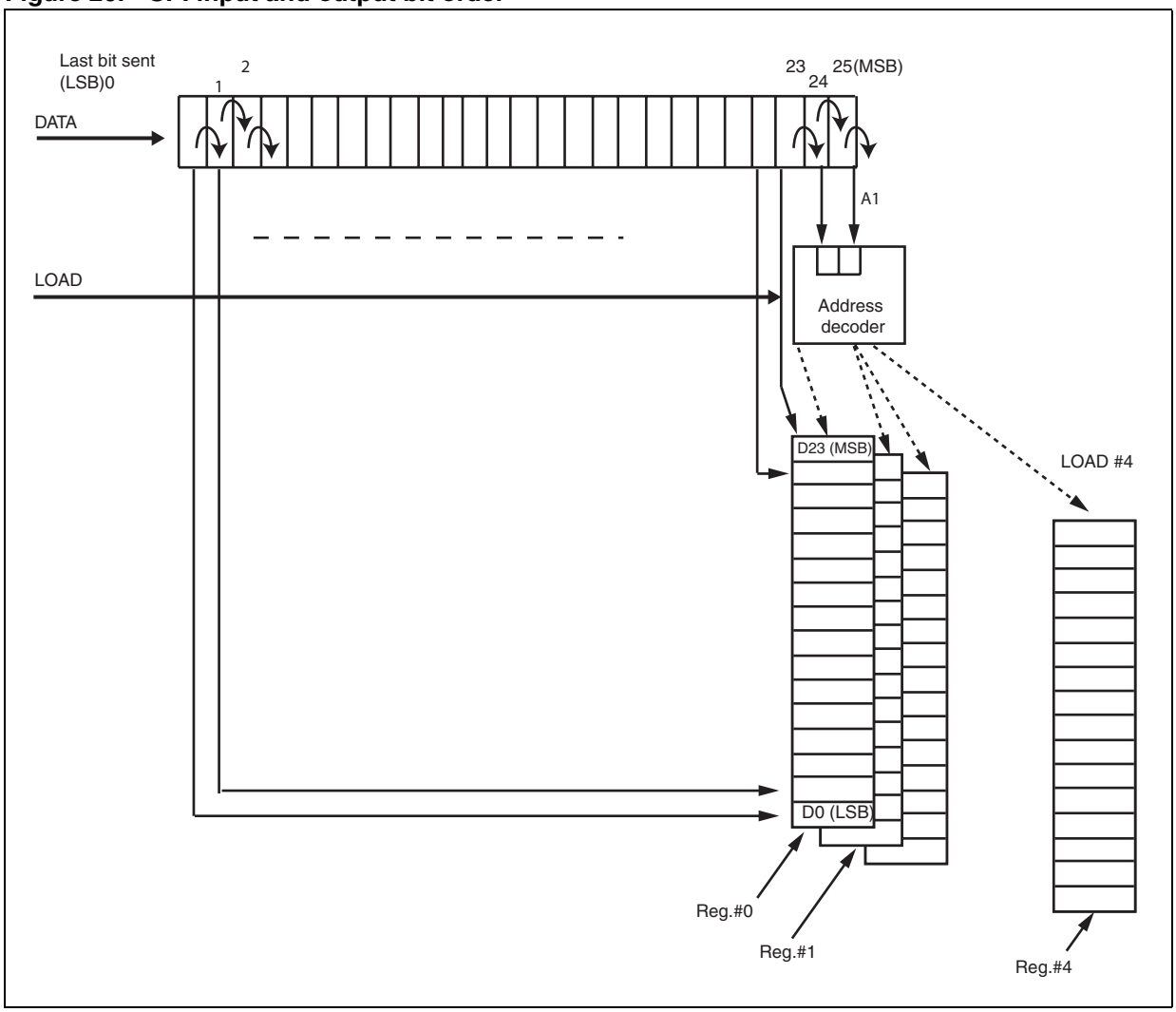


Table 19. SPI data structure (MSB is sent first)

MSB LSB

Address		Data for register (24 bits)																						
A1	A0	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 20. Address decoder and outputs

Address		Outputs			
A1	**A0**	**DATABITS D23-D0**	**No**	**Name**	**Function**
0	0	24	0	ST1	Reference divider, VCO amplitude, VCO calibration, charge pump current, prescaler modulus
0	1	24	1	ST2	Functional modes, VCO dividers
1	0	24	2	ST3	Reserved
1	1	24	3	ST4	Reserved

7.2 Timing specification

Figure 27. SPI timing specification

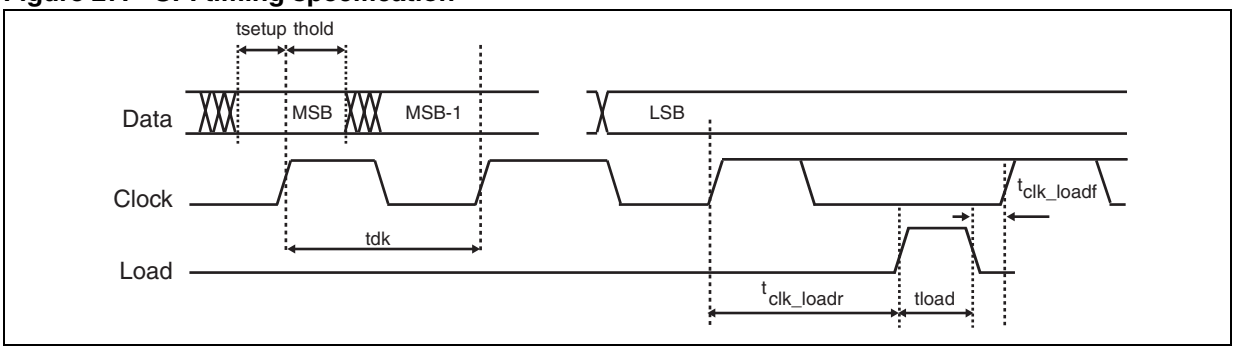


Table 21. SPI timing specification

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{setup}	DATA to CLOCK setup time	0.8			ns
t_{hold}	DATA to CLOCK hold time	0.2			ns
t_{clk}	CLOCK cycle period	10			ns
t_{load}	LOAD pulse width	3			ns
t_{clk_loadr}	CLOCK to LOAD rising edge	2			ns
t_{clk_loadf}	CLOCK to LOAD falling edge	0.5			ns

7.3 Bit tables

Table 22. Bits at 00h and ST1

Serial interface address = 00h		Register name = ST1
Bit	**Name**	**Description**
[23]	R9	Reference clock divider ratio
[22]	R8	
[21]	R7	
[20]	R6	
[19]	R5	
[18]	R4	
[17]	R3	
[16]	R2	
[15]	R1	
[14]	R0	
[13]	PLL_A1	VCO amplitude control
[12]	PLL_A0	
[11]	CPSEL2	Charge pump output current control
[10]	CPSEL1	
[9]	CPSEL0	
[8]	PSC_SEL	Prescaler modulus select (0 for P=16, 1 for P=19)
[7]	INITCAL	For test purposes only; must be set to 0
[6]	SERCAL	Enable VCO calibration (see *Section 7.4*)
[5]	SELEXTCAL	For test purposes only; must be set to ‘0’
[4]	CAL4	For test purposes only; must be set to ‘0’
[3]	CAL3	
[2]	CAL2	
[1]	CAL1	
[0]	CAL0	

Table 23. Bits at 01h and ST2

Serial interface address = 01h		Register name = ST2
Bit	**Name**	**Description**
[23]	OUTBUF_CTRL_EN	Output buffer control mode enable (0 = Off, 1 = On)
[22]	CAL_AUTOSTART_EN	VCO calibration auto restart enable (0 = Off, 1 = On)
[21]	PD4	Device functional modes: 0. Power down 1. Enable VCO A, output frequency divided by 2 2. Enable VCO B, output frequency divided by 2 3. Enable external VCO, output frequency divided by 2 4. Enable VCO A, output frequency divided by 4 5. Enable VCO B, output frequency divided by 4 6. Enable external VCO, output frequency divided by 4 7. Enable VCO A, direct output 8. Enable VCO B, direct output 9. Enable external VCO, direct output
[20]	PD3	
[19]	PD2	
[18]	PD1	
[17]	PD0	
[16]	B11	B_COUNTER bits
[15]	B10	
[14]	B9	
[13]	B8	
[12]	B7	
[11]	B6	
[10]	B5	
[9]	B4	
[8]	B3	
[7]	B2	
[6]	B1	
[5]	B0	
[4]	A4	A_COUNTER bits
[3]	A3	
[2]	A2	
[1]	A1	
[0]	A0	

The LO output frequency is programmed by setting the proper value for A, B and R according to the following formula:

$$F_{OUT} = D_R \times (B \times P + A) \times \frac{F_{REF-CLK}}{R}$$

where D_R equals $\begin{cases} 1 & \text{for direct output} \\ 0.5 & \text{for output divided by 2} \\ 0.25 & \text{for output divided by 4} \end{cases}$

and P is the selected prescaler modulus.

7.3.1 Default configuration

At power on, all the bits are set to '0'. Consequently the part starts in power down mode.

7.4 VCO calibration procedure

Calibration of the VCO center frequency is activated when the SERCAL bit (ST1 register bit[6]) is set to 1.

To program the device properly while ensuring VCO calibration, perform the following steps before every channel change:

1. Program the ST2 register with the desired settings (functional mode, B and A counters).
2. Program the ST1 register with the desired settings (R counter, VCO amplitude, charge pump, prescaler modulus) and with the SERCAL bit set to 1.

The maximum allowed PFD frequency (F_{PFD}) during calibration is 1 MHz; if you want a F_{PFD} higher than 1 MHz, perform the following additional steps:

- Perform all the steps (step 1 and 2 above) of the calibration procedure, making sure to program the desired VCO frequency with proper settings of the R, B and A counters so that F_{PFD} is ≤1 MHz.
- Program the device with the desired VCO and PFD frequency settings as per steps 1 and 2 above with SERCAL bit set to 0.

7.4.1 VCO calibration auto-restart feature

The VCO calibration auto-restart feature can be enabled in two steps:

1. Set the desired frequency ensuring VCO calibration as described above (*Section 7.4*)
2. Program the ST2 register with the CAL_AUTOSTART_EN bit set to '1' while keeping unchanged the others.

8 Application information

The STW81103 features three different alternately selectable bands: direct output (2.5 to 3.05 GHz and 4.35 to 5.0 GHz), divided by 2 (1.25 to 1.525 GHz and 2.175 to 2.5 GHz) and divided by 4 (625 to 762.5 MHz and 1087.5 to 1250 MHz). To achieve a suitable power level, a good matching network is necessary to adapt the output stage to a 50Ω load. Moreover, since most commercial RF components have single-ended input and output terminations, a differential to single-ended conversion may be required.

The different matching configurations shown below for each of the three bands are suggested as a guideline when designing your own application board.

Inside the evaluation kit is the ADS design for each matching configuration suggested in this chapter. The name of the corresponding ADS design is given in each figure.

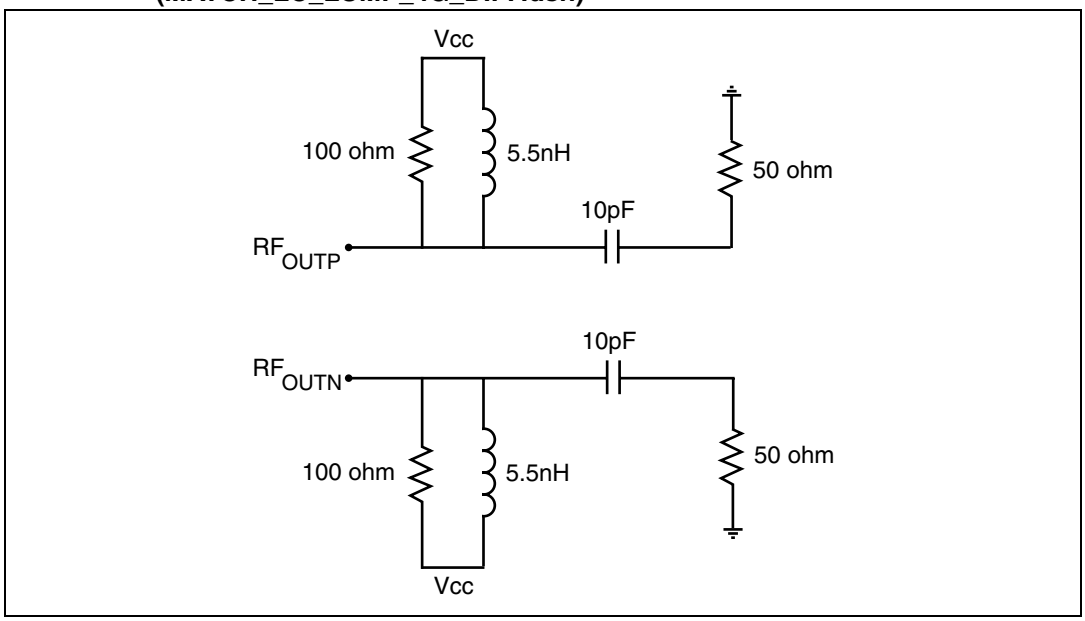
The ADS designs provide only a first indication of the output stage matching, and should be reworked according to the choices of layout, board substrate, components and so on.

The ADS designs of the evaluation boards are provided with a complete electromagnetic modelling (board, components, and so on).

8.1 Direct output

If you do not need a differential to single conversion, you can match the output buffer of the STW81103 in the simple way shown in *Figure 28*. This illustrates the differential to single-ended output network in the 2.5 - 5.0 GHz range (MATCH_LC_LUMP_4G_DIFF.dsn).

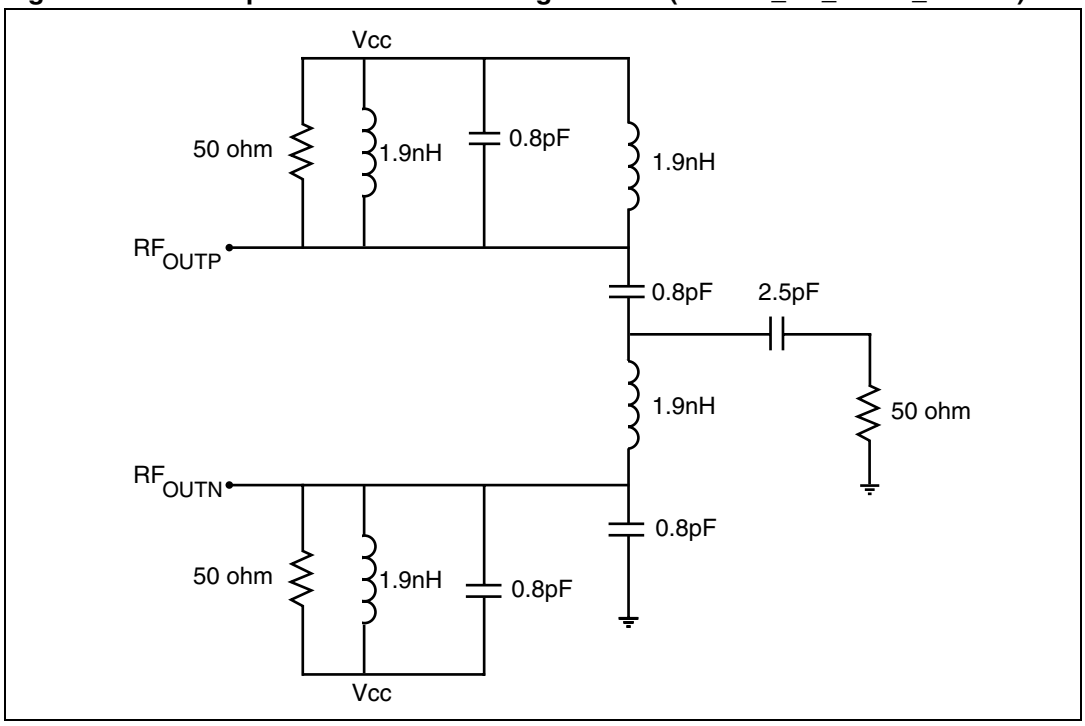
Figure 28. Differential/single-ended output network (MATCH_LC_LUMP_4G_DIFF.dsn)



Since most discrete components for microwave applications are single-ended, you can easily use one of the two outputs and terminate the other one to 50Ω with a 3 dB power loss.

Alternatively, you can combine the two outputs in other ways. A first topology for the direct output (2.5 to 5.0 GHz) is suggested in *Figure 29*. It basically consists of a simple LC balun and a matching network to adapt the output to a 50Ω load. The two LC networks shift output signal phase of -90° and +90°, thus combining the two outputs. This topology, designed for a center frequency of 4 GHz, is intrinsically narrow-band since the LC balun is tuned at a single frequency. If the application requires a different sub-band, the LC combiner can be easily tuned to the frequency of interest.

Figure 29. LC lumped balun and matching network (MATCH_LC_LUMP_4G.dsn)

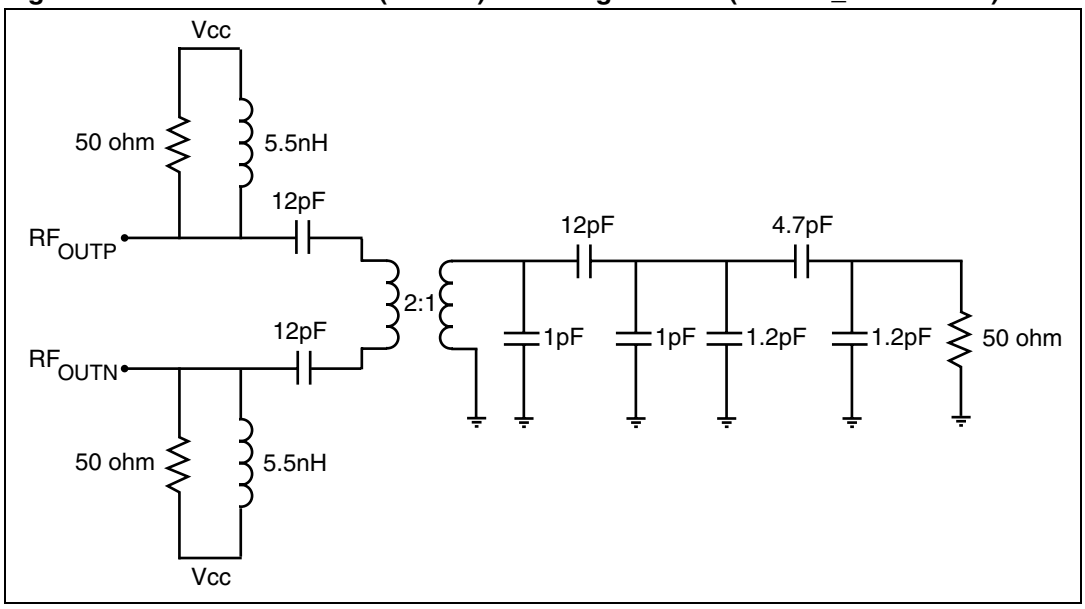


The 1.9 nH shunt inductor works as a DC feed for one of the open collector terminals as well as a matching element along with the other components. The 1.9 nH series inductors are used to resonate the parasitic capacitance of the chip.

For optimum output matching, it is recommended to use 0402 Murata or AVX capacitors and 0403 or 0604 HQ Coilcraft inductors. It is also advisable to use short interconnection paths to minimize losses and undesired impedance shift.

An alternative topology that permits a more broadband matching as well as balanced to unbalanced conversion, is shown in *Figure 30*.

Figure 30. Evaluation board (EVB4G) matching network (MATCH_EVB4G.dsn)

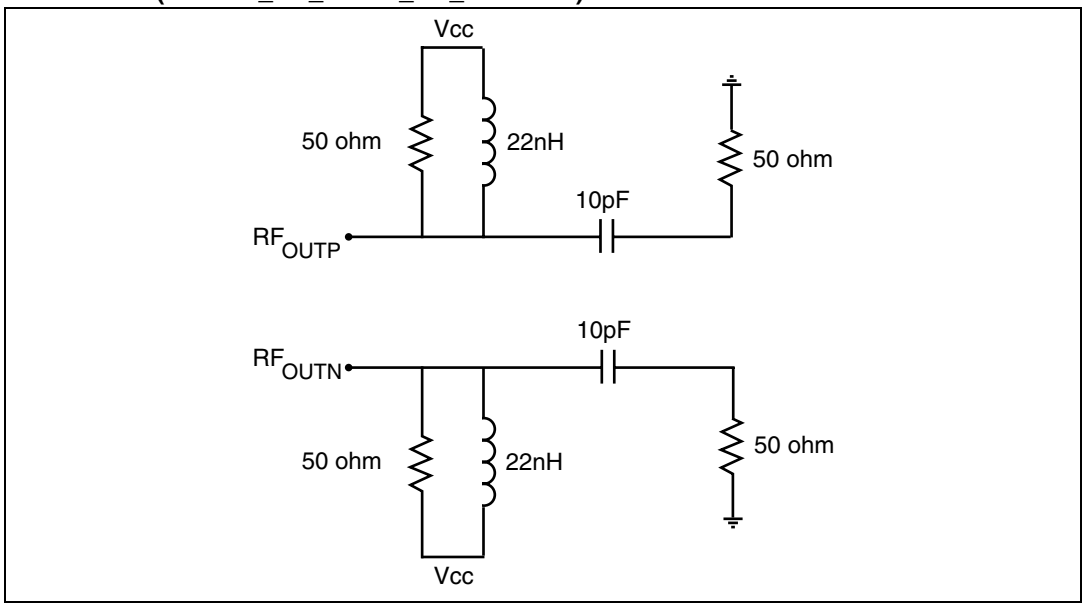


For differential to single conversion, the 50 to 100Ω Johanson balun is recommended (3700BL15B100).

8.2 Divided by 2 output

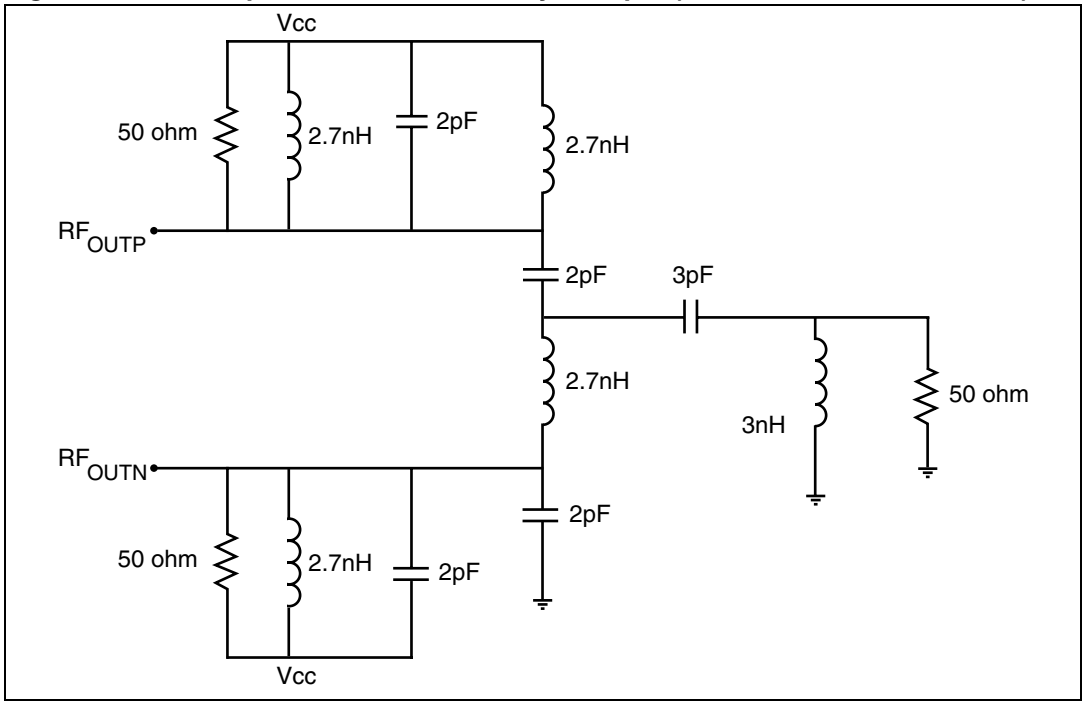
If your application does not require a balanced to unbalanced conversion, the output matching reduces to the simple circuit shown below (*Figure 31*), which illustrates a differential to single-ended output network in the 1.25 - 2.5 GHz range (MATCH_LC_LUMP_2G_DIFF.dsn). You can easily use this solution to provide one single-ended output that terminates the other output at 50Ω with a 3 dB power loss.

Figure 31. Differential/single-ended output network (MATCH_LC_LUMP_2G_DIFF.dsn)



A first solution to combine the differential outputs is the lumped LC type balun tuned in the 2 GHz band (*Figure 32*).

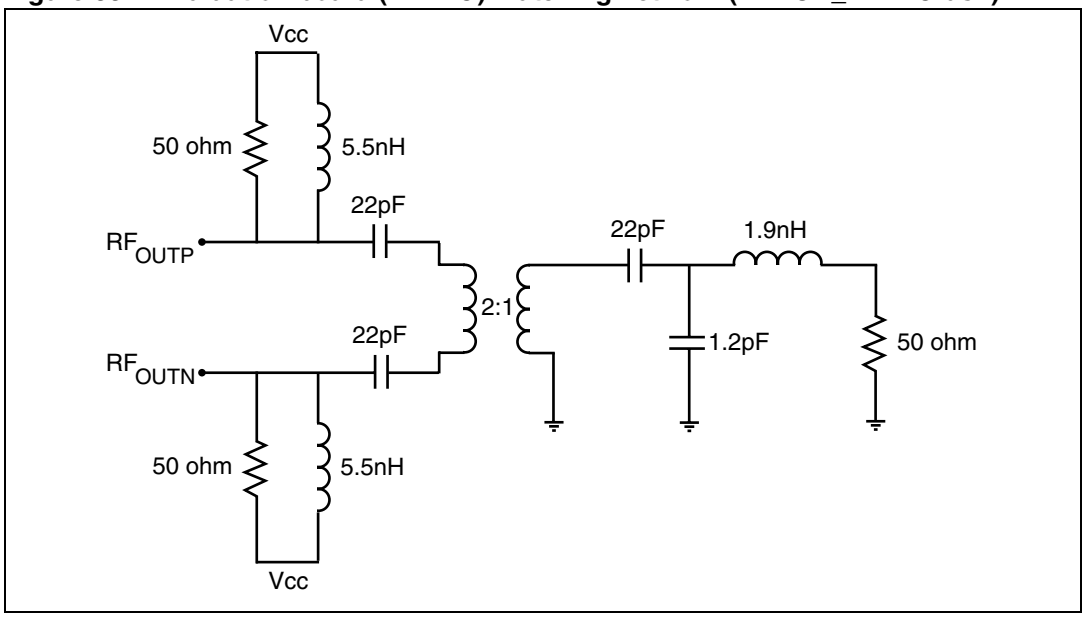
Figure 32. LC lumped balun for divided by 2 output (MATCH_LC_LUMP_2G.dsn)



The same recommendation for the SMD components also applies to the divided by 2 output.

Another topology suited to combining the two outputs for the divided by 2 frequencies is represented in *Figure 33*.

Figure 33. Evaluation board (EVB2G) matching network (MATCH_EVB2G.dsn)



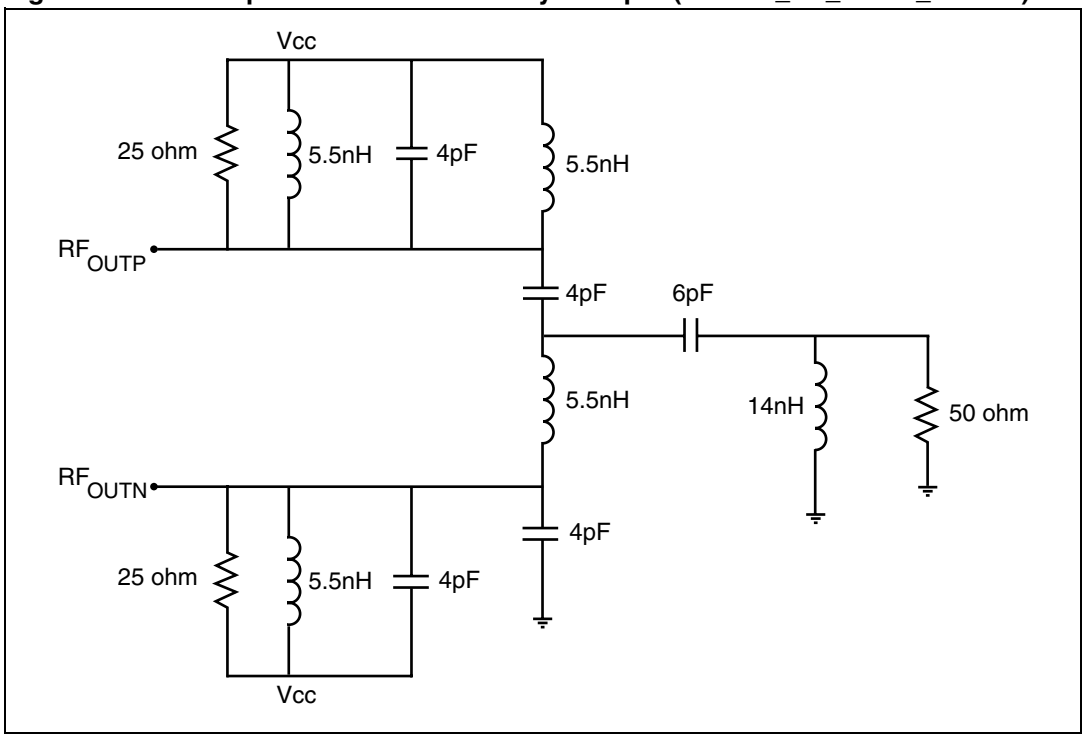
For differential to single conversion, the 50 to 100Ω Johanson balun (1600BL15B100) is recommended.

8.3 Divided by 4 output

The topology, components, values and considerations of *Figure 31* also apply to the divided by 4 output (MATCH_LC_LUMP_1G_DIFF.dsn).

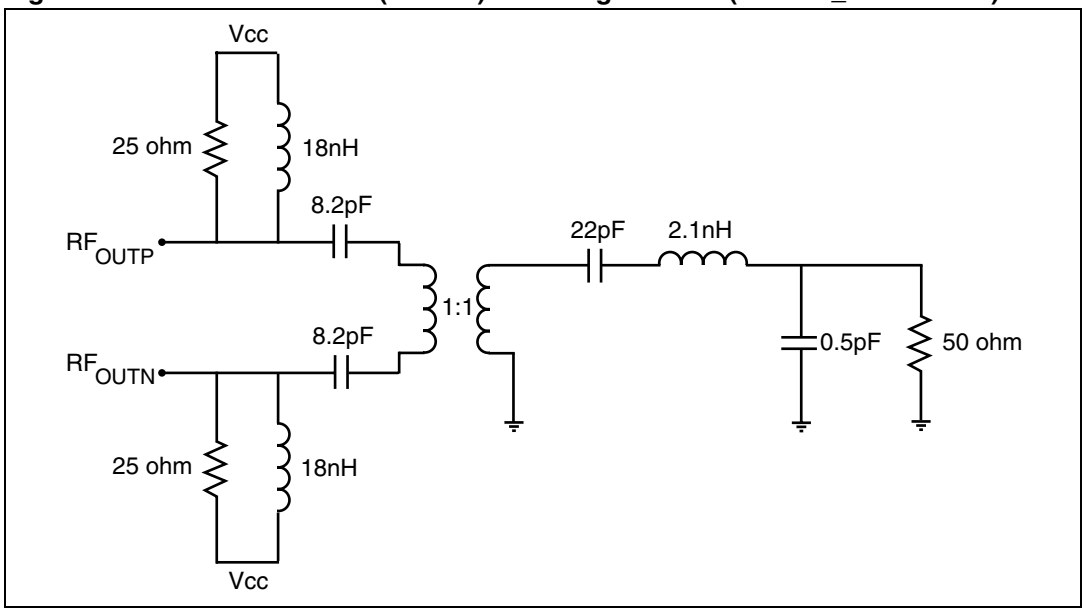
As for the previous sections, a solution to combine the differential outputs is the lumped LC type balun tuned in the 1 GHz band (*Figure 34*).

Figure 34. LC lumped balun for divided by 4 output (MATCH_LC_LUMP_1G.dsn)



If you prefer to use an RF balun, you can adapt the topology depicted in *Figure 33*, and change the balun and the matching components (*Figure 35*). The suggested balun for the 0.625 - 1.25 GHz frequency range is the 1:1 Johanson 900BL15C050.

Figure 35. Evaluation board (EVB1G) matching network (MATCH_EVB1G.dsn)



8.4 Evaluation kit

An evaluation kit can be delivered upon request, including the following:

- Evaluation board
- GUI (graphical user interface) to program the device
- Measured S parameters of the RF output
- ADS2005 schematics providing guidelines for application board design
- STWPLLSim software for PLL loop filter design and noise simulation
- Application programming interface (API)

Three different evaluation kits are available, each optimized for one of the following frequency ranges:

- 1 GHz
- 2 GHz
- 4 GHz

When ordering, please specify one of the following order codes:

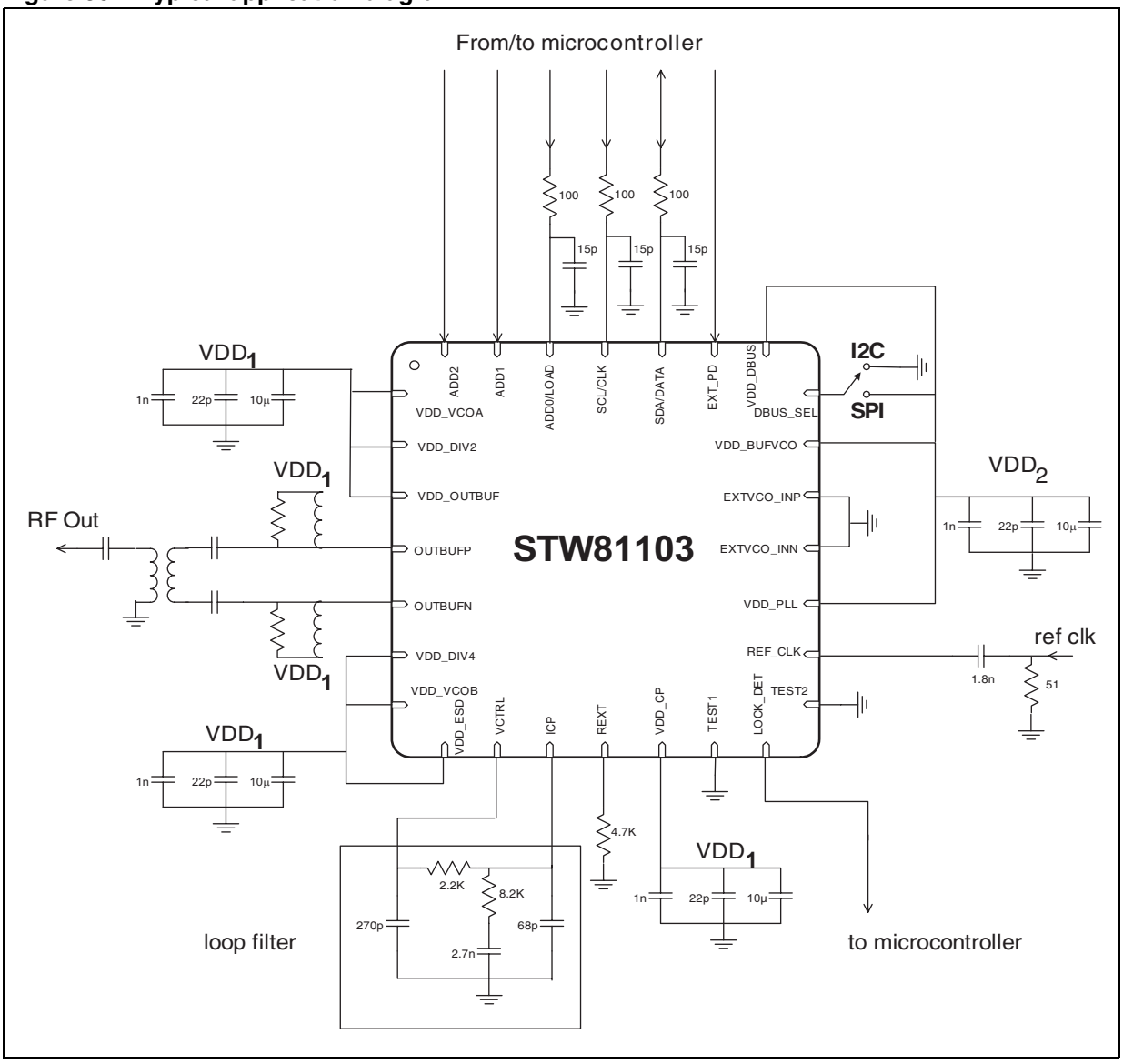
Table 24. Order code of the evaluation kit

Part number	Description
STW81103-EVB1G	1 GHz frequency range - divider by 4 output optimized
STW81103-EVB2G	2 GHz frequency range - divider by 2 output optimized
STW81103-EVB4G	4 GHz frequency range - direct output optimized

The three evaluation kits differ only for the output stage network and can be adapted from one frequency band variant to a different one replacing properly the matching components and the balun.

9 Application diagram

Figure 36. Typical application diagram



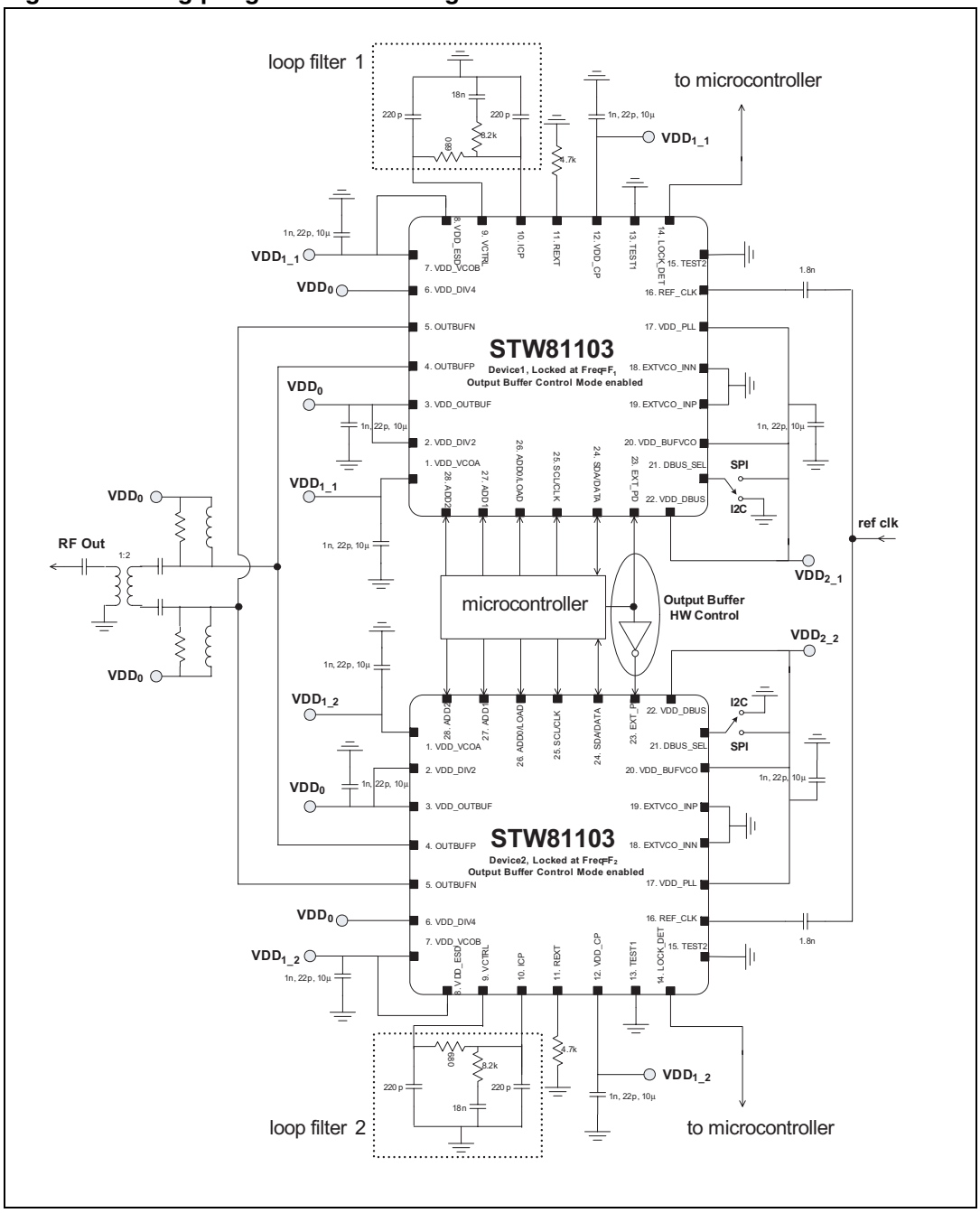
Note: 1 See Section 8: Application information for further information on output matching topology.

2 EXT_PD, ADD2, ADD1 (and ADD0 when the I^2C bus is selected) can be hard wired directly on the board.

3 Loop filter values are for F_{STEP} = 200 kHz.

4 For best performance VDD_1 must be a low noise supply (20 μV_{RMS} in 10 Hz-100 kHz BW).

Figure 37. Ping-pong architecture diagram



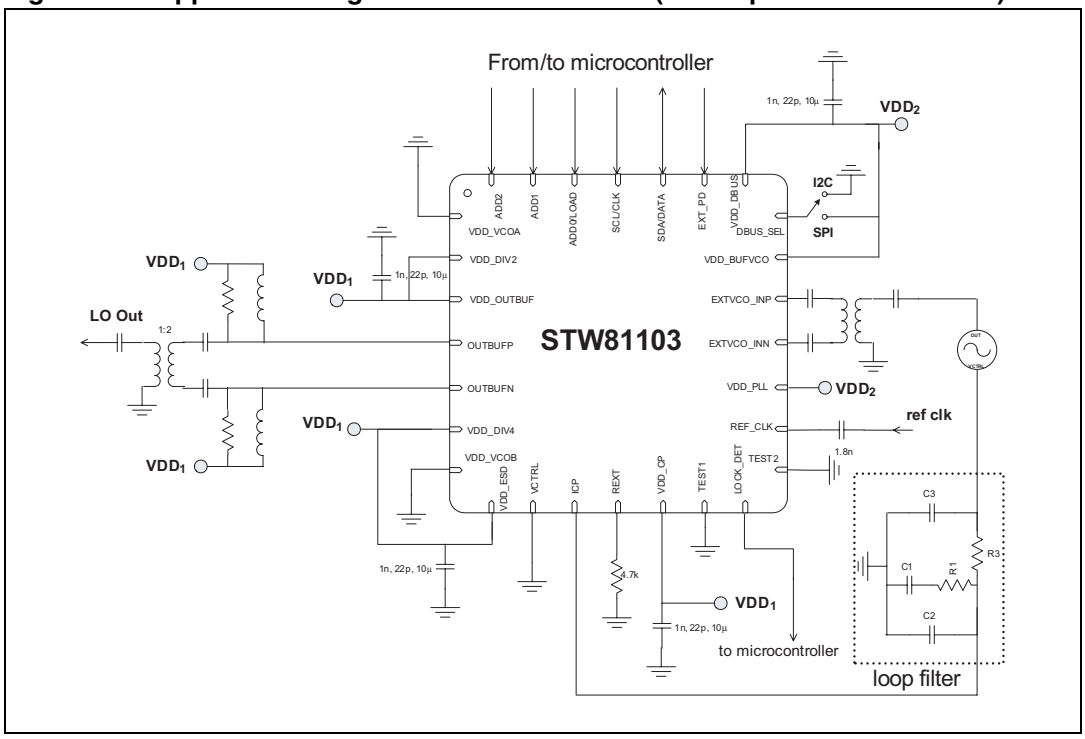
Note: 1 See Section 8: Application information for further information on output matching topology.

2 EXT_PD, ADD2, ADD1 (and ADD0 when the I^2C bus is selected) can be hard wired directly on the board.

3 Loop filter values are for F_{STEP} = 200 kHz.

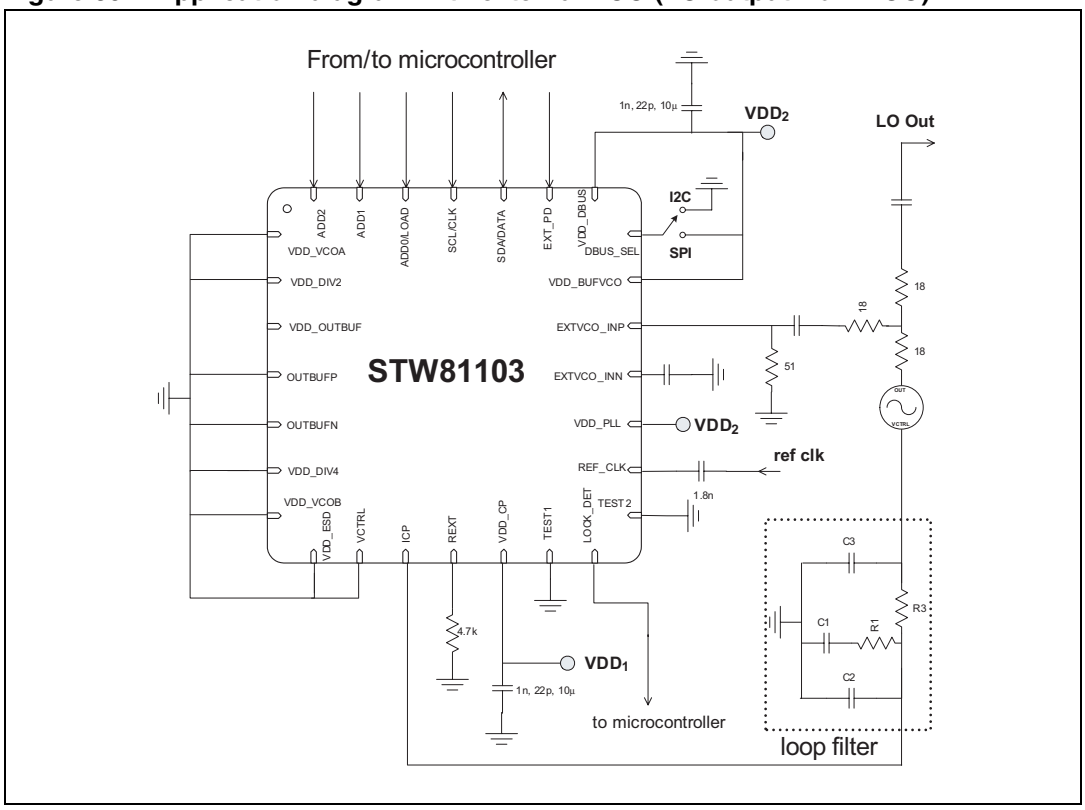
4 For best performance VDD_{1_1} and VDD_{1_2} must be low noise supplies (20 μV_{RMS} in 10 Hz-100 KHz BW).

Figure 38. Application diagram with external VCO (LO output from STW81103)



Note: See Section 8: Application information for further information on output matching topology.

Figure 39. Application diagram with external VCO (LO output from VCO)

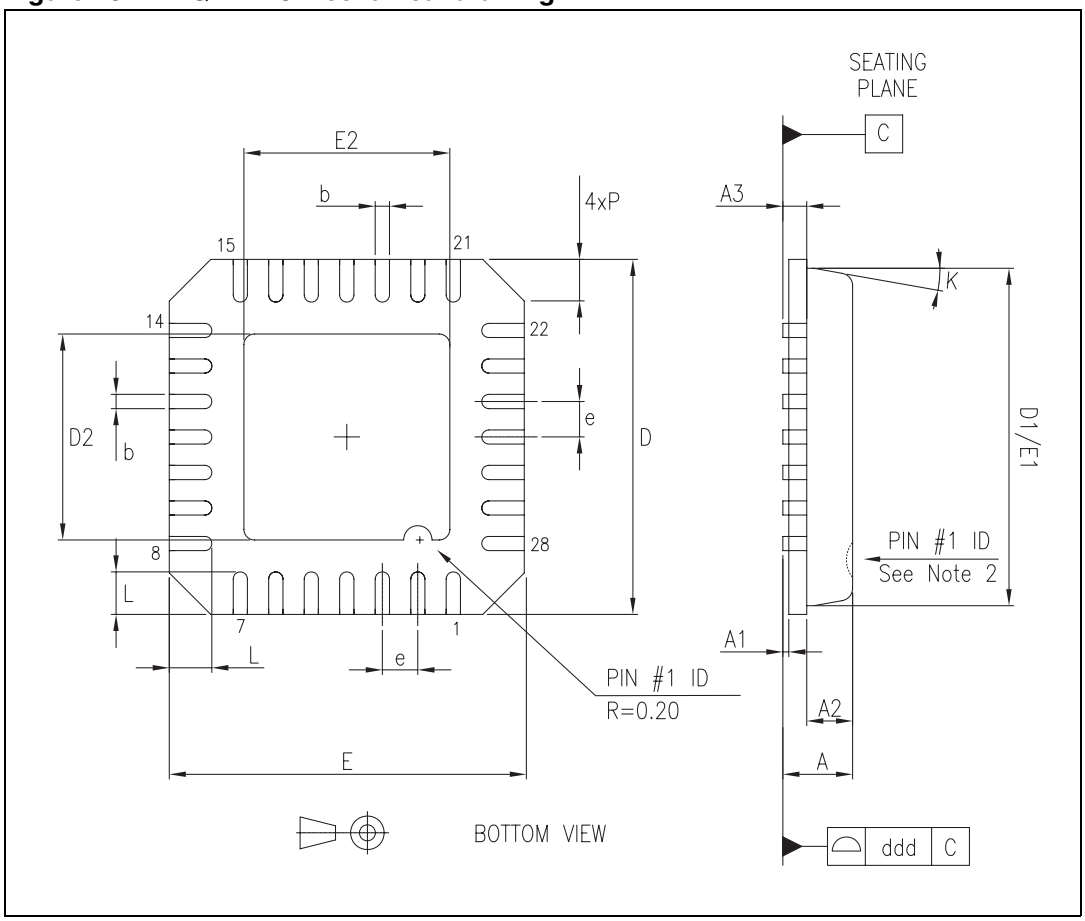


10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages, which have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

ECOPACK specifications are available at: http://www.st.com.

Figure 40. VFQFPN28 mechanical drawing



Note: 1 VFQFPN stands for Thermally Enhanced Very thin Fine pitch Quad Flat Package No lead. (Very thin: A=1.00 Max)

2 Details of the terminal 1 identifier are optional, but if given, must be located on the top surface of the package by using either a mold or marked features.

Table 25. Package dimensions

Ref.	Min.	Typ.	Max.	Unit
A	0.800	0.900	1.000	mm
A1		0.020	0.050	mm
A2		0.650	1.000	mm
A3		0.200		mm
b	0.180	0.250	0.300	mm
D	4.850	5.000	5.150	mm
D1		4.750		mm
D2	2.950	3.100	3.250	mm
E	4.850	5.000	5.150	mm
E1		4.750		mm
E2	2.950	3.100	3.250	mm
e		0.500		mm
L	0.350	0.550	0.750	mm
P			0.600	mm
K			14	degrees
ddd			0.080	mm

11 Ordering information

Table 26. Order codes

Part number	Temp range, °C	Package	Packing
STW81103AT	-40 to 85	VFQFPN28	Tray
STW81103ATR	-40 to 85	VFQFPN28	Tape and reel

12 Revision history

Table 27. Document revision history

Date	Revision	Changes
18-Jul-2007	1	Initial release.
14-Aug-2007	2	Added *Chapter 8: Application information*. Modified *Section 6.4: VCO calibration procedure*, and pin #23 description in *Table 1*.
28-Mar-2008	3	Updated *Table 1: Pin description*. Updated *Table 2: Absolute maximum ratings*, *Table 3: Operating conditions*, *Table 5: Electrical specifications* and *Table 6: Phase noise specification*. Updated *Section 5.8.2: VCO frequency calibration*. Added *VCO calibration auto-restart feature*. Updated *Section 5.8.3: VCO voltage amplitude control*. Added *Section 5.9: Output stage* and *Section 5.10: External VCO buffer*. Updated *FUNCTIONAL_MODE* and *CALIBRATION* registers. Added *Section 6.3.3: Default configuration*. Updated *Section 6.4: VCO calibration procedure* and added *Section 6.4.1: VCO calibration auto-restart feature*. Updated *Table 23: Bits at 01h and ST2*. Added *Section 7.3.1: Default configuration*. Updated *Section 7.4: VCO calibration procedure* and added *Section 7.4.1: VCO calibration auto-restart feature*. Added 'Application program interface API' item in *Section 8.4*. Modified notes after *Figure 36*. Added *Figure 37*, *Figure 38* and *Figure 39*. Modified *Figure 40*.

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