

74LVC38A

Quad 2-input NAND gate; open-drain

Rev. 4 — 4 November 2011

Product data sheet

1. General description

The 74LVC38A provides four 2-input NAND functions. The outputs are open-drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V applications.

2. Features and benefits

- 5 V tolerant inputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Open-drain outputs
- Complies with JEDEC standard:
 - ◆ JESD8-7A (1.65 V to 1.95 V)
 - ◆ JESD8-5A (2.3 V to 2.7 V)
 - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115B exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC38AD	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVC38ADB	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LVC38APW	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVC38ABQ	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85\text{ mm}$	SOT762-1



4. Functional diagram

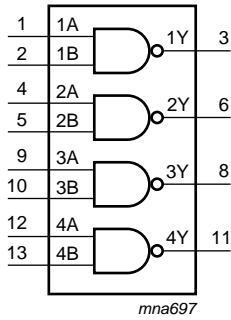


Fig 1. Logic symbol

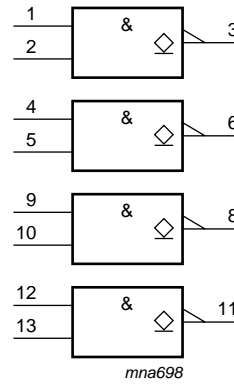


Fig 2. IEC logic symbol

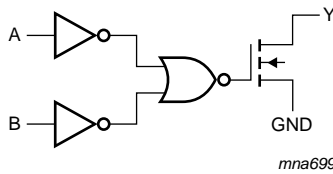


Fig 3. Logic diagram for one gate

5. Pinning information

5.1 Pinning

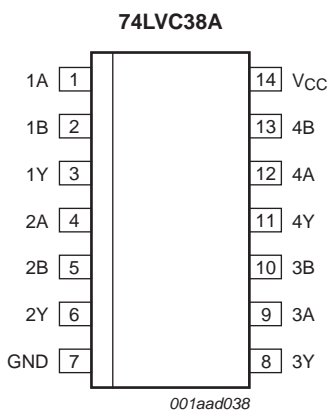
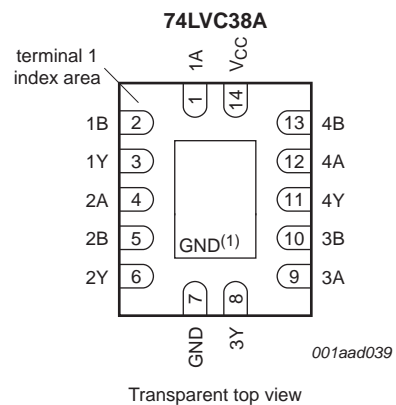


Fig 4. Pin configuration for SO14 and (T)SSOP14



- (1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 5. Pin configuration for DHVQFN14

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A	1, 4, 9, 12	data input
1B, 2B, 3B, 4B	2, 5, 10, 13	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function selection^[1]

Input		Output
nA	nB	nY
L	L	Z
L	H	Z
H	L	Z
H	H	L

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0	-50	-	mA
V _I	input voltage		^[1] -0.5	+6.5	V
I _{OK}	output clamping current	V _O < 0	-50	-	mA
V _O	output voltage	active mode	^[2] -0.5	+6.5	V
		high-impedance mode	^[2] -0.5	+6.5	V
I _O	output current	V _O = 0 V to V _{CC}	-	50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	^[3] -	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO14 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
 For (T)SSOP14 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
 For DHVQFN14 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
		functional	1.2	-	-	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	active mode	0	-	V_{CC}	V
		high-impedance mode	0	-	5.5	V
T_{amb}	ambient temperature	in free air	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65\text{ V to }2.7\text{ V}$	0	-	20	ns/V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.2\text{ V}$	1.08	-	-	1.08	-	V
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	-	-	$0.65 \times V_{CC}$	-	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	-	-	1.7	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0	-	-	2.0	-	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.7 \times V_{CC}$	-	-	$0.7 \times V_{CC}$	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.2\text{ V}$	-	-	0.12	-	0.12	V
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	-	$0.35 \times V_{CC}$	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.7	-	0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.8	-	0.8	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	$0.30 \times V_{CC}$	-	$0.30 \times V_{CC}$	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		$I_O = 100\ \mu\text{A}$; $V_{CC} = 1.65\text{ V to }5.5\text{ V}$	-	-	0.20	-	0.3	V
		$I_O = 4\text{ mA}$; $V_{CC} = 1.65\text{ V}$	-	-	0.45	-	0.65	V
		$I_O = 8\text{ mA}$; $V_{CC} = 2.3\text{ V}$	-	-	0.6	-	0.8	V
		$I_O = 12\text{ mA}$; $V_{CC} = 2.7\text{ V}$	-	-	0.4	-	0.6	V
		$I_O = 24\text{ mA}$; $V_{CC} = 3.0\text{ V}$	-	-	0.55	-	0.8	V
I_I	input leakage current	$V_I = 5.5\text{ V or GND}$; $V_{CC} = 1.65\text{ V to }5.5\text{ V}$	-	± 0.1	± 5	-	± 20	μA
		$V_I = V_{IH}$; $V_O = 5.5\text{ V or GND}$; $V_{CC} = 1.65\text{ V to }5.5\text{ V}$	-	0.1	± 5	-	± 20	μA
I_{OFF}	power-off leakage current	V_I or $V_O = 5.5\text{ V}$; $V_{CC} = 0\text{ V}$	-	± 0.1	± 10	-	± 20	μA

Table 6. Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	0.1	10	-	40	μA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 2.7 V to 5.5 V	-	5	500	-	5000	μA
C _I	input capacitance	V _{CC} = 0 V to 5.5 V; V _I = GND to V _{CC}	-	4.0	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{PZL}	OFF-state to LOW propagation delay	nA, nB to nY; see Figure 6						
		V _{CC} = 1.2 V	-	5.7	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	1.0	2.6	6.0	1.0	6.9	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	1.8	3.3	0.5	3.8	ns
		V _{CC} = 2.7 V	0.5	1.7	2.9	0.5	4.0	ns
t _{PLZ}	LOW to OFF-state propagation delay	V _{CC} = 3.0 V to 3.6 V	0.5	1.8	3.0	0.5	4.0	ns
		nA, nB to nY; see Figure 6						
		V _{CC} = 1.2 V	-	5.7	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	1.0	2.7	6.0	1.0	6.9	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	1.5	3.3	0.5	3.8	ns
t _{sk(o)}	output skew time	V _{CC} = 2.7 V	1.0	2.6	3.8	1.0	5.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.3	3.6	1.0	4.5	ns
		^[2]	-	-	1.0	-	1.5	ns

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
C _{PD}	power dissipation capacitance	per gate; V _I = GND to V _{CC} ^[3]						
		V _{CC} = 1.65 V to 1.95 V	-	6.2	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	9.7	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	12.9	-	-	-	pF

- [1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.
- [2] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; f_o = output frequency in MHz
 C_L = output load capacitance in pF
 V_{CC} = supply voltage in Volts
 N = number of inputs switching
 Σ(C_L × V_{CC}² × f_o) = sum of the outputs

11. AC waveforms

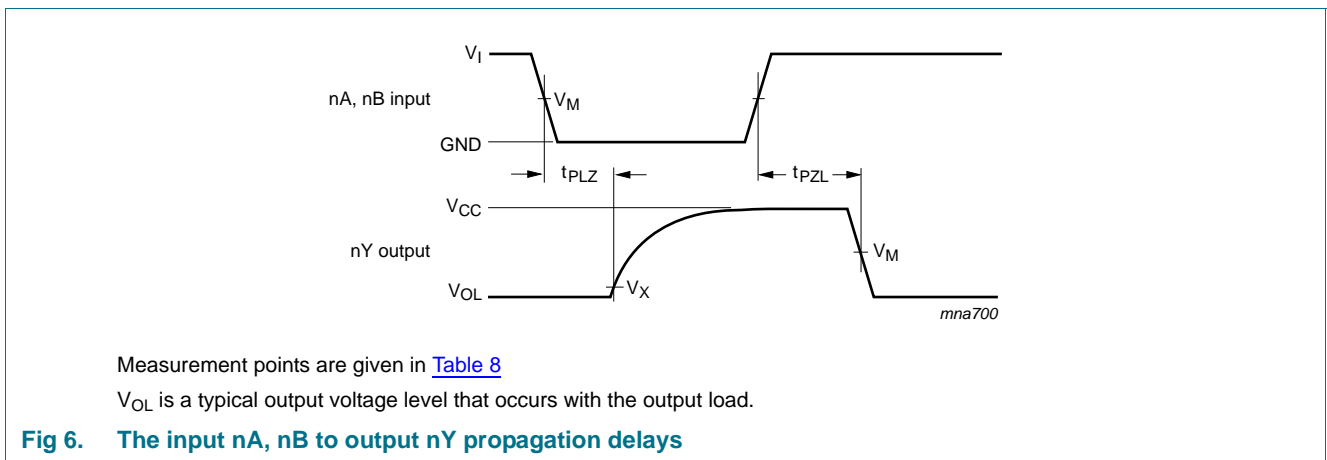
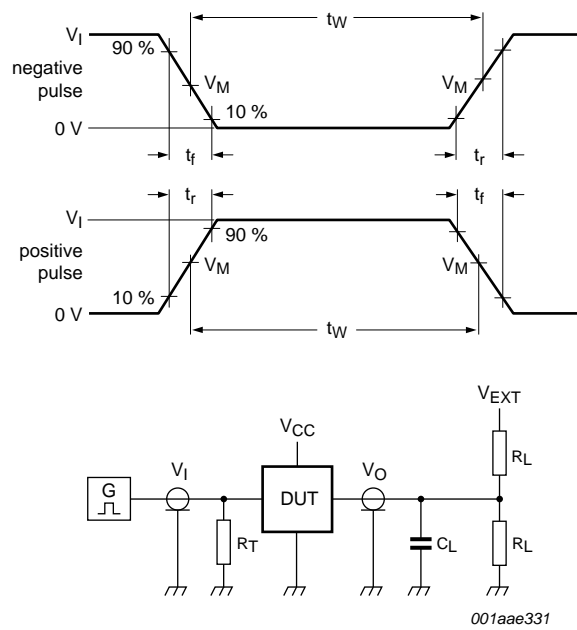


Table 8. Measurement points

Supply voltage	Input	Output
V _{CC}	V _M	V _X
<2.7 V	0.5 × V _{CC}	V _{OL} + 0.15 V
≥2.7 V to 3.6 V	1.5 V	V _{OL} + 0.3 V



Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 7. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}	
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	$2 \times V_{CC}$
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

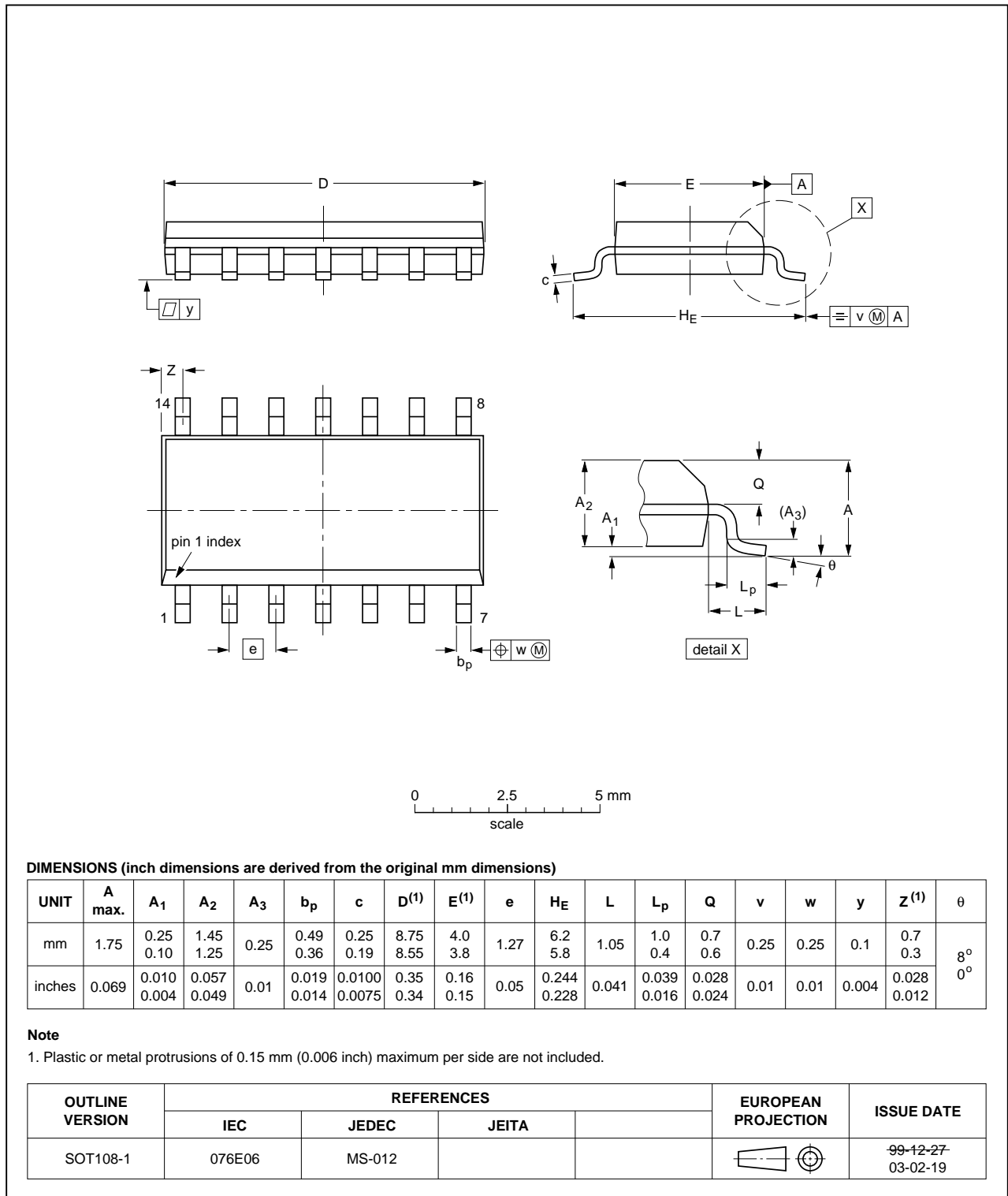


Fig 8. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

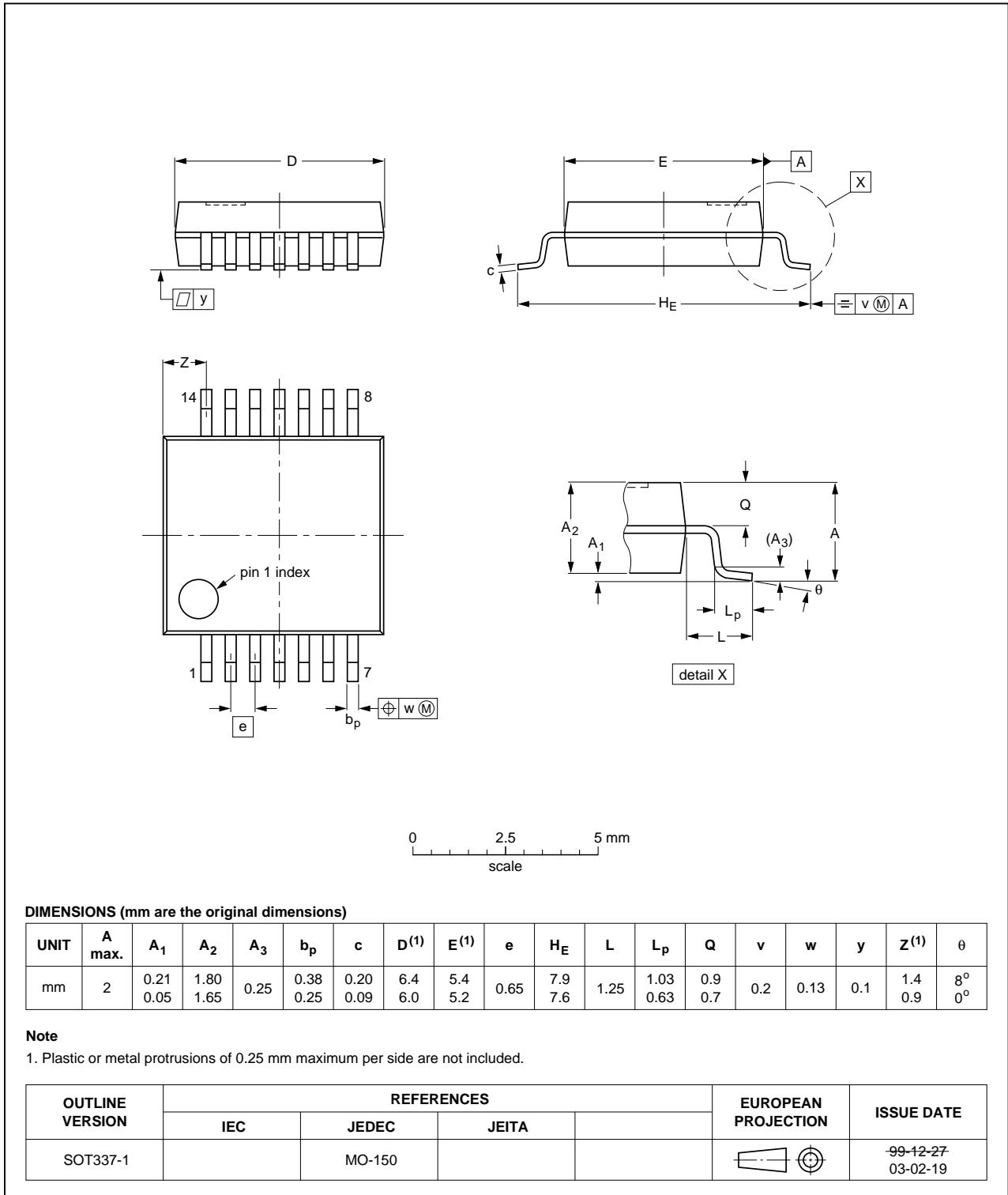


Fig 9. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

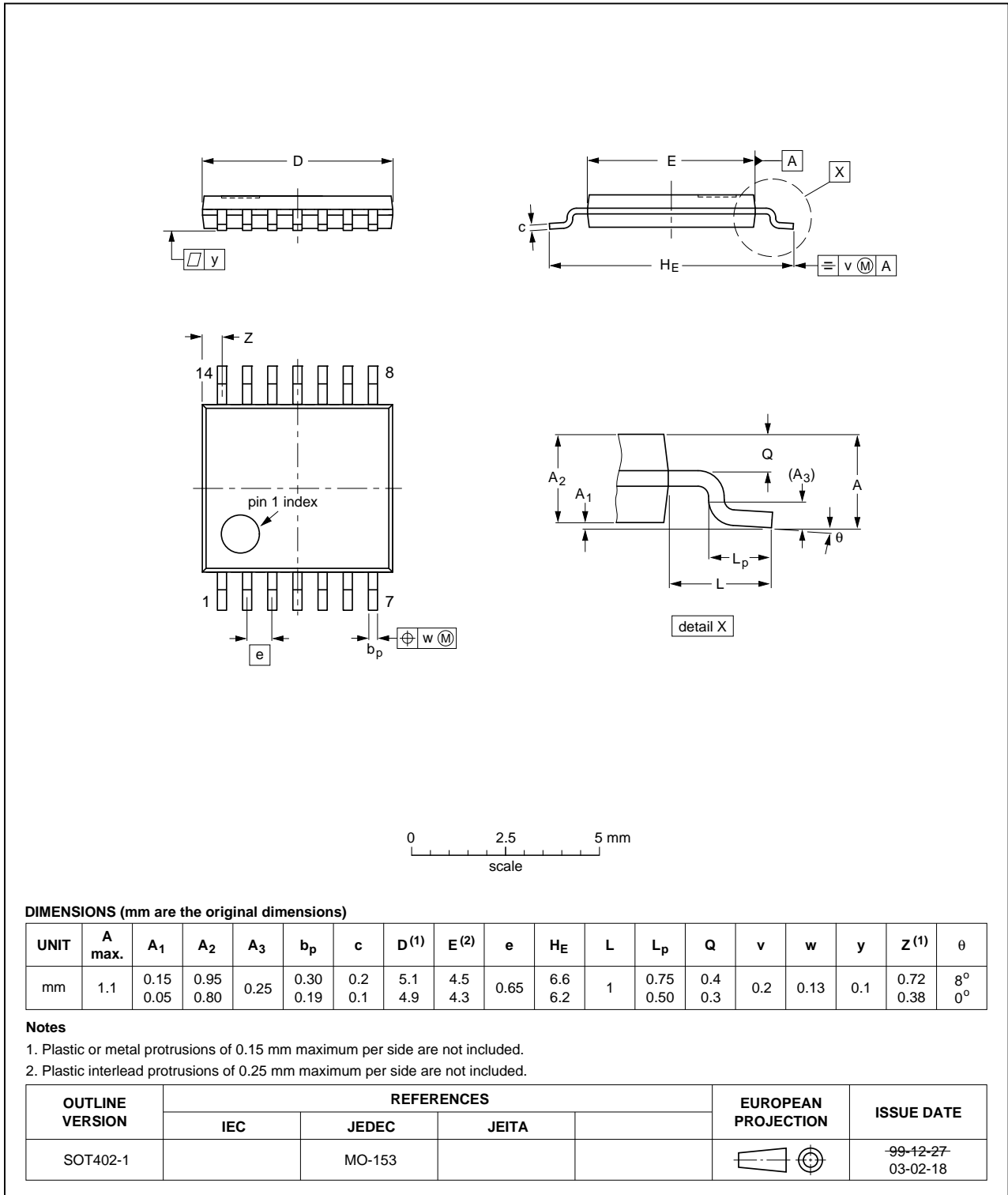


Fig 10. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

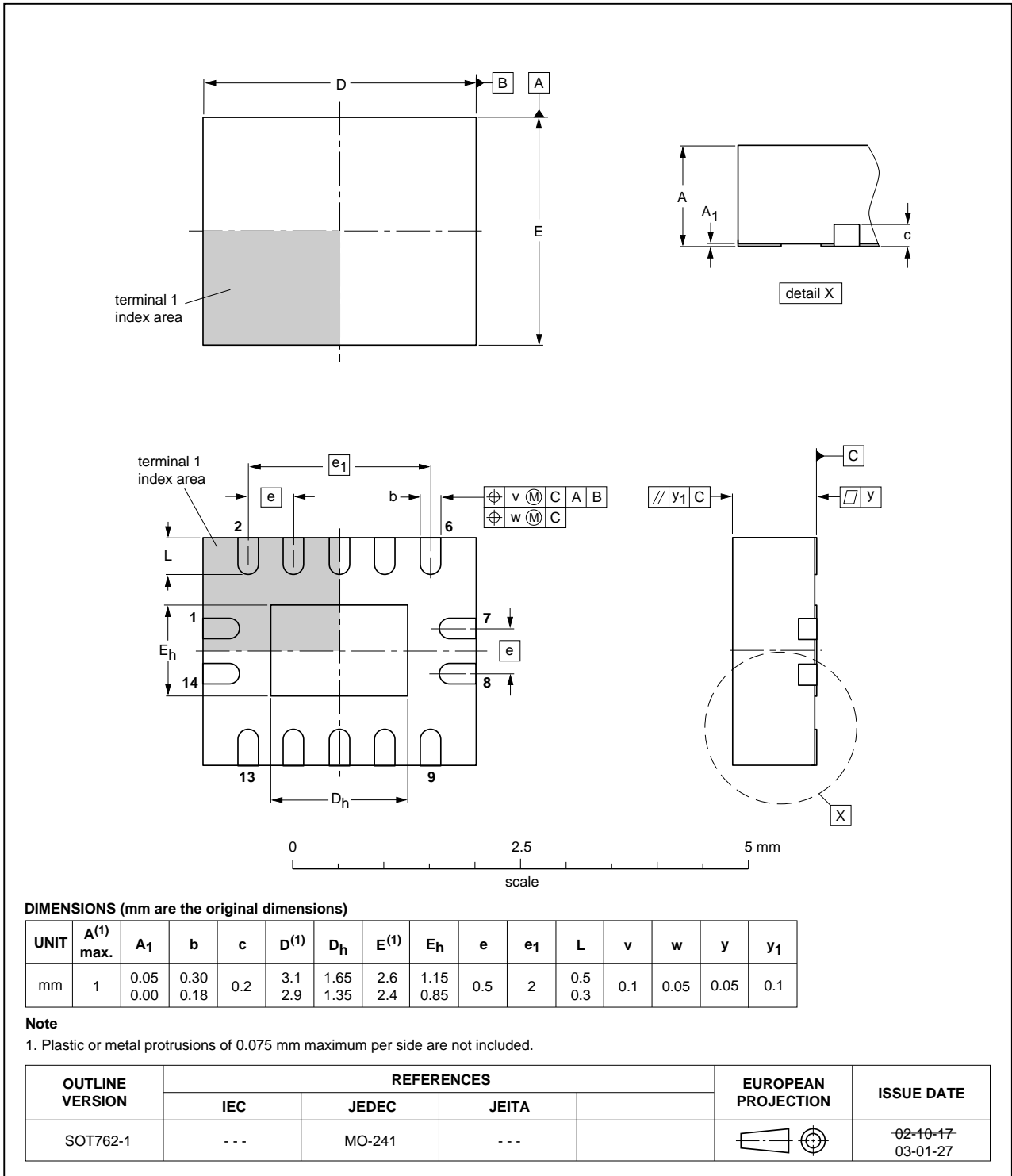


Fig 11. Package outline SOT762-1 (DHVQFN14)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC38A v.4	20111104	Product data sheet	-	74LVC38A v.3
Modifications:	<ul style="list-style-type: none"> The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Table 4, Table 5, Table 6, Table 7 and Table 8: values added for lower voltage ranges. 			
74LVC38A v.3	20040322	Product specification	-	74LVC38A v.2
74LVC38A v.2	20040310	Product specification	-	74LVC38A v.1
74LVC38A v.1	20020408	-	-	-

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15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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17. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	1
4	Functional diagram	2
5	Pinning information	2
5.1	Pinning	2
5.2	Pin description	3
6	Functional description	3
7	Limiting values	3
8	Recommended operating conditions	4
9	Static characteristics	4
10	Dynamic characteristics	5
11	AC waveforms	6
12	Package outline	8
13	Abbreviations	12
14	Revision history	12
15	Legal information	13
15.1	Data sheet status	13
15.2	Definitions	13
15.3	Disclaimers	13
15.4	Trademarks	14
16	Contact information	14
17	Contents	15

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