



**THE DATASHEET OF
74LVC2G66DC,125**



74LVC2G66

Bilateral switch

Rev. 11 — 30 October 2018

Product data sheet

1. General description

The 74LVC2G66 is a low-power, low-voltage, high-speed Si-gate CMOS device.

The 74LVC2G66 provides two single pole, single-throw analog switch functions. Each switch has two input/output terminals (nY and nZ) and an active HIGH enable input (nE). When nE is LOW, the analog switch is turned off.

Schmitt trigger action at the enable inputs makes the circuit tolerant of slower input rise and fall times across the entire V_{CC} range from 1.65 V to 5.5 V.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- Very low ON resistance:
 - 7.5 Ω (typical) at $V_{CC} = 2.7$ V
 - 6.5 Ω (typical) at $V_{CC} = 3.3$ V
 - 6 Ω (typical) at $V_{CC} = 5$ V
- Switch current capability of 32 mA
- High noise immunity
- CMOS low power consumption
- TTL interface compatibility at 3.3 V
- Latch-up performance meets requirements of JESD78 Class I
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Enable input accepts voltages up to 5.5 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC2G66DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC2G66DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC2G66GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm	SOT833-1
74LVC2G66GM	-40 °C to +125 °C	XQFN8	plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.5 mm	SOT902-2
74LVC2G66GN	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 x 1.0 x 0.35 mm	SOT1116

4. Marking

Table 2. Marking codes

Type number	Marking code ^[1]
74LVC2G66DP	V66
74LVC2G66DC	V66
74LVC2G66GT	V66
74LVC2G66GM	V66
74LVC2G66GN	VL

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

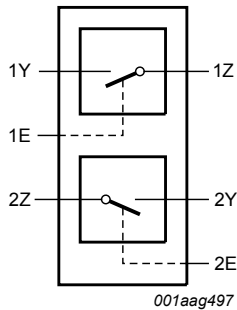


Fig. 1. Logic symbol

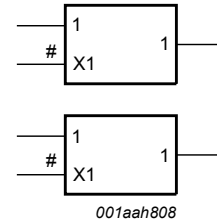


Fig. 2. IEC logic symbol

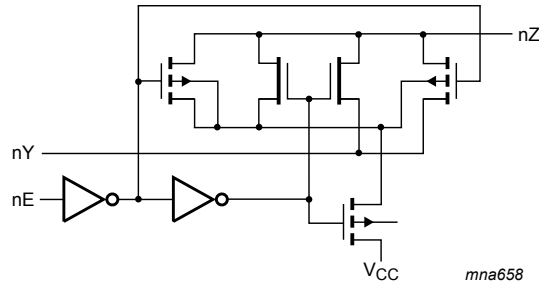
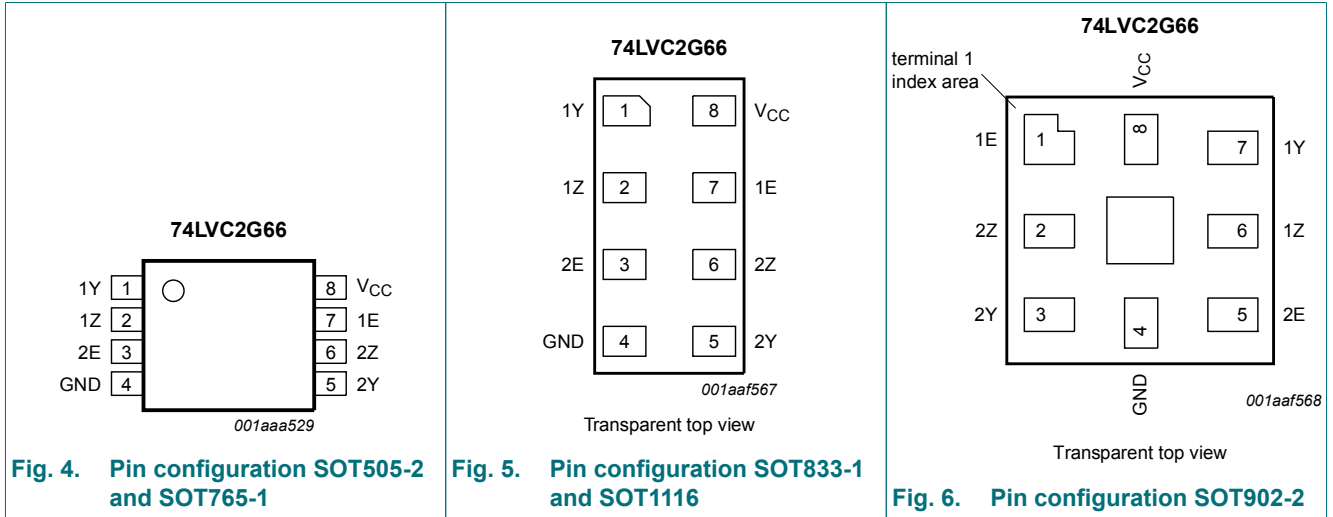


Fig. 3. Logic diagram (one switch)

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT505-2, SOT765-1, SOT833-1 and SOT1116	SOT902-2	
1Y	1	7	independent input or output
1Z	2	6	independent input or output
2E	3	5	enable input (active HIGH)
GND	4	4	ground (0 V)
2Y	5	3	independent input or output
2Z	6	2	independent input or output
1E	7	1	enable input (active HIGH)
V _{CC}	8	8	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input nE	Switch
L	OFF-state
H	ON-state

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
V_I	input voltage	[1]	-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$	-50	-	mA
I_{SK}	switch clamping current	$V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$	-	± 50	mA
V_{SW}	switch voltage	enable and disable mode [2]	-0.5	$V_{CC} + 0.5$	V
I_{SW}	switch current	$V_{SW} > -0.5 \text{ V}$ or $V_{SW} < V_{CC} + 0.5 \text{ V}$	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40 \text{ °C}$ to $+125 \text{ °C}$ [3]	-	250	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.

[3] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.

For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K.

For XSON8 and XQFN8 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_{SW}	switch voltage	[1][2]	0	V_{CC}	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65 \text{ V}$ to 2.7 V [3]	-	20	ns/V
		$V_{CC} = 2.7 \text{ V}$ to 5.5 V	-	10	ns/V

[1] To avoid sinking GND current from terminal nZ when switch current flows in terminal nY, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no GND current will flow from terminal nY. In this case, there is no limit for the voltage drop across the switch.

[2] For overvoltage tolerant switch voltage capability, refer to 74LVCV2G66.

[3] Applies to control signal levels.

10. Static characteristics

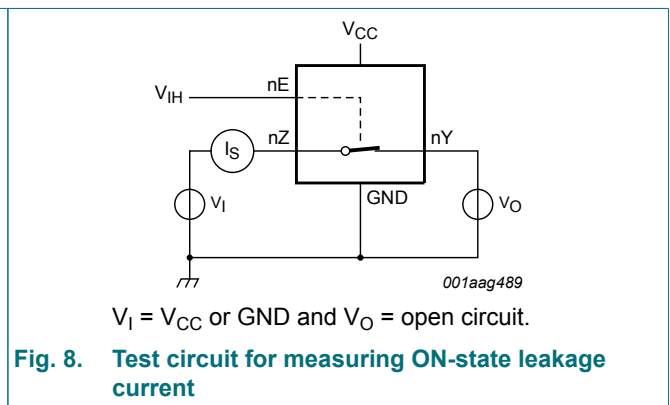
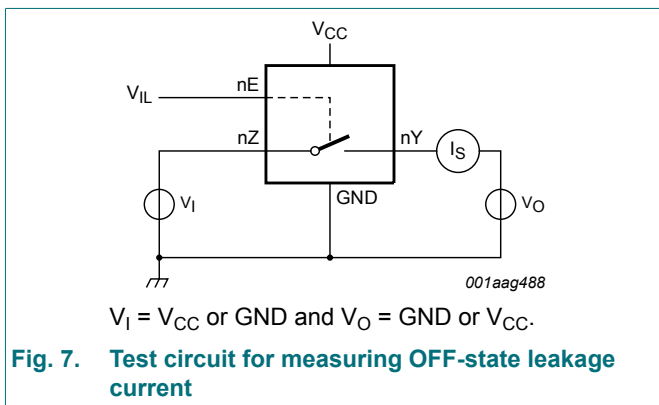
Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65×V _{CC}	-	-	0.65×V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7×V _{CC}	-	-	0.7×V _{CC}	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35×V _{CC}	-	0.35×V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3×V _{CC}	-	0.3×V _{CC}	V
I _I	input leakage current	pin nE; V _I = 5.5 V or GND; [2] V _{CC} = 0 V to 5.5 V	-	±0.1	±1	-	±1	µA
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 5.5 V; see Fig. 7. [2]	-	±0.1	±0.2	-	±0.5	µA
I _{S(ON)}	ON-state leakage current	V _{CC} = 5.5 V; see Fig. 8. [2]	-	±0.1	±1	-	±2	µA
I _{CC}	supply current	V _I = 5.5 V or GND; [2] V _{SW} = GND or V _{CC} ; V _{CC} = 1.65 V to 5.5 V	-	0.1	4	-	4	µA
ΔI _{CC}	additional supply current	pin nE; V _I = V _{CC} - 0.6 V; [2] V _{SW} = GND or V _{CC} ; V _{CC} = 5.5 V	-	5	500	-	500	µA
C _I	input capacitance		-	2.0	-	-	-	pF
C _{S(OFF)}	OFF-state capacitance		-	5.0	-	-	-	pF
C _{S(ON)}	ON-state capacitance		-	9.5	-	-	-	pF

- [1] All typical values are measured at T_{amb} = 25 °C.
- [2] These typical values are measured at V_{CC} = 3.3 V.

10.1. Test circuits



10.2. ON resistance

Table 8. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground 0 V); for graphs see [Fig. 10](#) to [Fig. 15](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
R _{ON(peak)}	ON resistance (peak)	V _I = GND to V _{CC} ; see Fig. 9 .						
		I _{SW} = 4 mA; V _{CC} = 1.65 V to 1.95 V	-	34.0	130	-	195	Ω
		I _{SW} = 8 mA; V _{CC} = 2.3 V to 2.7 V	-	12.0	30	-	45	Ω
		I _{SW} = 12 mA; V _{CC} = 2.7 V	-	10.4	25	-	38	Ω
		I _{SW} = 24 mA; V _{CC} = 3 V to 3.6 V	-	7.8	20	-	30	Ω
		I _{SW} = 32 mA; V _{CC} = 4.5 V to 5.5 V	-	6.2	15	-	23	Ω
R _{ON(rail)}	ON resistance (rail)	V _I = GND; see Fig. 9						
		I _{SW} = 4 mA; V _{CC} = 1.65 V to 1.95 V	-	8.2	18	-	27	Ω
		I _{SW} = 8 mA; V _{CC} = 2.3 V to 2.7 V	-	7.1	16	-	24	Ω
		I _{SW} = 12 mA; V _{CC} = 2.7 V	-	6.9	14	-	21	Ω
		I _{SW} = 24 mA; V _{CC} = 3 V to 3.6 V	-	6.5	12	-	18	Ω
		I _{SW} = 32 mA; V _{CC} = 4.5 V to 5.5 V	-	5.8	10	-	15	Ω
		V _I = V _{CC} ; see Fig. 9						
		I _{SW} = 4 mA; V _{CC} = 1.65 V to 1.95 V	-	10.4	30	-	45	Ω
		I _{SW} = 8 mA; V _{CC} = 2.3 V to 2.7 V	-	7.6	20	-	30	Ω
		I _{SW} = 12 mA; V _{CC} = 2.7 V	-	7.0	18	-	27	Ω
		I _{SW} = 24 mA; V _{CC} = 3 V to 3.6 V	-	6.1	15	-	23	Ω
		I _{SW} = 32 mA; V _{CC} = 4.5 V to 5.5 V	-	4.9	10	-	15	Ω
		R _{ON(flat)}	ON resistance (flatness)	V _I = GND to V _{CC} [2]				
I _{SW} = 4 mA; V _{CC} = 1.65 V to 1.95 V	-			26.0	-	-	-	Ω
I _{SW} = 8 mA; V _{CC} = 2.3 V to 2.7 V	-			5.0	-	-	-	Ω
I _{SW} = 12 mA; V _{CC} = 2.7 V	-			3.5	-	-	-	Ω
I _{SW} = 24 mA; V _{CC} = 3 V to 3.6 V	-			2.0	-	-	-	Ω
I _{SW} = 32 mA; V _{CC} = 4.5 V to 5.5 V	-			1.5	-	-	-	Ω

[1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.

[2] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V_{CC} and temperature.

10.3. ON resistance test circuit and graphs

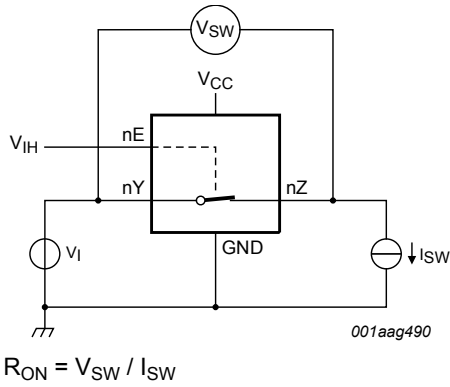
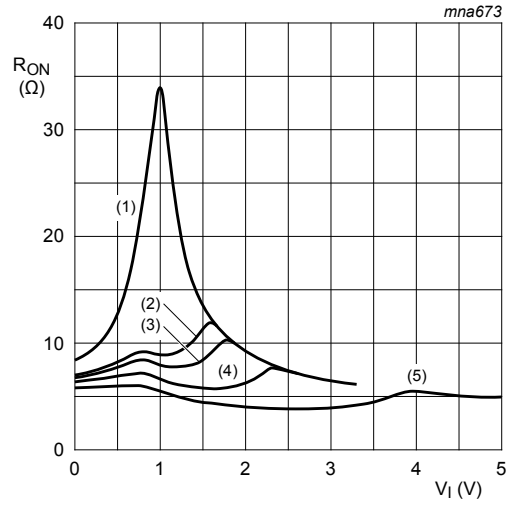
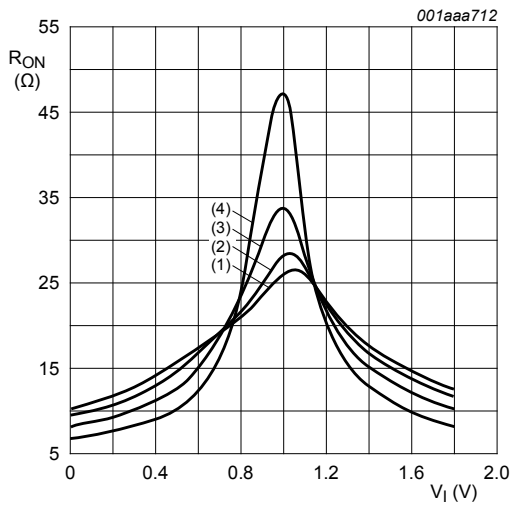


Fig. 9. Test circuit for measuring ON resistance



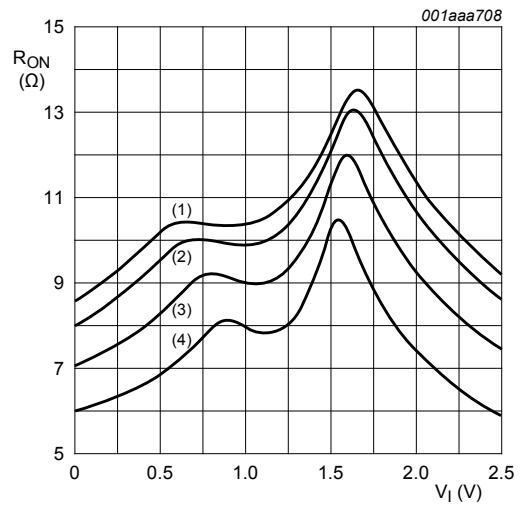
- (1) $V_{CC} = 1.8 \text{ V}$
- (2) $V_{CC} = 2.5 \text{ V}$
- (3) $V_{CC} = 2.7 \text{ V}$
- (4) $V_{CC} = 3.3 \text{ V}$
- (5) $V_{CC} = 5.0 \text{ V}$

Fig. 10. Typical ON resistance as a function of input voltage; $T_{amb} = 25 \text{ }^\circ\text{C}$



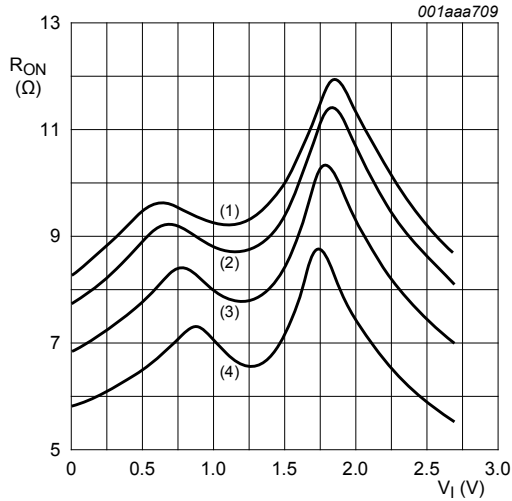
- (1) $T_{amb} = 125 \text{ }^\circ\text{C}$
- (2) $T_{amb} = 85 \text{ }^\circ\text{C}$
- (3) $T_{amb} = 25 \text{ }^\circ\text{C}$
- (4) $T_{amb} = -40 \text{ }^\circ\text{C}$

Fig. 11. ON resistance as a function of input voltage; $V_{CC} = 1.8 \text{ V}$



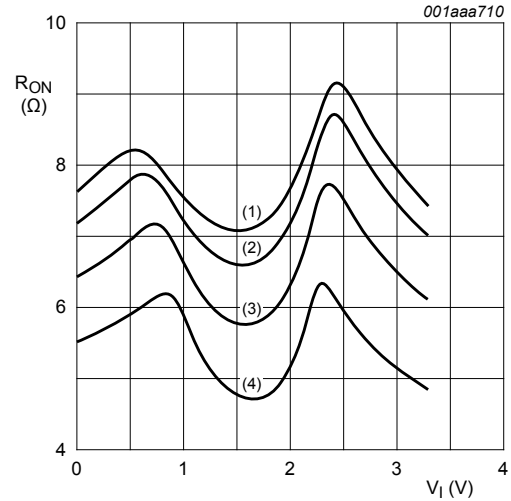
- (1) $T_{amb} = 125 \text{ }^\circ\text{C}$
- (2) $T_{amb} = 85 \text{ }^\circ\text{C}$
- (3) $T_{amb} = 25 \text{ }^\circ\text{C}$
- (4) $T_{amb} = -40 \text{ }^\circ\text{C}$

Fig. 12. ON resistance as a function of input voltage; $V_{CC} = 2.5 \text{ V}$



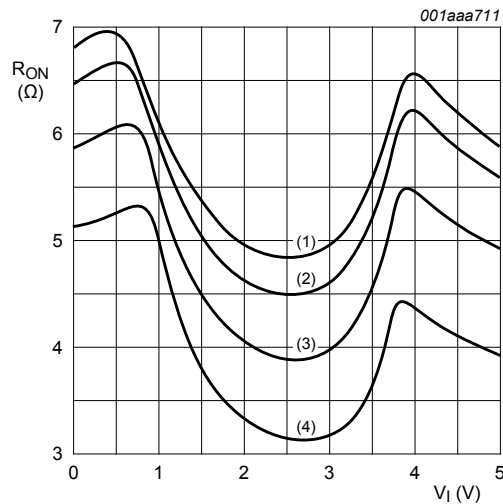
- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}$
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}$
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}$

Fig. 13. ON resistance as a function of input voltage; $V_{CC} = 2.7\text{ V}$



- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}$
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}$
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}$

Fig. 14. ON resistance as a function of input voltage; $V_{CC} = 3.3\text{ V}$



- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}$
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}$
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}$

Fig. 15. ON resistance as a function of input voltage; $V_{CC} = 5.0\text{ V}$

11. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 18.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t _{pd}	propagation delay	nY to nZ or nZ to nY; see Fig. 16. [2][3]						
		V _{CC} = 1.65 V to 1.95 V	-	0.8	2.0	-	3.0	ns
		V _{CC} = 2.3 V to 2.7 V	-	0.4	1.2	-	2.0	ns
		V _{CC} = 2.7 V	-	0.4	1.0	-	1.5	ns
		V _{CC} = 3.0 V to 3.6 V	-	0.3	0.8	-	1.5	ns
		V _{CC} = 4.5 V to 5.5 V	-	0.2	0.6	-	1.0	ns
t _{en}	enable time	nE to nY or nZ; see Fig. 17. [4]						
		V _{CC} = 1.65 V to 1.95 V	1.0	4.6	10	1.0	13.0	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	2.7	5.6	1.0	7.5	ns
		V _{CC} = 2.7 V	1.0	2.7	5.0	1.0	6.5	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.4	4.4	1.0	6.0	ns
		V _{CC} = 4.5 V to 5.5 V	1.0	1.8	3.9	1.0	5.0	ns
t _{dis}	disable time	nE to nY or nZ; see Fig. 17. [5]						
		V _{CC} = 1.65 V to 1.95 V	1.0	3.8	9.0	1.0	11.5	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	2.1	5.5	1.0	7.0	ns
		V _{CC} = 2.7 V	1.0	3.5	6.5	1.0	8.5	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	3.0	6.0	1.0	8.0	ns
		V _{CC} = 4.5 V to 5.5 V	1.0	2.2	5.0	1.0	6.5	ns
C _{PD}	power dissipation capacitance	C _L = 50 pF; f _i = 10 MHz; V _I = GND to V _{CC} [6]						
		V _{CC} = 2.5 V	-	9.0	-	-	-	pF
		V _{CC} = 3.3 V	-	11.0	-	-	-	pF
		V _{CC} = 5.0 V	-	15.7	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified capacitance when driven by an ideal voltage source (zero output impedance).

[4] t_{en} is the same as t_{PZH} and t_{PZL}.

[5] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[6] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum \{(C_L + C_{S(ON)}) \times V_{CC}^2 \times f_o\} \text{ where:}$$

f_i = input frequency in MHz; f_o = output frequency in MHz;

C_L = output load capacitance in pF;

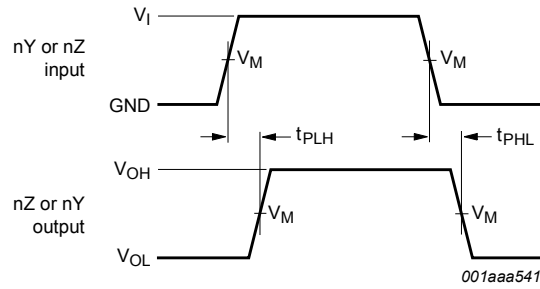
C_{S(ON)} = maximum ON-state switch capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum \{(C_L + C_{S(ON)}) \times V_{CC}^2 \times f_o\}$ = sum of the outputs.

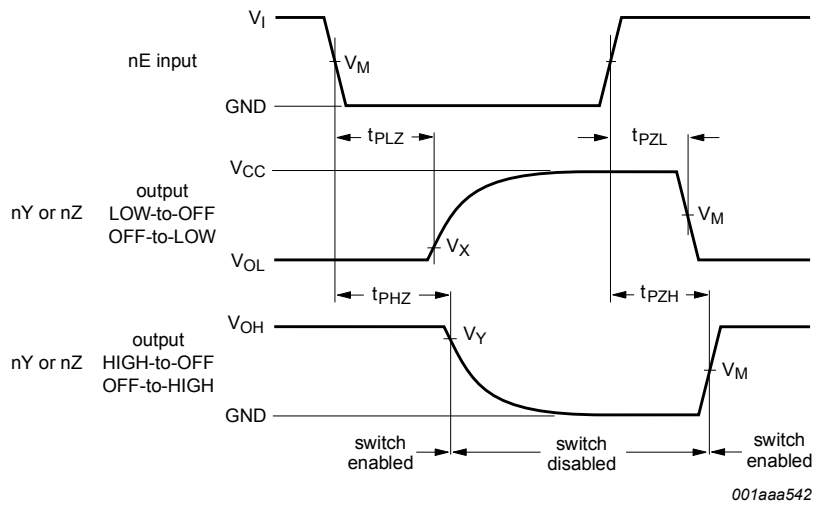
11.1. Waveforms and test circuit



Measurement points are given in [Table 10](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 16. Input (nY or nZ) to output (nZ or nY) propagation delays



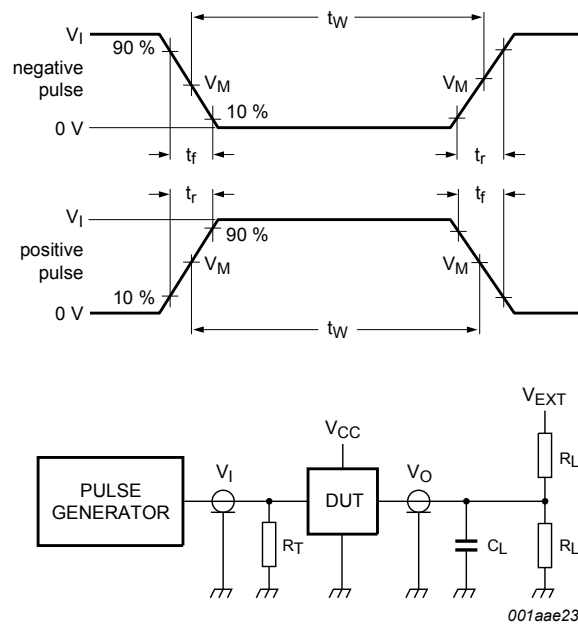
Measurement points are given in [Table 10](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 17. Enable and disable times

Table 10. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Test data is given in [Table 11](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

V_{EXT} = External voltage for measuring switching times.

Fig. 18. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 k Ω	open	GND	$2 \times V_{CC}$
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

11.2. Additional dynamic characteristics

Table 12. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	$R_L = 10\text{ k}\Omega$; $C_L = 50\text{ pF}$; $f_i = 1\text{ kHz}$; see Fig. 19.				
		$V_{CC} = 1.65\text{ V}$	-	0.032	-	%
		$V_{CC} = 2.3\text{ V}$	-	0.008	-	%
		$V_{CC} = 3.0\text{ V}$	-	0.006	-	%
		$V_{CC} = 4.5\text{ V}$	-	0.005	-	%
		$R_L = 10\text{ k}\Omega$; $C_L = 50\text{ pF}$; $f_i = 10\text{ kHz}$; see Fig. 19.				
		$V_{CC} = 1.65\text{ V}$	-	0.068	-	%
		$V_{CC} = 2.3\text{ V}$	-	0.009	-	%
		$V_{CC} = 3.0\text{ V}$	-	0.008	-	%
		$V_{CC} = 4.5\text{ V}$	-	0.006	-	%
$f_{(-3\text{dB})}$	-3 dB frequency response	$R_L = 600\text{ }\Omega$; $C_L = 50\text{ pF}$; see Fig. 20.				
		$V_{CC} = 1.65\text{ V}$	-	135	-	MHz
		$V_{CC} = 2.3\text{ V}$	-	145	-	MHz
		$V_{CC} = 3.0\text{ V}$	-	150	-	MHz
		$V_{CC} = 4.5\text{ V}$	-	155	-	MHz
		$R_L = 50\text{ }\Omega$; $C_L = 10\text{ pF}$; see Fig. 20.				
		$V_{CC} = 1.65\text{ V}$	-	200	-	MHz
		$V_{CC} = 2.3\text{ V}$	-	350	-	MHz
		$V_{CC} = 3.0\text{ V}$	-	410	-	MHz
		$V_{CC} = 4.5\text{ V}$	-	440	-	MHz
		$R_L = 50\text{ }\Omega$; $C_L = 5\text{ pF}$; see Fig. 20.				
		$V_{CC} = 1.65\text{ V}$	-	> 500	-	MHz
		$V_{CC} = 2.3\text{ V}$	-	> 500	-	MHz
		$V_{CC} = 3.0\text{ V}$	-	> 500	-	MHz
$V_{CC} = 4.5\text{ V}$	-	> 500	-	MHz		
α_{iso}	isolation (OFF-state)	$R_L = 600\text{ }\Omega$; $C_L = 50\text{ pF}$; $f_i = 1\text{ MHz}$; see Fig. 21.				
		$V_{CC} = 1.65\text{ V}$	-	-46	-	dB
		$V_{CC} = 2.3\text{ V}$	-	-46	-	dB
		$V_{CC} = 3.0\text{ V}$	-	-46	-	dB
		$V_{CC} = 4.5\text{ V}$	-	-46	-	dB
		$R_L = 50\text{ }\Omega$; $C_L = 5\text{ pF}$; $f_i = 1\text{ MHz}$; see Fig. 21.				
		$V_{CC} = 1.65\text{ V}$	-	-37	-	dB
		$V_{CC} = 2.3\text{ V}$	-	-37	-	dB
		$V_{CC} = 3.0\text{ V}$	-	-37	-	dB
		$V_{CC} = 4.5\text{ V}$	-	-37	-	dB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V _{ct}	crosstalk voltage	between digital inputs and switch; R _L = 600 Ω; C _L = 50 pF; f _i = 1 MHz; t _r = t _f = 2 ns; see Fig. 22.					
		V _{CC} = 1.65 V	-	-	-	mV	
		V _{CC} = 2.3 V	-	91	-	mV	
		V _{CC} = 3.0 V	-	119	-	mV	
		V _{CC} = 4.5 V	-	205	-	mV	
Xtalk	crosstalk	between switches; R _L = 600 Ω; C _L = 50 pF; f _i = 1 MHz; see Fig. 23.					
		V _{CC} = 1.65 V	-	-	-	dB	
		V _{CC} = 2.3 V	-	-56	-	dB	
		V _{CC} = 3.0 V	-	-56	-	dB	
		V _{CC} = 4.5 V	-	-56	-	dB	
		between switches; R _L = 50 Ω; C _L = 5 pF; f _i = 1 MHz; see Fig. 23.					
		V _{CC} = 1.65 V	-	-	-	dB	
		V _{CC} = 2.3 V	-	-29	-	dB	
		V _{CC} = 3.0 V	-	-28	-	dB	
		V _{CC} = 4.5 V	-	-28	-	dB	
Q _{inj}	charge injection	C _L = 0.1 nF; V _{gen} = 0 V; R _{gen} = 0 Ω; f _i = 1 MHz; R _L = 1 MΩ; see Fig. 24.					
		V _{CC} = 1.8 V	-	3.3	-	pC	
		V _{CC} = 2.5 V	-	4.1	-	pC	
		V _{CC} = 3.3 V	-	5.0	-	pC	
		V _{CC} = 4.5 V	-	6.4	-	pC	
		V _{CC} = 5.5 V	-	7.5	-	pC	

11.3. Test circuits

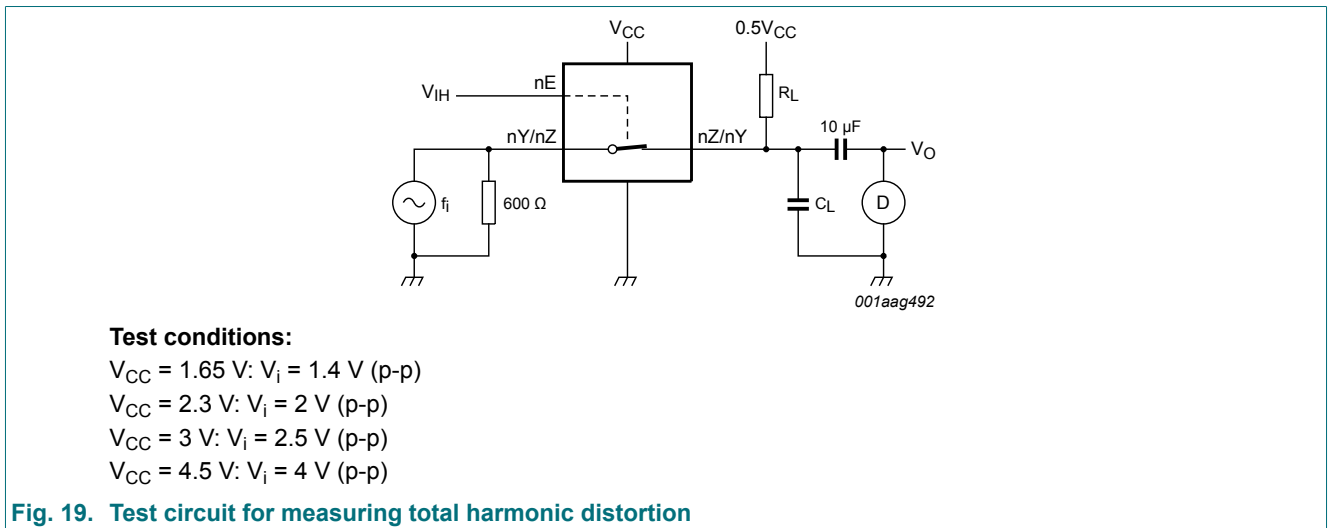
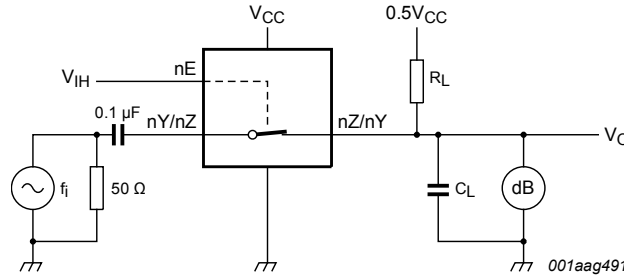
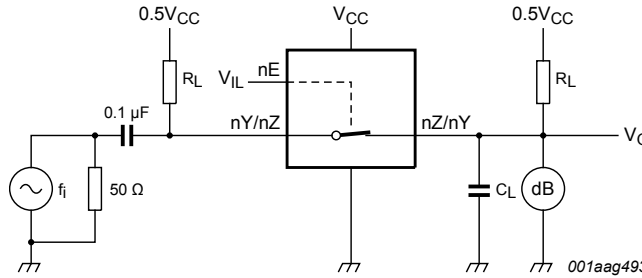


Fig. 19. Test circuit for measuring total harmonic distortion



Adjust f_i voltage to obtain 0 dBm level at output. Increase f_i frequency until dB meter reads -3 dB.

Fig. 20. Test circuit for measuring the frequency response when switch is in ON-state



Adjust f_i voltage to obtain 0 dBm level at input.

Fig. 21. Test circuit for measuring isolation (OFF-state)

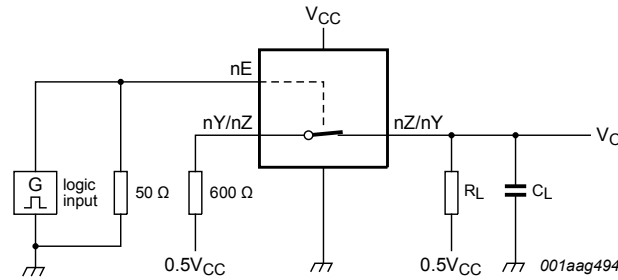
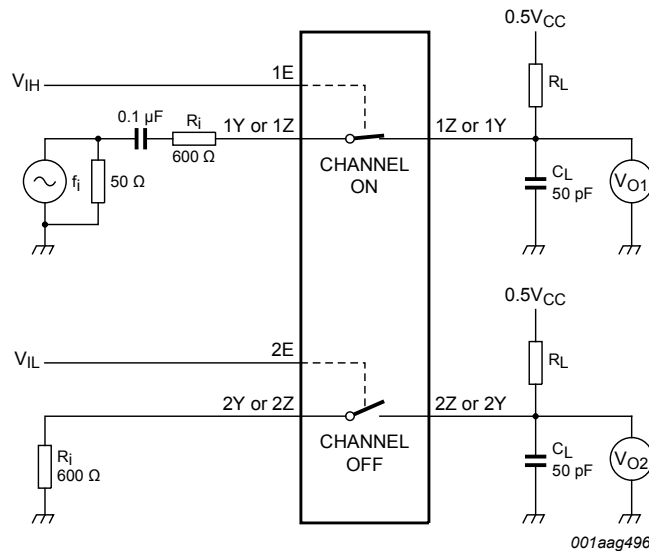
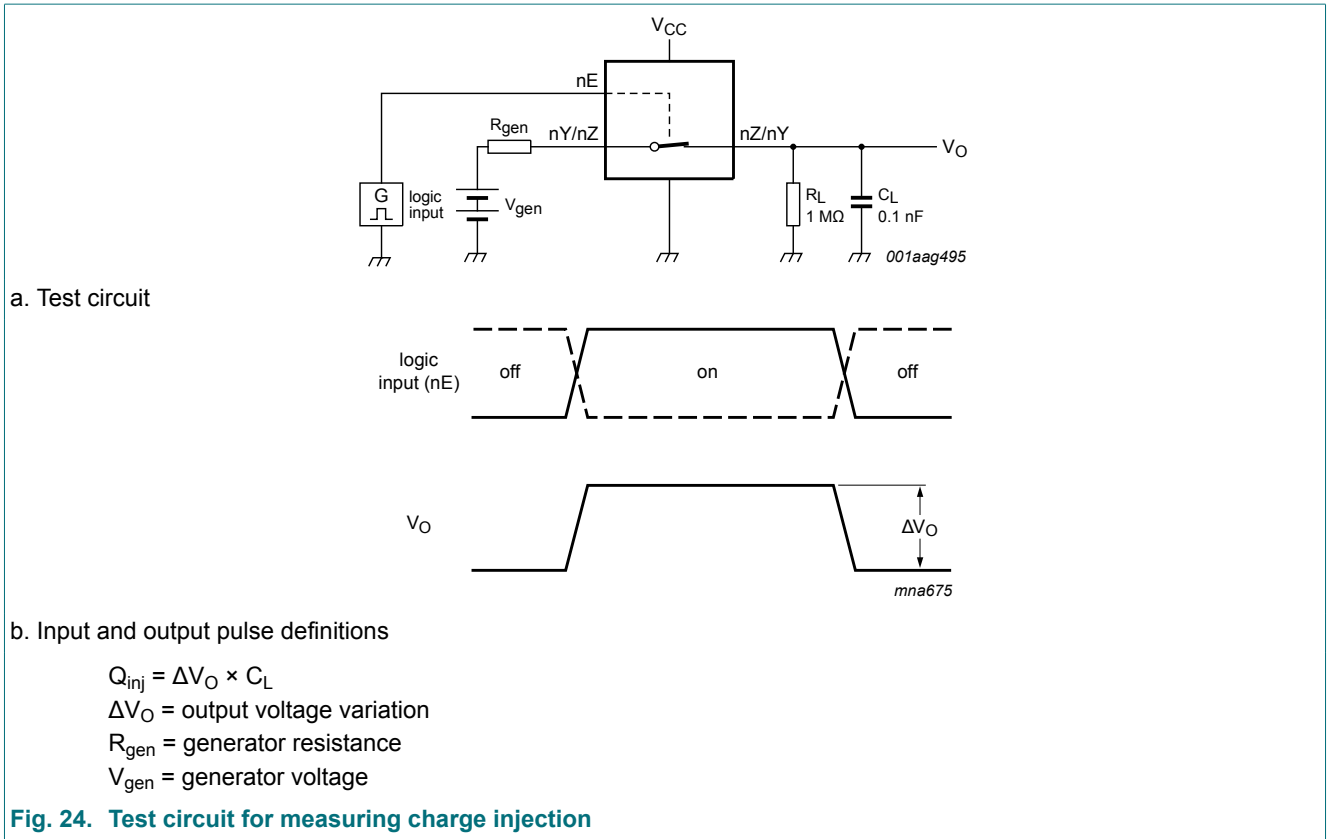


Fig. 22. Test circuit for measuring crosstalk voltage (between digital inputs and switch)



$20 \log_{10} (V_{O2} / V_{O1})$ or $20 \log_{10} (V_{O1} / V_{O2})$.

Fig. 23. Test circuit for measuring crosstalk between switches



12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

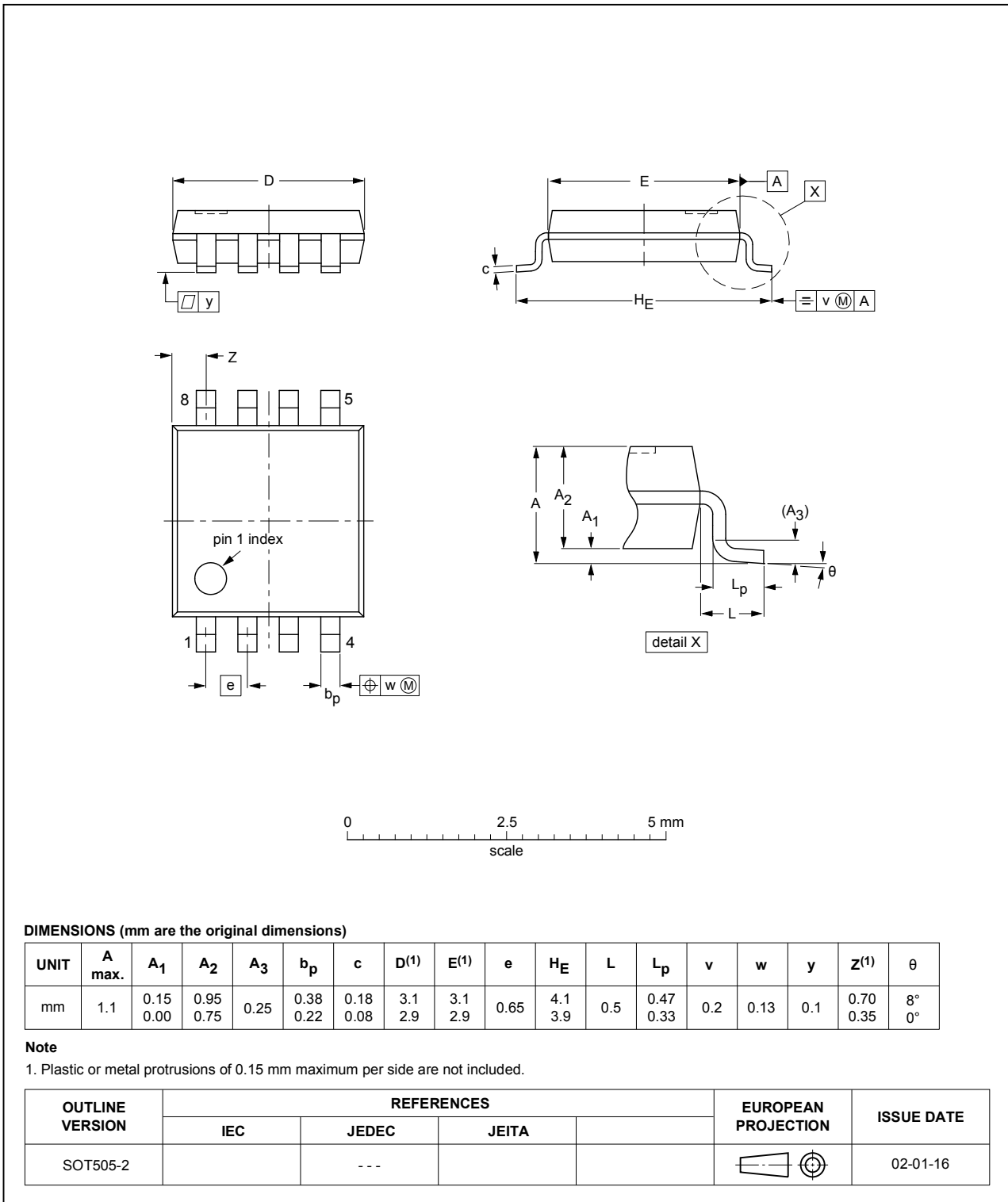


Fig. 25. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

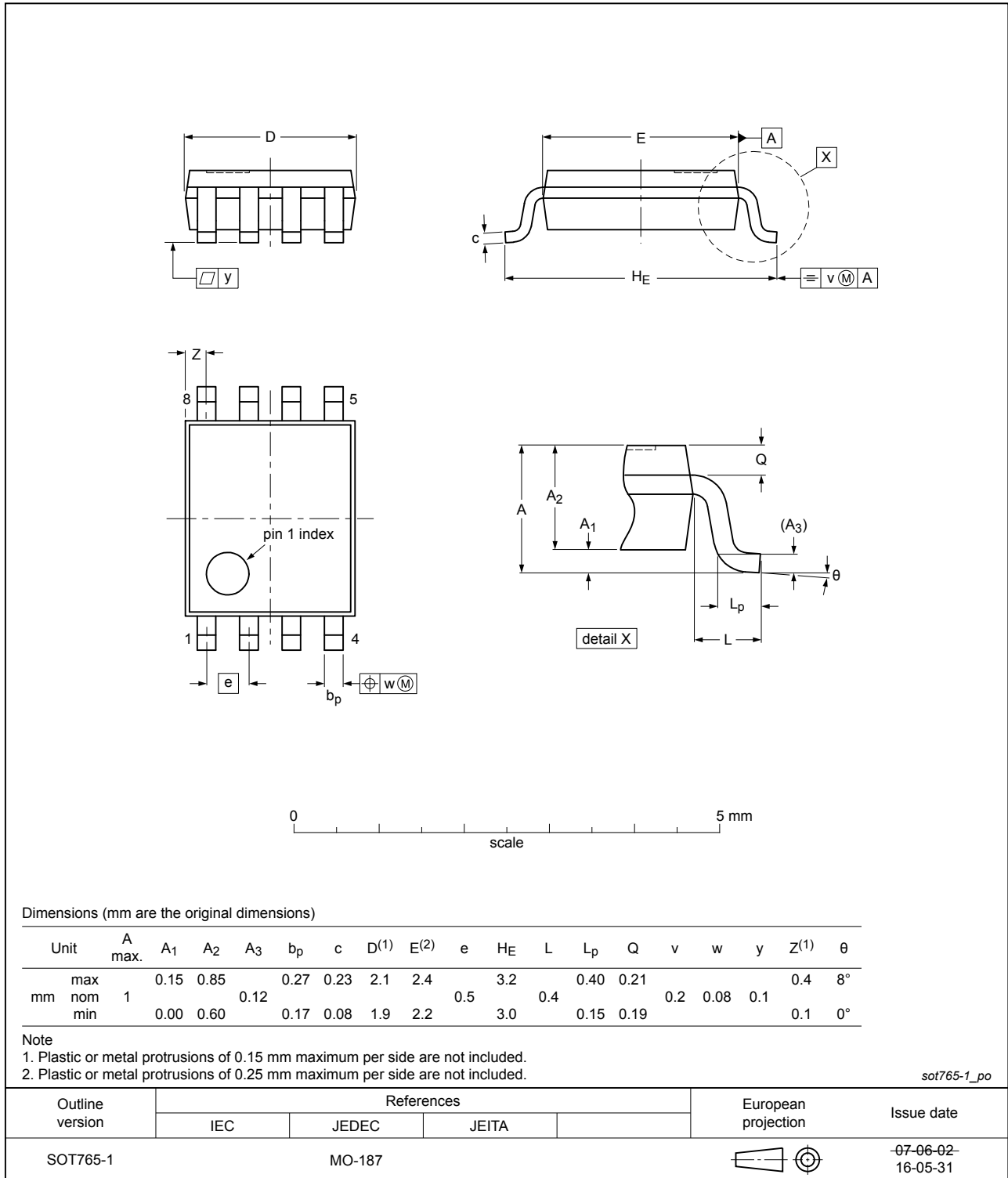


Fig. 26. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1

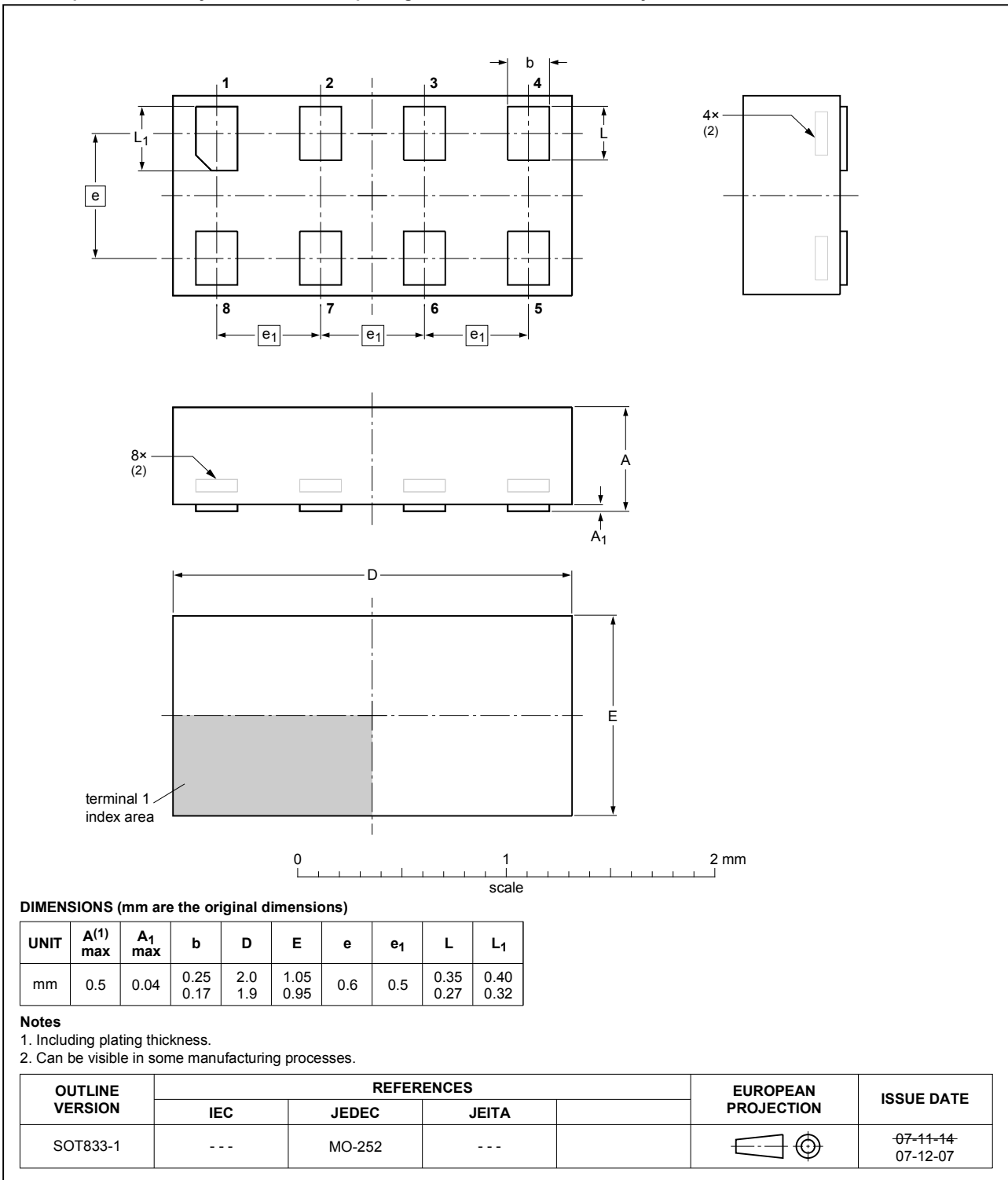


Fig. 27. Package outline SOT833-1 (XSON8)

XQFN8: plastic, extremely thin quad flat package; no leads;
8 terminals; body 1.6 x 1.6 x 0.5 mm

SOT902-2

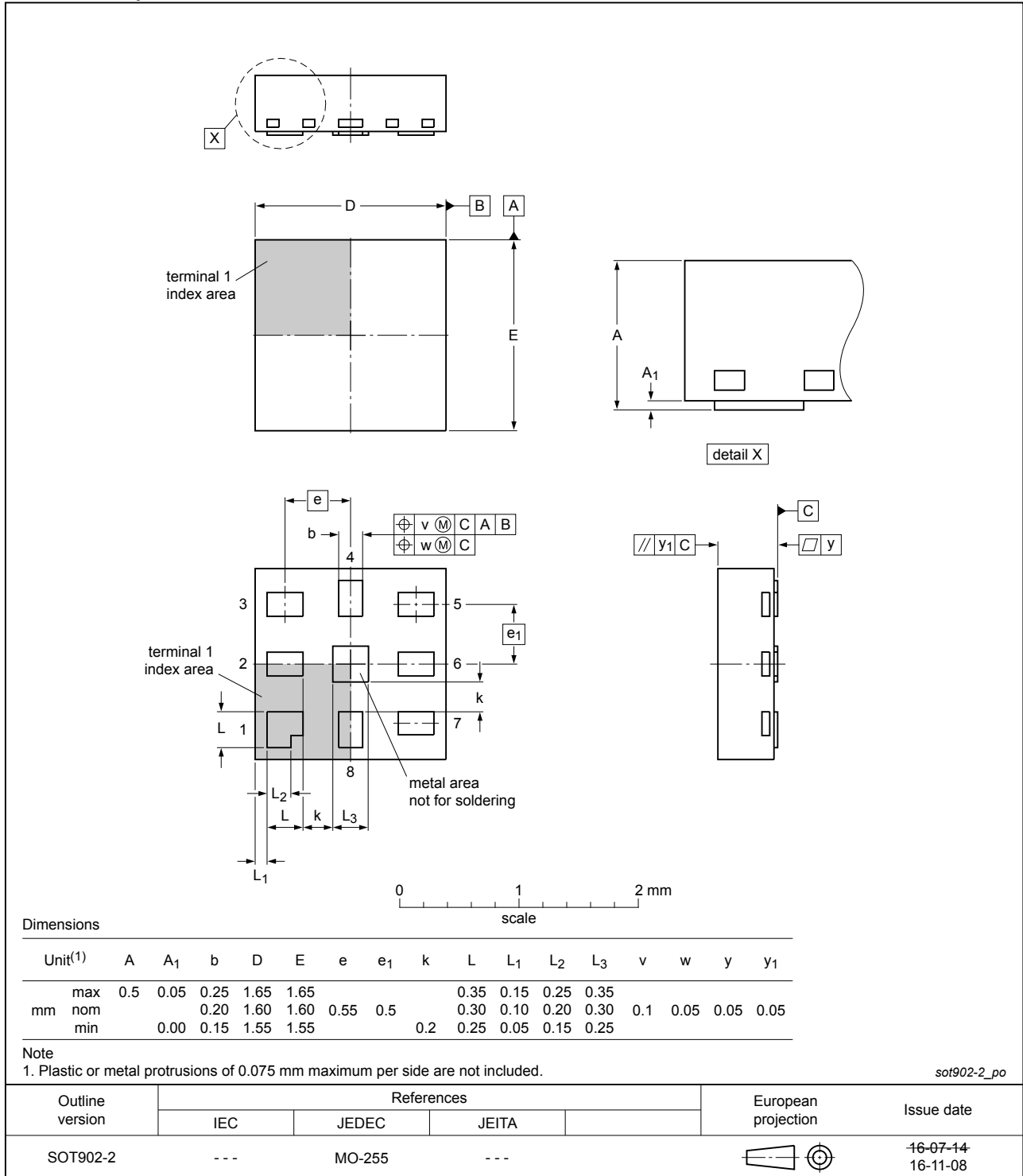


Fig. 28. Package outline SOT902-2 (XQFN8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.2 x 1.0 x 0.35 mm

SOT1116

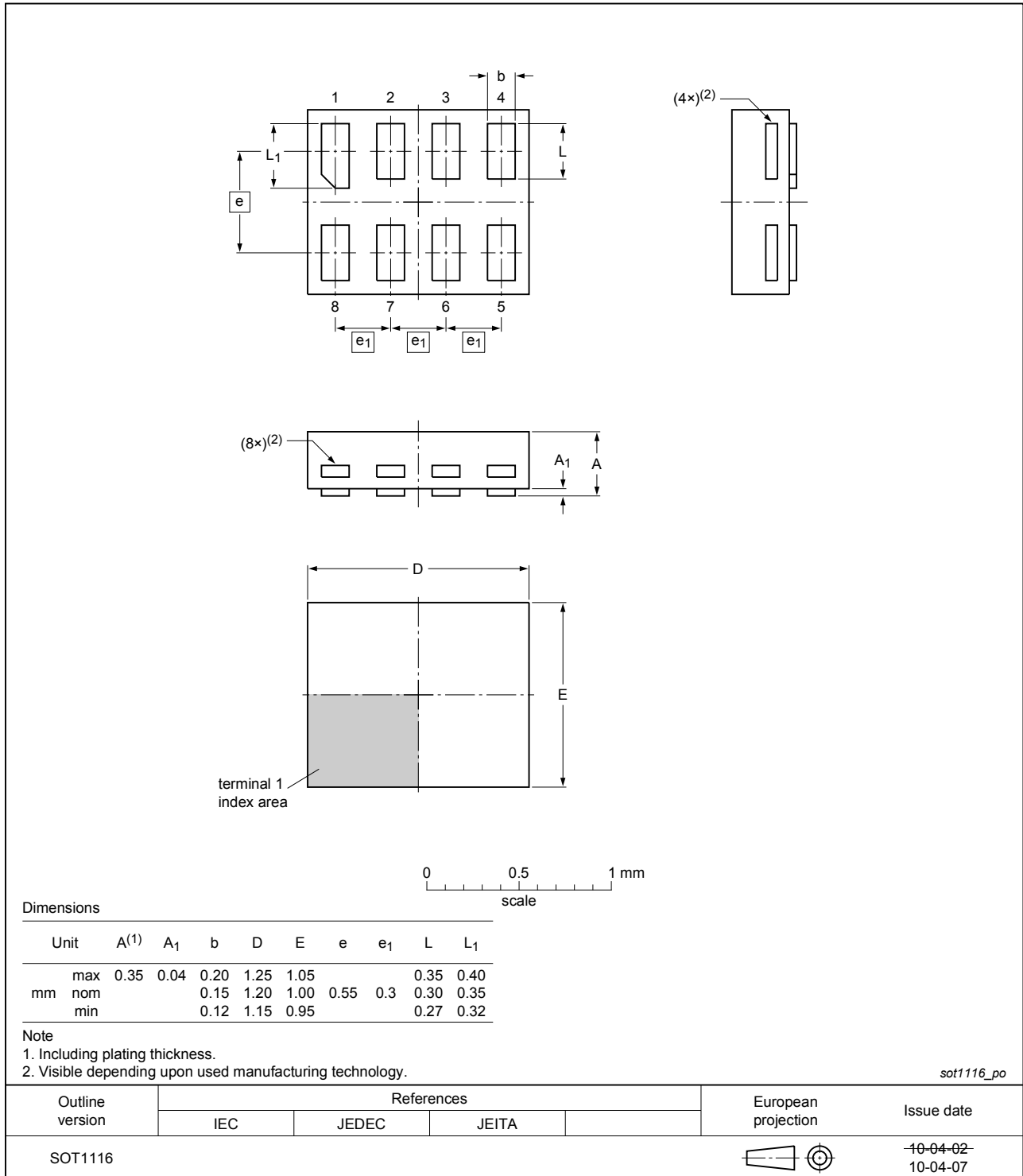


Fig. 29. Package outline SOT1116 (XSON8)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC2G66 v.11	20181030	Product data sheet	-	74LVC2G66 v.10
Modifications:	<ul style="list-style-type: none"> Type number 74LVC2G66GD (XSON8/SOT996-2) removed. 			
74LVC2G66 v.10	20170413	Product data sheet	-	74LVC2G66 v.9
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type number 74LVC2G66GN (XSON8/SOT1116) has been added. 			
74LVC2G66 v.9	20161215	Product data sheet	-	74LVC2G66 v.8
Modifications:	<ul style="list-style-type: none"> Table 7: The maximum limits for leakage current and supply current have changed. 			
74LVC2G66 v.8	20130402	Product data sheet	-	74LVC2G66 v.7
Modifications:	<ul style="list-style-type: none"> For type number 74LVC2G66GD XSON8U has changed to XSON8. 			
74LVC2G66 v.7	20120622	Product data sheet	-	74LVC2G66 v.6
Modifications:	<ul style="list-style-type: none"> For type number 74LVC2G66GM the SOT code has changed to SOT902-2. 			
74LVC2G66 v.6	20111129	Product data sheet	-	74LVC2G66 v.5
Modifications:	<ul style="list-style-type: none"> Legal pages updated. 			
74LVC2G66 v.5	20100616	Product data sheet	-	74LVC2G66 v.4
74LVC2G66 v.4	20080701	Product data sheet	-	74LVC2G66 v.3
74LVC2G66 v.3	20080310	Product data sheet	-	74LVC2G66 v.2
74LVC2G66 v.2	20070828	Product data sheet	-	74LVC2G66 v.1
74LVC2G66 v.1	20040629	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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