

74LVC27

Triple 3-input NOR gate

Rev. 6 — 27 October 2011

Product data sheet

1. General description

The 74LVC27 provides three 3-input NOR functions.

2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Complies with JEDEC standard:
 - ◆ JESD8-7A (1.65 V to 1.95 V)
 - ◆ JESD8-5A (2.3 V to 2.7 V)
 - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-B exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC27D	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVC27DB	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LVC27PW	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVC27BQ	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85\text{ mm}$	SOT762-1



4. Functional diagram

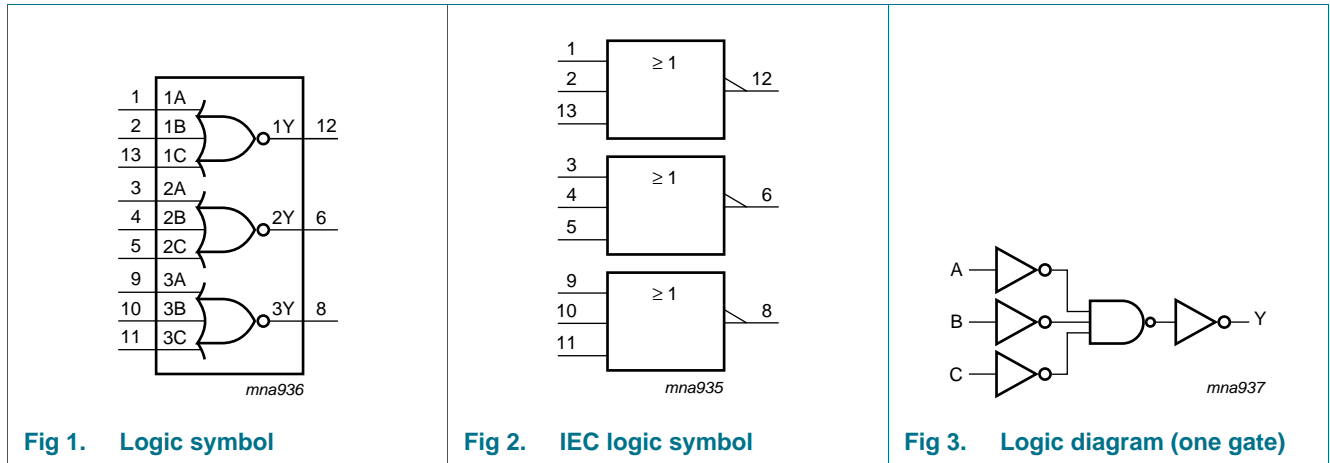


Fig 1. Logic symbol

Fig 2. IEC logic symbol

Fig 3. Logic diagram (one gate)

5. Pinning information

5.1 Pinning

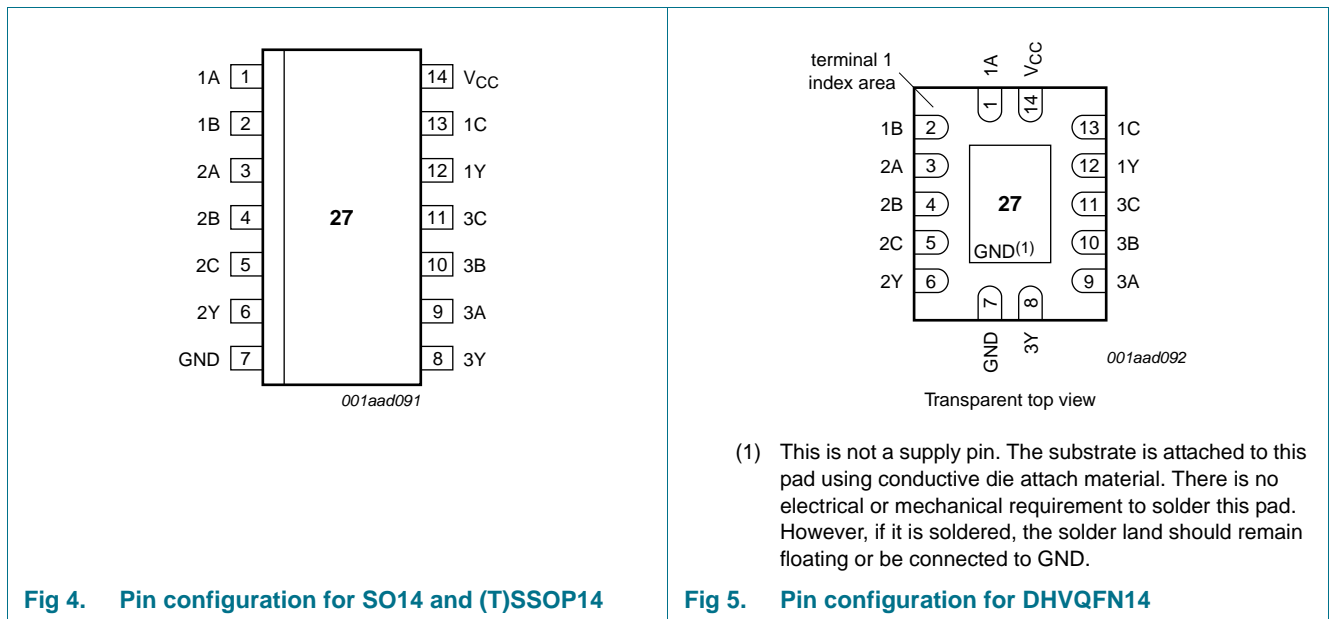


Fig 4. Pin configuration for SO14 and (T)SSOP14

Fig 5. Pin configuration for DHVQFN14

- (1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A	1, 3, 9	data input
1B, 2B, 3B	2, 4, 10	data input
1C, 2C, 3C	13, 5, 11	data input
1Y, 2Y, 3Y	12, 6, 8	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function selection^[1]

Input			Output
nA	nB	nC	nY
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0	-50	-	mA
V _I	input voltage		^[1] -0.5	+5.5	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0	-	±50	mA
V _O	output voltage		^[2] -0.5	V _{CC} + 0.5	V
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-60	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +85 °C	^[3] -	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO14 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
 For (T)SSOP14 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
 For DHVQFN14 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V _{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	0.65 × V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -100 μA; V _{CC} = 1.65 V to 3.6 V	V _{CC} - 0.2	-	-	V _{CC} - 0.3	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I _O = -18 mA; V _{CC} = 3.0 V	2.4	-	-	2.25	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 μA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V
I _I	input leakage current	V _{CC} = 3.6 V; V _I = 5.5 V or GND	-	±0.1	±5	-	±20	μA

Table 6. Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.1	10	-	40	μA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	500	-	5000	μA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC}	-	5.0	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	nA, nB, nC to nY; see Figure 6 ^[2]						
		V _{CC} = 1.65 V to 1.95 V	0.5	4.6	11.6	0.5	13.4	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	2.7	6.6	1.0	7.6	ns
		V _{CC} = 2.7 V	1.1	2.8	7.0	1.1	8.1	ns
		V _{CC} = 3.0 V to 3.6 V	0.8	2.4	5.9	0.8	6.8	ns
C _{PD}	power dissipation capacitance	per gate; V _I = GND to V _{CC} ^[3]						
		V _{CC} = 1.65 V to 1.95 V	-	3.3	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	6.4	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	9.2	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz; f_o = output frequency in MHz

C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

Σ(C_L × V_{CC}² × f_o) = sum of the outputs

11. AC waveforms

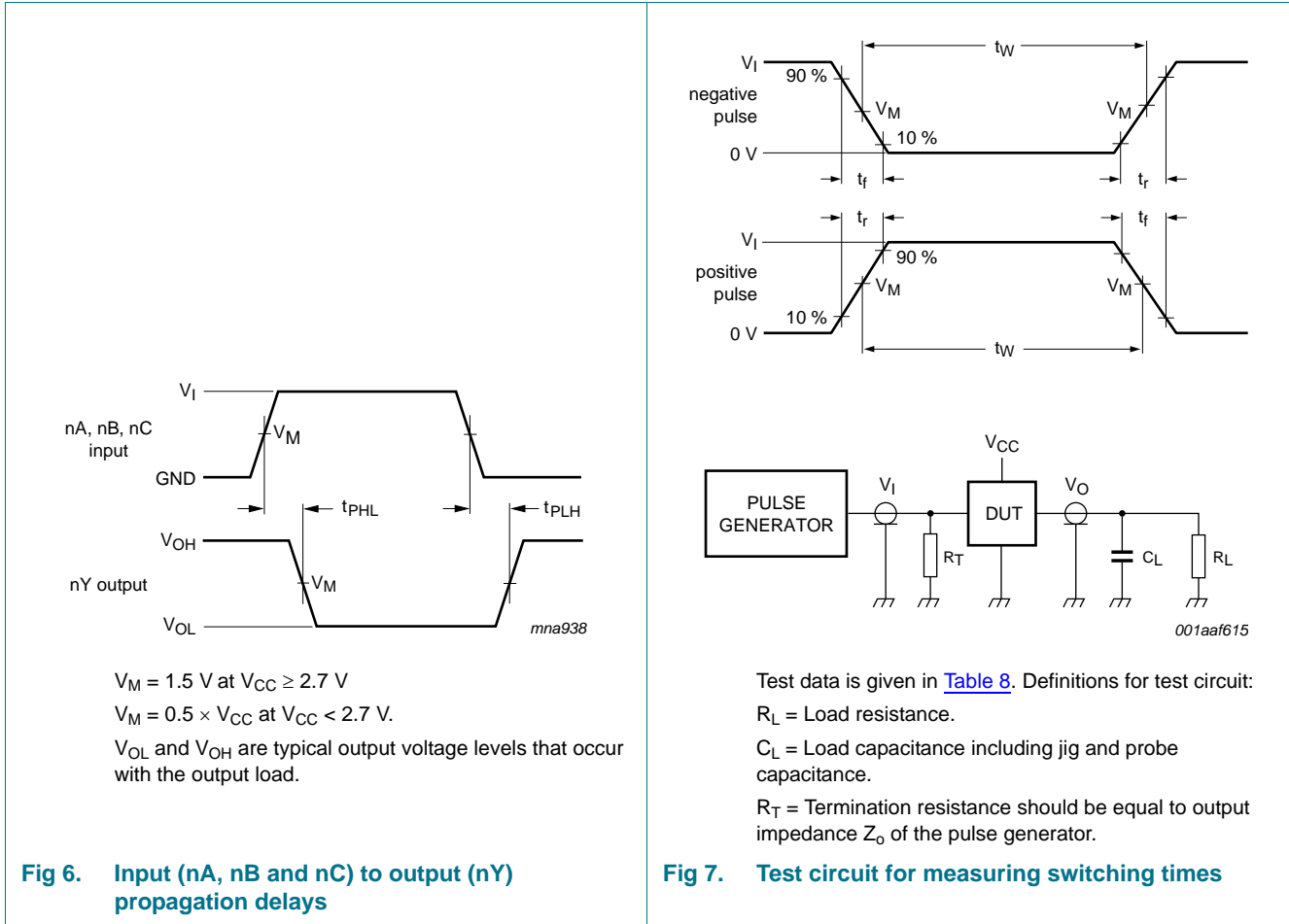


Table 8. Test data

Supply voltage	Input		Load	
	V_I	t_r, t_f	C_L	R_L
1.2 V	V_{CC}	$\leq 2 \text{ ns}$	30 pF	1 k Ω
1.65 V to 1.95 V	V_{CC}	$\leq 2 \text{ ns}$	30 pF	1 k Ω
2.3 V to 2.7 V	V_{CC}	$\leq 2 \text{ ns}$	30 pF	500 Ω
2.7 V	2.7 V	$\leq 2.5 \text{ ns}$	50 pF	500 Ω
3.0 V to 3.6 V	2.7 V	$\leq 2.5 \text{ ns}$	50 pF	500 Ω

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

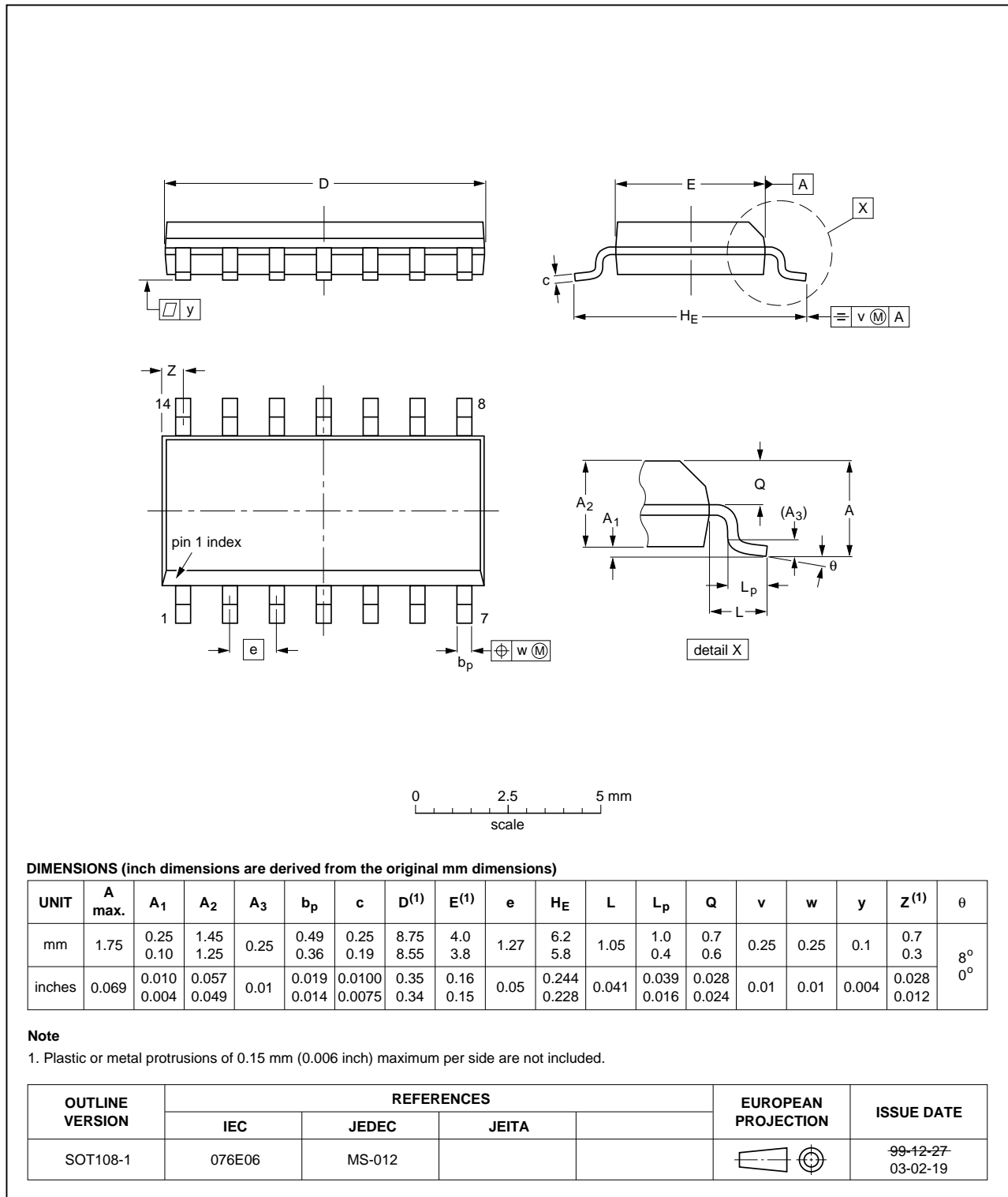


Fig 8. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

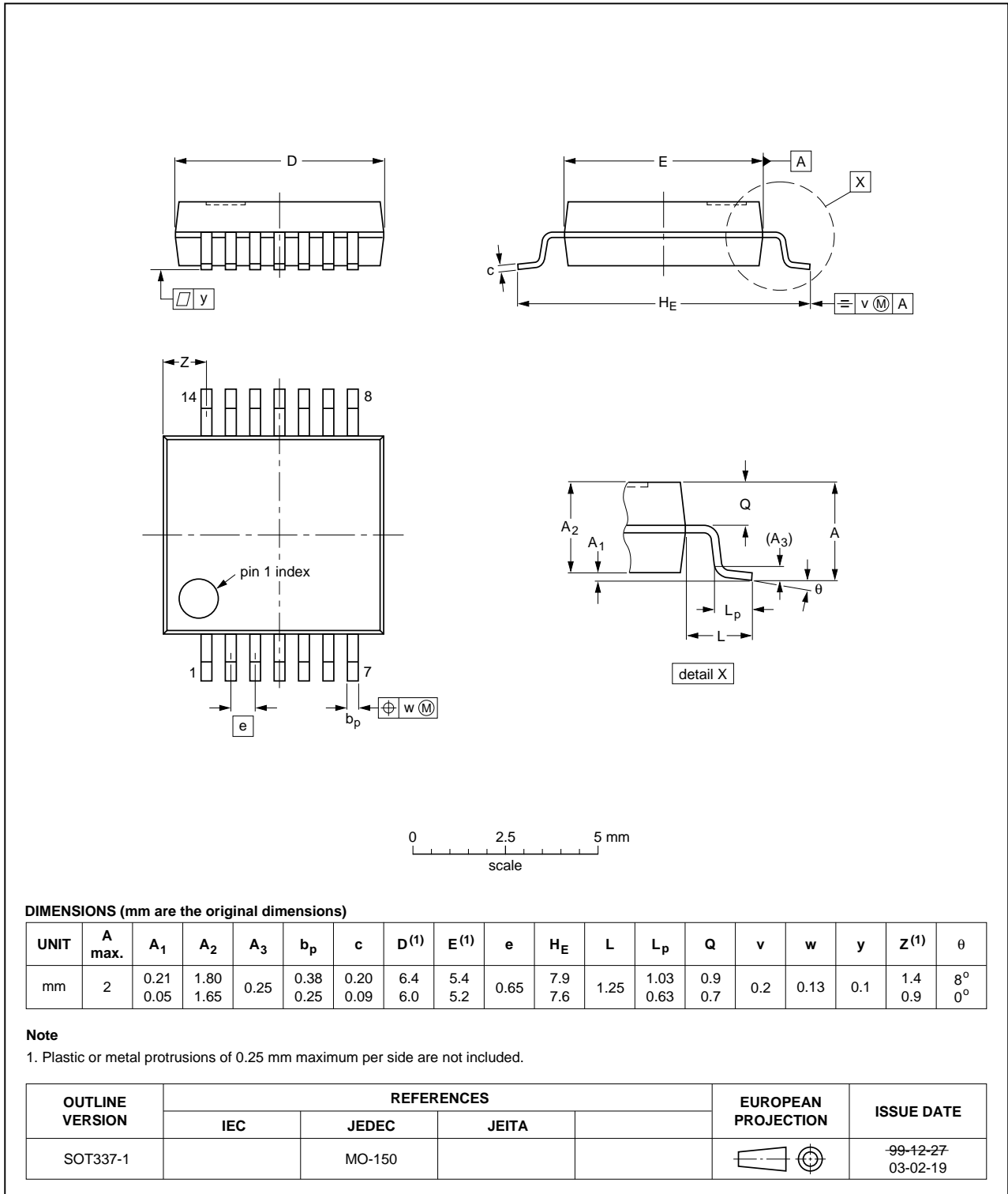


Fig 9. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

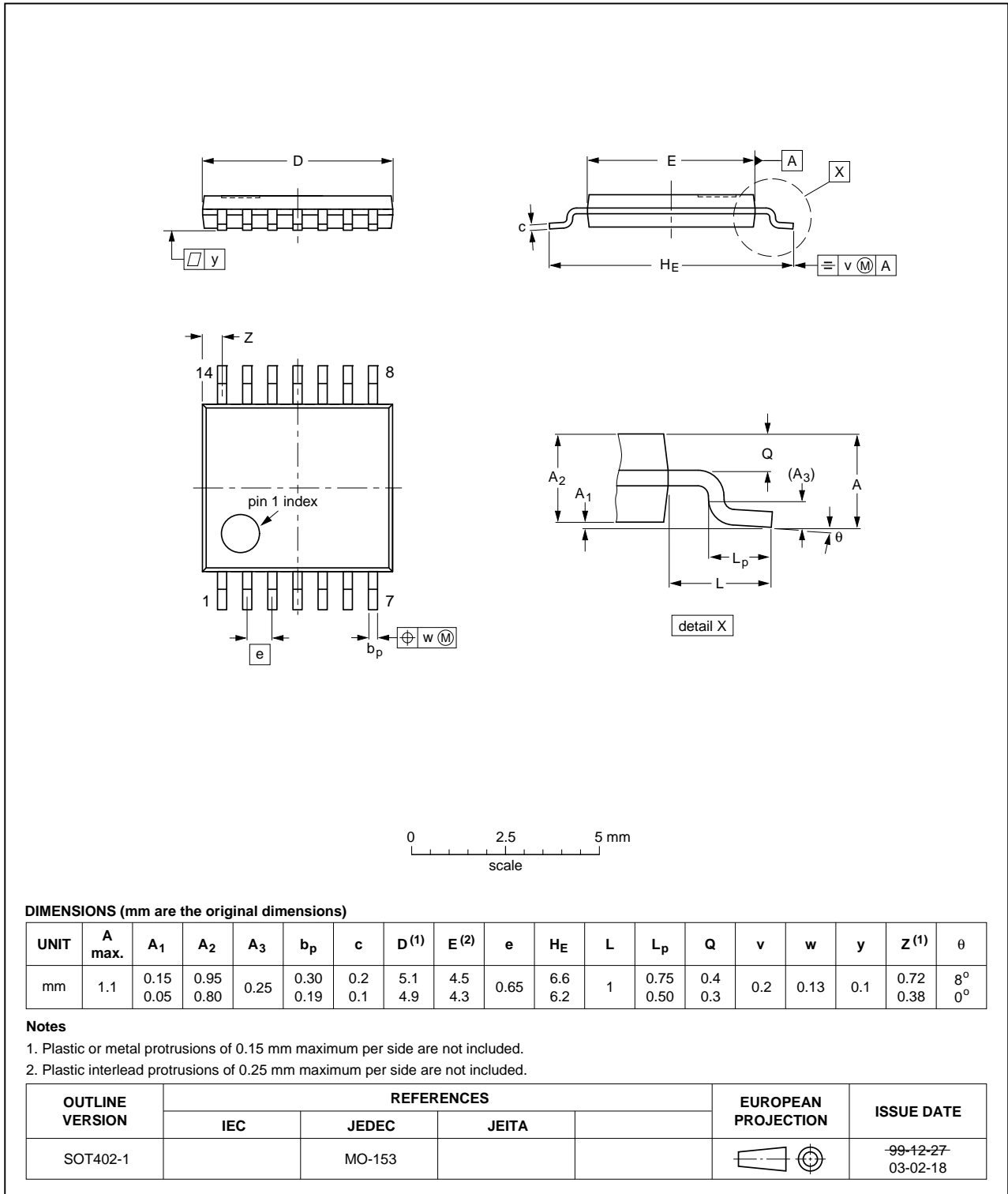


Fig 10. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

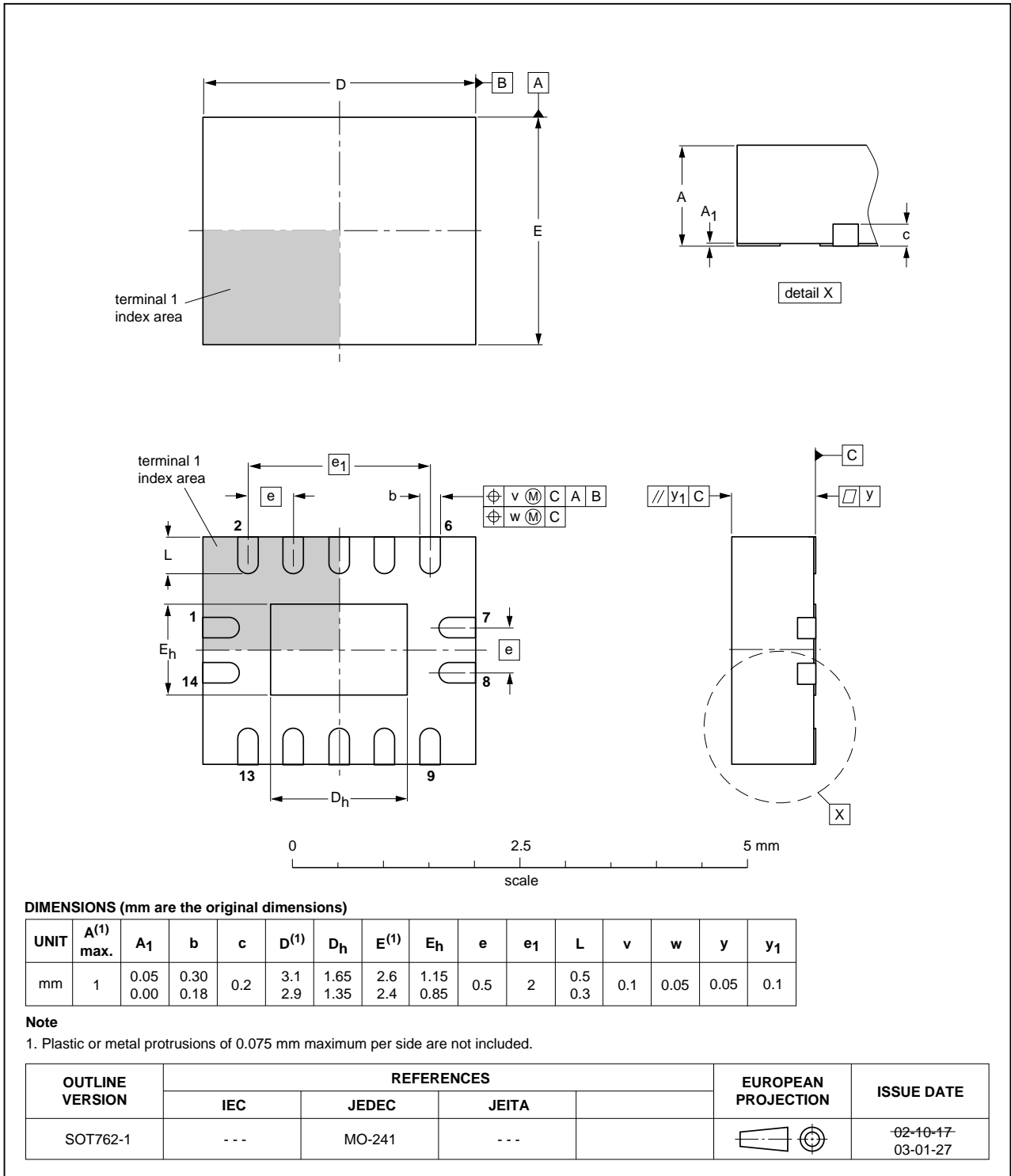


Fig 11. Package outline SOT762-1 (DHVQFN14)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC27 v.6	20111027	Product data sheet	-	74LVC27 v.5
Modifications:	<ul style="list-style-type: none"> • Table 7 : values added for lower voltage ranges. 			
74LVC27 v.5	20110909	Product data sheet	-	74LVC27 v.4
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 4, Table 5, Table 6, Table 7 and Table 8: values added for lower voltage ranges. 			
74LVC27 v.4	20040113	Product specification	-	74LVC27 v.3
74LVC27 v.3	19980428	Product specification	-	74LVC27 v.2
74LVC27 v.2	19980406	Product specification	-	74LVC27 v.1
74LVC27 v.1	-	-	-	-

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17. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	1
4	Functional diagram	2
5	Pinning information	2
5.1	Pinning	2
5.2	Pin description	3
6	Functional description	3
7	Limiting values	3
8	Recommended operating conditions	4
9	Static characteristics	4
10	Dynamic characteristics	5
11	AC waveforms	6
12	Package outline	7
13	Abbreviations	11
14	Revision history	11
15	Legal information	12
15.1	Data sheet status	12
15.2	Definitions	12
15.3	Disclaimers	12
15.4	Trademarks	13
16	Contact information	13
17	Contents	14

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