# THE DATASHEET OF

# STM32F101T4U6A

www.win-source.net 0086-755-83957316

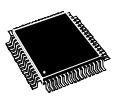
# STM32F101x4
# STM32F101x6

## Low-density access line, ARM®-based 32 bit MCU with 16 or 32 KB Flash, 5 timers, ADC and 4 communication interfaces

**Datasheet - production data**

## Features

- Core: ARM® 32-bit Cortex®-M3 CPU
  - 36 MHz maximum frequency, 1.25 DMIPS/MHz (Dhrystone 2.1) performance at 0 wait state memory access
  - Single-cycle multiplication and hardware division
- Memories
  - 16 to 32 Kbytes of Flash memory
  - 4 to 6 Kbytes of SRAM
- Clock, reset and supply management
  - 2.0 to 3.6 V application supply and I/Os
  - POR, PDR and programmable voltage detector (PVD)
  - 4-to-16 MHz crystal oscillator
  - Internal 8 MHz factory-trimmed RC
  - Internal 40 kHz RC
  - PLL for CPU clock
  - 32 kHz oscillator for RTC with calibration
- Low power
  - Sleep, Stop and Standby modes
  - $V_{BAT}$ supply for RTC and backup registers
- Debug mode
  - Serial wire debug (SWD) and JTAG interfaces
- DMA
  - 7-channel DMA controller
  - Peripherals supported: timers, ADC, SPIs, $I^2C$s and USARTs
- 1 × 12-bit, 1 µs A/D converter (up to 16 channels)
  - Conversion range: 0 to 3.6 V
  - Temperature sensor
- Up to 51 fast I/O ports
  - 26/37/51 I/Os, all mappable on 16 external interrupt vectors and almost all 5 V-tolerant



LQFP64
10 x 10 mm

LQFP48
7 x 7 mm

VFQFPN36
6 × 6 mm

- Up to 5 timers
  - Up to two16-bit timers, each with up to 4 IC/OC/PWM or pulse counter
  - 2 watchdog timers (Independent and Window)
  - SysTick timer: 24-bit downcounter
- Up to 4 communication interfaces
  - 1 x $I^2C$ interface (SMBus/PMBus)
  - Up to 2 USARTs (ISO 7816 interface, LIN, IrDA capability, modem control)
  - 1 × SPI (18 Mbit/s)
- CRC calculation unit, 96-bit unique ID
- ECOPACK® packages

**Table 1. Device summary**

| Reference | Part number |
|---|---|
| STM32F101x4 | STM32F101C4, STM32F101R4, STM32F101T4 |
| STM32F101x6 | STM32F101C6, STM32F101R6, STM32F101T6 |



This is information on a product in full production. www.st.com

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# 1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F101x4 and STM32F101x6 low-density access line microcontrollers. For more details on the whole STMicroelectronics STM32F101xx family, please refer to *Section 2.2: Full compatibility throughout the family*.

The Low-density STM32F101xx datasheet should be read in conjunction with the low-, medium- and high-density STM32F10xxx reference manual.
For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10xxx Flash programming manual.*
The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the www.arm.com website.

# 2 Description

The STM32F101x4 and STM32F101x6 Low-density access line family incorporates the high-performance ARM Cortex®-M3 32-bit RISC core operating at a 36 MHz frequency, high-speed embedded memories (Flash memory of 16 to 32 Kbytes and SRAM of 4 to 6 Kbytes), and an extensive range of enhanced peripherals and I/Os connected to two APB buses. All devices offer standard communication interfaces (one $I^2C$, one SPI, and two USARTs), one 12-bit ADC and up to two general-purpose 16-bit timers.

The STM32F101xx Low-density access line family operates in the –40 to +85 °C temperature range, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F101xx Low-density access line family includes devices in three different packages ranging from 36 pins to 64 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F101xx Low-density access line microcontroller family suitable for a wide range of applications such as application control and user interface, medical and handheld equipment, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, Video intercoms, and HVACs.

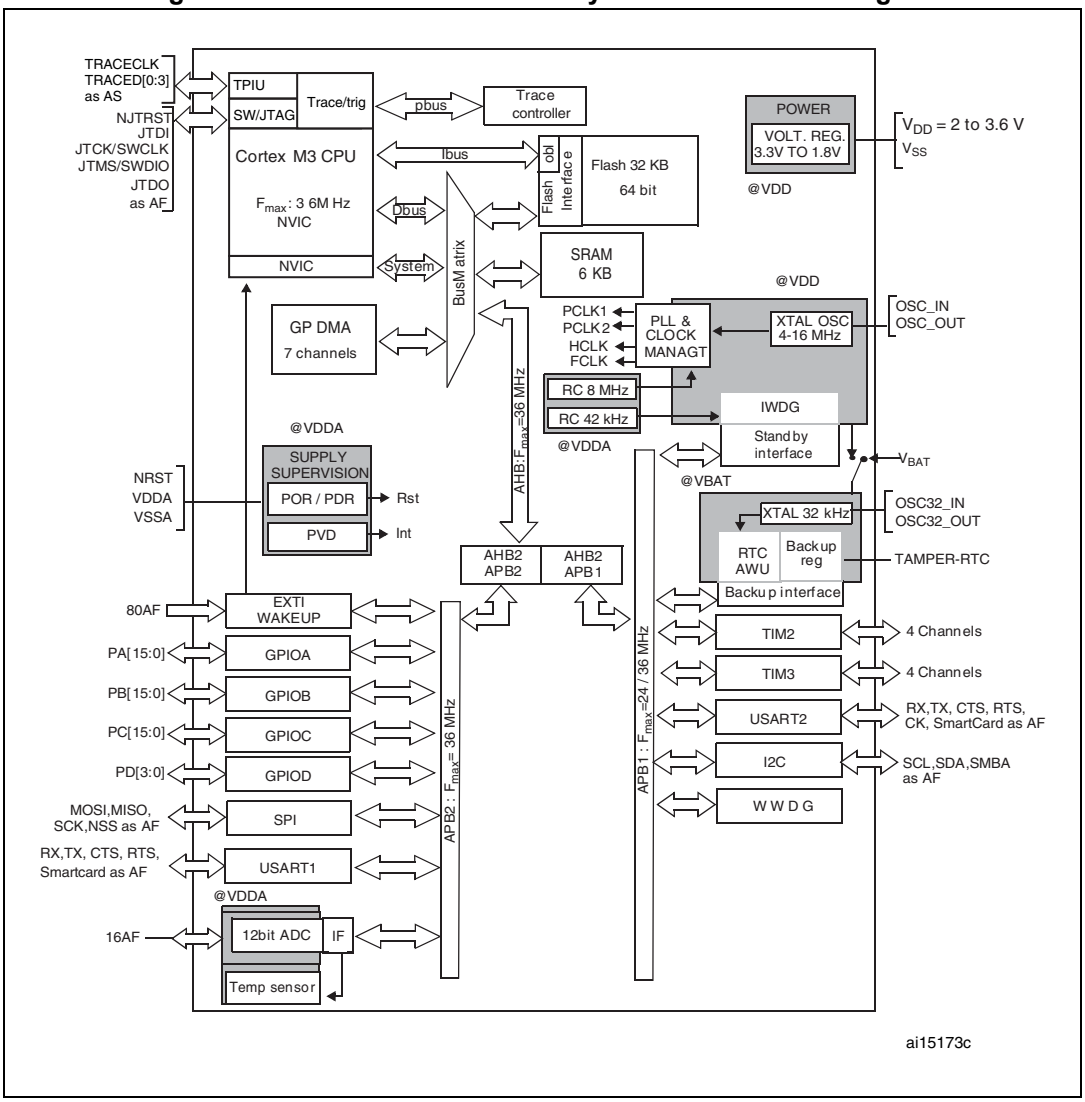
## 2.1 Device overview

*Figure 1* shows the general block diagram of the device family.

**Table 2. Low-density STM32F101xx device features and peripheral counts**

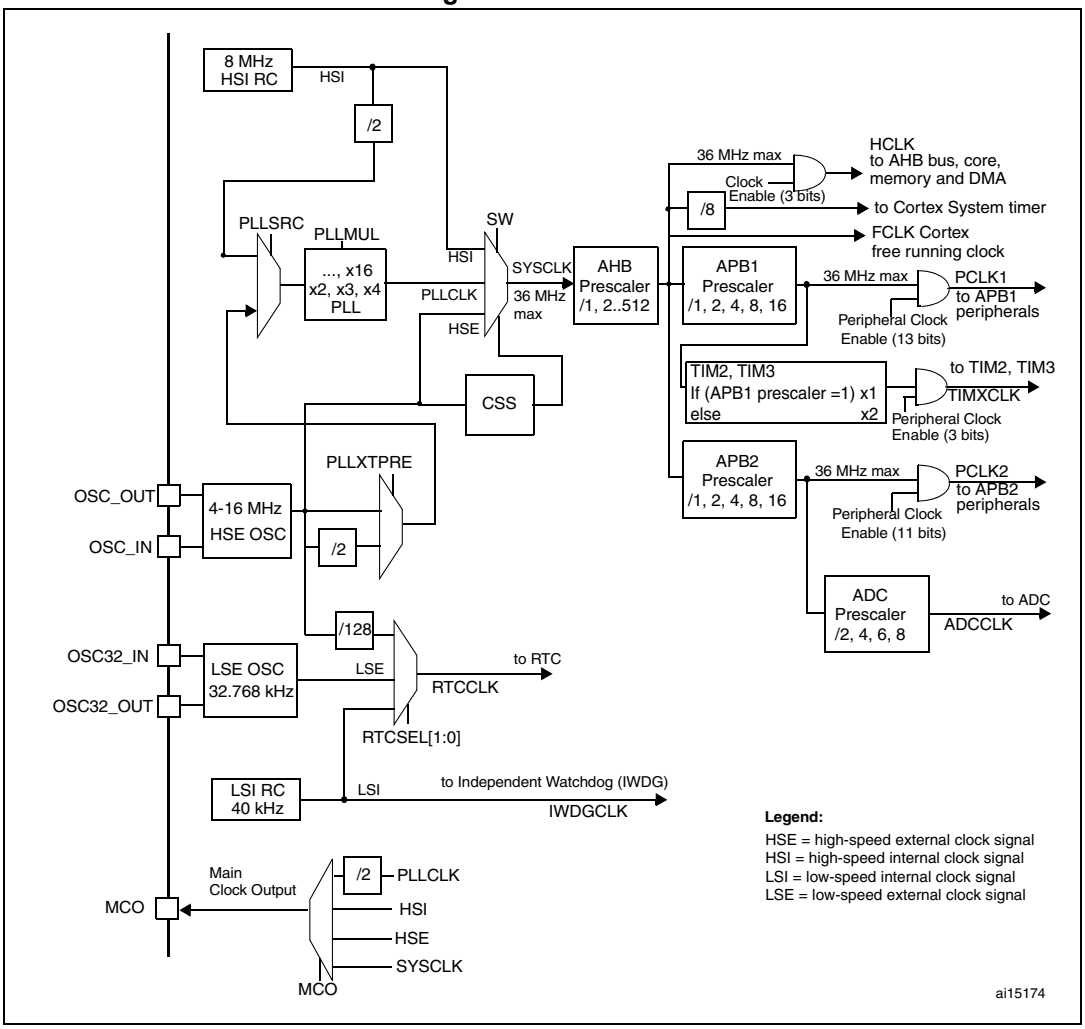
| Peripheral | | STM32F101Tx | | STM32F101Cx | | STM32F101Rx | |
|---|---|---|---|---|---|---|---|
| Flash - Kbytes | | 16 | 32 | 16 | 32 | 16 | 32 |
| SRAM - Kbytes | | 4 | 6 | 4 | 6 | 4 | 6 |
| Timers | General-purpose | 2 | 2 | 2 | 2 | 2 | 2 |
| Communication | SPI | 1 | 1 | 1 | 1 | 1 | 1 |
| | $I^2C$ | 1 | 1 | 1 | 1 | 1 | 1 |
| | USART | 2 | 2 | 2 | 2 | 2 | 2 |
| 12-bit synchronized ADC number of channels | | 1<br>10 channels | | 1<br>10 channels | | 1<br>16 channels | |
| GPIOs | | 26 | | 37 | | 51 | |
| CPU frequency | | 36 MHz | | | | | |
| Operating voltage | | 2.0 to 3.6 V | | | | | |
| Operating temperatures | | Ambient temperature: –40 to +85 °C (see *Table 8*)<br>Junction temperature: –40 to +105 °C (see *Table 8*) | | | | | |
| Packages | | VFQFPN36 | | LQFP48 | | LQFP64 | |

**Figure 1. STM32F101xx Low-density access line block diagram**




1. AF = alternate function on I/O port pin.
2. $T_A$ = –40 °C to +85 °C (junction temperature up to 105 °C).

**Figure 2. Clock tree**




1. When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 36 MHz.
2. To have an ADC conversion time of 1 µs, APB2 must be at 14 MHz or 28 MHz.

## 2.2 Full compatibility throughout the family

The STM32F101xx is a complete family whose members are fully pin-to-pin, software and feature compatible. In the reference manual, the STM32F101x4 and STM32F101x6 are referred to as low-density devices, the STM32F101x8 and STM32F101xB are referred to as medium-density devices, and the STM32F101xC, STM32F101xD and STM32F101xE are referred to as high-density devices.

Low- and high-density devices are an extension of the STM32F101x8/B devices, they are specified in the STM32F101x4/6 and STM32F101xC/D/E datasheets, respectively. Low-density devices feature lower Flash memory and RAM capacities and a timer less. High-density devices have higher Flash memory and RAM capacities, and additional peripherals like FSMC and DAC, while remaining fully compatible with the other members of the STM32F101xx family.
The STM32F101x4, STM32F101x6, STM32F101xC, STM32F101xD and STM32F101xE are a drop-in replacement for the STM32F101x8/B medium-density devices, allowing the user to try different memory densities and providing a greater degree of freedom during the development cycle.

Moreover, the STM32F101xx performance line family is fully compatible with all existing STM32F101xx access line and STM32F102xx USB access line devices.

**Table 3. STM32F101xx family**

<table>
<tr><th rowspan="3">Pinout</th><th colspan="7">Memory size</th></tr>
<tr><th colspan="2">Low-density devices</th><th colspan="2">Medium-density devices</th><th colspan="3">High-density devices</th></tr>
<tr><th>16 KB Flash</th><th>32 KB Flash(1)</th><th>64 KB Flash</th><th>128 KB Flash</th><th>256 KB Flash</th><th>384 KB Flash</th><th>512 KB Flash</th></tr>
<tr><th></th><th>4 KB RAM</th><th>6 KB RAM</th><th>10 KB RAM</th><th>16 KB RAM</th><th>32 KB RAM</th><th>48 KB RAM</th><th>48 KB RAM</th></tr>
<tr><td>144</td><td>-</td><td>-</td><td>-</td><td>-</td><td colspan="3" rowspan="2">5 × USARTs<br>4 × 16-bit timers, 2 × basic timers<br>3 × SPIs, 2 × I2Cs, 1 × ADC,<br>2 × DACs, FSMC (100 and 144 pins)</td></tr>
<tr><td>100</td><td>-</td><td>-</td><td colspan="3" rowspan="3">3 × USARTs<br>3 × 16-bit timers<br>2 × SPIs, 2 × I2Cs,<br>1 × ADC</td></tr>
<tr><td>64</td><td colspan="2" rowspan="3">2 × USARTs<br>2 × 16-bit timers<br>1 × SPI, 1 × I2C<br>1 × ADC</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>48</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>36</td><td>-</td><td>-</td><td>-</td></tr>
</table>

1. For orderable part numbers that do not show the A internal code after the temperature range code (6), the reference datasheet for electrical characteristics is that of the STM32F101x8/B medium-density devices.

## 2.3 Overview

### 2.3.1 ARM® Cortex® -M3 core with embedded Flash and SRAM

The ARM® Cortex®-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex®-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F101xx Low-density access line family having an embedded ARM core, is therefore compatible with all ARM tools and software.

### 2.3.2 Embedded Flash memory

16 or 32 Kbytes of embedded Flash is available for storing programs and data.

### 2.3.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

### 2.3.4 Embedded SRAM

Up to 6 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

### 2.3.5 Nested vectored interrupt controller (NVIC)

The STM32F101xx Low-density access line embeds a nested vectored interrupt controller able to handle up to 43 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

### 2.3.6 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 80 GPIOs can be connected to the 16 external interrupt lines.

### 2.3.7 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 36 MHz. See *Figure 2* for details on the clock tree.

### 2.3.8 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1. For further details please refer to AN2606.

### 2.3.9 Power supply schemes

- $V_{DD}$ = 2.0 to 3.6 V: External power supply for I/Os and the internal regulator. Provided externally through $V_{DD}$ pins.
- $V_{SSA}$, $V_{DDA}$ = 2.0 to 3.6 V: External analog power supplies for ADC, Reset blocks, RCs and PLL (minimum voltage to be applied to $V_{DDA}$ is 2.4 V when the ADC is used). $V_{DDA}$ and $V_{SSA}$ must be connected to $V_{DD}$ and $V_{SS}$, respectively.
- $V_{BAT}$ = 1.8 to 3.6 V: Power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when $V_{DD}$ is not present.

For more details on how to connect power pins, refer to *Figure 10: Power supply scheme*.

### 2.3.10 Power supply supervisor

The device has an integrated power on reset (POR)/power down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when $V_{DD}$ is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the $V_{DD}/V_{DDA}$ power supply and compares it to the $V_{PVD}$ threshold. An interrupt can be generated when $V_{DD}/V_{DDA}$ drops below the $V_{PVD}$ threshold and/or when $V_{DD}/V_{DDA}$ is

higher than the $V_{PVD}$ threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

Refer to *Table 10: Embedded reset and power control block characteristics* for the values of $V_{POR/PDR}$ and $V_{PVD}$.

### 2.3.11 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop mode
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode, providing high impedance output.

### 2.3.12 Low-power modes

The STM32F101xx Low-density access line supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop** mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.
  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output or the RTC alarm.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), a IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

*Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.*

### 2.3.13 DMA

The flexible 7-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, $I^2C$, USART, general purpose timers TIMx and ADC.

### 2.3.14 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on $V_{DD}$ supply when present or through the $V_{BAT}$ pin. The backup registers are ten 16-bit registers used to store 20 bytes of user application data when $V_{DD}$ power is not present.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the high-speed external clock divided by 128. The internal low power RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural crystal deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

### 2.3.15 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

### 2.3.16 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

### 2.3.17 SysTick timer

This timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

### 2.3.18 General-purpose timers (TIMx)

There areup to two  synchronizable general-purpose timers embedded in the STM32F101xx Low-density access line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture,

output compare, PWM or one pulse mode output. This gives up to 12 input captures / output compares / PWMs on the largest packages.
The general-purpose timers can work together via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

### 2.3.19 I²C bus

The I²C bus interface can operate in multimaster and slave modes. It can support standard and fast modes.

It supports dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.
The interface can be served by DMA and it supports SM Bus 2.0/PM Bus.

### 2.3.20 Universal synchronous/asynchronous receiver transmitter (USART)

The available USART interfaces communicate at up to 2.25 Mbit/s. They provide hardware management of the CTS and RTS signals, support IrDA SIR ENDEC, are ISO 7816 compliant and have LIN Master/Slave capability.

The USART interfaces can be served by the DMA controller.

### 2.3.21 Serial peripheral interface (SPI)

The SPI interface is able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The SPI interface can be served by the DMA controller.

### 2.3.22 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

### 2.3.23 ADC (analog to digital converter)

The 12-bit analog to digital converter has up to 16 external channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

### 2.3.24 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < $V_{DDA}$ < 3.6 V. The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

### 2.3.25 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

# 3 Pinouts and pin description

**Figure 3. STM32F101xx Low-density access line LQFP64 pinout**

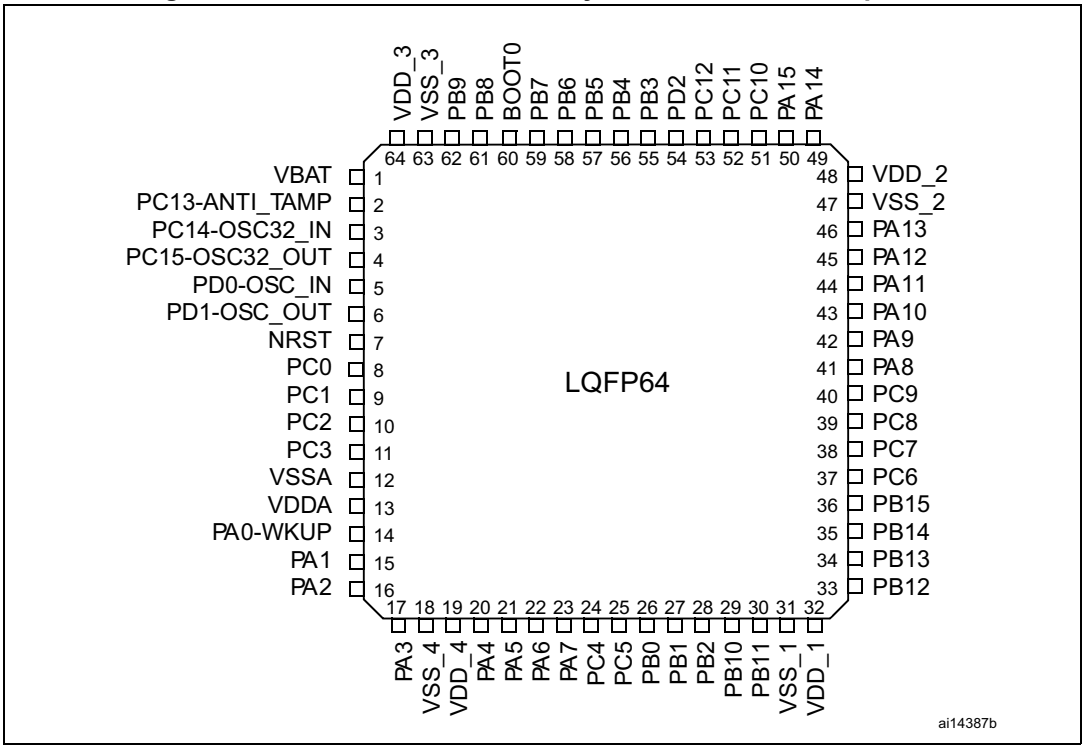



**Figure 4. STM32F101xx Low-density access line LQFP48 pinout**

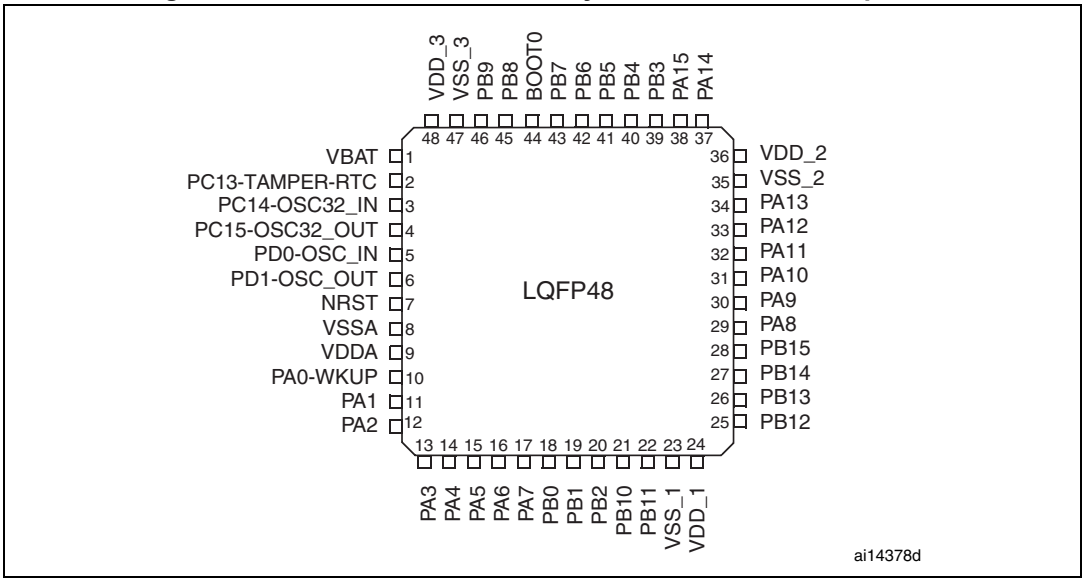


**Figure 5. STM32F101xx Low-density access line UFQPFN48 pinout**

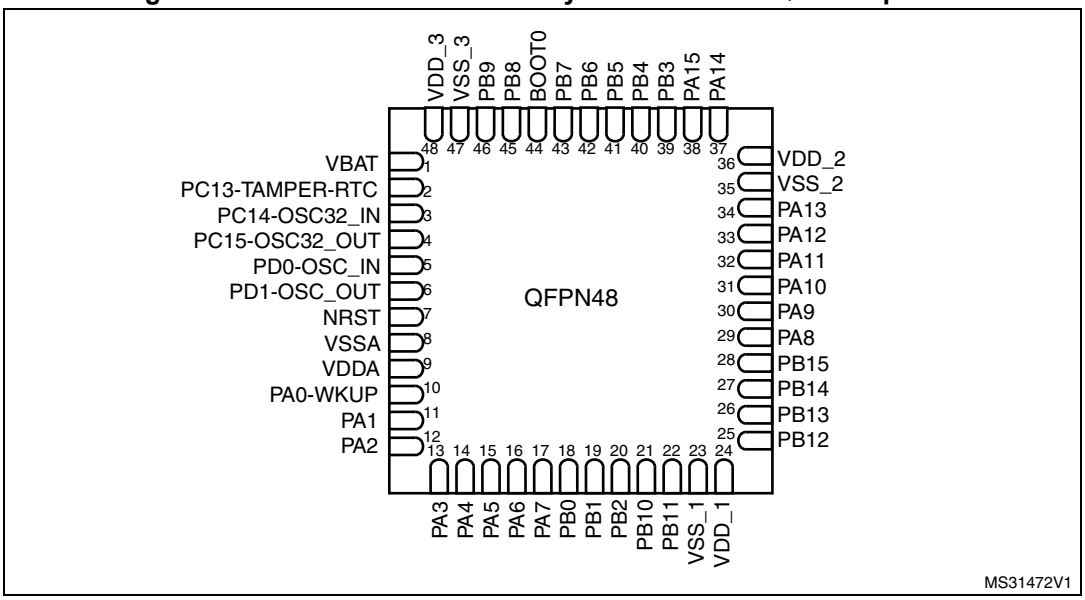



**Figure 6. STM32F101xx Low-density access line VFQPFN36 pinout**

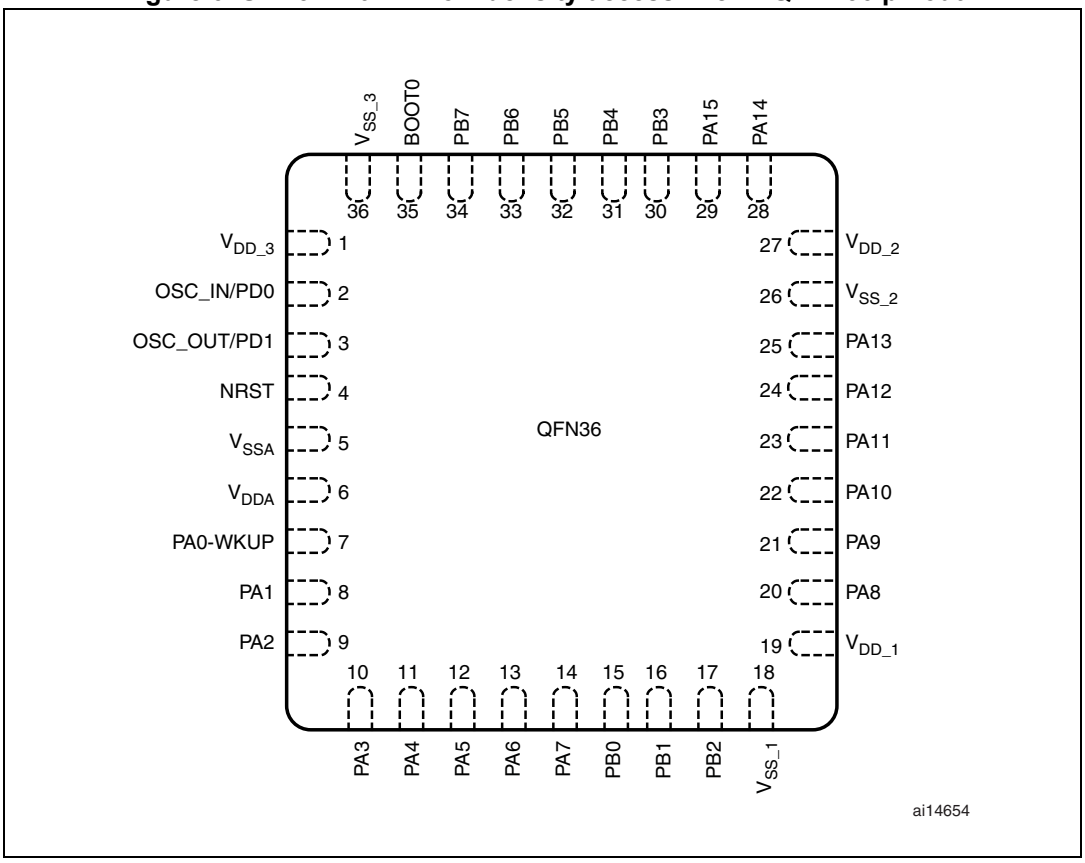


**Table 4. Low-density STM32F101xx pin definitions**

| Pins | | | Pin name | Type[1] | I / O level[2] | Main function[3] (after reset) | Alternate functions[3][4] | |
|---|---|---|---|---|---|---|---|---|
| LQFP48 | LQFP64 | VFQFPN36 | | | | | Default | Remap |
| 1 | 1 | - | $V_{BAT}$ | S | - | $V_{BAT}$ | - | - |
| 2 | 2 | - | PC13-TAMPER-RTC[5] | I/O | - | PC13[6] | TAMPER-RTC | - |
| 3 | 3 | - | PC14-OSC32_IN[5] | I/O | - | PC14[6] | OSC32_IN | - |
| 4 | 4 | - | PC15-OSC32_OUT[5] | I/O | - | PC15[6] | OSC32_OUT | - |
| 5 | 5 | 2 | OSC_IN | I | - | OSC_IN | - | - |
| 6 | 6 | 3 | OSC_OUT | O | - | OSC_OUT | - | - |
| 7 | 7 | 4 | NRST | I/O | - | NRST | - | - |
| - | 8 | - | PC0 | I/O | - | PC0 | ADC_IN10 | - |
| - | 9 | - | PC1 | I/O | - | PC1 | ADC_IN11 | - |
| - | 10 | - | PC2 | I/O | - | PC2 | ADC_IN12 | - |
| - | 11 | - | PC3 | I/O | - | PC3 | ADC_IN13 | - |
| 8 | 12 | 5 | $V_{SSA}$ | S | - | $V_{SSA}$ | - | - |
| 9 | 13 | 6 | $V_{DDA}$ | S | - | $V_{DDA}$ | - | - |
| 10 | 14 | 7 | PA0-WKUP | I/O | - | PA0 | WKUP/USART2_CTS/ ADC_IN0/ TIM2_CH1_ETR[7] | - |
| 11 | 15 | 8 | PA1 | I/O | - | PA1 | USART2_RTS/ ADC_IN1/TIM2_CH2[7] | - |
| 12 | 16 | 9 | PA2 | I/O | - | PA2 | USART2_TX/ ADC_IN2/TIM2_CH3[7] | - |
| 13 | 17 | 10 | PA3 | I/O | - | PA3 | USART2_RX/ ADC_IN3/TIM2_CH4[7] | - |
| - | 18 | - | $V_{SS_4}$ | S | - | $V_{SS_4}$ | - | - |
| - | 19 | - | $V_{DD_4}$ | S | - | $V_{DD_4}$ | - | - |
| 14 | 20 | 11 | PA4 | I/O | - | PA4 | SPI_NSS[7]/ADC_IN4 USART2_CK | - |
| 15 | 21 | 12 | PA5 | I/O | - | PA5 | SPI_SCK[7]/ADC_IN5 | - |
| 16 | 22 | 13 | PA6 | I/O | - | PA6 | SPI_MISO[7]/ADC_IN6/ TIM3_CH1[7] | - |

Table 4. Low-density STM32F101xx pin definitions (continued)

| Pins | | | Pin name | Type[1] | I / O level[2] | Main function[3] (after reset) | Alternate functions[3][4] | |
|---|---|---|---|---|---|---|---|---|
| LQFP48 | LQFP64 | VFQFPN36 | | | | | Default | Remap |
| 17 | 23 | 14 | PA7 | I/O | - | PA7 | SPI_MOSI[7]/ADC_IN7/ TIM3_CH2[7] | - |
| - | 24 | - | PC4 | I/O | - | PC4 | ADC_IN14 | - |
| - | 25 | - | PC5 | I/O | - | PC5 | ADC_IN15 | - |
| 18 | 26 | 15 | PB0 | I/O | - | PB0 | ADC_IN8/TIM3_CH3[7] | - |
| 19 | 27 | 16 | PB1 | I/O | - | PB1 | ADC_IN9/TIM3_CH4[7] | - |
| 20 | 28 | 17 | PB2 | I/O | FT | PB2/BOOT1 | - | - |
| 21 | 29 | - | PB10 | I/O | FT | PB10 | - | TIM2_CH3 |
| 22 | 30 | - | PB11 | I/O | FT | PB11 | - | TIM2_CH4 |
| 23 | 31 | 18 | $V_{SS_1}$ | S | - | $V_{SS_1}$ | - | - |
| 24 | 32 | 19 | $V_{DD_1}$ | S | - | $V_{DD_1}$ | - | - |
| 25 | 33 | - | PB12 | I/O | FT | PB12 | - | - |
| 26 | 34 | - | PB13 | I/O | FT | PB13 | - | - |
| 27 | 35 | - | PB14 | I/O | FT | PB14 | - | - |
| 28 | 36 | - | PB15 | I/O | FT | PB15 | - | - |
| - | 37 | - | PC6 | I/O | FT | PC6 | - | TIM3_CH1 |
| - | 38 | - | PC7 | I/O | FT | PC7 | - | TIM3_CH2 |
| - | 39 | - | PC8 | I/O | FT | PC8 | - | TIM3_CH3 |
| - | 40 | - | PC9 | I/O | FT | PC9 | - | TIM3_CH4 |
| 29 | 41 | 20 | PA8 | I/O | FT | PA8 | USART1_CK/MCO | - |
| 30 | 42 | 21 | PA9 | I/O | FT | PA9 | USART1_TX[7] | - |
| 31 | 43 | 22 | PA10 | I/O | FT | PA10 | USART1_RX[7] | - |
| 32 | 44 | 23 | PA11 | I/O | FT | PA11 | USART1_CTS | - |
| 33 | 45 | 24 | PA12 | I/O | FT | PA12 | USART1_RTS | - |
| 34 | 46 | 25 | PA13 | I/O | FT | JTMS-SWDIO | - | PA13 |
| 35 | 47 | 26 | $V_{SS_2}$ | S | - | $V_{SS_2}$ | - | - |
| 36 | 48 | 27 | $V_{DD_2}$ | S | - | $V_{DD_2}$ | - | - |

**Table 4. Low-density STM32F101xx pin definitions (continued)**

| Pins | | | Pin name | Type[1] | I / O level[2] | Main function[3] (after reset) | Alternate functions[3][4] | |
|---|---|---|---|---|---|---|---|---|
| LQFP48 | LQFP64 | VFQFPN36 | | | | | Default | Remap |
| 37 | 49 | 28 | PA14 | I/O | FT | JTCK/SWCLK | - | PA14 |
| 38 | 50 | 29 | PA15 | I/O | FT | JTDI | - | TIM2_CH1_ETR/ PA15 / SPI_NSS |
| - | 51 | - | PC10 | I/O | FT | PC10 | - | - |
| - | 52 | - | PC11 | I/O | FT | PC11 | - | - |
| - | 53 | - | PC12 | I/O | FT | PC12 | - | - |
| 5 | 5 | 2 | PD0 | I/O | FT | OSC_IN[8] | - | - |
| 6 | 6 | 3 | PD1 | I/O | FT | OSC_OUT[8] | - | - |
| - | 54 | - | PD2 | I/O | FT | PD2 | TIM3_ETR | - |
| 39 | 55 | 30 | PB3 | I/O | FT | JTDO | - | TIM2_CH2 / PB3 TRACESWO SPI_SCK |
| 40 | 56 | 31 | PB4 | I/O | FT | NJTRST | - | TIM3_CH1 / PB4 SPI_MISO |
| 41 | 57 | 32 | PB5 | I/O | - | PB5 | I2C_SMBA | TIM3_CH2 / SPI_MOSI |
| 42 | 58 | 33 | PB6 | I/O | FT | PB6 | I2C_SCL[7] | USART1_TX |
| 43 | 59 | 34 | PB7 | I/O | FT | PB7 | I2C_SDA[7] | USART1_RX |
| 44 | 60 | 35 | BOOT0 | I | - | BOOT0 | - | - |
| 45 | 61 | - | PB8 | I/O | FT | PB8 | - | I2C_SCL |
| 46 | 62 | - | PB9 | I/O | FT | PB9 | - | I2C_SDA |
| 47 | 63 | 36 | $V_{SS_3}$ | S | - | $V_{SS_3}$ | - | - |
| 48 | 64 | 1 | $V_{DD_3}$ | S | - | $V_{DD_3}$ | - | - |

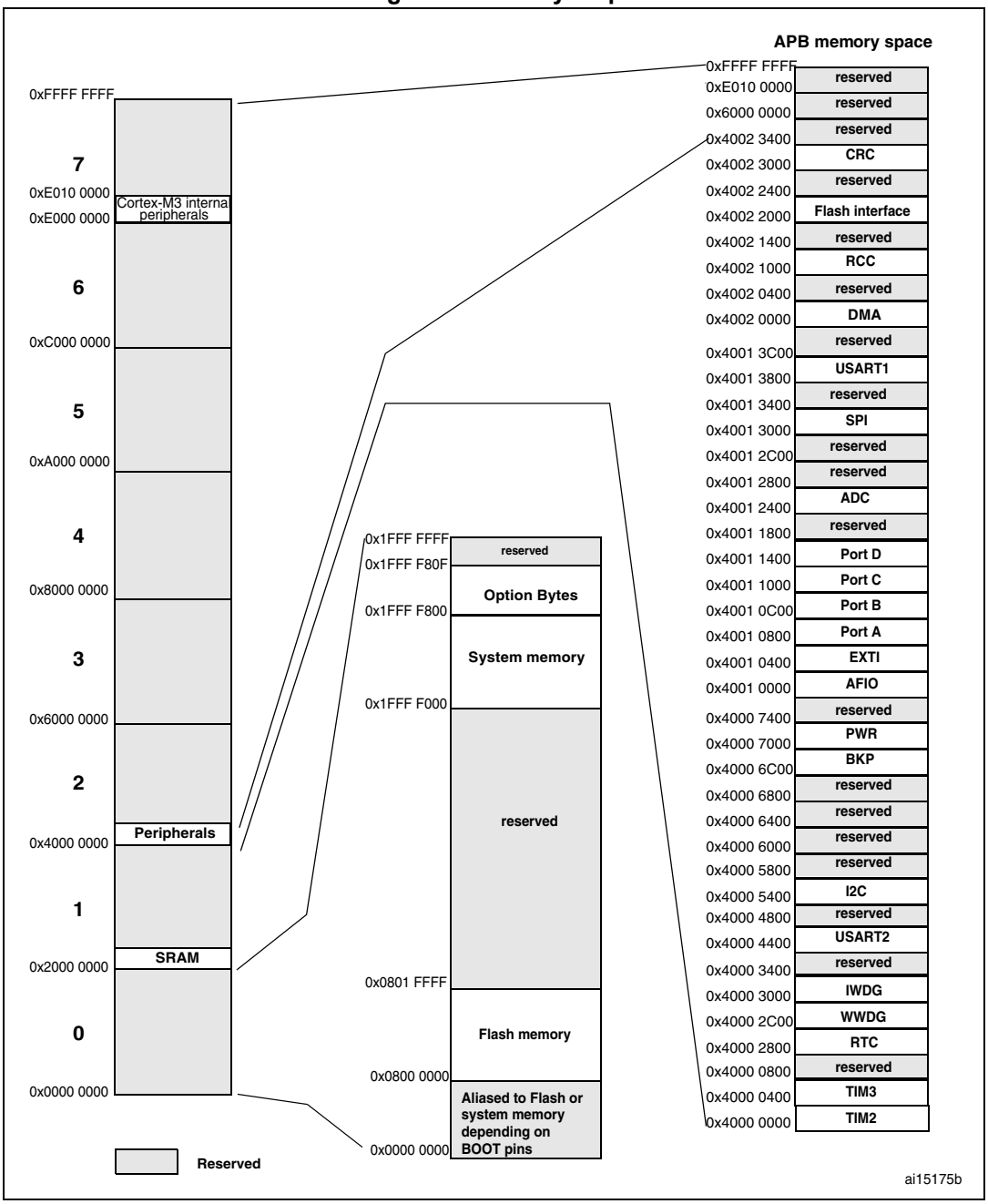
1. I = input, O = output, S = supply.
2. FT= 5 V tolerant.
3. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripherals that is included. For example, if a device has only one SPI, two USARTs and two timers, they will be called SPI, USART1 & USART2 and TIM2 & TIM 3, respectively. Refer to *Table 2 on page 11*.
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).

6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
7. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
8. The pins number 2 and 3 in the VFQFPN36 package, and 5 and 6 in the LQFP48 and LQFP64 packages are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.

# 4 Memory mapping

The memory map is shown in *Figure 7*.

**Figure 7. Memory map**



# 5 Electrical characteristics

## 5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to $V_{SS}$.

### 5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A$ = 25 °C and $T_A$ = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

### 5.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A$ = 25 °C, $V_{DD}$ = 3.3 V (for the 2 V ≤ $V_{DD}$ ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

### 5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

### 5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

### 5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

**Figure 8. Pin loading conditions**

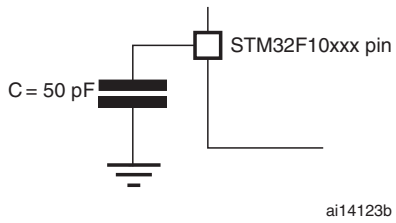
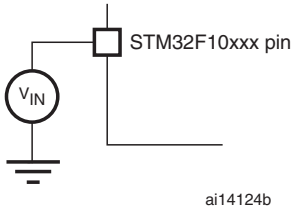
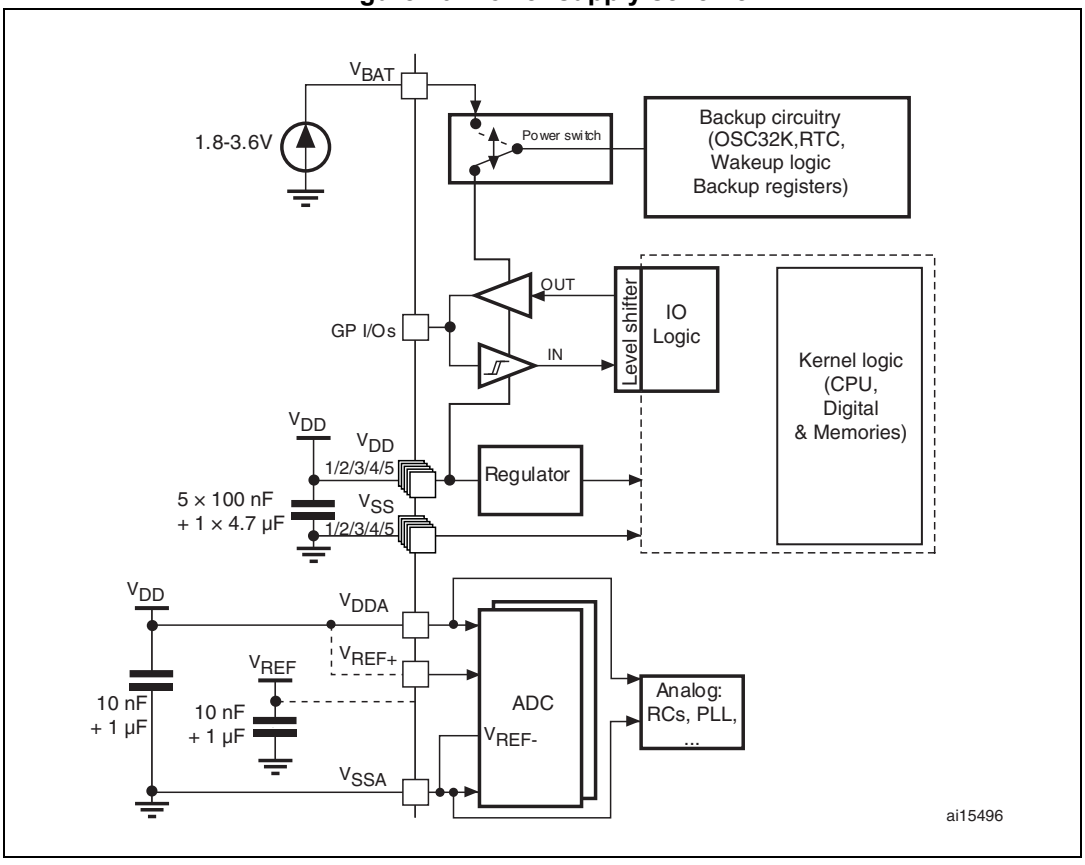



**Figure 9. Pin input voltage**




## 5.1.6 Power supply scheme

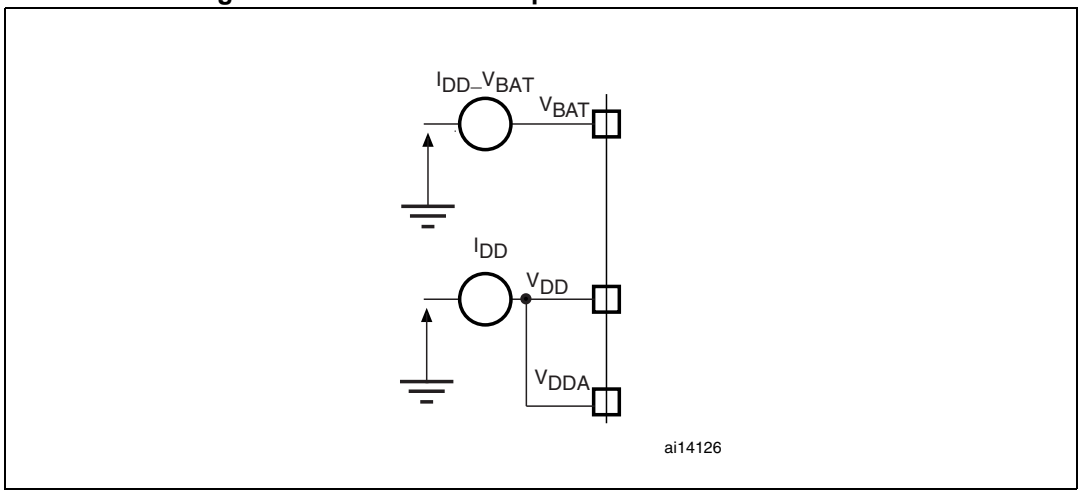
**Figure 10. Power supply scheme**




**Caution:** In *Figure 10*, the 4.7 µF capacitor must be connected to $V_{DD3}$.

### 5.1.7 Current consumption measurement

**Figure 11. Current consumption measurement scheme**




## 5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 5: Voltage characteristics*, *Table 6: Current characteristics*, and *Table 7: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 5. Voltage characteristics**

| Symbol | Ratings | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$ –$V_{SS}$ | External main supply voltage (including $V_{DDA}$ and $V_{DD}$)(1) | –0.3 | 4.0 | V |
| $V_{IN}$(2) | Input voltage on five volt tolerant pin | $V_{SS}$ –0.3 | $V_{DD}$ +4.0 | |
| | Input voltage on any other pin | $V_{SS}$ –0.3 | 4.0 | |
| $\|\Delta V_{DDx}\|$ | Variations between different $V_{DD}$ power pins | - | 50 | mV |
| $\|V_{SSX} - V_{SS}\|$ | Variations between all the different ground pins | - | 50 | |
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | see *Section 5.3.11: Absolute maximum ratings (electrical sensitivity)* | | - |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. $V_{IN}$ maximum must always be respected. Refer to *Table 6: Current characteristics* for the maximum allowed injected current values.

**Table 6. Current characteristics**

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $I_{VDD}$ | Total current into $V_{DD}/V_{DDA}$ power lines (source)(1) | 150 | mA |
| $I_{VSS}$ | Total current out of $V_{SS}$ ground lines (sink)(1) | 150 | |
| $I_{IO}$ | Output current sunk by any I/O and control pin | 25 | |
| | Output current source by any I/Os and control pin | –25 | |
| $I_{INJ(PIN)}$(2) | Injected current on five volt tolerant pins(3) | -5/+0 | |
| | Injected current on any other pin(4) | ± 5 | |
| $\Sigma I_{INJ(PIN)}$ | Total injected current (sum of all I/O and control pins)(5) | ± 25 | |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See note in *Section 5.3.17: 12-bit ADC characteristics*.
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 5: Voltage characteristics* for the maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 5: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

**Table 7. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $T_J$ | Maximum junction temperature | 150 | °C |

# 5.3 Operating conditions

## 5.3.1 General operating conditions

**Table 8. General operating conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{HCLK}$ | Internal AHB clock frequency | - | 0 | 36 | MHz |
| $f_{PCLK1}$ | Internal APB1 clock frequency | - | 0 | 36 | |
| $f_{PCLK2}$ | Internal APB2 clock frequency | - | 0 | 36 | |
| $V_{DD}$ | Standard operating voltage | - | 2 | 3.6 | V |
| $V_{DDA}$(1) | Analog operating voltage (ADC not used) | Must be the same potential as $V_{DD}$(2) | 2 | 3.6 | |
| | Analog operating voltage (ADC used) | | 2.4 | 3.6 | |
| $V_{BAT}$ | Backup operating voltage | - | 1.8 | 3.6 | |

**Table 8. General operating conditions (continued)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $P_D$ | Power dissipation at $T_A$ = 85 °C(3) | LQFP64 | - | 444 | mW |
| | | LQFP48 | - | 363 | |
| | | VFQFPN36 | - | 1000 | |
| $T_A$ | Ambient temperature | Maximum power dissipation | –40 | 85 | °C |
| | | Low power dissipation(4) | –40 | 105 | |
| $T_J$ | Junction temperature range | - | –40 | 105 | |

1. When the ADC is used, refer to *Table 41: ADC characteristics*.
2. It is recommended to power $V_{DD}$ and $V_{DDA}$ from the same source. A maximum difference of 300 mV between $V_{DD}$ and $V_{DDA}$ can be tolerated during power-up and operation.
3. If $T_A$ is lower, higher $P_D$ values are allowed as long as $T_J$ does not exceed $T_J$max (see *Table 6.5: Thermal characteristics on page 82*).
4. In low power dissipation state, $T_A$ can be extended to this range as long as $T_J$ does not exceed $T_J$max (see *Table 6.5: Thermal characteristics on page 82*).

### 5.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for $T_A$.

**Table 9. Operating conditions at power-up / power-down**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | - | 0 | ∞ | µs/V |
| | $V_{DD}$ fall time rate | | 20 | ∞ | |

### 5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 10* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 8*.

**Table 10. Embedded reset and power control block characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD}$ | Programmable voltage detector level selection | PLS[2:0]=000 (rising edge) | 2.1 | 2.18 | 2.26 | V |
| | | PLS[2:0]=000 (falling edge) | 2 | 2.08 | 2.16 | |
| | | PLS[2:0]=001 (rising edge) | 2.19 | 2.28 | 2.37 | |
| | | PLS[2:0]=001 (falling edge) | 2.09 | 2.18 | 2.27 | |
| | | PLS[2:0]=010 (rising edge) | 2.28 | 2.38 | 2.48 | |
| | | PLS[2:0]=010 (falling edge) | 2.18 | 2.28 | 2.38 | |
| | | PLS[2:0]=011 (rising edge) | 2.38 | 2.48 | 2.58 | |
| | | PLS[2:0]=011 (falling edge) | 2.28 | 2.38 | 2.48 | |
| | | PLS[2:0]=100 (rising edge) | 2.47 | 2.58 | 2.69 | |
| | | PLS[2:0]=100 (falling edge) | 2.37 | 2.48 | 2.59 | |
| | | PLS[2:0]=101 (rising edge) | 2.57 | 2.68 | 2.79 | |
| | | PLS[2:0]=101 (falling edge) | 2.47 | 2.58 | 2.69 | |
| | | PLS[2:0]=110 (rising edge) | 2.66 | 2.78 | 2.9 | |
| | | PLS[2:0]=110 (falling edge) | 2.56 | 2.68 | 2.8 | |
| | | PLS[2:0]=111 (rising edge) | 2.76 | 2.88 | 3 | |
| | | PLS[2:0]=111 (falling edge) | 2.66 | 2.78 | 2.9 | |
| $V_{PVDhyst}$(2) | PVD hysteresis | - | - | 100 | - | mV |
| $V_{POR/PDR}$ | Power on/power down reset threshold | Falling edge | 1.8(1) | 1.88 | 1.96 | V |
| | | Rising edge | 1.84 | 1.92 | 2.0 | |
| $V_{PDRhyst}$(2) | PDR hysteresis | - | - | 40 | - | mV |
| $t_{RSTTEMPO}$(2) | Reset temporization | - | 1.5 | 2.5 | 4.5 | ms |

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design, not tested in production.

### 5.3.4 Embedded reference voltage

The parameters given in *Table 11* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 8*.

**Table 11. Embedded internal reference voltage**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT}$ | Internal reference voltage | –40 °C < $T_A$ < +85 °C | 1.16 | 1.20 | 1.24 | V |
| $T_{S_vrefint}$(1) | ADC sampling time when reading the internal reference voltage | - | - | 5.1 | 17.1(2) | µs |
| $V_{RERINT}$(2) | Internal reference voltage spread over the temperature range | $V_{DD}$ = 3 V ±10 mV | - | - | 10 | mV |
| $T_{Coeff}$(2) | Temperature coefficient | - | - | - | 100 | ppm/ °C |

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production.

### 5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 11: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

#### Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)
- All peripherals are disabled except if it is explicitly mentioned
- The Flash access time is adjusted to $f_{HCLK}$ frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 36 MHz)
- Prefetch in on (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK/2}$, $f_{PCLK2} = f_{HCLK}$

The parameters given in *Table 12* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 8*.

**Table 12. Maximum current consumption in Run mode, code with data processing running from Flash**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Max(1) $T_A$ = 85 °C | Unit |
|---|---|---|---|---|---|
| $I_{DD}$ | Supply current in Run mode | External clock (2), all peripherals enabled | 36 MHz | 26 | mA |
| | | | 24 MHz | 18 | |
| | | | 16 MHz | 13 | |
| | | | 8 MHz | 7 | |
| | | External clock (2), all peripherals Disabled | 36 MHz | 19 | |
| | | | 24 MHz | 13 | |
| | | | 16 MHz | 10 | |
| | | | 8 MHz | 6 | |

1. Based on characterization, not tested in production.
2. External clock is 8 MHz and PLL is on when $f_{HCLK}$ > 8 MHz.

**Table 13. Maximum current consumption in Run mode, code with data processing running from RAM**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Max(1) $T_A$ = 85 °C | Unit |
|---|---|---|---|---|---|
| $I_{DD}$ | Supply current in Run mode | External clock (2), all peripherals enabled | 36 MHz | 20 | mA |
| | | | 24 MHz | 14 | |
| | | | 16 MHz | 10 | |
| | | | 8 MHz | 6 | |
| | | External clock(2) all peripherals disabled | 36 MHz | 15 | |
| | | | 24 MHz | 10 | |
| | | | 16 MHz | 7 | |
| | | | 8 MHz | 5 | |

1. Based on characterization, tested in production at $V_{DD}$ max, $f_{HCLK}$ max.
2. External clock is 8 MHz and PLL is on when $f_{HCLK}$ > 8 MHz.

**Figure 12. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled**

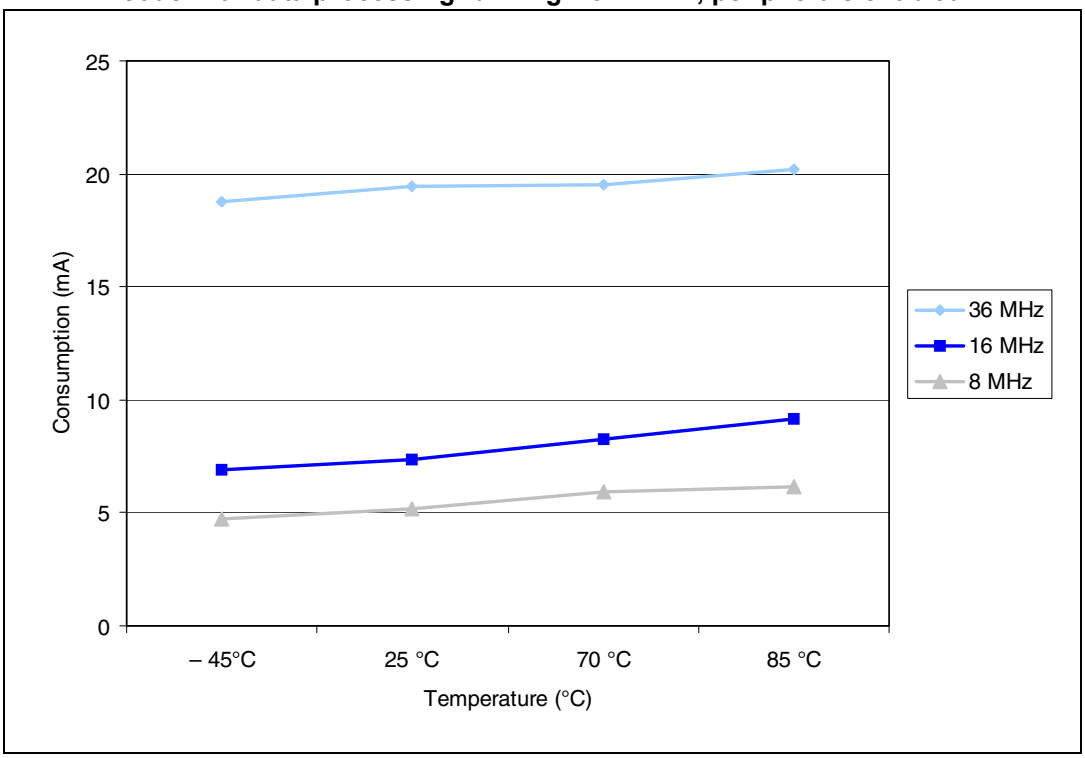



**Figure 13. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled**

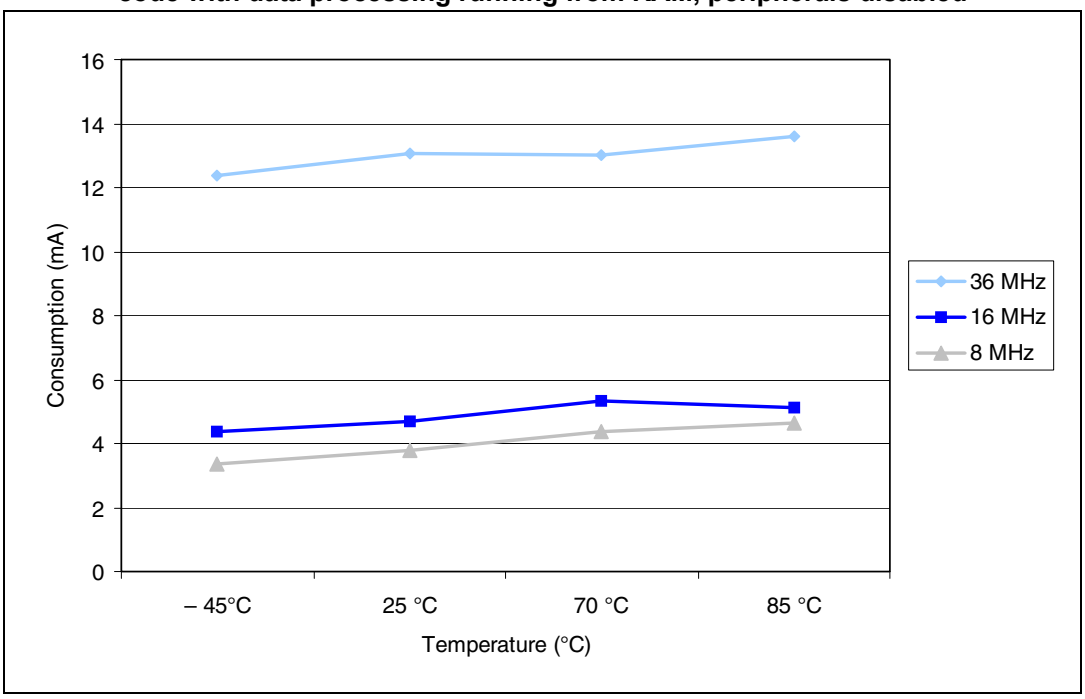


**Table 14. Maximum current consumption in Sleep mode, code running from Flash or RAM**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Max(1) | Unit |
|---|---|---|---|---|---|
| | | | | $T_A$ = 85 °C | |
| $I_{DD}$ | Supply current in Sleep mode | External clock(2) all peripherals enabled | 36 MHz | 14 | mA |
| | | | 24 MHz | 10 | |
| | | | 16 MHz | 7 | |
| | | | 8 MHz | 4 | |
| | | External clock(2), all peripherals disabled | 36 MHz | 5 | |
| | | | 24 MHz | 4.5 | |
| | | | 16 MHz | 4 | |
| | | | 8 MHz | 3 | |

1. Based on characterization, tested in production at $V_{DD}$ max and $f_{HCLK}$ max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when $f_{HCLK}$ > 8 MHz.

**Table 15. Typical and maximum current consumptions in Stop and Standby modes**

| Symbol | Parameter | Conditions | Typ(1) | | | Max | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}/V_{BAT}$ = 2.0 V | $V_{DD}/V_{BAT}$ = 2.4 V | $V_{DD}/V_{BAT}$ = 3.3 V | $T_A$ = 85 °C(2) | |
| $I_{DD}$ | Supply current in Stop mode | Regulator in Run mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | - | 21.3 | 21.7 | 160 | µA |
| | | Regulator in Low Power mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | - | 11.3 | 11.7 | 145 | |
| | Supply current in Standby mode | Low-speed internal RC oscillator and independent watchdog ON | - | 2.6 | 3.4 | - | |
| | | Low-speed internal RC oscillator ON, independent watchdog OFF | - | 2.4 | 3.2 | - | |
| | | Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF | - | 1.7 | 2 | 3.2 | |
| $I_{DD_VBAT}$ | Backup domain supply current | Low-speed oscillator and RTC ON | 0.9 | 1.1 | 1.4 | 1.9 | |

1. Typical values are measured at $T_A$ = 25 °C.
2. Based on characterization, not rested in production.

**Figure 14. Typical current consumption on $V_{BAT}$ with RTC on versus temperature at different $V_{BAT}$ values**

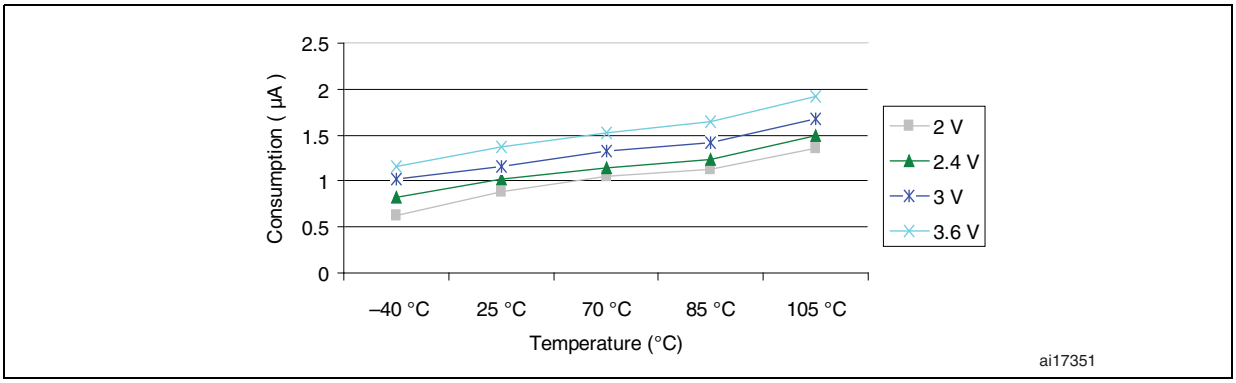



**Figure 15. Typical current consumption in Stop mode with regulator in Run mode versus temperature at $V_{DD}$ = 3.3 V and 3.6 V**

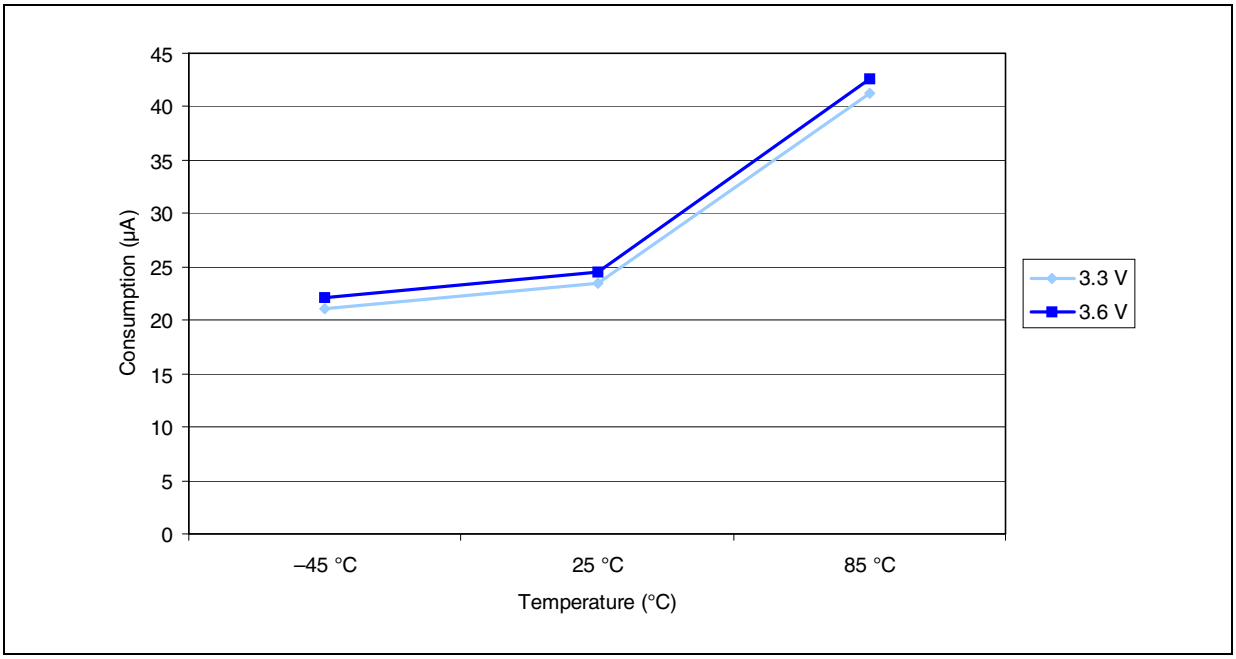


**Figure 16. Typical current consumption in Stop mode with regulator in Low-power mode versus temperature at $V_{DD}$ = 3.3 V and 3.6 V**

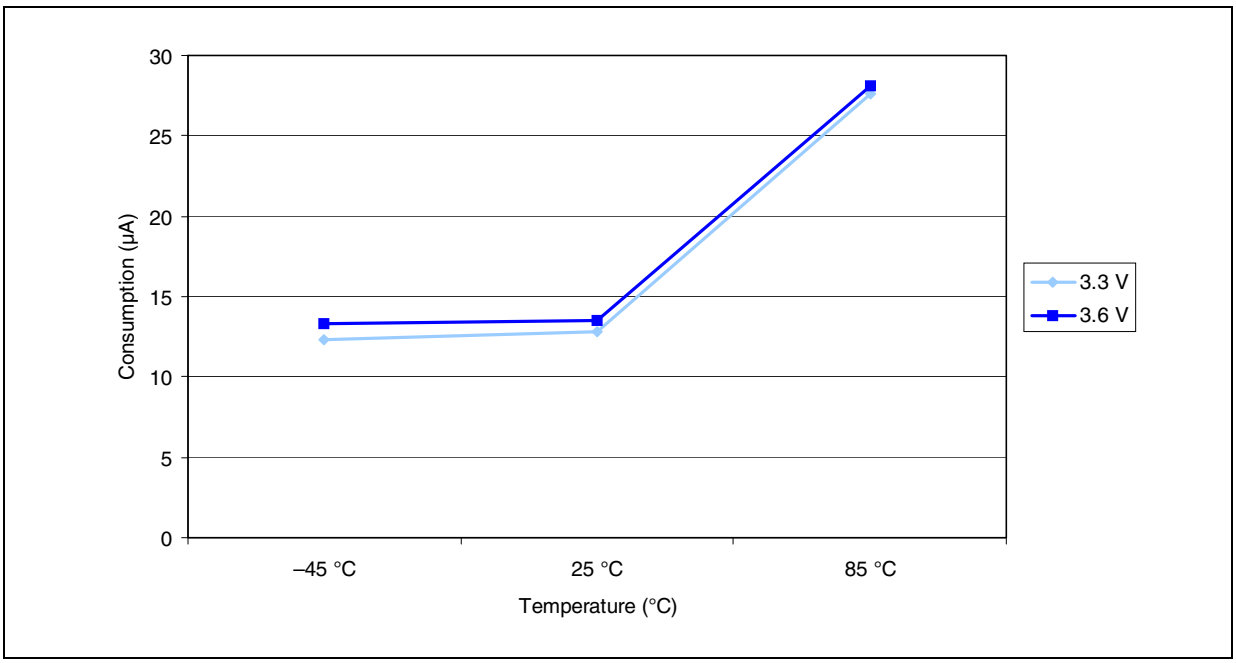
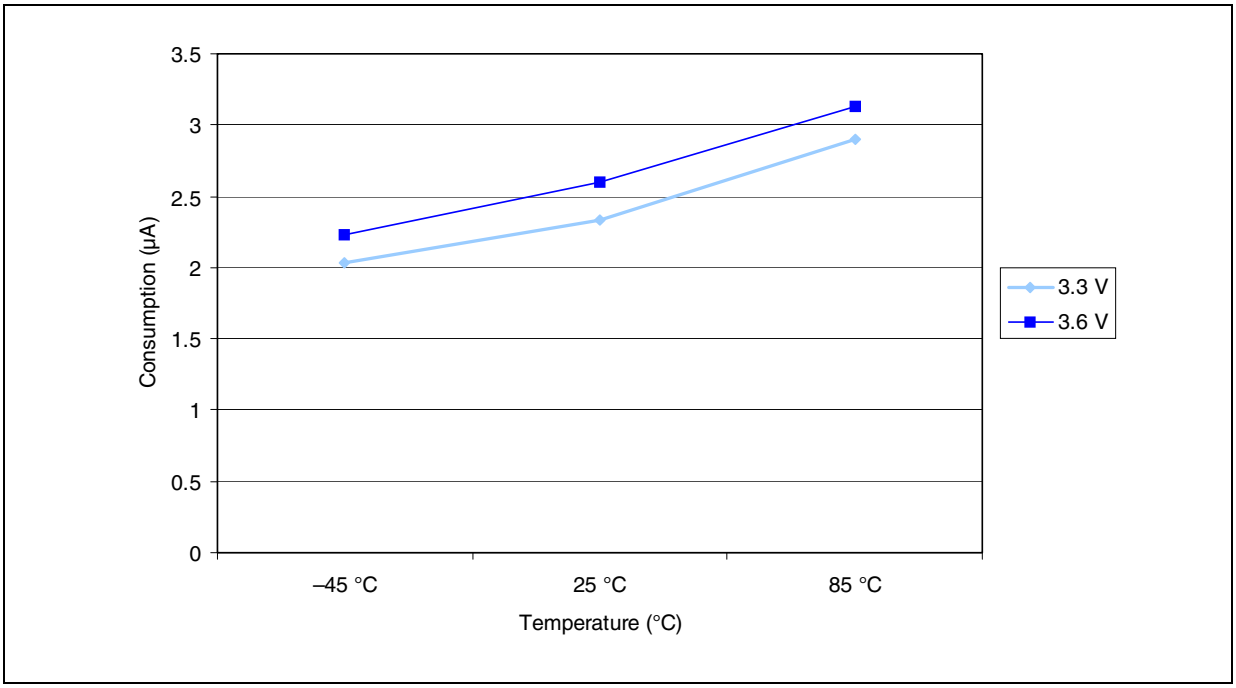



**Figure 17. Typical current consumption in Standby mode versus temperature at $V_{DD}$ = 3.3 V and 3.6 V**



### Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)
- All peripherals are disabled except if it is explicitly mentioned
- The Flash access time is adjusted to $f_{HCLK}$ frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 36 MHz)
- Prefetch is on (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK/4}$, $f_{PCLK2} = f_{HCLK/2}$, $f_{ADCCLK} = f_{PCLK2}/4$

The parameters given in *Table 16* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 8*.

**Table 16. Typical current consumption in Run mode, code with data processing running from Flash**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typ(1) All peripherals enabled(2) | Typ(1) All peripherals disabled | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current in Run mode | External clock(3) | 36 MHz | 17.2 | 13.8 | mA |
| | | | 24 MHz | 11.2 | 8.9 | |
| | | | 16 MHz | 8.1 | 6.6 | |
| | | | 8 MHz | 5 | 4.2 | |
| | | | 4 MHz | 3 | 2.6 | |
| | | | 2 MHz | 2 | 1.8 | |
| | | | 1 MHz | 1.5 | 1.4 | |
| | | | 500 kHz | 1.2 | 1.2 | |
| | | | 125 kHz | 1.05 | 1 | |
| | | Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency | 36 MHz | 16.5 | 13.1 | |
| | | | 24 MHz | 10.5 | 8.2 | |
| | | | 16 MHz | 7.4 | 5.9 | |
| | | | 8 MHz | 4.3 | 3.6 | |
| | | | 4 MHz | 2.4 | 2 | |
| | | | 2 MHz | 1.5 | 1.3 | |
| | | | 1 MHz | 1 | 0.9 | |
| | | | 500 kHz | 0.7 | 0.65 | |
| | | | 125 kHz | 0.5 | 0.45 | |

1. Typical values are measures at $T_A = 25$ °C, $V_{DD} = 3.3$ V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

**Table 17. Typical current consumption in Sleep mode, code running from Flash or RAM**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typ(1) All peripherals enabled(2) | Typ(1) All peripherals disabled | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current in Sleep mode | External clock(3) | 36 MHz | 6.7 | 3.1 | mA |
| | | | 24 MHz | 4.8 | 2.3 | |
| | | | 16 MHz | 3.4 | 1.8 | |
| | | | 8 MHz | 2 | 1.2 | |
| | | | 4 MHz | 1.5 | 1.1 | |
| | | | 2 MHz | 1.25 | 1 | |
| | | | 1 MHz | 1.1 | 0.98 | |
| | | | 500 kHz | 1.05 | 0.96 | |
| | | | 125 kHz | 1 | 0.95 | |
| | | Running on High Speed Internal RC (HSI), AHB prescaler used to reduce the frequency | 36 MHz | 6.1 | 2.5 | |
| | | | 24 MHz | 4.2 | 1.7 | |
| | | | 16 MHz | 2.8 | 1.2 | |
| | | | 8 MHz | 1.4 | 0.55 | |
| | | | 4 MHz | 0.9 | 0.5 | |
| | | | 2 MHz | 0.7 | 0.45 | |
| | | | 1 MHz | 0.55 | 0.42 | |
| | | | 500 kHz | 0.48 | 0.4 | |
| | | | 125 kHz | 0.4 | 0.38 | |

1. Typical values are measures at $T_A$ = 25 °C, $V_{DD}$ = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when $f_{HCLK}$ > 8 MHz.

### On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 18*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and $V_{DD}$ supply voltage conditions summarized in *Table 5*.

**Table 18. Peripheral current consumption**

| Peripheral | | Typical consumption at 25 °C | Unit |
|---|---|---|---|
| AHB (up to 36 MHz) | DMA1 | 15.97 | µA/MHz |
| | CRC | 1.67 | |
| | BusMatrix(1) | 8.33 | |
| APB1 (up to 18 MHz) | APB1-Bridge | 7.22 | |
| | TIM2 | 33.33 | |
| | TIM3 | 33.61 | |
| | USART2 | 12.78 | |
| | I2C1 | 10.83 | |
| | WWDG | 3.33 | |
| | PWR | 1.94 | |
| | BKP | 2.78 | |
| | IWDG | 1.39 | |
| APB2 (up to 36 MHz) | APB2-Bridge | 3.33 | |
| | GPIO A | 7.50 | |
| | GPIO B | 6.81 | |
| | GPIO C | 7.22 | |
| | GPIO D | 6.94 | |
| | SPI1 | 4.86 | |
| | USART1 | 12.78 | |
| | ADC1(2) | 15.54 | |

1. The BusMatrix is automatically active when at least one master is ON. (CPU, DMA1).
2. Specific conditions for measuring ADC current consumption: $f_{HCLK}$ = 28 MHz, $f_{APB1} = f_{HCLK}$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2} / 2$. When ADON bit in the ADC_CR2 register is set to 1, a current consumption of analog part equal to 0.7 mA must be added.

## 5.3.6 External clock source characteristics

### High-speed external user clock generated from an external source

The characteristics given in *Table 19* result from tests performed using an high-speed external clock source, and under the ambient temperature and supply voltage conditions summarized in *Table 8*.

**Table 19. High-speed external user clock characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSE_ext}$ | User external clock source frequency(1) | - | 1 | 8 | 25 | MHz |
| $V_{HSEH}$ | OSC_IN input pin high level voltage | | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| $V_{HSEL}$ | OSC_IN input pin low level voltage | | $V_{SS}$ | - | $0.3V_{DD}$ | |
| $t_{w(HSE)}$ $t_{w(HSE)}$ | OSC_IN high or low time(1) | | 5 | - | - | ns |
| $t_{r(HSE)}$ $t_{f(HSE)}$ | OSC_IN rise or fall time(1) | | - | - | 20 | |
| $C_{in(HSE)}$ | OSC_IN input capacitance(1) | - | - | 5 | - | pF |
| $DuCy_{(HSE)}$ | Duty cycle | - | 45 | - | 55 | % |
| $I_L$ | OSC_IN Input leakage current | $V_{SS} \le V_{IN} \le V_{DD}$ | - | - | ±1 | µA |

1. Guaranteed by design, not tested in production.

### Low-speed external user clock generated from an external source

The characteristics given in *Table 20* result from tests performed using an low-speed external clock source, and under the ambient temperature and supply voltage conditions summarized in *Table 8*.

**Table 20. Low-speed external user clock characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSE_ext}$ | User external clock source frequency(1) | - | - | 32.768 | 1000 | kHz |
| $V_{LSEH}$ | OSC32_IN input pin high level voltage | | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| $V_{LSEL}$ | OSC32_IN input pin low level voltage | | $V_{SS}$ | - | $0.3V_{DD}$ | |
| $t_{w(LSE)}$ $t_{w(LSE)}$ | OSC32_IN high or low time(1) | | 450 | - | - | ns |
| $t_{r(LSE)}$ $t_{f(LSE)}$ | OSC32_IN rise or fall time(1) | | - | - | 50 | |
| $C_{in(LSE)}$ | OSC32_IN input capacitance(1) | - | - | 5 | - | pF |
| $DuCy_{(LSE)}$ | Duty cycle | - | 30 | - | 70 | % |
| $I_L$ | OSC32_IN Input leakage current | $V_{SS} \le V_{IN} \le V_{DD}$ | - | - | ±1 | µA |

1. Guaranteed by design, not tested in production.

**Figure 18. High-speed external clock source AC timing diagram**

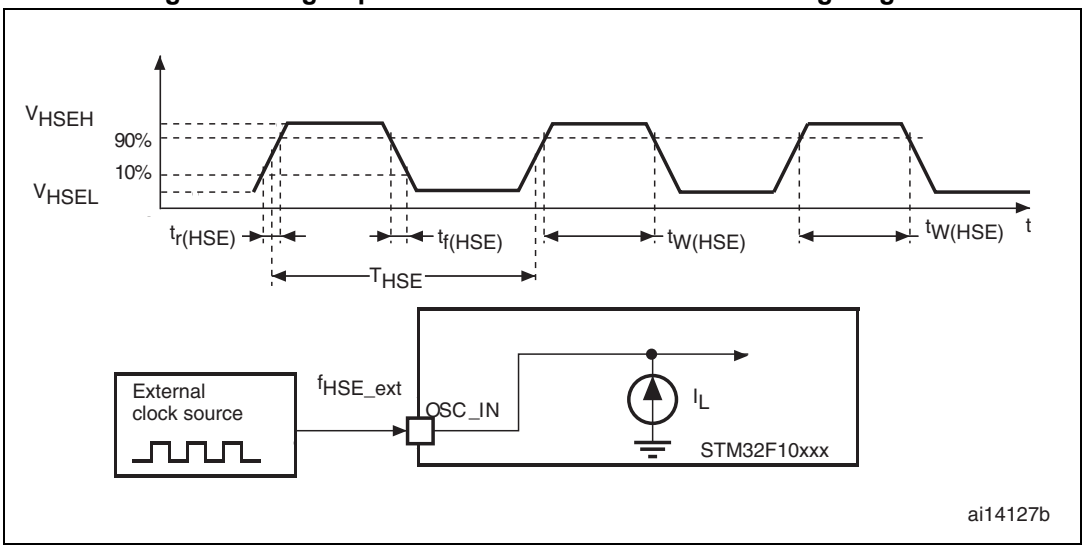
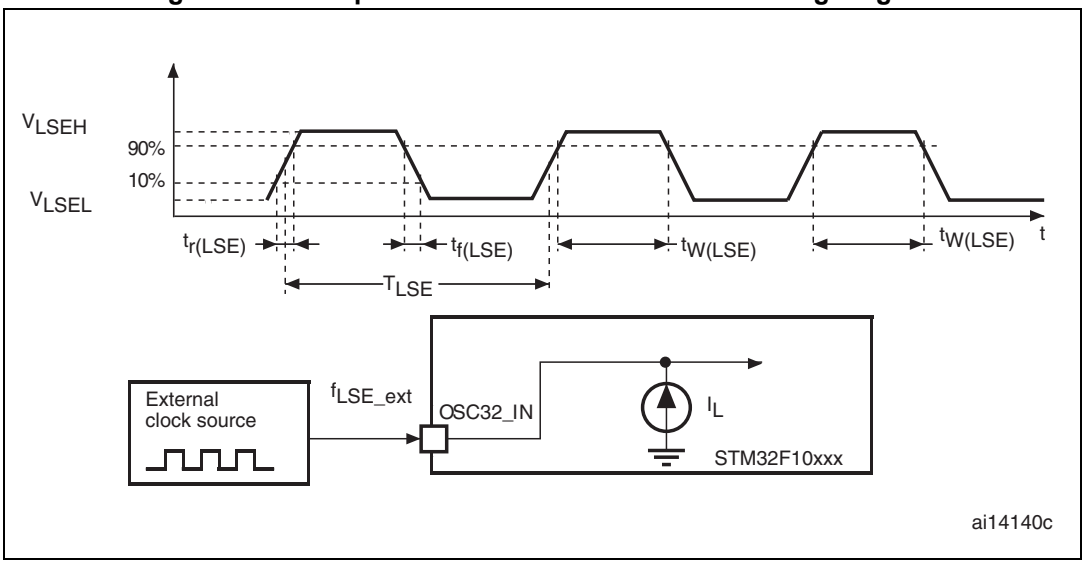



**Figure 19. Low-speed external clock source AC timing diagram**




### High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 21*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

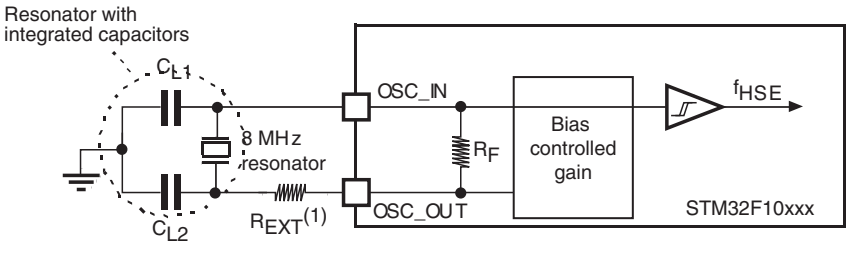
**Table 21. HSE 4-16 MHz oscillator characteristics(1)(2)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{OSC_IN}$ | Oscillator frequency | - | 4 | 8 | 16 | MHz |
| $R_F$ | Feedback resistor | - | - | 200 | - | kΩ |
| C | Recommended load capacitance versus equivalent serial resistance of the crystal ($R_S$)(3) | $R_S$ = 30 Ω | - | 30 | - | pF |
| $i_2$ | HSE driving current | $V_{DD}$ = 3.3 V, $V_{IN}$ = $V_{SS}$ with 30 pF load | - | - | 1 | mA |
| $g_m$ | Oscillator transconductance | Startup | 25 | - | - | mA/V |
| $t_{SU(HSE)}$(4) | Startup time | $V_{DD}$ is stabilized | - | 2 | - | ms |

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization, not tested in production.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For $C_{L1}$ and $C_{L2}$, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 20*). $C_{L1}$ and $C_{L2}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of $C_{L1}$ and $C_{L2}$. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing $C_{L1}$ and $C_{L2}$. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

**Figure 20. Typical application with an 8 MHz crystal**




1. $R_{EXT}$ value depends on the crystal characteristics.

### Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 22*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization

time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 22. LSE oscillator characteristics ($f_{LSE}$ = 32.768 kHz)(1) (2)**

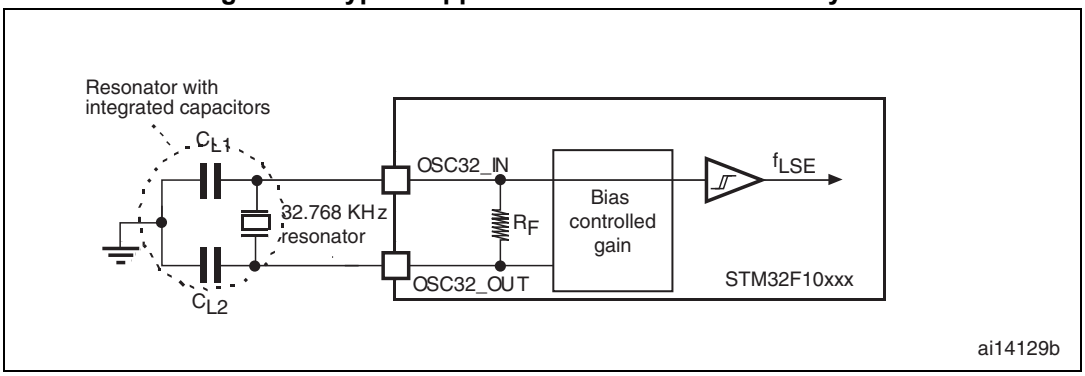
| Symbol | Parameter | Conditions | - | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_F$ | Feedback resistor | - | - | - | 5 | - | MΩ |
| C | Recommended load capacitance versus equivalent serial resistance of the crystal ($R_S$) | $R_S$ = 30 KΩ | - | - | - | 15 | pF |
| $I_2$ | LSE driving current | $V_{DD}$ = 3.3 V<br>$V_{IN}$ = $V_{SS}$ | - | - | - | 1.4 | µA |
| $g_m$ | Oscillator transconductance | - | - | 5 | - | - | µA/V |
| $t_{SU(LSE)}$(3) | Startup time | $V_{DD}$ is stabilized | $T_A$ = 50 °C | - | 1.5 | - | s |
| | | | $T_A$ = 25 °C | - | 2.5 | - | |
| | | | $T_A$ = 10 °C | - | 4 | - | |
| | | | $T_A$ = 0 °C | - | 6 | - | |
| | | | $T_A$ = -10 °C | - | 10 | - | |
| | | | $T_A$ = -20 °C | - | 17 | - | |
| | | | $T_A$ = -30 °C | - | 32 | - | |
| | | | $T_A$ = -40 °C | - | 60 | - | |

1. Based on characterization, not tested in production.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

*Note:* For CL1 and CL2 it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator. CL1 and CL2, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of CL1 and CL2.
*Load capacitance* CL *has the following formula:* CL = CL1 *x* CL2 */ (*CL1 + CL2*) +* $C_{stray}$
*where* $C_{stray}$ *is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.*

**Caution:** To avoid exceeding the maximum value of CL1 and CL2 (15 pF) it is strongly recommended to use a resonator with a load capacitance CL ≤7 pF. Never use a resonator with a load capacitance of 12.5 pF.
**Example:** if resonator with a load capacitance of CL = 6 pF, and $C_{stray}$ = 2 pF is chosen, then CL1 = CL2 = 8 pF.

**Figure 21. Typical application with a 32.768 kHz crystal**




## 5.3.7 Internal clock source characteristics

The parameters given in *Table 23* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 8*.

### High-speed internal (HSI) RC oscillator

**Table 23. HSI oscillator characteristics(1)**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{HSI}$ | Frequency | - | | - | 8 | - | MHz |
| $DuCy_{(HSI)}$ | Duty cycle | - | | 45 | - | 55 | % |
| $ACC_{HSI}$ | Accuracy of the HSI oscillator | User-trimmed with the RCC_CR register(2) | | - | - | 1(3) | % |
| | | Factory-calibrated (4) (5) | $T_A$ = –40 to 105 °C | –2 | - | 2.5 | % |
| | | | $T_A$ = –10 to 85 °C | –1.5 | - | 2.2 | % |
| | | | $T_A$ = 0 to 70 °C | –1.3 | - | 2 | % |
| | | | $T_A$ = 25 °C | –1.1 | - | 1.8 | % |
| $t_{su(HSI)}$(4) | HSI oscillator startup time | - | | 1 | - | 2 | µs |
| $I_{DD(HSI)}$(4) | HSI oscillator power consumption | - | | - | 80 | 100 | µA |

1. $V_{DD}$ = 3.3 V, $T_A$ = –40 to 105 °C unless otherwise specified.
2. Refer to application note AN2868 “STM32F10xxx internal RC oscillator (HSI) calibration” available from the ST website *www.st.com*.
3. Guaranteed by design, not tested in production.
4. Based on characterization, not tested in production.
5. The actual frequency of HSI oscillator may be impacted by a reflow, but does not drift out of the specified range.

### Low-speed internal (LSI) RC oscillator

**Table 24. LSI oscillator characteristics (1)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{LSI}$(2) | Frequency | 30 | 40 | 60 | kHz |
| $t_{su(LSI)}$(3) | LSI oscillator startup time | - | - | 85 | µs |
| $I_{DD(LSI)}$(3) | LSI oscillator power consumption | - | 0.65 | 1.2 | µA |

1. $V_{DD}$ = 3 V, $T_A$ = –40 to 85 °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.

### Wakeup time from low-power mode

The wakeup times given in *Table 25* are measured on a wakeup phase with an 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 8*.

**Table 25. Low-power mode wakeup timings**

| Symbol | Parameter | Typ | Unit |
|---|---|---|---|
| $t_{WUSLEEP}$(1) | Wakeup from Sleep mode | 1.8 | µs |
| $t_{WUSTOP}$(1) | Wakeup from Stop mode (regulator in run mode) | 3.6 | µs |
| | Wakeup from Stop mode (regulator in low-power mode) | 5.4 | |
| $t_{WUSTDBY}$(1) | Wakeup from Standby mode | 50 | µs |

1. The wakeup times are measured from the wakeup event to the point at which the user application code reads the first instruction.

## 5.3.8 PLL characteristics

The parameters given in *Table 26* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 8*.

**Table 26. PLL characteristics**

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min(1) | Typ | Max(1) | |
| $f_{PLL_IN}$ | PLL input clock(2) | 1 | 8.0 | 25 | MHz |
| | PLL input clock duty cycle | 40 | - | 60 | % |
| $f_{PLL_OUT}$ | PLL multiplier output clock | 16 | - | 36 | MHz |

**Table 26. PLL characteristics (continued)**

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min(1) | Typ | Max(1) | |
| $t_{LOCK}$ | PLL lock time | - | - | 200 | µs |
| Jitter | Cycle-to-cycle jitter | - | - | 300 | ps |

1. Based on device characterization, not tested in production.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by $f_{PLL_OUT}$.

## 5.3.9 Memory characteristics

### Flash memory

The characteristics are given at $T_A$ = –40 to 85 °C unless otherwise specified.

**Table 27. Flash memory characteristics**

| Symbol | Parameter | Conditions | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $t_{prog}$ | 16-bit programming time | $T_A$ = –40 to +85 °C | 40 | 52.5 | 70 | µs |
| $t_{ERASE}$ | Page (1 KB) erase time | $T_A$ = –40 to +85 °C | 20 | - | 40 | ms |
| $t_{ME}$ | Mass erase time | $T_A$ = –40 to +85 °C | 20 | - | 40 | ms |
| $I_{DD}$ | Supply current | Read mode $f_{HCLK}$ = 36 MHz with 1 wait state, $V_{DD}$ = 3.3 V | - | - | 20 | mA |
| | | Write / Erase modes $f_{HCLK}$ = 36 MHz, $V_{DD}$ = 3.3 V | - | - | 5 | mA |
| | | Power-down mode / Halt, $V_{DD}$ = 3.0 to 3.6 V | - | - | 50 | µA |
| $V_{prog}$ | Programming voltage | - | 2 | - | 3.6 | V |

1. Guaranteed by design, not tested in production.

## 5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

### Functional EMS (Electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 28*. They are based on the EMS levels and classes defined in application note AN1709.

**Table 28. EMS characteristics**

| Symbol | Parameter | Conditions | Level/Class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, $T_A$ = +25 °C, $f_{HCLK}$= 36 MHz conforms to IEC 61000-4-2 | 2B |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$ = 3.3 V, $T_A$ = +25 °C, $f_{HCLK}$ = 36 MHz conforms to IEC 61000-4-4 | 4A |

### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

### Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second. To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

### Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC61967-2 standard which specifies the test board and the pin loading.

**Table 29. EMI characteristics**

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. [$f_{HSE}/f_{HCLK}$] | Unit |
|---|---|---|---|---|---|
| | | | | 8/36 MHz | |
| $S_{EMI}$ | Peak level | $V_{DD}$ = 3.3 V, $T_A$ = 25 °C, compliant with IEC 61967-2 | 0.1 MHz to 30 MHz | 7 | dBµV |
| | | | 30 MHz to 130 MHz | 8 | |
| | | | 130 MHz to 1GHz | 13 | |
| | | | EMI Level | 3.5 | - |

## 5.3.11 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

**Table 30. ESD absolute maximum ratings**

| Symbol | Ratings | Conditions | Class | Maximum value(1) | Unit |
|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$ = +25 °C conforming to JESD22-A114 | 2 | 2000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$ = +25 °C conforming to ANSI/ESD STM5.3.1 | II | 500 | |

1. Based on characterization results, not tested in production.

### Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78 IC latch-up standard.

**Table 31. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latch-up class | $T_A$ = +85 °C conforming to JESD78A | II level A |

## 5.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below $V_{SS}$ or above $V_{DD}$ (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

### Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 32*

**Table 32. I/O current injection susceptibility**

| Symbol | Description | Functional susceptibility | | Unit |
|---|---|---|---|---|
| | | Negative injection | Positive injection | |
| $I_{INJ}$ | Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13 | -0 | +0 | mA |
| | Injected current on all FT pins | -5 | +0 | |
| | Injected current on any other pin | -5 | +5 | |

## 5.3.13 I/O port characteristics

### General input/output characteristics

Unless otherwise specified, the parameters given in *Table 33* are derived from tests performed under the conditions summarized in *Table 8*. All I/Os are CMOS and TTL compliant.

**Table 33. I/O static characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Standard IO input low level voltage | - | -0.3 | - | 0.28*($V_{DD}$-2 V)+0.8 V(1) | V |
| | IO FT(2) input low level voltage | | -0.3 | - | 0.32*($V_{DD}$-2 V)+0.75 V(1) | |
| $V_{IH}$ | Standard IO input high level voltage | - | 0.41*($V_{DD}$-2 V)+1.3 V(1) | - | $V_{DD}$+0.3 | |
| | IO FT(2) input high level voltage | $V_{DD}$ > 2 V | 0.42*($V_{DD}$-2 V)+1 V(1) | - | 5.5 | |
| | | $V_{DD}$ ≤ 2 V | | | 5.2 | |
| $V_{hys}$ | Standard IO Schmitt trigger voltage hysteresis(3) | - | 200 | - | - | mV |
| | IO FT Schmitt trigger voltage hysteresis(3) | - | 5% $V_{DD}$(4) | - | - | |
| $I_{lkg}$ | Input leakage current (5) | $V_{SS}$ ≤ $V_{IN}$ ≤ $V_{DD}$ Standard I/Os | - | - | ±1 | µA |
| | | $V_{IN}$ = 5 V I/O FT | - | - | 3 | |
| $R_{PU}$ | Weak pull-up equivalent resistor(6) | $V_{IN}$ = $V_{SS}$ | 30 | 40 | 50 | kΩ |
| $R_{PD}$ | Weak pull-down equivalent resistor(6) | $V_{IN}$ = $V_{DD}$ | 30 | 40 | 50 | |
| $C_{IO}$ | I/O pin capacitance | - | - | 5 | - | pF |

1. Data based on design simulation.
2. FT = Five-volt tolerant. In order to sustain a voltage higher than $V_{DD}$+0.3 the internal pull-up/pull-down resistors must be disabled.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.
4. With a minimum of 100 mV.
5. Leakage could be higher than max. if negative current is injected on adjacent pins.
6. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 22* and *Figure 23* for standard I/Os, and in *Figure 24* and *Figure 25* for 5 V tolerant I/Os.

**Figure 22. Standard I/O input characteristics - CMOS port**

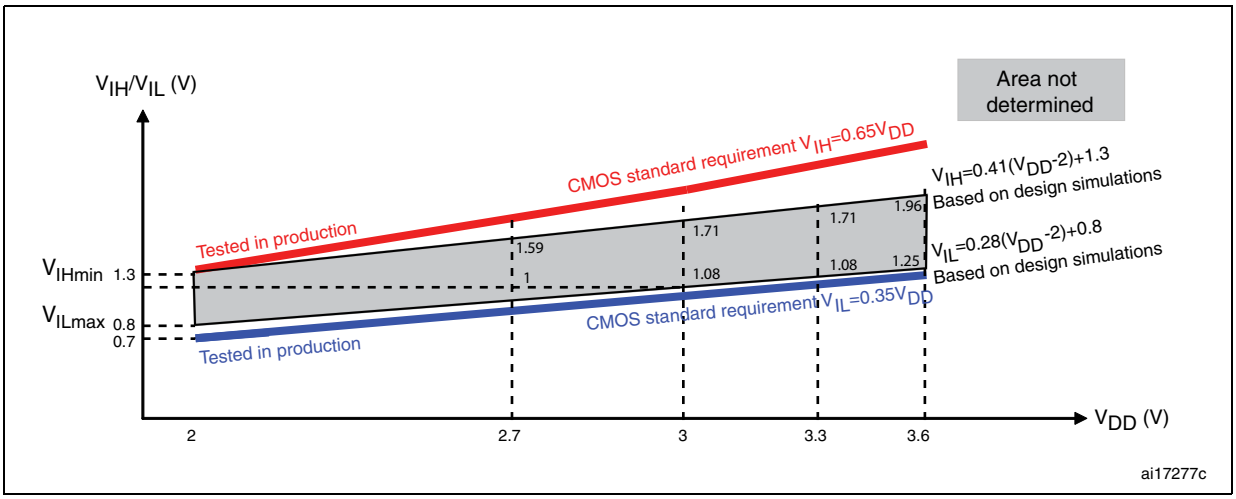



**Figure 23. Standard I/O input characteristics - TTL port**

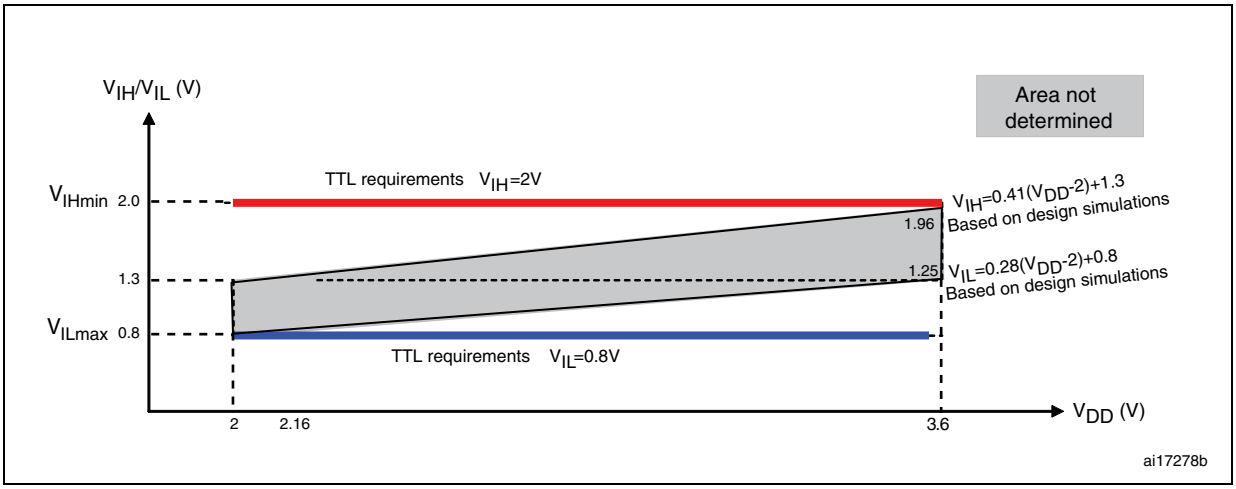


Figure 24. 5 V tolerant I/O input characteristics - CMOS port

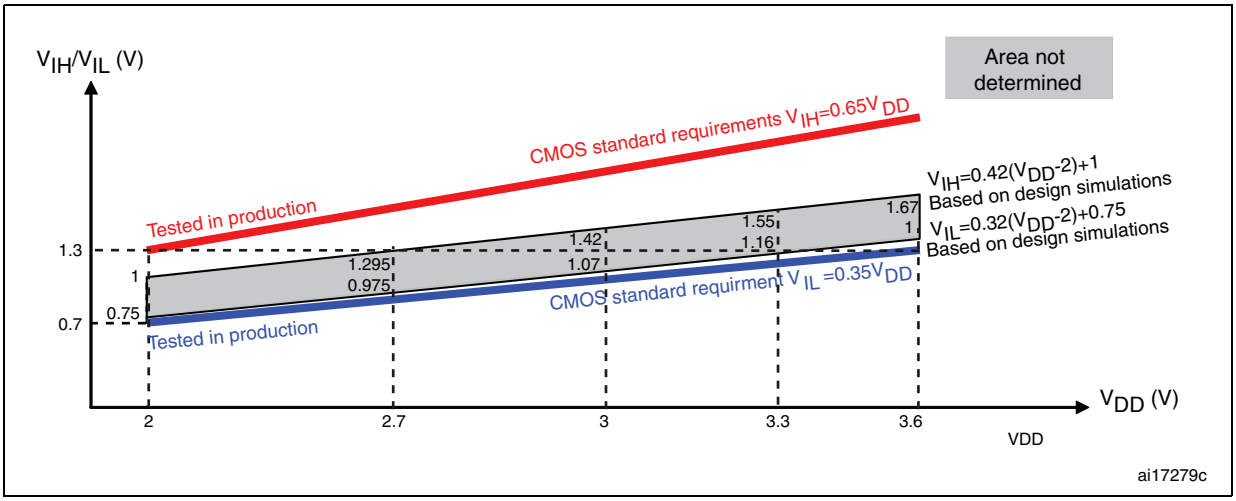
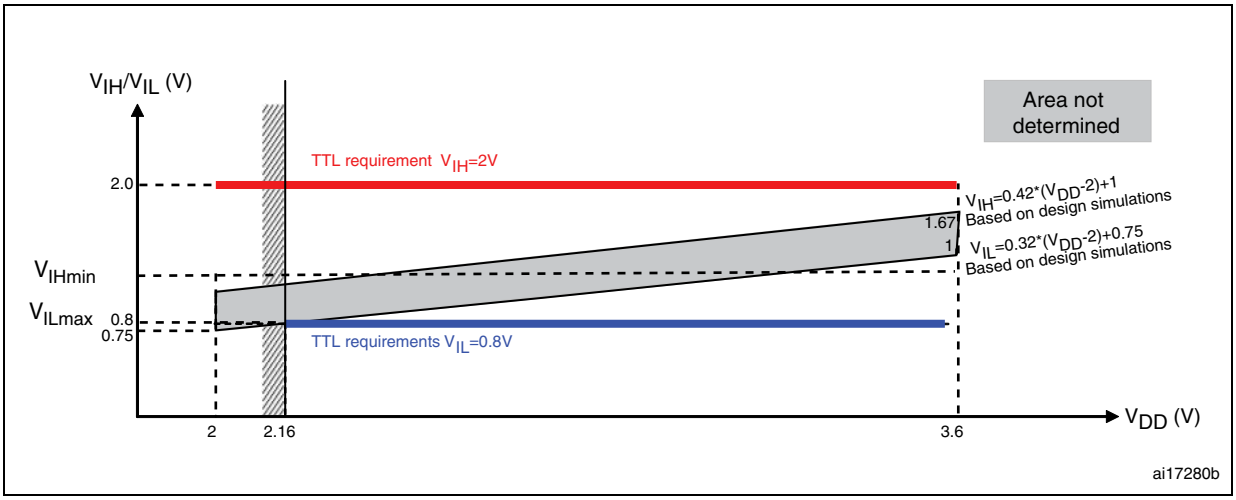



Figure 25. 5 V tolerant I/O input characteristics - TTL port



### Output driving current

The GPIOs (general-purpose inputs/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed $V_{OL}/V_{OH}$) except PC13, PC14 and PC15 which can sink or source up to +/-3mA. When using the GPIOs PC13 to PC15 in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $I_{VDD}$ (see *Table 6*).
- The sum of the currents sunk by all the I/Os on $V_{SS}$ plus the maximum Run consumption of the MCU sunk on $V_{SS}$ cannot exceed the absolute maximum rating $I_{VSS}$ (see *Table 6*).

### Output voltage levels

Unless otherwise specified, the parameters given in *Table 34* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 8*. All I/Os are CMOS and TTL compliant.

**Table 34. Output voltage characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$(1) | Output Low level voltage for an I/O pin when 8 pins are sunk at the same time | CMOS port(2),, $I_{IO}$ = +8 mA, 2.7 V < $V_{DD}$ < 3.6 V | - | 0.4 | V |
| $V_{OH}$(3) | Output High level voltage for an I/O pin when 8 pins are sourced at the same time | | $V_{DD}$–0.4 | - | |
| $V_{OL}$(1) | Output low level voltage for an I/O pin when 8 pins are sunk at the same time | TTL port(2) $I_{IO}$ = +8 mA 2.7 V < $V_{DD}$ < 3.6 V | - | 0.4 | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin when 8 pins are sourced at the same time | | 2.4 | - | |
| $V_{OL}$(1) | Output low level voltage for an I/O pin when 8 pins are sunk at the same time | $I_{IO}$ = +20 mA(4) 2.7 V < $V_{DD}$ < 3.6 V | - | 1.3 | V |
| $V_{OH}$ (3) | Output high level voltage for an I/O pin when 8 pins are sourced at the same time | | $V_{DD}$–1.3 | - | |
| $V_{OL}$(1) | Output low level voltage for an I/O pin when 8 pins are sunk at the same time | $I_{IO}$ = +6 mA(4) 2 V < $V_{DD}$ < 2.7 V | - | 0.4 | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin when 8 pins are sourced at the same time | | $V_{DD}$–0.4 | - | |

1. The $I_{IO}$ current sunk by the device must always respect the absolute maximum rating specified in *Table 6* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The $I_{IO}$ current sourced by the device must always respect the absolute maximum rating specified in *Table 6* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VDD}$.
4. Based on characterization data, not tested in production.

### Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 26* and *Table 35*, respectively.

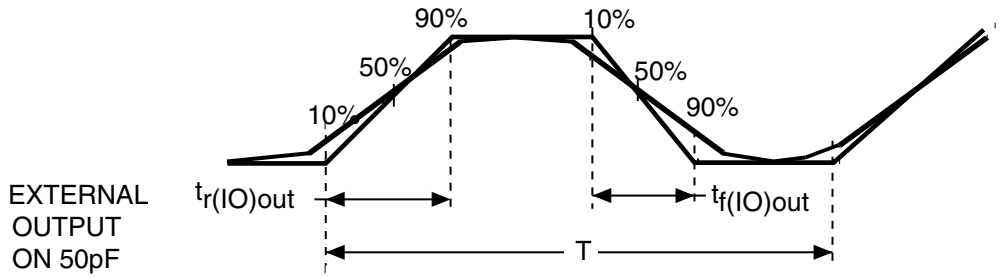
Unless otherwise specified, the parameters given in *Table 35* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 8*.

**Table 35. I/O AC characteristics(1)**

| MODEx [1:0] bit value(1) | Symbol | Parameter | Conditions | Max | Unit |
|---|---|---|---|---|---|
| 10 | $f_{max(IO)out}$ | Maximum frequency(2) | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 3.6 V | 2 | MHz |
| | $t_{f(IO)out}$ | Output high to low level fall time | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 3.6 V | 125(3) | ns |
| | $t_{r(IO)out}$ | Output low to high level rise time | | 125(3) | |
| 01 | $f_{max(IO)out}$ | Maximum frequency(2) | $C_L$= 50 pF, $V_{DD}$ = 2 V to 3.6 V | 10 | MHz |
| | $t_{f(IO)out}$ | Output high to low level fall time | $C_L$= 50 pF, $V_{DD}$ = 2 V to 3.6 V | 25(3) | ns |
| | $t_{r(IO)out}$ | Output low to high level rise time | | 25(3) | |
| 11 | $F_{max(IO)out}$ | Maximum Frequency(2) | $C_L$= 30 pF, $V_{DD}$ = 2.7 V to 3.6 V | 50 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | 30 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 2.7 V | 20 | MHz |
| | $t_{f(IO)out}$ | Output high to low level fall time | $C_L$ = 30 pF, $V_{DD}$ = 2.7 V to 3.6 V | 5(3) | ns |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | 8(3) | |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 2.7 V | 12(3) | |
| | $t_{r(IO)out}$ | Output low to high level rise time | $C_L$ = 30 pF, $V_{DD}$ = 2.7 V to 3.6 V | 5(3) | |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | 8(3) | |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 2.7 V | 12(3) | |
| - | $t_{EXTIpw}$ | Pulse width of external signals detected by the EXTI controller | - | 10 | ns |

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 26*.
3. Guaranteed by design, not tested in production.

**Figure 26. I/O AC characteristics definition**




Maximum frequency is achieved if $(t_r + t_f) \leq 2/3)T$ and if the duty cycle is (45-55%) when loaded by 50pF

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## 5.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, $R_{PU}$ (see *Table 33*).

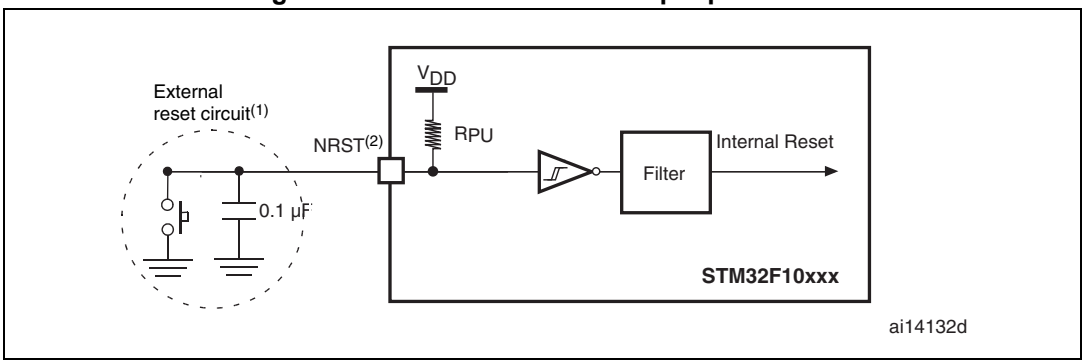
Unless otherwise specified, the parameters given in *Table 36* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 8*.

**Table 36. NRST pin characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$(1) | NRST Input low level voltage | - | –0.5 | - | 0.8 | V |
| $V_{IH(NRST)}$(1) | NRST Input high level voltage | - | 2 | - | $V_{DD}$+0.5 | |
| $V_{hys(NRST)}$ | NRST Schmitt trigger voltage hysteresis | - | - | 200 | - | mV |
| $R_{PU}$ | Weak pull-up equivalent resistor(2) | $V_{IN} = V_{SS}$ | 30 | 40 | 50 | kΩ |
| $V_{F(NRST)}$(1) | NRST Input filtered pulse | - | - | - | 100 | ns |
| $V_{NF(NRST)}$(1) | NRST Input not filtered pulse | - | 300 | - | - | ns |

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

**Figure 27. Recommended NRST pin protection**




1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 36*. Otherwise the reset will not be taken into account by the device.

### 5.3.15 TIM timer characteristics

The parameters given in *Table 37* are guaranteed by design.

Refer to *Section 5.3.12: I/O current injection characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

**Table 37. TIMx(1) characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{res(TIM)}$ | Timer resolution time | - | 1 | - | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 36 MHz | 27.8 | - | ns |
| $f_{EXT}$ | Timer external clock frequency on CH1 to CH4 | | 0 | $f_{TIMxCLK}/2$ | MHz |
| | | $f_{TIMxCLK}$ = 36 MHz | 0 | 18 | MHz |
| $Res_{TIM}$ | Timer resolution | - | - | 16 | bit |
| $t_{COUNTER}$ | 16-bit counter clock period when internal clock is selected | - | 1 | 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 36 MHz | 0.0278 | 1820 | µs |
| $t_{MAX_COUNT}$ | Maximum possible count | - | - | 65536 × 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 36 MHz | - | 119.2 | s |

1. TIMx is used as a general term to refer to the TIM2, TIM3 and TIM4 timers.

### 5.3.16 Communications interfaces

#### $I^2C$ interface characteristics

The STM32F101xx Low-density access line $I^2C$ interface meets the requirements of the standard $I^2C$ communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and $V_{DD}$ is disabled, but is still present.

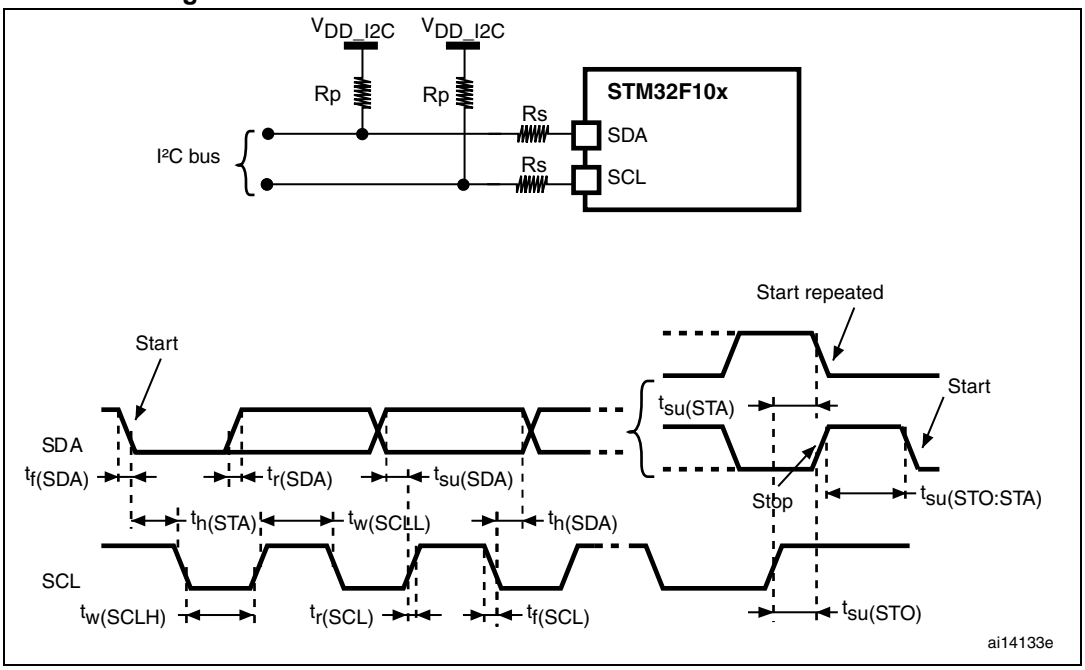
The $I^2C$ characteristics are described in *Table 38*. Refer also to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

**Table 38. $I^2C$ characteristics**

| Symbol | Parameter | Standard mode $I^2C$(1) | | Fast mode $I^2C$(1)(2) | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | - | 1.3 | - | µs |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | - | 0.6 | - | |
| $t_{su(SDA)}$ | SDA setup time | 250 | - | 100 | - | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0 | - | 0(3) | 900(4) | |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | SDA and SCL rise time | - | 1000 | 20+0.1$C_b$ | 300 | |
| $t_{f(SDA)}$ $t_{f(SCL)}$ | SDA and SCL fall time | - | 300 | - | 300 | |
| $t_{h(STA)}$ | Start condition hold time | 4.0 | - | 0.6 | - | µs |
| $t_{su(STA)}$ | Repeated Start condition setup time | 4.7 | - | 0.6 | - | |
| $t_{su(STO)}$ | Stop condition setup time | 4.0 | - | 0.6 | - | µs |
| $t_{w(STO:STA)}$ | Stop to Start condition time (bus free) | 4.7 | - | 1.3 | - | µs |
| $C_b$ | Capacitive load for each bus line | - | 400 | - | 400 | pF |

1. Guaranteed by design, not tested in production.
2. $f_{PCLK1}$ must be at least 2 MHz to achieve standard mode $I^2C$ frequencies. It must be at least 4 MHz to achieve fast mode $I^2C$ frequencies. It must be a multiple of 10 MHz to reach the 400 kHz maximum I2C fast mode clock.
3. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
4. The maximum Data hold time has only to be met if the interface does not stretch the low period of SCL signal.

**Figure 28. I²C bus AC waveforms and measurement circuit(1)**




1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.
2. Rs = Series protection resistors, Rp = Pull-up resistors, $V_{DD_I2C}$ = I2C bus supply.

**Table 39. SCL frequency ($f_{PCLK1}$= MHz, $V_{DD_I2C}$ = 3.3 V)(1)(2)**

| $f_{SCL}$ (kHz) | I2C_CCR value |
|---|---|
| | $R_P$ = 4.7 kΩ |
| 400 | 0x801E |
| 300 | 0x8028 |
| 200 | 0x803C |
| 100 | 0x00B4 |
| 50 | 0x0168 |
| 20 | 0x0384 |

1. $R_P$ = External pull-up resistance, $f_{SCL}$ = I²C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

### SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 40* are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 8*.

Refer to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

**Table 40. SPI characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | SPI clock frequency | Master mode | 0 | 18 | MHz |
| | | Slave mode | 0 | 18 | |
| $t_{r(SCK)}$<br>$t_{f(SCK)}$ | SPI clock rise and fall time | Capacitive load: C = 30 pF | | 8 | ns |
| $t_{su(NSS)}$ (1) | NSS setup time | Slave mode | 4 $t_{PCLK}$ | - | |
| $t_{h(NSS)}$ (1) | NSS hold time | Slave mode | 73 | - | |
| $t_{w(SCKH)}$ (1)<br>$t_{w(SCKL)}$ (1) | SCK high and low time | Master mode, $f_{PCLK}$ = 36 MHz, presc = 4 | 50 | 60 | |
| $t_{su(MI)}$ (1) | Data input setup time Master mode | SPI | 1 | - | |
| $t_{su(SI)}$ (1) | Data input setup time Slave mode | - | 1 | - | |
| $t_{h(MI)}$ (1) | Data input hold time Master mode | SPI | 1 | - | |
| $t_{h(SI)}$ (1) | Data input hold time Slave mode | - | 3 | - | |
| $t_{a(SO)}$ (1)(2) | Data output access time | Slave mode, $f_{PCLK}$ = 36 MHz, presc = 4 | 0 | 55 | |
| | | Slave mode, $f_{PCLK}$ = 24 MHz | 0 | 4 $t_{PCLK}$ | |
| $t_{dis(SO)}$ (1)(3) | Data output disable time | Slave mode | 10 | | |
| $t_{v(SO)}$ (1) | Data output valid time | Slave mode (after enable edge) | - | 25 | |
| $t_{v(MO)}$ (1) | Data output valid time | Master mode (after enable edge) | - | 3 | |
| $t_{h(SO)}$ (1) | Data output hold time | Slave mode (after enable edge) | 25 | - | |
| $t_{h(MO)}$ (1) | | Master mode (after enable edge) | 4 | - | |

1. Based on characterization, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

**Figure 29. SPI timing diagram - slave mode and CPHA = 0**

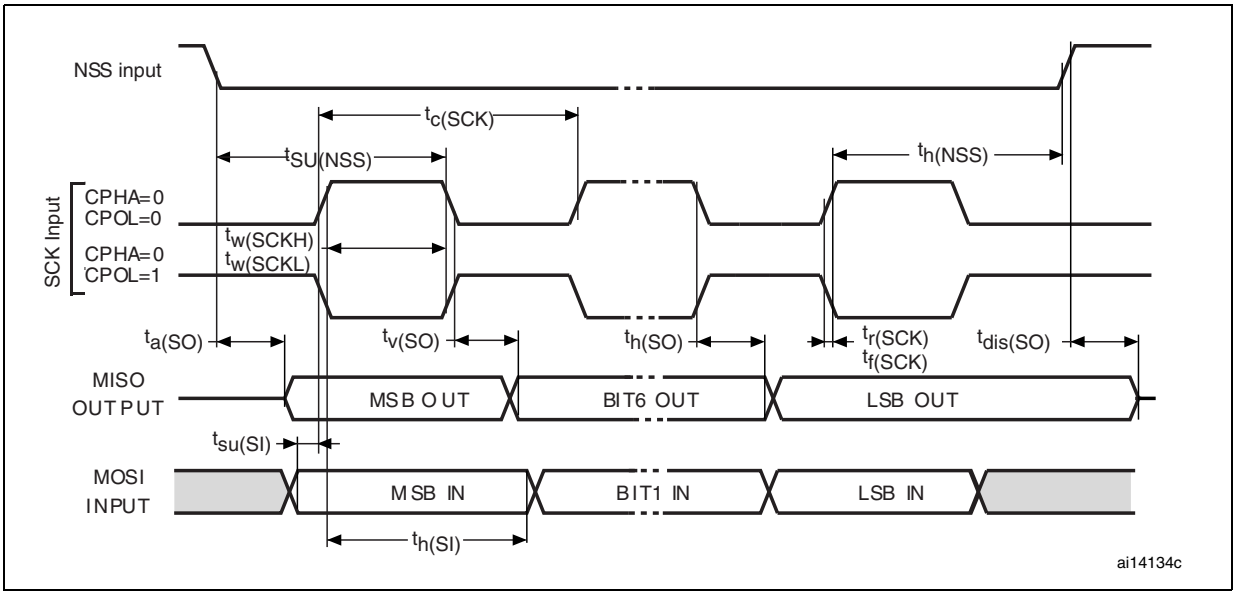
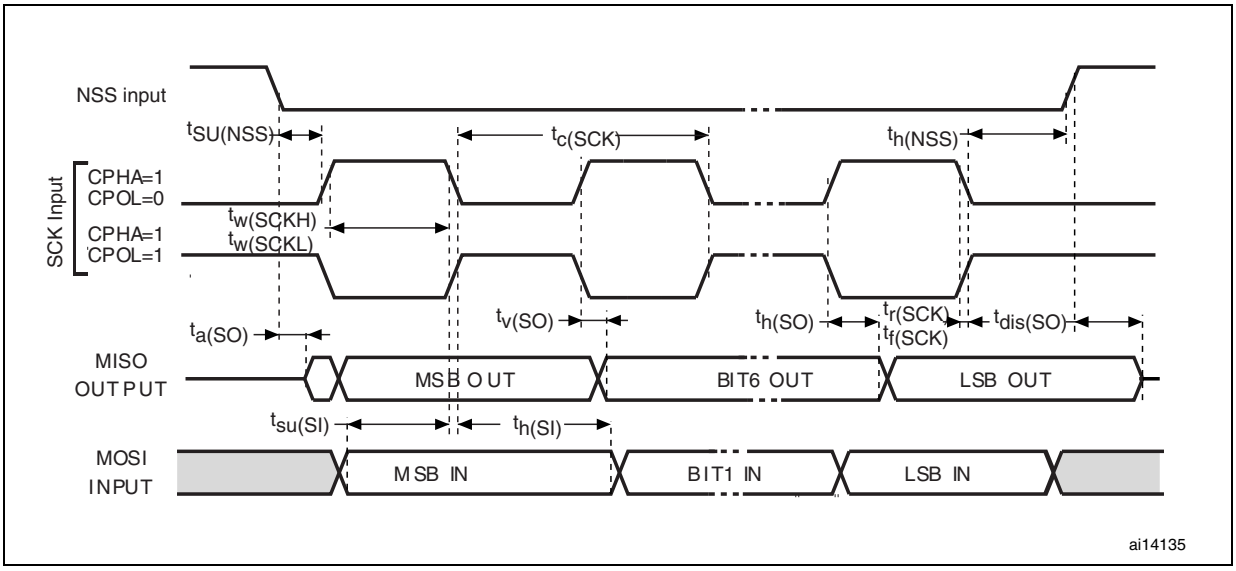
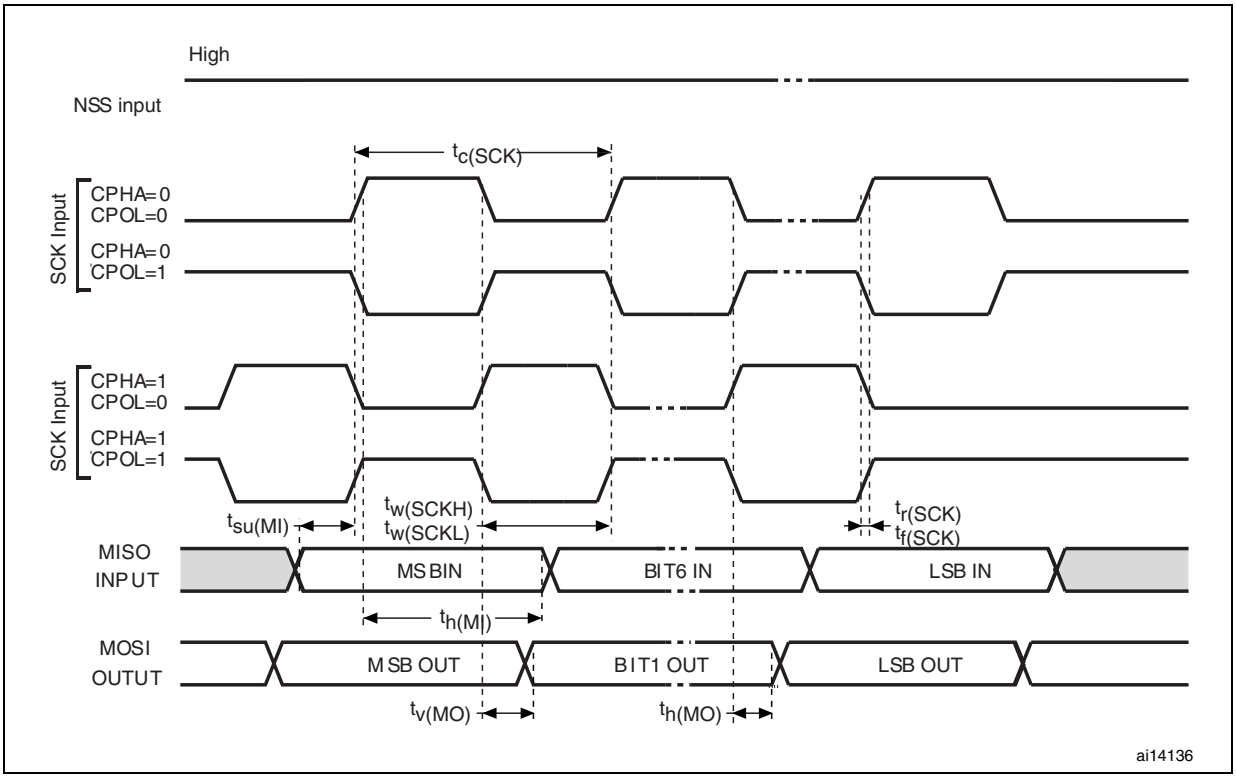



**Figure 30. SPI timing diagram - slave mode and CPHA = 1(1)**




1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

**Figure 31. SPI timing diagram - master mode(1)**




1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

### 5.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 41* are derived from tests performed under the ambient temperature, $f_{PCLK2}$ frequency and $V_{DDA}$ supply voltage conditions summarized in *Table 8*.

*Note: It is recommended to perform a calibration after each power-up.*

**Table 41. ADC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Power supply | - | 2.4 | - | 3.6 | V |
| $f_{ADC}$ | ADC clock frequency | - | 0.6 | - | 14 | MHz |
| $f_S$(1) | Sampling rate | - | 0.043 | - | 1 | MHz |
| $f_{TRIG}$(1) | External trigger frequency | $f_{ADC}$ = 14 MHz | - | - | 823 | kHz |
| | | - | - | - | 17 | $1/f_{ADC}$ |
| $V_{AIN}$ | Conversion voltage range(2) | - | 0 ($V_{SSA}$ or $V_{REF-}$ tied to ground) | - | $V_{REF+}$ | V |
| $R_{AIN}$(1) | External input impedance | See *Equation 1* and *Table 42* for details | - | - | 50 | kΩ |
| $R_{ADC}$(1) | Sampling switch resistance | - | - | - | 1 | kΩ |
| $C_{ADC}$(1) | Internal sample and hold capacitor | - | - | - | 8 | pF |
| $t_{CAL}$(1) | Calibration time | $f_{ADC}$ = 14 MHz | 5.9 | | | µs |
| | | - | 83 | | | $1/f_{ADC}$ |
| $t_{lat}$(1) | Injection trigger conversion latency | $f_{ADC}$ = 14 MHz | - | - | 0.214 | µs |
| | | - | - | - | 3(3) | $1/f_{ADC}$ |
| $t_{latr}$(1) | Regular trigger conversion latency | $f_{ADC}$ = 14 MHz | - | - | 0.143 | µs |
| | | - | - | - | 2(3) | $1/f_{ADC}$ |
| $t_S$(1) | Sampling time | $f_{ADC}$ = 14 MHz | 0.107 | - | 17.1 | µs |
| | | | 1.5 | - | 239.5 | $1/f_{ADC}$ |
| $t_{STAB}$(1) | Stabilization time | - | 14 | | | $1/f_{ADC}$ |
| $t_{CONV}$(1) | Total conversion time (including sampling time) | $f_{ADC}$ = 14 MHz | 1 | - | 18 | µs |
| | | - | 14 to 252 ($t_S$ for sampling +12.5 for successive approximation) | | | $1/f_{ADC}$ |

1. Guaranteed by design, not tested in production.
2. $V_{REF+}$ is internally connected to $V_{DDA}$ and $V_{REF-}$ is be internally connected to $V_{SSA}$.
3. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 41*.

**Equation 1: $R_{AIN}$ max formula:**

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

**Table 42. $R_{AIN}$ max for $f_{ADC}$ = 14 MHz(1)**

| $T_s$ (cycles) | $t_S$ (µs) | $R_{AIN}$ max (kΩ) |
|---|---|---|
| 1.5 | 0.11 | 0.4 |
| 7.5 | 0.54 | 5.9 |
| 13.5 | 0.96 | 11.4 |
| 28.5 | 2.04 | 25.2 |
| 41.5 | 2.96 | 37.2 |
| 55.5 | 3.96 | 50 |
| 71.5 | 5.11 | NA |
| 239.5 | 17.1 | NA |

1. Guaranteed by design, not tested in production.

**Table 43. ADC accuracy - limited test conditions(1) (2)**

| Symbol | Parameter | Test conditions | Typ | Max(3) | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error | $f_{PCLK2}$ = 28 MHz, $f_{ADC}$ = 14 MHz, $R_{AIN}$ < 10 kΩ, $V_{DDA}$ = 3 V to 3.6 V $T_A$ = 25 °C Measurements made after ADC calibration | ±1.3 | ±2 | LSB |
| EO | Offset error | | ±1 | ±1.5 | |
| EG | Gain error | | ±0.5 | ±1.5 | |
| ED | Differential linearity error | | ±0.7 | ±1 | |
| EL | Integral linearity error | | ±0.8 | ±1.5 | |

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.12* does not affect the ADC accuracy.
3. Based on characterization, not tested in production.

**Table 44. ADC accuracy(1) (2) (3)**

| Symbol | Parameter | Test conditions | Typ | Max(4) | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error | $f_{PCLK2}$ = 28 MHz, $f_{ADC}$ = 14 MHz, $R_{AIN}$ < 10 kΩ, $V_{DDA}$ = 2.4 V to 3.6 V Measurements made after ADC calibration | ±2 | ±5 | LSB |
| EO | Offset error | | ±1.5 | ±2.5 | |
| EG | Gain error | | ±1.5 | ±3 | |
| ED | Differential linearity error | | ±1 | ±2 | |
| EL | Integral linearity error | | ±1.5 | ±3 | |

1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted $V_{DD}$, frequency and temperature ranges.
3. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.12* does not affect the ADC accuracy.
4. Based on characterization, not tested in production.

**Figure 32. ADC accuracy characteristics**

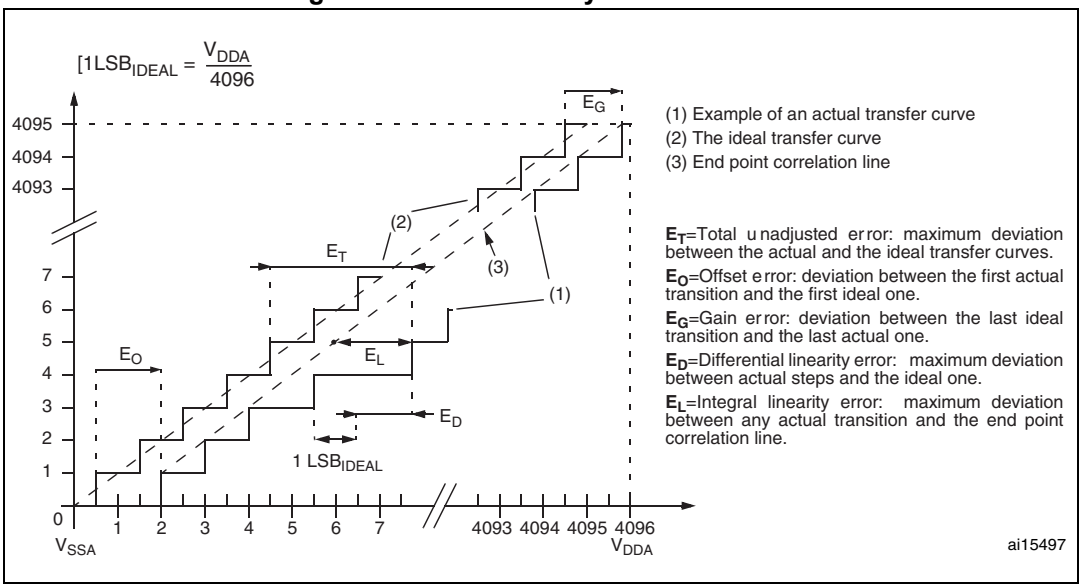
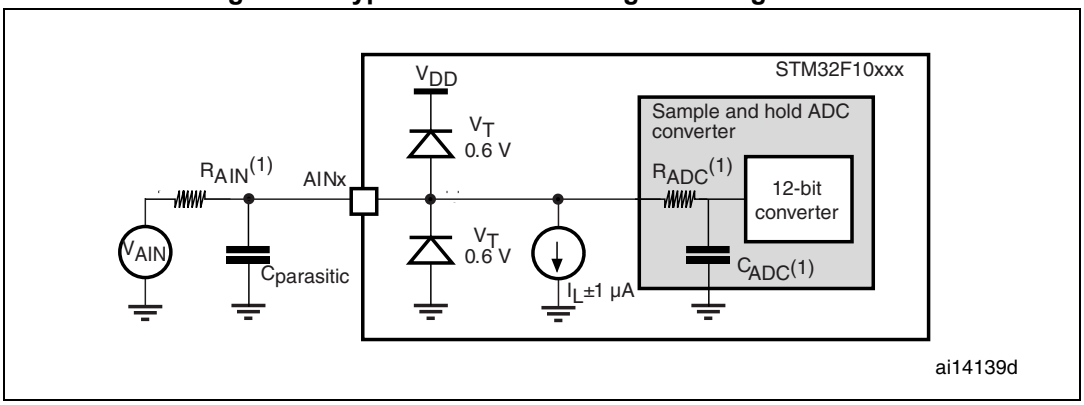


**Figure 33. Typical connection diagram using the ADC**

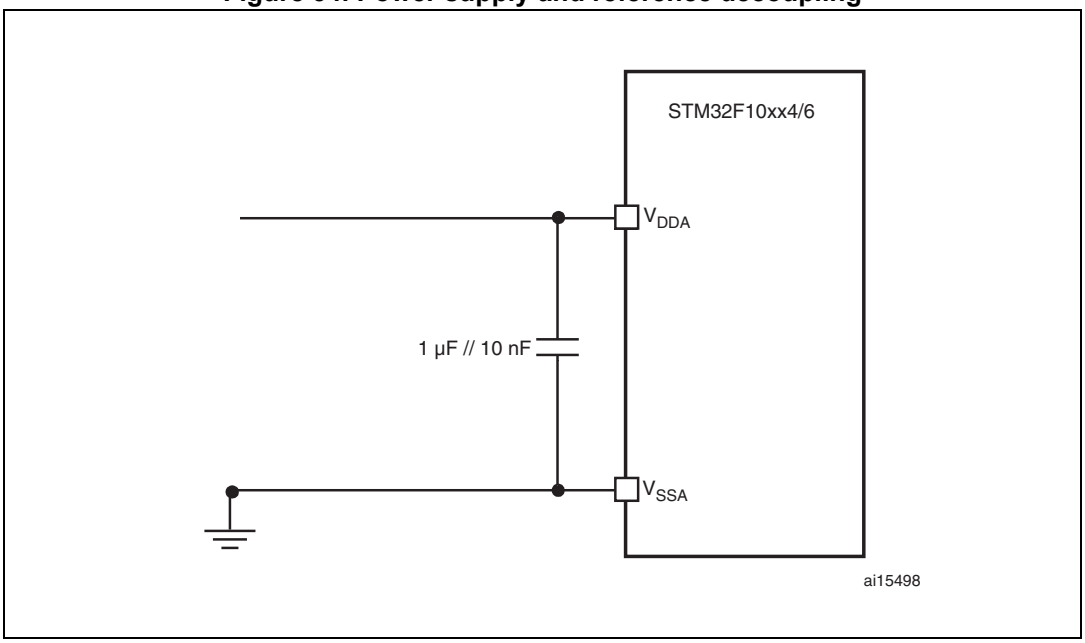



1. Refer to *Table 41* for the values of $R_{AIN}$, $R_{ADC}$ and $C_{ADC}$.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

## General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 34*. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

**Figure 34. Power supply and reference decoupling**



### 5.3.18 Temperature sensor characteristics

**Table 45. TS characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_L$[1] | $V_{SENSE}$ linearity with temperature | - | ±1 | ±2 | °C |
| Avg_Slope[1] | Average slope | 4.0 | 4.3 | 4.6 | mV/°C |
| $V_{25}$[1] | Voltage at 25°C | 1.34 | 1.43 | 1.52 | V |
| $t_{START}$[2] | Startup time | 4 | - | 10 | µs |
| $T_{S_temp}$[3][2] | ADC sampling time when reading the temperature | - | - | 17.1 | µs |

1. Guaranteed by characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

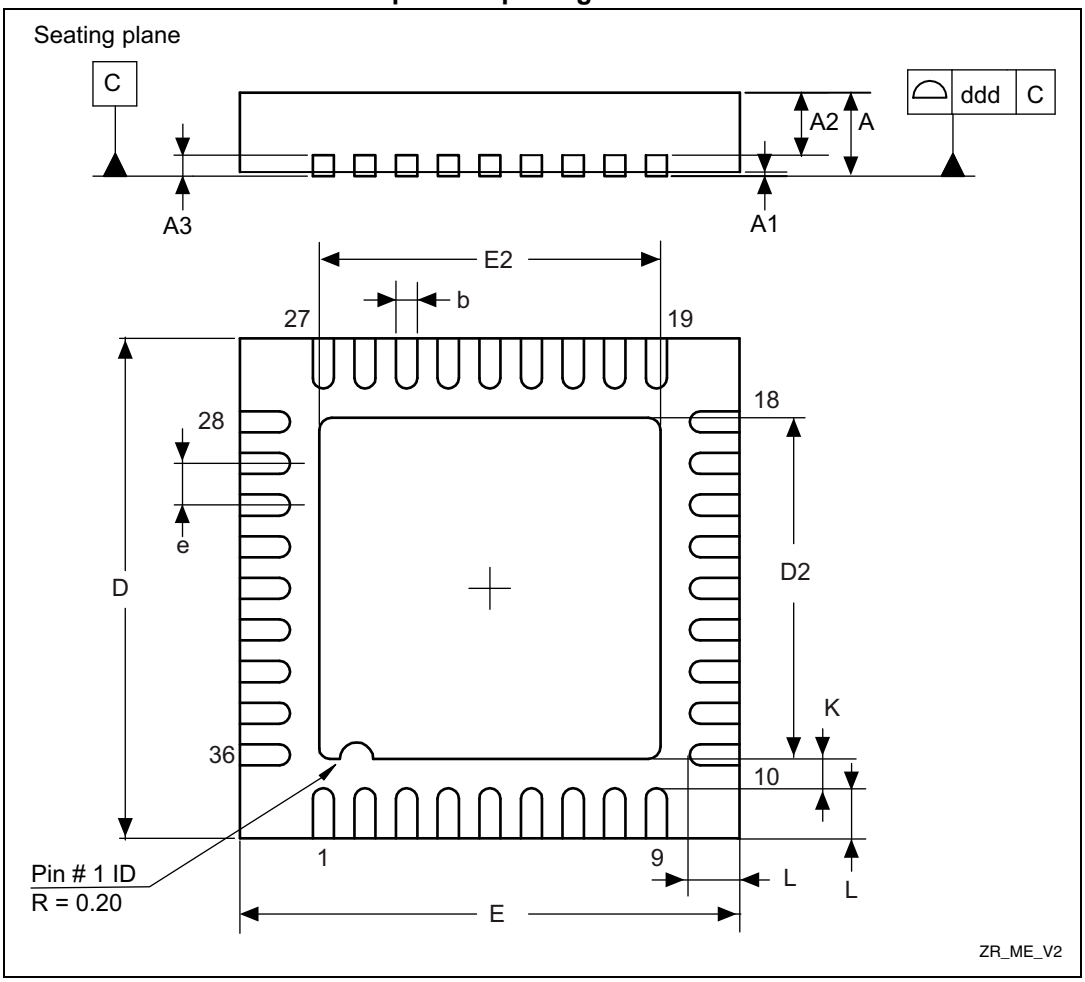
# 6 Package characteristics

## 6.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

## 6.2 VFQFPN36 package information

**Figure 35. VFQFPN36 - 36-pin, 6x6 mm, 0.5 mm pitch very thin profile fine pitch quad flat package outline**



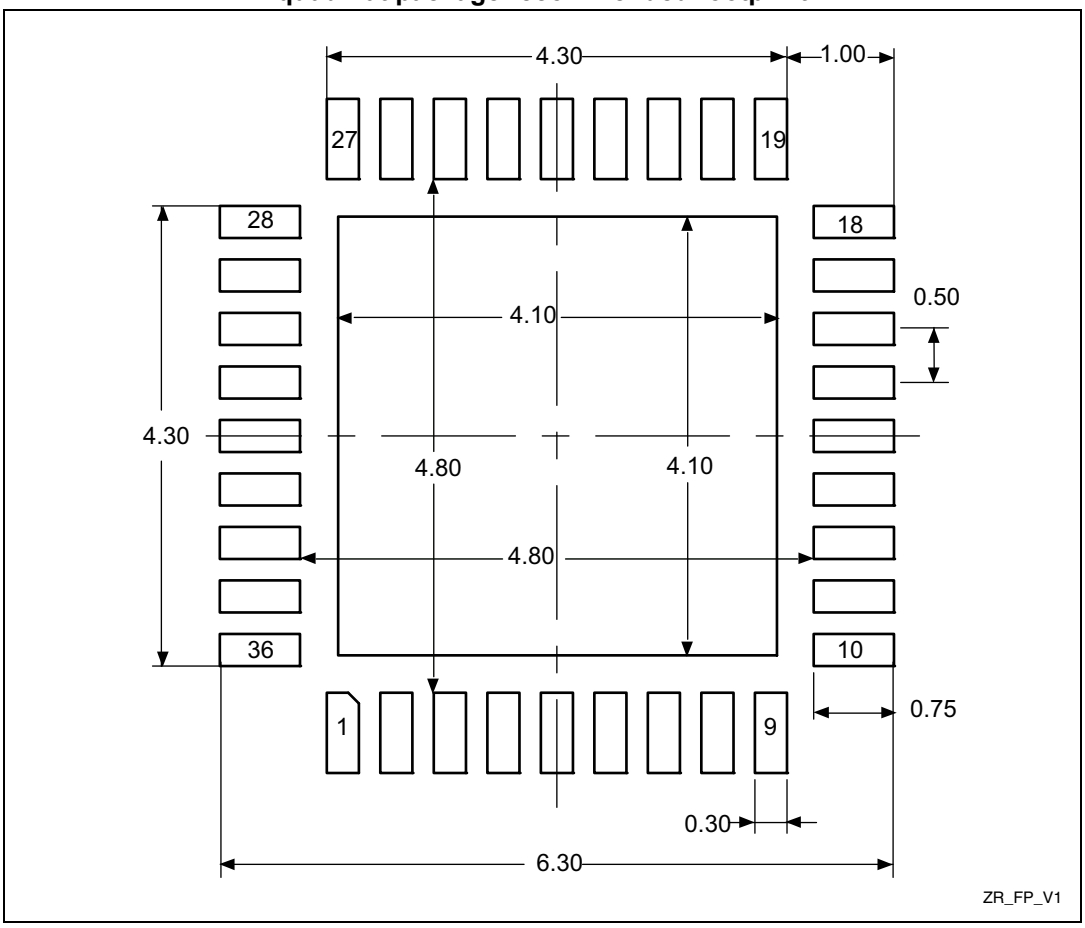

1. Drawing is not to scale.

**Table 46. VFQFPN36 - 36-pin, 6x6 mm, 0.5 mm pitch very thin profile fine pitch quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.800 | 0.900 | 1.000 | 0.0315 | 0.0354 | 0.0394 |
| A1 | - | 0.020 | 0.050 | - | 0.0008 | 0.0020 |
| A2 | - | 0.650 | 1.000 | - | 0.0256 | 0.0394 |
| A3 | - | 0.200 | - | - | 0.0079 | - |
| b | 0.180 | 0.230 | 0.300 | 0.0071 | 0.0091 | 0.0118 |
| D | 5.875 | 6.000 | 6.125 | 0.2313 | 0.2362 | 0.2411 |
| D2 | 1.750 | 3.700 | 4.250 | 0.0689 | 0.1457 | 0.1673 |
| E | 5.875 | 6.000 | 6.125 | 0.2313 | 0.2362 | 0.2411 |
| E2 | 1.750 | 3.700 | 4.250 | 0.0689 | 0.1457 | 0.1673 |
| e | 0.450 | 0.500 | 0.550 | 0.0177 | 0.0197 | 0.0217 |
| L | 0.350 | 0.550 | 0.750 | 0.0138 | 0.0217 | 0.0295 |
| K | 0.250 | - | - | 0.0098 | - | - |
| ddd | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 36. VFQFPN36 - 36-pin, 6x6 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint**

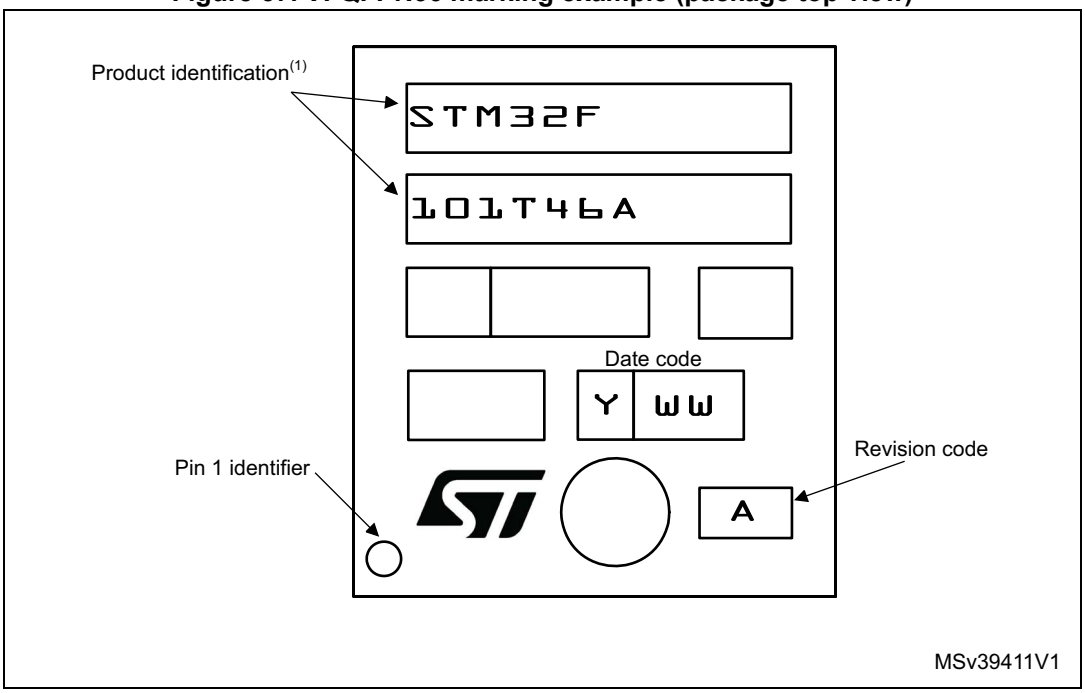



1. Dimensions are expressed in millimeters.

### Device Marking for VFQFPN36

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

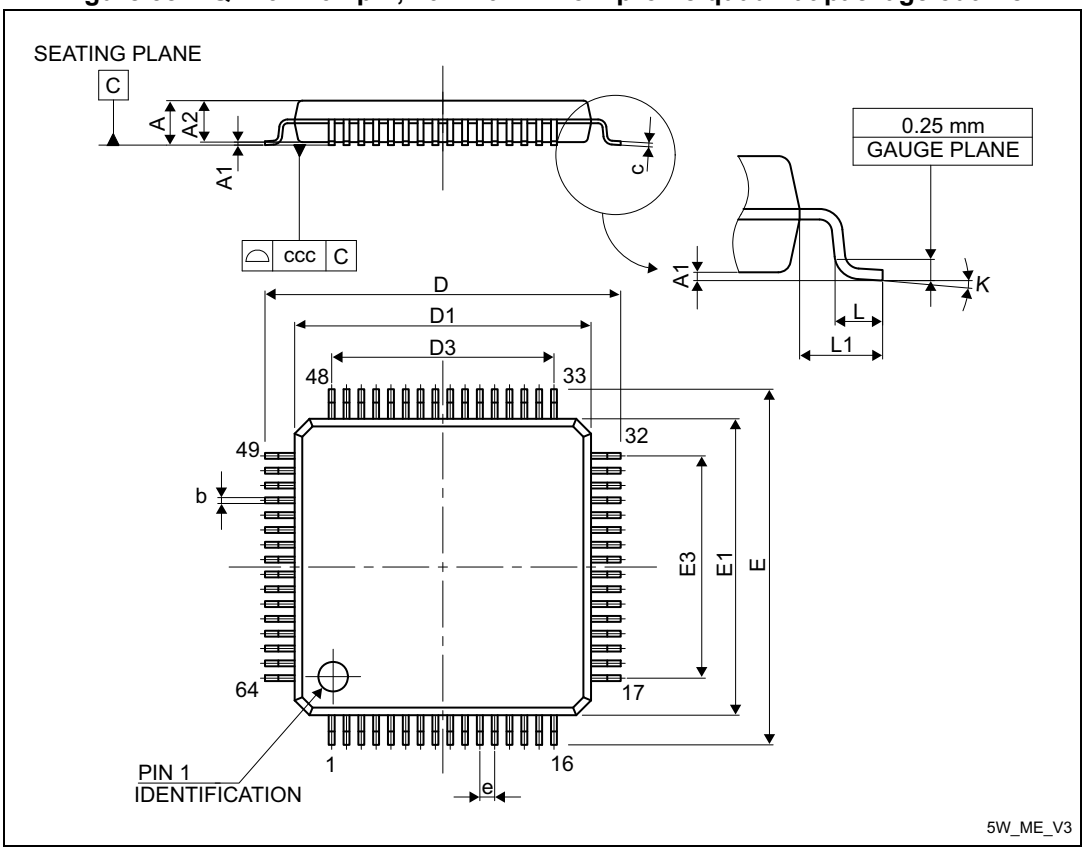
**Figure 37. VFQFPN36 marking example (package top view)**




1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

## 6.3 LQFP64 package information

**Figure 38. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline**




1. Drawing is not to scale.

**Table 47. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data**

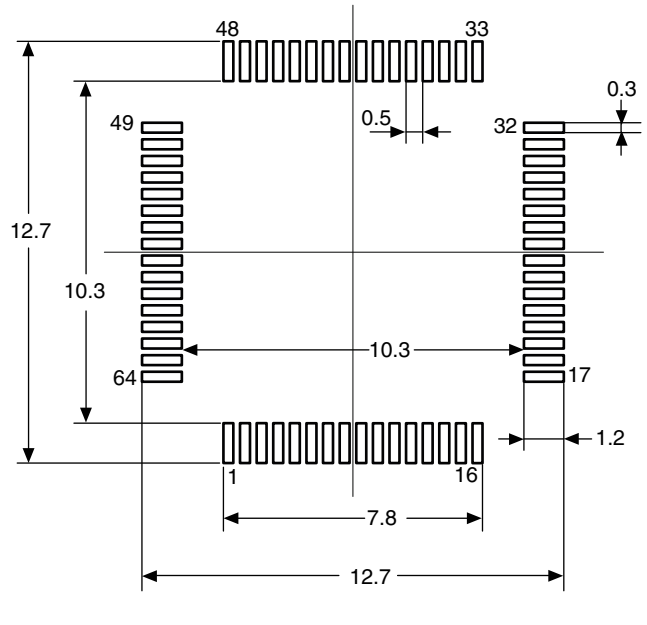
| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | - | 12.000 | - | - | 0.4724 | - |
| D1 | - | 10.000 | - | - | 0.3937 | - |
| D3 | - | 7.500 | - | - | 0.2953 | - |
| E | - | 12.000 | - | - | 0.4724 | - |
| E1 | - | 10.000 | - | - | 0.3937 | - |

**Table 47. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| E3 | - | 7.500 | - | - | 0.2953 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| K | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 39. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint**

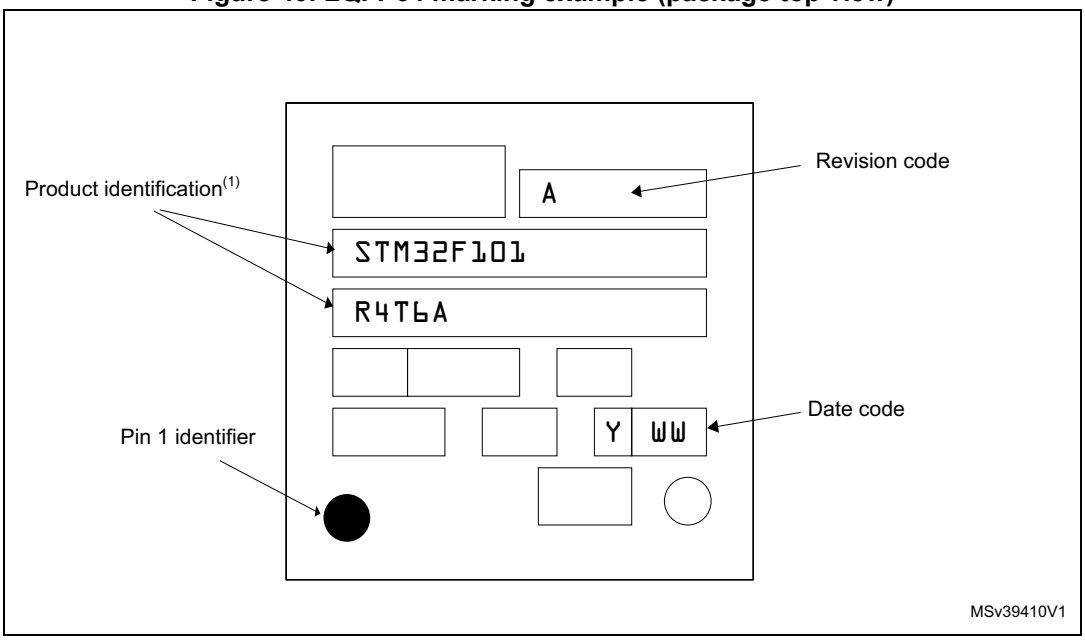



1. Dimensions are expressed in millimeters.

### Device Marking for LQFP64

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

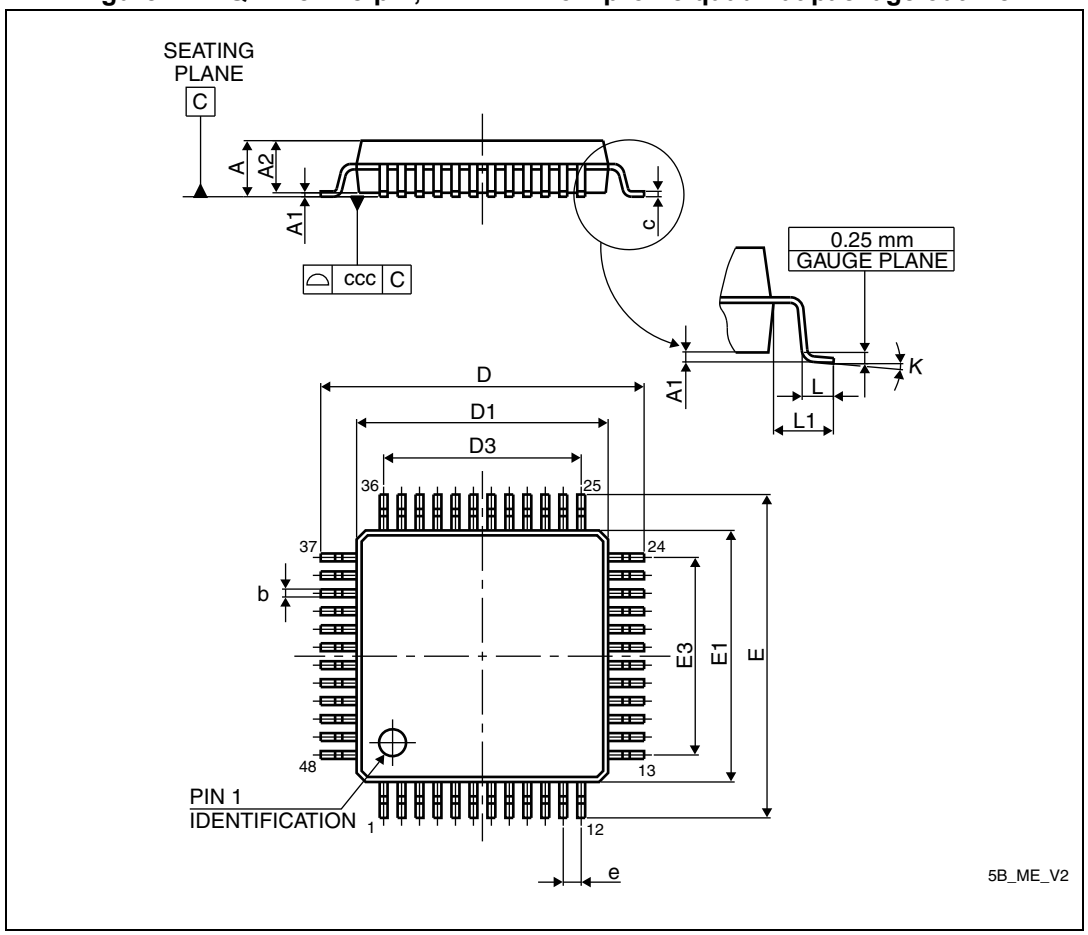
**Figure 40. LQFP64 marking example (package top view)**




1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

## 6.4 LQFP48 package information

**Figure 41. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline**



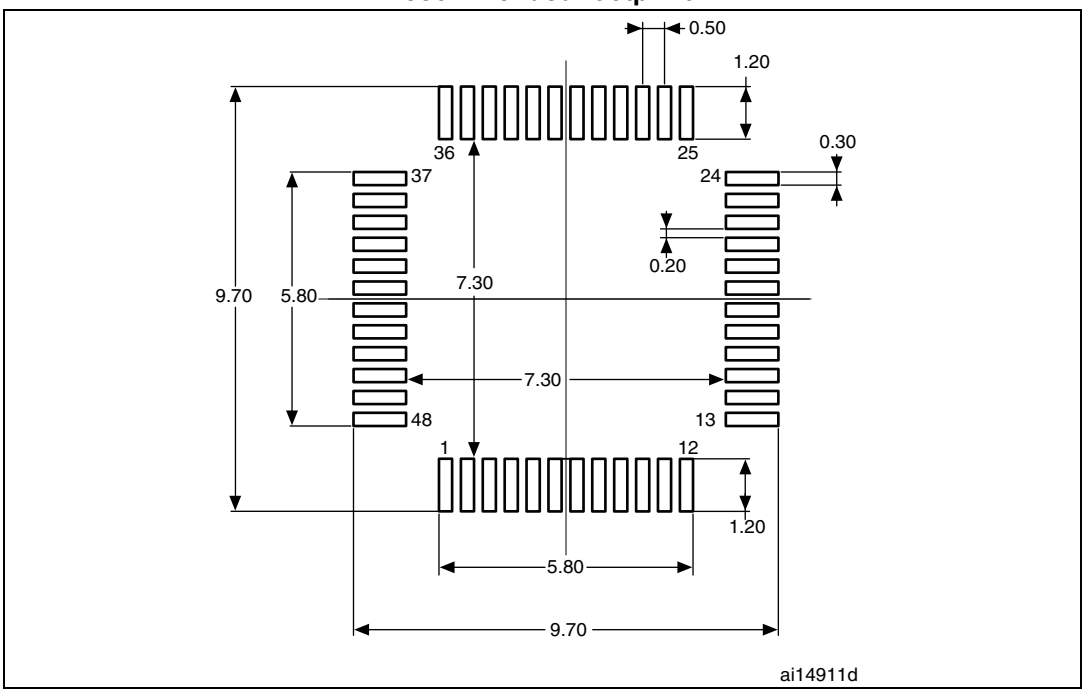

1. Drawing is not to scale.

**Table 48. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | - | 5.500 | - | - | 0.2165 | - |
| E | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| E3 | - | 5.500 | - | - | 0.2165 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 42. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint**

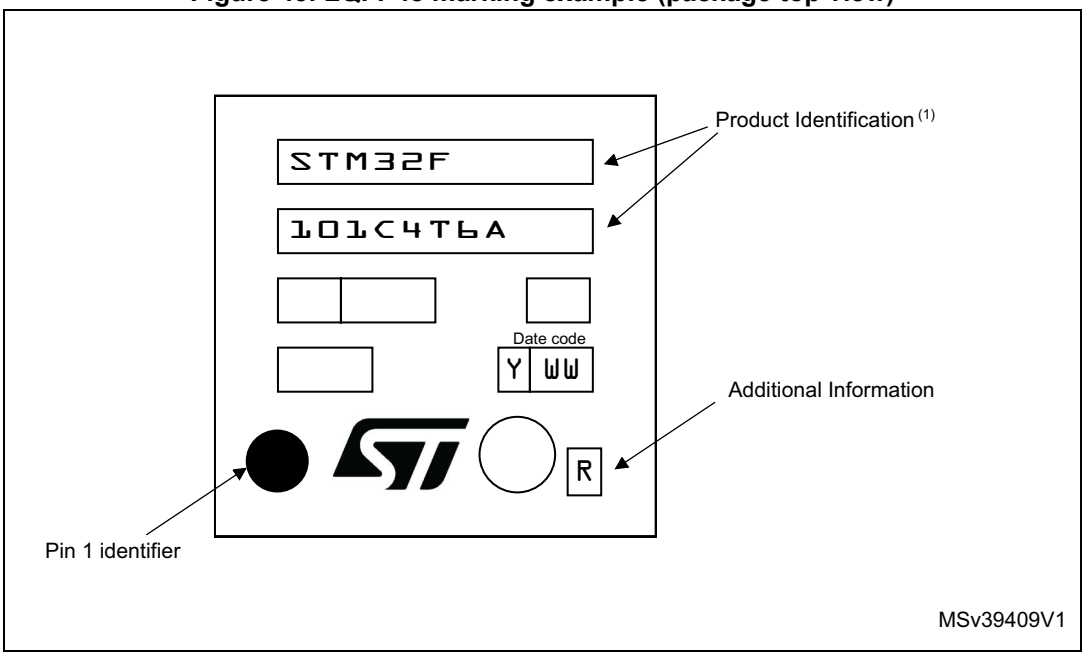



1. Dimensions are expressed in millimeters.

### Device Marking for LQFP48

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

**Figure 43. LQFP48 marking example (package top view)**




1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

## 6.5 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 8: General operating conditions on page 31*.

The maximum chip-junction temperature, $T_J$ max, in degrees Celsius, may be calculated using the following equation:

$T_J$ max = $T_A$ max + ($P_D$ max x $\Theta_{JA}$)

Where:

- $T_A$ max is the maximum ambient temperature in °C,
- $\Theta_{JA}$ is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D$ max is the sum of $P_{INT}$ max and $P_{I/O}$ max ($P_D$ max = $P_{INT}$ max + $P_{I/O}$max),
- $P_{INT}$ max is the product of $I_{DD}$ and $V_{DD}$, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual $V_{OL}$ / $I_{OL}$ and $V_{OH}$ / $I_{OH}$ of the I/Os at low and high level in the application.

**Table 49. Package thermal characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\Theta_{JA}$ | **Thermal resistance junction-ambient** LQFP 64 - 10 x 10 mm / 0.5 mm pitch | 45 | °C/W |
| | **Thermal resistance junction-ambient** LQFP 48 - 7 x 7 mm / 0.5 mm pitch | 55 | |
| | **Thermal resistance junction-ambient** UFQFPN 48 - 6 x 6 mm / 0.5 mm pitch | 32 | |
| | **Thermal resistance junction-ambient** VFQFPN 36 - 6 x 6 mm / 0.5 mm pitch | 18 | |

### 6.5.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

### 6.5.2 Evaluating the maximum junction temperature for an application

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 50: Ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature. Here, only temperature range 6 is available (–40 to 85 °C).

The following example shows how to calculate the temperature range needed for a given application, making it possible to check whether the required temperature range is compatible with the STM32F101xx junction temperature range.

#### Example: high-performance application

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax}$ = 82 °C (measured according to JESD51-2), $I_{DDmax}$ = 50 mA, $V_{DD}$ = 3.5 V, maximum 20 I/Os used at the same time in output at low level with $I_{OL}$ = 8 mA, $V_{OL}$= 0.4 V and maximum 8 I/Os used at the same time in output mode at low level with $I_{OL}$ = 20 mA, $V_{OL}$= 1.3 V

$P_{INTmax}$ = 50 mA × 3.5 V= 175 mW

$P_{IOmax}$ = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: $P_{INTmax}$ = 175 mW and $P_{IOmax}$ = 272 mW

$P_{Dmax}$ = 175 + 272 = 447 mW

Thus: $P_{Dmax}$ = 447 mW

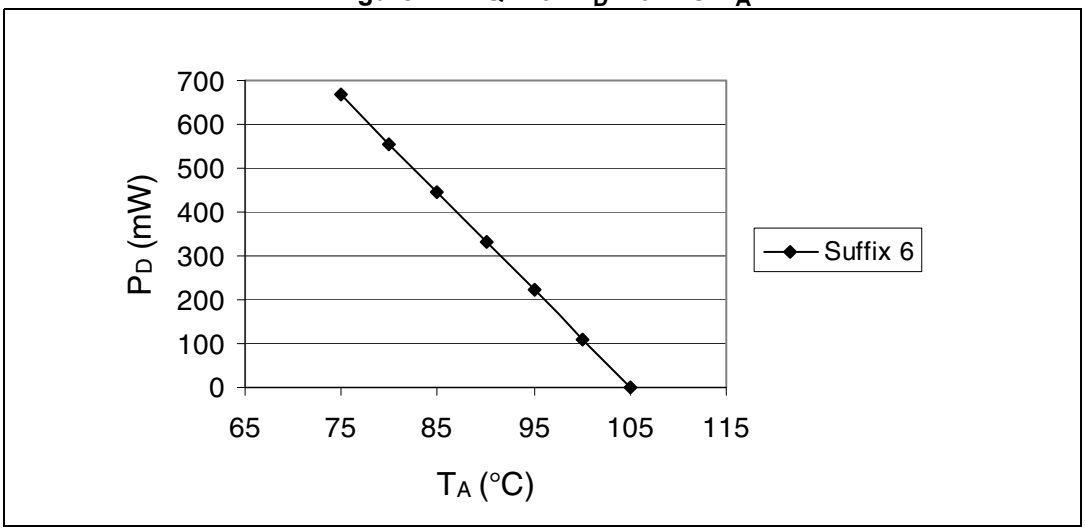
Using the values obtained in *Table 49* $T_{Jmax}$ is calculated as follows:

– For LQFP64, 45 °C/W

$T_{Jmax}$ = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.1 °C = 102.1 °C

This is within the junction temperature range of the STM32F101xx (–40 < $T_J$ < 105 °C).

**Figure 44. LQFP64 $P_D$ max vs. $T_A$**



# 7 Ordering information scheme

**Table 50. Ordering information scheme**

Example: STM32 F 101 C 4 T 6 A xxx

**Device family**

STM32 = ARM-based 32-bit microcontroller

**Product type**

F = general-purpose

Device subfamily

101 = access line

Pin count

T = 36 pins

C = 48 pins

R = 64 pins

**Flash memory size**

4 = 16 Kbytes of Flash memory

6 = 32 Kbytes of Flash memory

**Package**

T = LQFP

U = VFQFPN

**Temperature range**

6 = Industrial temperature range, –40 to 85 °C.

**Internal code**

“A” or blank(1)

Options

xxx = programmed parts

TR = tape and real

1. For STM32F101x6 devices with a blank internal code, please refer to the STM32F103x6/8/B datasheet available from the ST website: www.st.com.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact the nearest ST sales office.

# 8 Revision history

**Table 51. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 23-Sep-2008 | 1 | Initial release. |
| 07-Apr-2009 | 2 | I/O information clarified *on page 1*. *Figure 7: Memory map* modified.<br>In *Table 4: Low-density STM32F101xx pin definitions*: PB4, PB13, PB14, PB15, PB3/TRACESWO moved from Default column to Remap column.<br>$V_{REF-}$ is not available in the offered packages: *Figure 1: STM32F101xx Low-density access line block diagram*, *Figure 10: Power supply scheme* and *Figure 34: Power supply and reference decoupling* updated, *Figure 30: Power supply and reference decoupling (VREF+ not connected to VDDA)* removed.<br>Note modified in *Table 12: Maximum current consumption in Run mode, code with data processing running from Flash* and *Table 14: Maximum current consumption in Sleep mode, code running from Flash or RAM*. *Figure 15*, *Figure 16* and *Figure 17* show typical curves.<br>$ACC_{HSI}$ max values modified in *Table 23: HSI oscillator characteristics*. Small text changes. |
| 24-Sep-2009 | 3 | *Note 5* updated and *Note 4* added in *Table 4: Low-density STM32F101xx pin definitions*.<br>$V_{RERINT}$ and $T_{Coeff}$ added to *Table 11: Embedded internal reference voltage*. Typical $I_{DD_VBAT}$value added in *Table 15: Typical and maximum current consumptions in Stop and Standby modes*. *Figure 14: Typical current consumption on VBAT with RTC on versus temperature at different VBAT values* added.<br>$f_{HSE_ext}$ min modified in *Table 19: High-speed external user clock characteristics*.<br>$C_{L1}$ and $C_{L2}$ replaced by C in *Table 21: HSE 4-16 MHz oscillator characteristics* and *Table 22: LSE oscillator characteristics (fLSE = 32.768 kHz)*, notes modified and moved below the tables.<br>*Note 1* modified below *Figure 20: Typical application with an 8 MHz crystal*.<br>*Table 23: HSI oscillator characteristics* modified. Conditions removed from *Table 25: Low-power mode wakeup timings*.<br>*Figure 27: Recommended NRST pin protection* modified.<br>IEC 1000 standard updated to IEC 61000 and SAE J1752/3 updated to IEC 61967-2 in *Section 5.3.10: EMC characteristics on page 49*.<br>Jitter added to *Table 26: PLL characteristics*.<br>$C_{ADC}$ and $R_{AIN}$ parameters modified in *Table 41: ADC characteristics*. $R_{AIN}$ max values modified in *Table 42: RAIN max for fADC = 14 MHz*.<br>Small text changes. |
| 20-May-2010 | 4 | Added VFQFPN48 package.<br>Updated note 2 below *Table 38: I2C characteristics*<br>Updated *Figure 28: I2C bus AC waveforms and measurement circuit(1)*<br>Updated *Figure 27: Recommended NRST pin protection*<br>Updated *Section 5.3.12: I/O current injection characteristics* |

**Table 51. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 19-Apr-2011 | 5 | Updated footnotes below *Table 5: Voltage characteristics on page 30* and *Table 6: Current characteristics on page 31*<br>Updated tw min in *Table 19: High-speed external user clock characteristics on page 43*<br>Updated startup time in *Table 22: LSE oscillator characteristics (fLSE = 32.768 kHz) on page 46*<br>Added *Section 5.3.12: I/O current injection characteristics*<br>Updated *Section 5.3.13: I/O port characteristics* |
| 25-Sep-2015 | 6 | Updated:<br>– All GPIOs are high current...' in *Section 2.3.22: GPIOs (general-purpose inputs/outputs)*<br>– first sentence in *Output driving current*<br>– *Table 2: Low-density STM32F101xx device features and peripheral counts*, *Table 4: Low-density STM32F101xx pin definitions*,<br>– *Table 6: Current characteristics*<br>– *Table 8: General operating conditions*<br>– *Table 18: Peripheral current consumption*<br>– notes in *Table 38: I2C characteristics*<br>– note *2.* in *Table 44: ADC accuracy*<br>– title of *Table 39: SCL frequency (fPCLK1= MHz, VDD_I2C = 3.3 V)*<br>– reference for '$V_{ESD(CDM)}$' in *Table 30: ESD absolute maximum ratings*<br>– *Table 50: Ordering information scheme*,<br>– *Table 49: Package thermal characteristics*,<br>– *Figure 28: I2C bus AC waveforms and measurement circuit(1)*<br>Added<br>– note *5.* in *Table 23: HSI oscillator characteristics*<br>– *Figure 37: VFQFPN36 marking example (package top view)*<br>– *Figure 40: LQFP64 marking example (package top view)*<br>– *Figure 43: LQFP48 marking example (package top view)*<br>Corrected<br>– Corrected 'tf(IO)out' in *Figure 26: I/O AC characteristics definition*<br>– Sigma letter in *Section 5.1.1: Minimum and maximum values*<br>Removed<br>– UFDFPN48 package<br>– First sentence in *Section 5.3.16: Communications interfaces* |

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