

# 74LV573

Octal D-type transparent latch; 3-state

Rev. 03 — 15 April 2009

Product data sheet

## 1. General description

The 74LV573 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC573 and 74HCT573.

The 74LV573 consists of eight D-type transparent latches, featuring separate D-type inputs for each latch and 3-state true outputs for bus-oriented applications. A latch enable (LE) input and an output enable ( $\overline{OE}$ ) input are common to all internal latches.

When LE is HIGH, data at the Dn inputs enters the latches. In this condition, the latches are transparent, that is, a latch output will change each time its corresponding D-input changes. When LE is LOW, the latches store the information that was present at the D-inputs one set-up time preceding the HIGH-to-LOW transition of LE.

When  $\overline{OE}$  is LOW, the contents of the eight latches are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high-impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the latches.

The 74LV573 is functionally identical to the 74LV373, but has a different pin arrangement.

## 2. Features

- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between  $V_{CC} = 2.7$  V and  $V_{CC} = 3.6$  V
- Typical output ground bounce < 0.8 V at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C
- Typical HIGH-level output voltage ( $V_{OH}$ ) undershoot: > 2 V at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Common 3-state output enable input
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from  $-40$  °C to  $+85$  °C and from  $-40$  °C to  $+125$  °C

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LV573N	-40 °C to +125 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74LV573D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LV573DB	-40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74LV573PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

### 4. Functional diagram

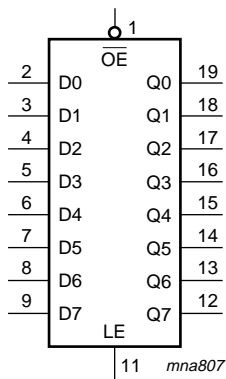


Fig 1. Logic symbol

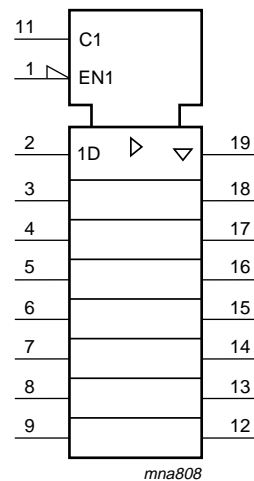


Fig 2. IEC logic symbol

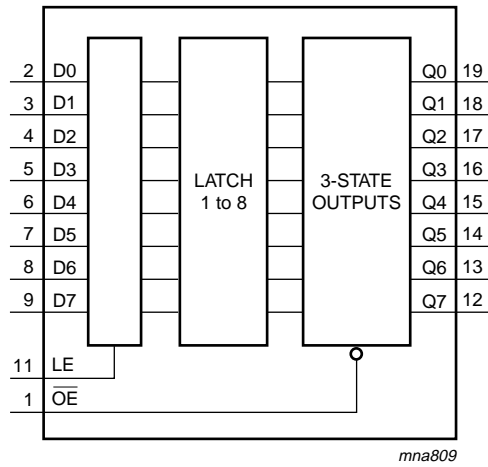


Fig 3. Functional diagram

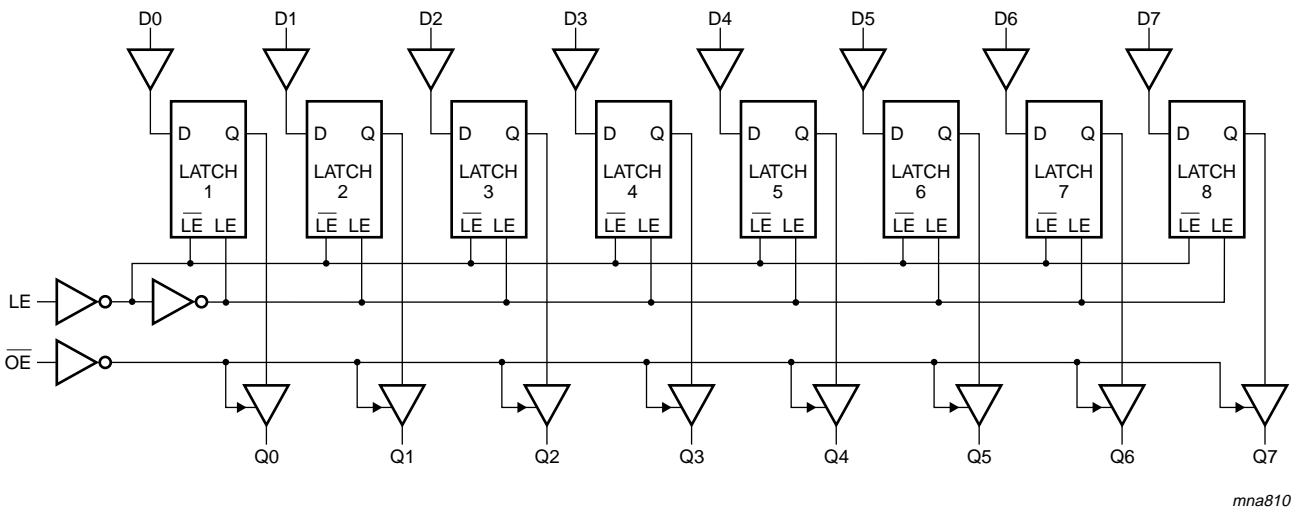


Fig 4. Logic diagram

## 5. Pinning information

### 5.1 Pinning

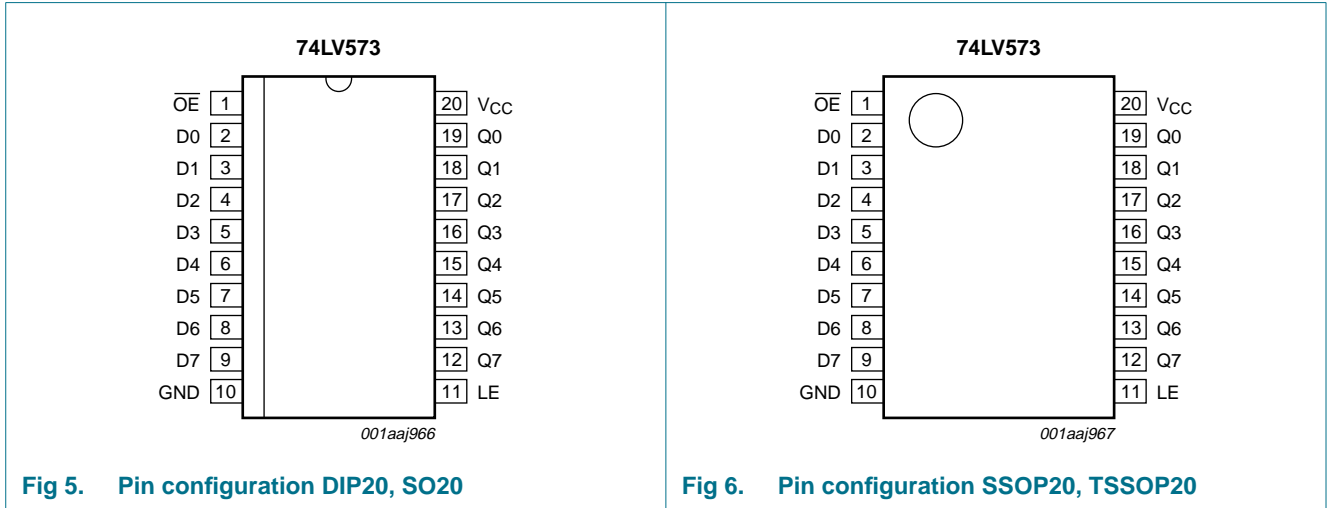


Fig 5. Pin configuration DIP20, SO20

Fig 6. Pin configuration SSOP20, TSSOP20

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
OE	1	output enable input (active LOW)
D0 to D7	2, 3, 4, 5, 6, 7, 8, 9	data input
GND	10	ground (0 V)
LE	11	latch enable input (active HIGH)
Q0 to Q7	19, 18, 17, 16, 15, 14, 13, 12	data output
VCC	20	supply voltage

## 6. Functional description

Table 3. Functional table<sup>[1]</sup>

Operating modes	Input			Internal latch	Output
	OE	LE	Dn		
Enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

[1] H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition; L = LOW voltage level; l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition; Z = high-impedance OFF-state.

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	[1] -	20	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	[1] -	50	mA
$I_O$	output current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$	-	35	mA
$I_{CC}$	supply current		-	70	mA
$I_{GND}$	ground current		-70	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$	[2]		
		DIP20	-	750	mW
		SO20, SSOP20 and TSSOP20	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For DIP20 packages: above 70 °C the value of  $P_{tot}$  derates linearly with 12 mW/K.

For SO20 packages: above 70 °C the value of  $P_{tot}$  derates linearly with 8 mW/K.

For (T)SSOP20 packages: above 60 °C the value of  $P_{tot}$  derates linearly with 5.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage[1]		1.0	3.3	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.0\text{ V}$ to $2.0\text{ V}$	-	-	500	ns/V
		$V_{CC} = 2.0\text{ V}$ to $2.7\text{ V}$	-	-	200	ns/V
		$V_{CC} = 2.7\text{ V}$ to $3.6\text{ V}$	-	-	100	ns/V
		$V_{CC} = 3.6\text{ V}$ to $5.5\text{ V}$	-	-	50	ns/V

[1] The static characteristics are guaranteed from  $V_{CC} = 1.2\text{ V}$  to  $V_{CC} = 5.5\text{ V}$ , but LV devices are guaranteed to function down to  $V_{CC} = 1.0\text{ V}$  (with input levels GND or  $V_{CC}$ ).

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	0.9	-	-	0.9	-	V
		V <sub>CC</sub> = 2.0 V	1.4	-	-	1.4	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7V <sub>CC</sub>	-	-	0.7V <sub>CC</sub>	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.3	-	0.3	V
		V <sub>CC</sub> = 2.0 V	-	-	0.6	-	0.6	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.3V <sub>CC</sub>	-	0.3V <sub>CC</sub>	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.2 V	-	1.2	-	-	-	V
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 2.0 V	1.8	2.0	-	1.8	-	V
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 2.7 V	2.5	2.7	-	2.5	-	V
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 3.0 V	2.8	3.0	-	2.8	-	V
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 4.5 V	4.3	4.5	-	4.3	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 3.0 V	2.4	2.82	-	2.2	-	V
		I <sub>O</sub> = -16 mA; V <sub>CC</sub> = 4.5 V	3.6	4.2	-	3.5	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.2 V	-	0	-	-	-	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 2.0 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 2.7 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 3.0 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 4.5 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 3.0 V	-	0.20	0.40	-	0.50	V
		I <sub>O</sub> = 16 mA; V <sub>CC</sub> = 4.5 V	-	0.35	0.55	-	0.65	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	1.0	-	1.0	μA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	5	-	10	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	20	-	160	μA
ΔI <sub>CC</sub>	additional supply current	per input; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	500	-	850	μA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 11](#).

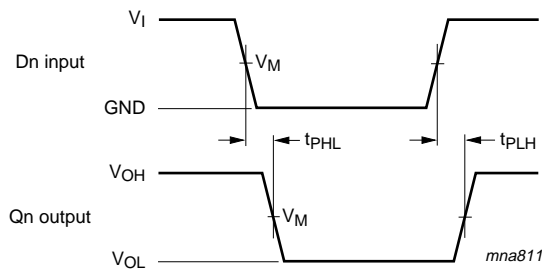
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>pd</sub>	propagation delay	Dn to Qn; see <a href="#">Figure 7</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.2 V	-	75	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	-	26	39	-	49	ns
		V <sub>CC</sub> = 2.7 V	-	19	29	-	36	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V; C <sub>L</sub> = 15 pF <sup>[3]</sup>	-	12	-	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	-	14	23	-	29	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	19	-	24	ns
		LE to Qn; see <a href="#">Figure 8</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.2 V	-	80	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	-	27	43	-	53	ns
		V <sub>CC</sub> = 2.7 V	-	20	31	-	34	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V; C <sub>L</sub> = 15 pF <sup>[3]</sup>	-	13	-	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	-	15	25	-	31	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	21	-	26	ns
t <sub>en</sub>	enable time	$\overline{OE}$ to Qn; see <a href="#">Figure 9</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.2 V	-	70	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	-	24	37	-	48	ns
		V <sub>CC</sub> = 2.7 V	-	18	28	-	35	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	-	13	22	-	28	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	18	-	23	ns
t <sub>dis</sub>	disable time	$\overline{OE}$ to Qn; see <a href="#">Figure 9</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.2 V	-	80	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	-	29	39	-	48	ns
		V <sub>CC</sub> = 2.7 V	-	22	29	-	36	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	-	17	24	-	29	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	20	-	24	ns
t <sub>w</sub>	pulse width	LE HIGH; see <a href="#">Figure 8</a>						
		V <sub>CC</sub> = 2.0 V	34	9	-	41	-	ns
		V <sub>CC</sub> = 2.7 V	25	6	-	30	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	20	5	-	24	-	ns
t <sub>su</sub>	set-up time	nD to nCP; see <a href="#">Figure 10</a>						
		V <sub>CC</sub> = 1.2 V	-	25	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	17	9	-	20	-	ns
		V <sub>CC</sub> = 2.7 V	13	6	-	15	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	10	5	-	12	-	ns

**Table 7. Dynamic characteristics ...continued**  
 Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 11](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>h</sub>	hold time	Dn to LE; see <a href="#">Figure 10</a>						
		V <sub>CC</sub> = 1.2 V	-	5	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	8	2	-	8	-	ns
		V <sub>CC</sub> = 2.7 V	8	2	-	8	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	<sup>[3]</sup> 8	1	-	8	-	ns
C <sub>PD</sub>	power dissipation capacitance	C <sub>L</sub> = 50 pF; f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub>	<sup>[4]</sup> -	26	-	-	-	pF

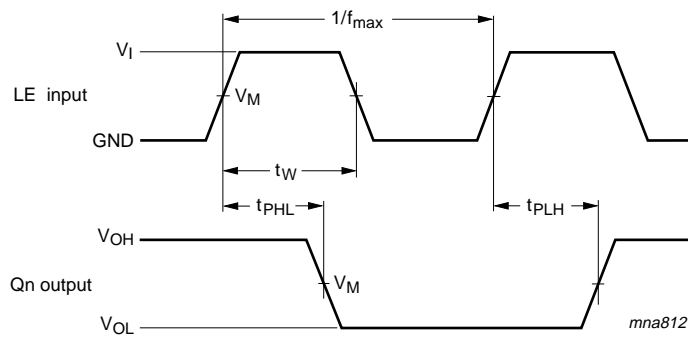
- [1] All typical values are measured at T<sub>amb</sub> = 25 °C.
- [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.  
 t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.  
 t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.
- [3] Typical values are measured at nominal supply voltage (V<sub>CC</sub> = 3.3 V).
- [4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz, f<sub>o</sub> = output frequency in MHz  
 C<sub>L</sub> = output load capacitance in pF  
 V<sub>CC</sub> = supply voltage in Volts  
 N = number of inputs switching  
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

## 11. Waveforms



Measurement points are given in [Table 8](#).  
 V<sub>OL</sub> and V<sub>OH</sub> are typical voltage output levels that occur with the output load.

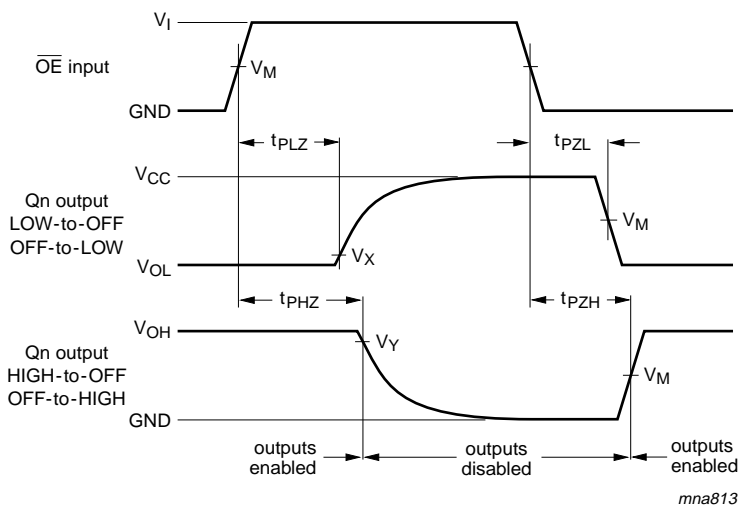
**Fig 7. Input (Dn) to output (Qn) propagation delays**



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

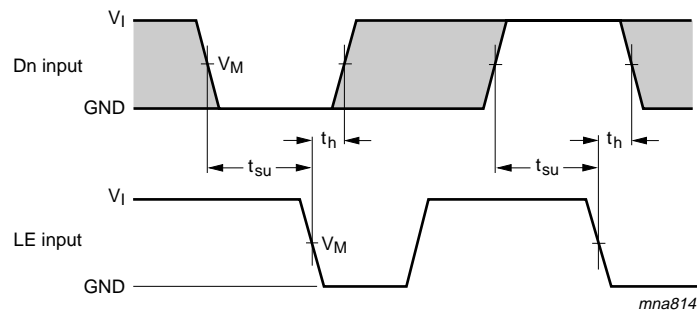
**Fig 8. Latch Enable input (LE) pulse width, the latch enable input to output (Qn) propagation delays**



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 9. Enable and disable times**



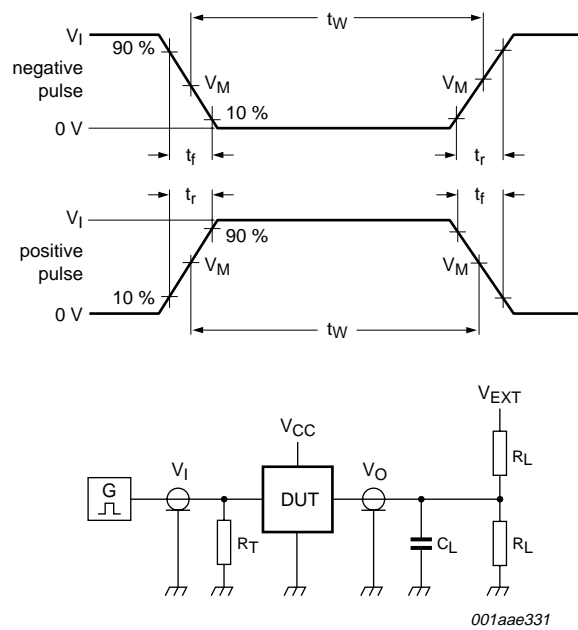
Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 10. Data set-up and hold times for the Dn input to the LE input**

**Table 8. Measurement points**

Supply voltage	Input	Output		
$V_{CC}$	$V_M$	$V_M$	$V_X$	$V_Y$
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
$\geq 4.5 V$	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$



Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig 11. Test circuit for measuring switching times**

**Table 9. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
< 2.7 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	1 k $\Omega$	open	GND	$2V_{CC}$
2.7 V to 3.6 V	2.7 V	$\leq 2.5$ ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$2V_{CC}$
$\geq 4.5$ V	$V_{CC}$	$\leq 2.5$ ns	50 pF	1 k $\Omega$	open	GND	$2V_{CC}$

12. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

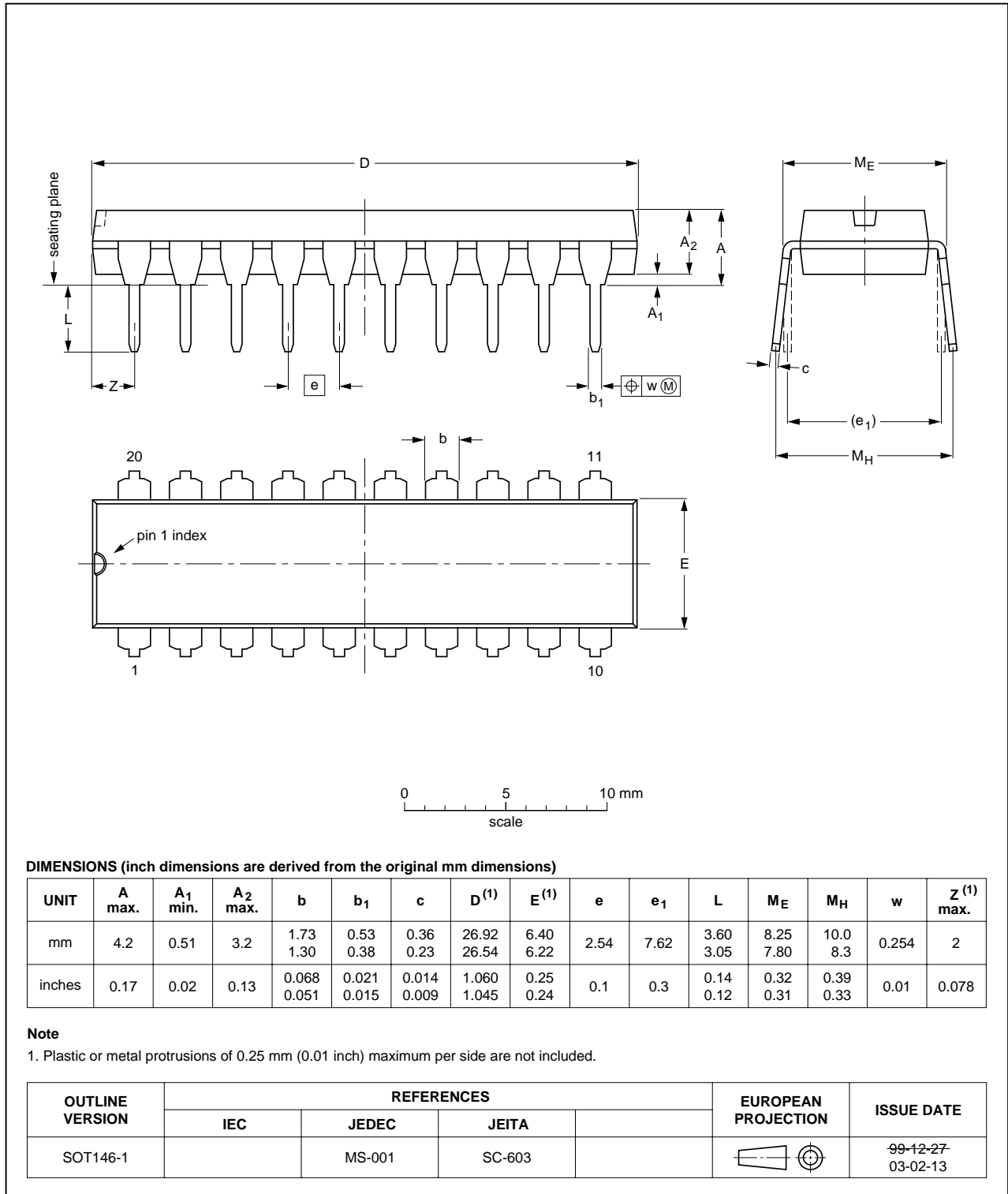


Fig 12. Package outline SOT146-1 (DIP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

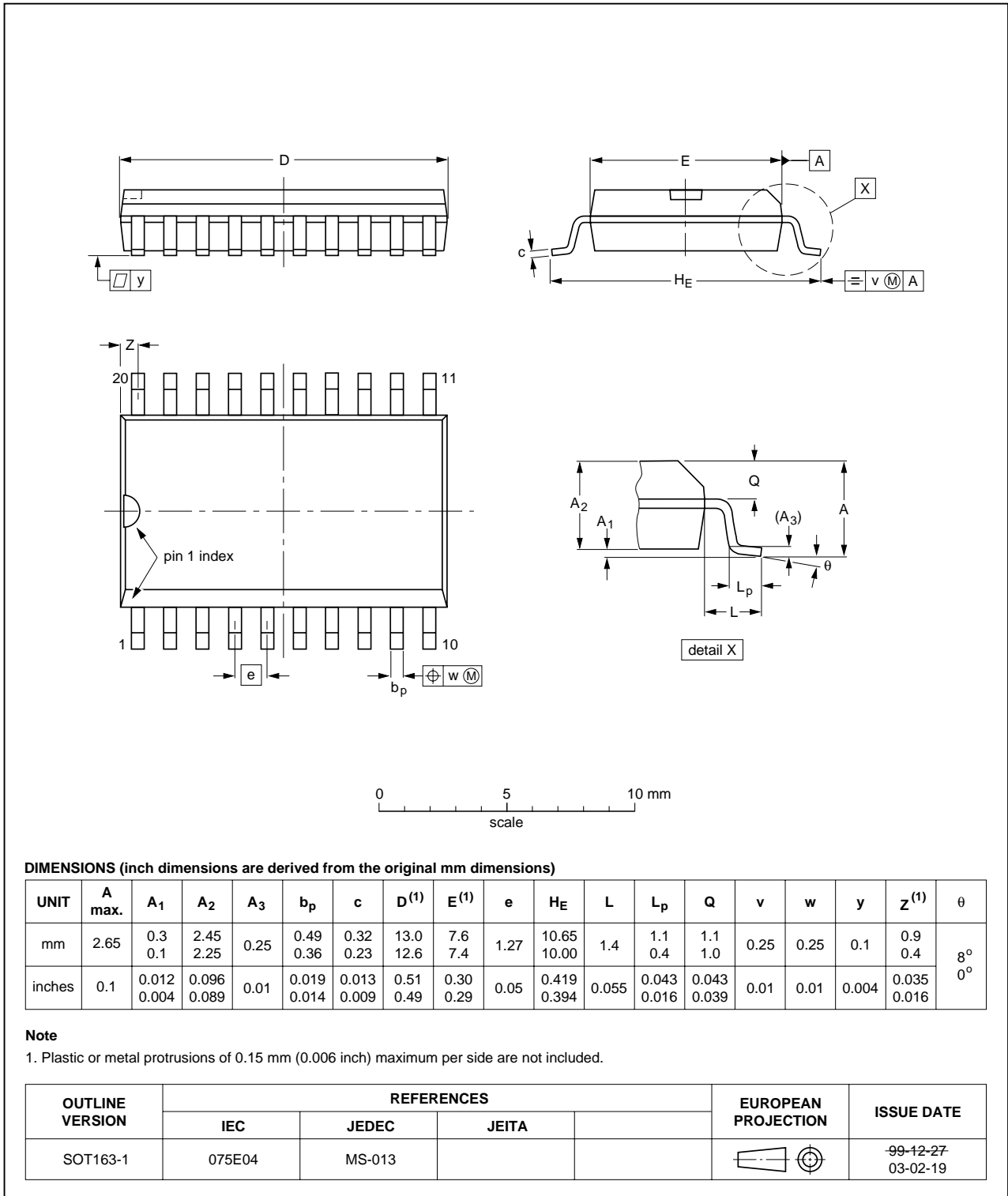


Fig 13. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

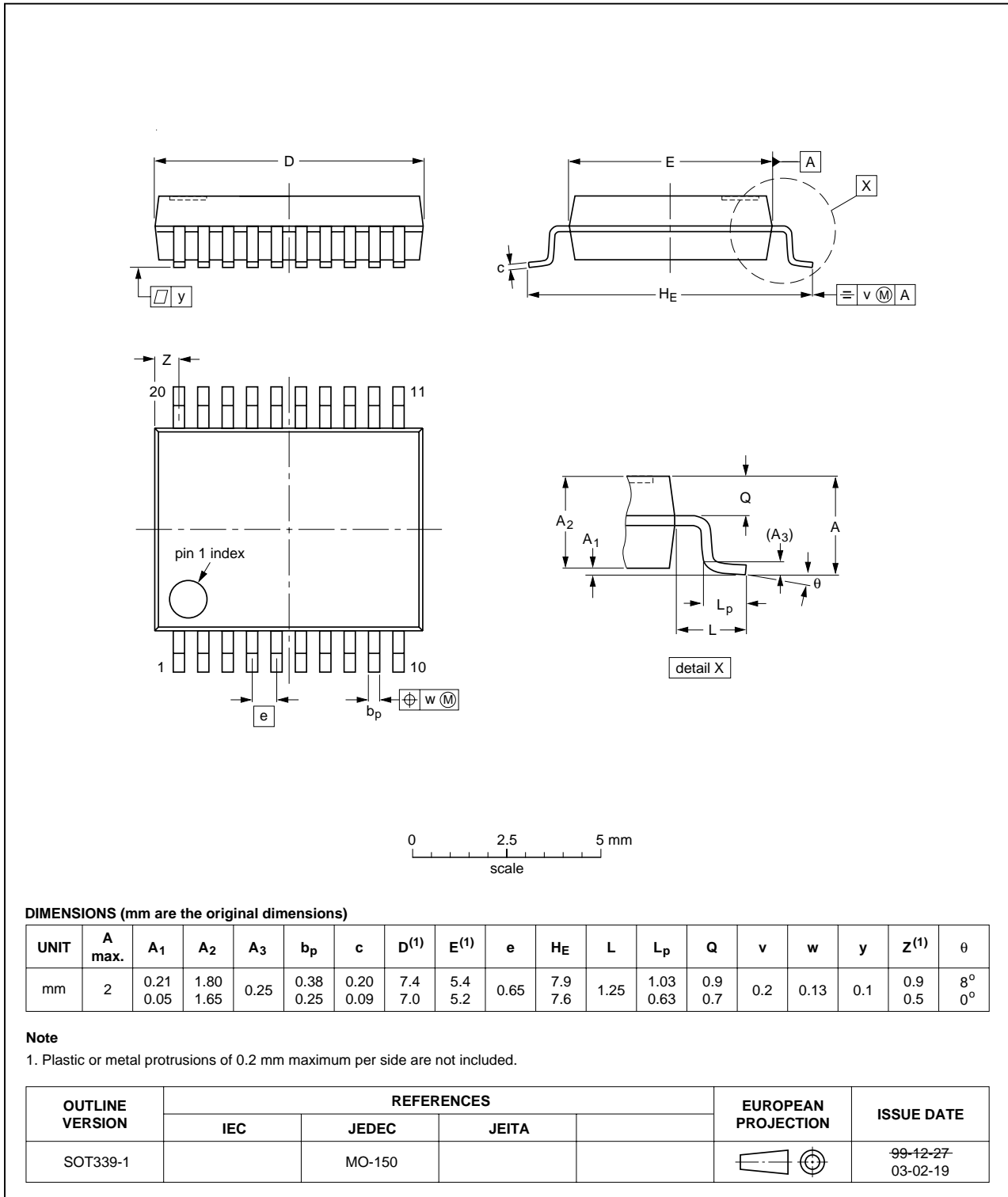


Fig 14. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

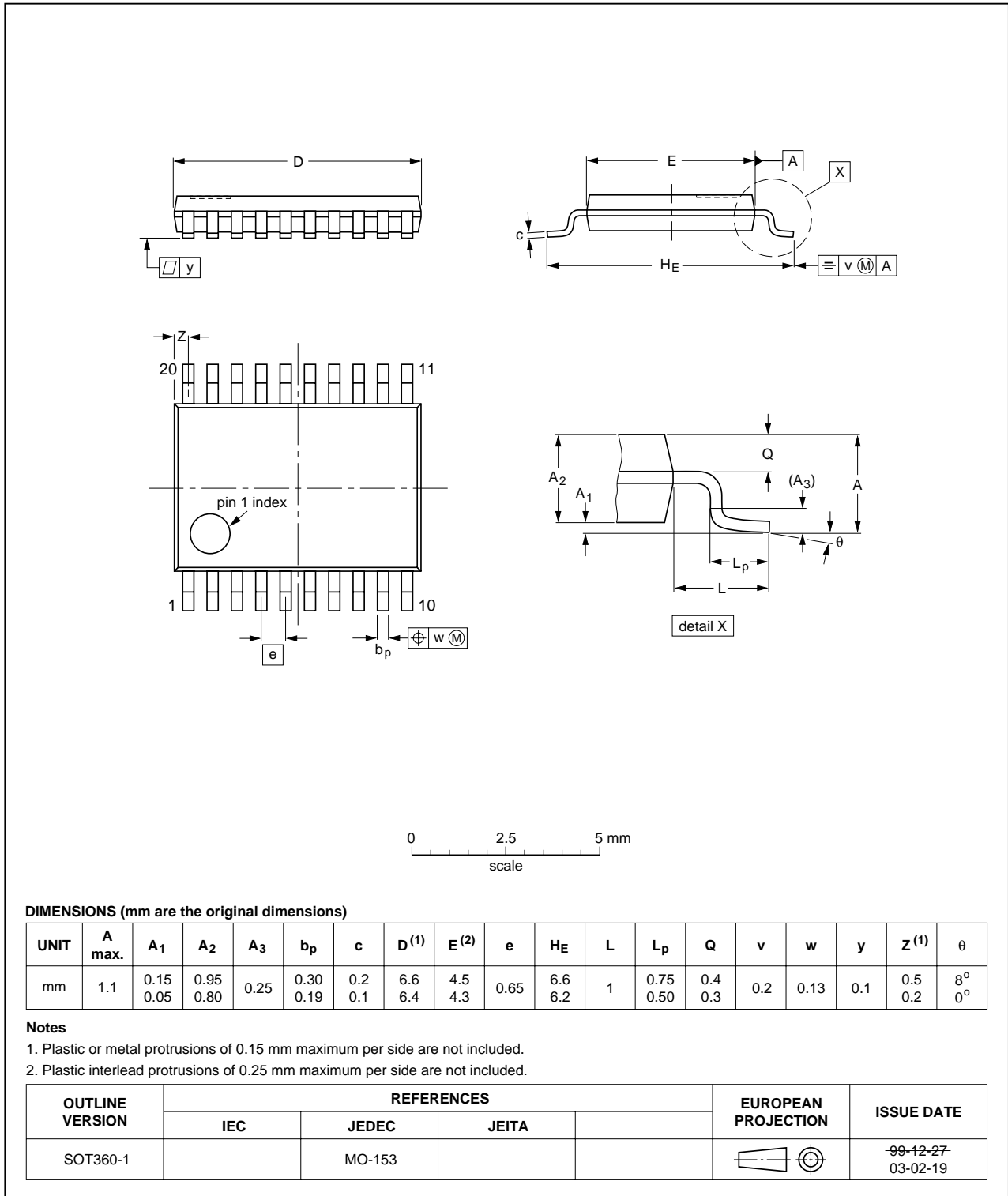


Fig 15. Package outline SOT360-1 (TSSOP20)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV573_3	20090415	Product data sheet	-	74LV573_2
Modifications:	<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name when appropriate.</li></ul>			
74LV573_2	19980610	Product specification	-	74LV573_1
74LV573_1	19970606	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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