

# 74LV164

## 8-bit serial-in/parallel-out shift register

Rev. 03 — 4 February 2005

Product data sheet

### 1. General description

The 74LV164 is a low-voltage, Si-gate CMOS device and is pin and function compatible with the 74HC164 and 74HCT164.

The 74LV164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (DSA or DSB) and either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the clock input (CP) and enters into Q0, which is the logical AND-function of the two data inputs (DSA and DSB) that existed one set-up time prior to the rising clock edge.

A LOW on the master reset input (MR) overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

### 2. Features

- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low-voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between  $V_{CC} = 2.7$  V and  $V_{CC} = 3.6$  V
- Typical  $V_{OLP}$  (output ground bounce):  $< 0.8$  V at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot):  $> 2$  V at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C
- Gated serial data inputs
- Asynchronous master reset
- ESD protection:
  - ◆ HBM EIA/JESD22-A114-B exceeds 2000 V
  - ◆ MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from  $-40$  °C to  $+80$  °C and from  $-40$  °C to  $+125$  °C.

### 3. Quick reference data

**Table 1: Quick reference data**

$GND = 0$  V;  $T_{amb} = 25$  °C;  $t_r = t_f \leq 2.5$  ns.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{PHL}$	propagation delay	$V_{CC} = 3.3$ V; $C_L = 15$ pF				
$t_{PLH}$	CP to Qn		-	12	-	ns
	$\overline{MR}$ to Qn		-	12	-	ns

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**Table 1: Quick reference data ...continued** $GND = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ;  $t_r = t_f \leq 2.5\text{ ns}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{max}$	maximum clock frequency	$V_{CC} = 3.3\text{ V}$ ; $C_L = 15\text{ pF}$	-	78	-	MHz
$C_I$	input capacitance		-	3.5	-	pF
$C_{PD}$	power dissipation capacitance per gate	$V_{CC} = 3.3\text{ V}$	[1] [2]	40	-	pF

[1]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

[2] The condition is  $V_I = GND$  to  $V_{CC}$ .

## 4. Ordering information

**Table 2: Ordering information**

Type number	Package			Version
	Temperature range	Name	Description	
74LV164N	-40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74LV164D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LV164DB	-40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LV164PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LV164BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

5. Functional diagram

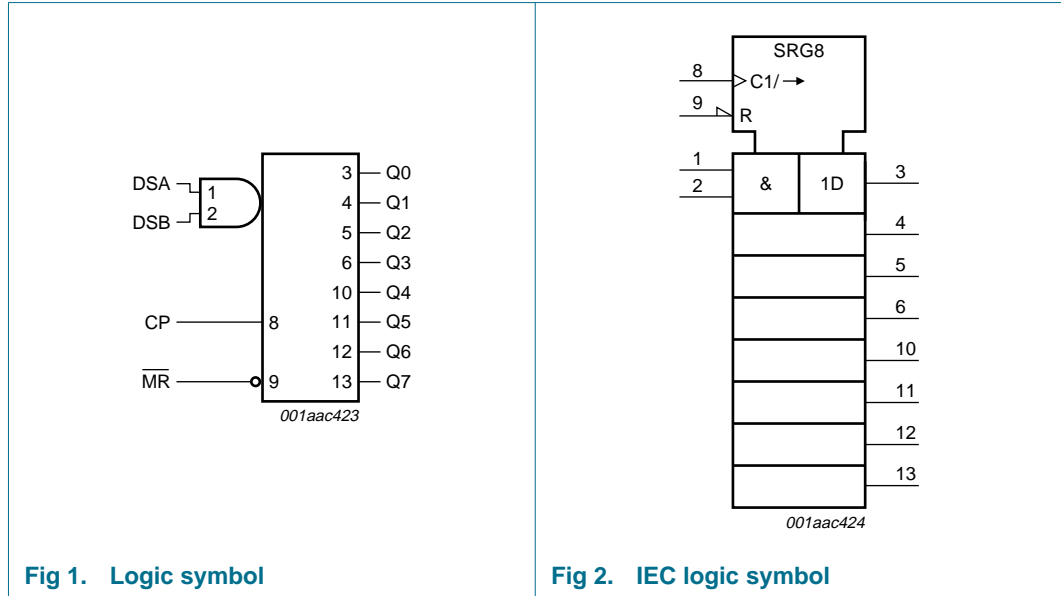


Fig 1. Logic symbol

Fig 2. IEC logic symbol

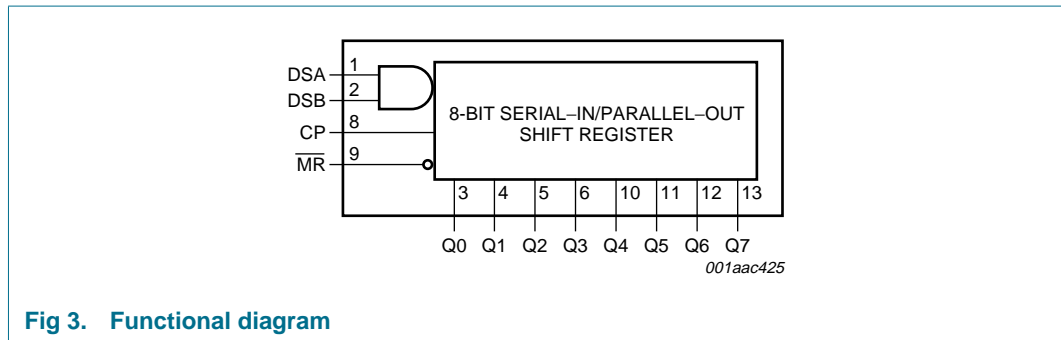
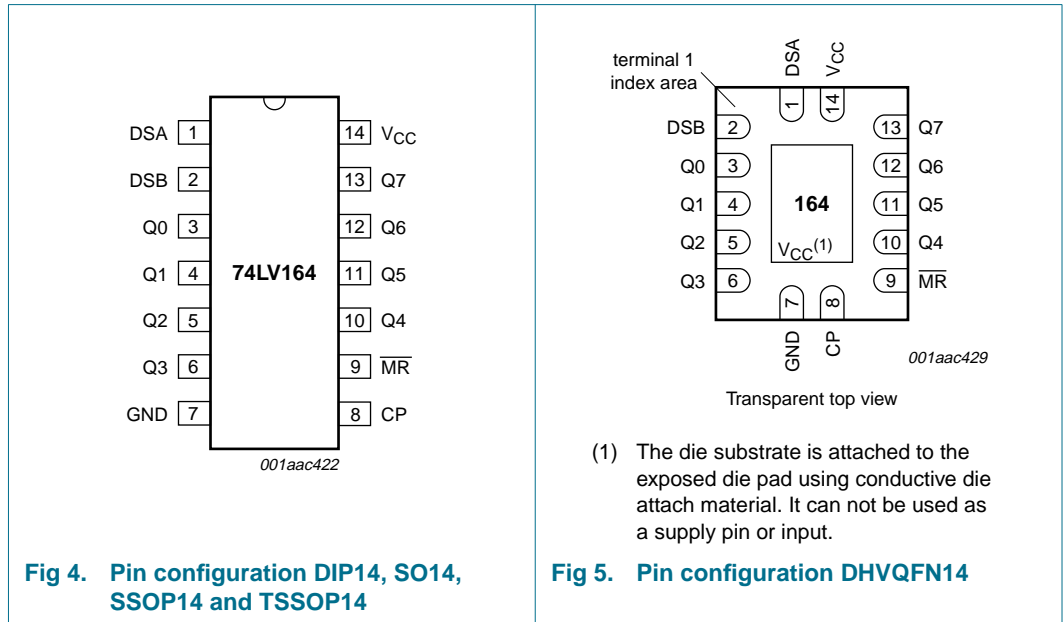


Fig 3. Functional diagram

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
DSA	1	data input SA
DSB	2	data input SB
Q0	3	output 0
Q1	4	output 1
Q2	5	output 2
Q3	6	output 3
GND	7	ground (0 V)
CP	8	clock input (edge triggered LOW-to-HIGH)
$\overline{\text{MR}}$	9	master reset input (active LOW)
Q4	10	output 4
Q5	11	output 5
Q6	12	output 6
Q7	13	output 7
V <sub>CC</sub>	14	supply voltage

## 7. Functional description

### 7.1 Function table

Table 4: Function table <sup>[1]</sup>

Operating mode	Input				Output	
	MR	CP	DSA	DSB	Q0	Q1 to Q7
Reset (clear)	L	X	X	X	L	L to L
Shift	H	↑	l	l	L	q0 to q6
	H	↑	l	h	L	q0 to q6
	H	↑	h	l	L	q0 to q6
	H	↑	h	h	H	q0 to q6

- [1] H = HIGH voltage level;  
 L = LOW voltage level;  
 ↑ = LOW-to-HIGH clock transition;  
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;  
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;  
 q = lower case letter indicates the state of referenced input one set-up time prior to the LOW-to-HIGH CP transition.

## 8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$I_{IK}$	input diode current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	±20	mA
$I_{OK}$	output diode current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	±50	mA
$I_O$	output source or sink current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$	<sup>[1]</sup> -	±25	mA
$I_{CC}, I_{GND}$	$V_{CC}$ or GND current		-	±50	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$			
	DIP14 package		<sup>[2]</sup> -	750	mW
	SO14, (T)SSOP14 and DHVQFN14 packages		<sup>[3]</sup> -	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 [2] DIP14 package:  $P_{tot}$  derates linearly with 12 mW/K above 70 °C.  
 [3] SO14 package:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.  
 (T)SSOP14 package:  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.  
 DHVQFN14 package:  $P_{tot}$  derates linearly with 4.5 mW/K above 60 °C.

## 9. Recommended operating conditions

**Table 6: Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		[1] 1.0	3.3	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+125	°C
$t_r, t_f$	input rise and fall times	$V_{CC} = 1.0\text{ V to }2.0\text{ V}$	-	-	500	ns/V
		$V_{CC} = 2.0\text{ V to }2.7\text{ V}$	-	-	200	ns/V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	100	ns/V
		$V_{CC} = 3.6\text{ V to }5.5\text{ V}$	-	-	50	ns/V

[1] The static characteristics are guaranteed from  $V_{CC} = 1.2\text{ V}$  to  $V_{CC} = 5.5\text{ V}$ , but LV devices are guaranteed to function down to  $V_{CC} = 1.0\text{ V}$  (with input levels GND or  $V_{CC}$ ).

## 10. Static characteristics

**Table 7: Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = -40\text{ °C to }+85\text{ °C}$ [1]						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.2\text{ V}$	0.9	-	-	V
		$V_{CC} = 2.0\text{ V}$	1.4	-	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0	-	-	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.7 \times V_{CC}$	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.2\text{ V}$	-	-	0.3	V
		$V_{CC} = 2.0\text{ V}$	-	-	0.6	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.8	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	$0.3 \times V_{CC}$	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -100\text{ }\mu\text{A}; V_{CC} = 1.2\text{ V}$	-	1.2	-	V
		$I_O = -100\text{ }\mu\text{A}; V_{CC} = 2.0\text{ V}$	1.8	2.0	-	V
		$I_O = -100\text{ }\mu\text{A}; V_{CC} = 2.7\text{ V}$	2.5	2.7	-	V
		$I_O = -100\text{ }\mu\text{A}; V_{CC} = 3.0\text{ V}$	2.8	3.0	-	V
		$I_O = -6\text{ mA}; V_{CC} = 3.0\text{ V}$	2.40	2.82	-	V
		$I_O = -100\text{ }\mu\text{A}; V_{CC} = 4.5\text{ V}$	4.3	4.5	-	V
		$I_O = -12\text{ mA}; V_{CC} = 4.5\text{ V}$	3.60	4.20	-	V

**Table 7: Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.2 V	-	0	-	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 2.0 V	-	0	0.2	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 2.7 V	-	0	0.2	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 3.0 V	-	0	0.2	V
		I <sub>O</sub> = 6 mA; V <sub>CC</sub> = 3.0 V	-	0.25	0.40	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 4.5 V	-	0	0.2	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 4.5 V	-	0.35	0.55	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	1.0	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	20.0	μA
ΔI <sub>CC</sub>	additional quiescent supply current per input	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	500	μA
C <sub>I</sub>	input capacitance		-	3.5	-	pF
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	0.9	-	-	V
		V <sub>CC</sub> = 2.0 V	1.4	-	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.3	V
		V <sub>CC</sub> = 2.0 V	-	-	0.6	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.3 × V <sub>CC</sub>	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.2 V	-	-	-	V
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 2.0 V	1.8	-	-	V
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 2.7 V	2.5	-	-	V
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 3.0 V	2.8	-	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC</sub> = 3.0 V	2.20	-	-	V
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 4.5 V	4.3	-	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 4.5 V	3.50	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.2 V	-	-	-	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 2.0 V	-	-	0.2	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 2.7 V	-	-	0.2	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 3.0 V	-	-	0.2	V
		I <sub>O</sub> = 6 mA; V <sub>CC</sub> = 3.0 V	-	-	0.50	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 4.5 V	-	-	0.2	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 4.5 V	-	-	0.65	V

**Table 7: Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{LI}$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	1.0	$\mu$ A
$I_{CC}$	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	160	$\mu$ A
$\Delta I_{CC}$	additional quiescent supply current per input	$V_I = V_{CC} - 0.6$ V; $V_{CC} = 2.7$ V to 3.6 V	-	-	850	$\mu$ A

[1] All typical values are measured at  $T_{amb} = 25$  °C.

## 11. Dynamic characteristics

**Table 8: Dynamic characteristics**GND = 0 V;  $t_r = t_f \leq 2.5$  ns;  $C_L = 50$  pF;  $R_L = 1$  k $\Omega$ ; for test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = -40</math> °C to <math>+85</math> °C [1]</b>						
$t_{PHL}$ , $t_{PLH}$	propagation delay CP to Qn	see <a href="#">Figure 6</a>				
		$V_{CC} = 1.2$ V	-	75	-	ns
		$V_{CC} = 2.0$ V	-	26	39	ns
		$V_{CC} = 2.7$ V	-	19	29	ns
		$V_{CC} = 3.0$ V to 3.6 V	-	14	23	ns
		$V_{CC} = 4.5$ V to 5.5 V	-	12	19	ns
		$V_{CC} = 3.3$ V; $C_L = 15$ pF	-	12	-	ns
$t_{PHL}$	propagation delay $\overline{MR}$ to Qn	see <a href="#">Figure 7</a>				
		$V_{CC} = 1.2$ V	-	75	-	ns
		$V_{CC} = 2.0$ V	-	26	39	ns
		$V_{CC} = 2.7$ V	-	19	29	ns
		$V_{CC} = 3.0$ V to 3.6 V	-	14	23	ns
		$V_{CC} = 4.5$ V to 5.5 V	-	12	19	ns
		$V_{CC} = 3.3$ V; $C_L = 15$ pF	-	12	-	ns
$t_W$	pulse width CP	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.0$ V	34	9	-	ns
		$V_{CC} = 2.7$ V	25	6	-	ns
		$V_{CC} = 3.0$ V to 3.6 V	20	5	-	ns
		$V_{CC} = 4.5$ V to 5.5 V	13	4	-	ns
$t_W$	pulse width $\overline{MR}$	see <a href="#">Figure 7</a>				
		$V_{CC} = 2.0$ V	34	10	-	ns
		$V_{CC} = 2.7$ V	25	8	-	ns
		$V_{CC} = 3.0$ V to 3.6 V	20	6	-	ns
		$V_{CC} = 4.5$ V to 5.5 V	13	5	-	ns

**Table 8: Dynamic characteristics ...continued**

$GND = 0\text{ V}$ ;  $t_r = t_f \leq 2.5\text{ ns}$ ;  $C_L = 50\text{ pF}$ ;  $R_L = 1\text{ k}\Omega$ ; for test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{rem}$	removal time $\overline{MR}$ to CP	see <a href="#">Figure 7</a>				
		$V_{CC} = 1.2\text{ V}$	-	30	-	ns
		$V_{CC} = 2.0\text{ V}$	19	10	-	ns
		$V_{CC} = 2.7\text{ V}$	14	8	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	11	6	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	8	5	-	ns
$t_{su}$	set-up time Dn to CP	see <a href="#">Figure 8</a>				
		$V_{CC} = 1.2\text{ V}$	-	15	-	ns
		$V_{CC} = 2.0\text{ V}$	22	5	-	ns
		$V_{CC} = 2.7\text{ V}$	16	4	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	13	3	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	9	2	-	ns
$t_h$	hold time Dn to CP	see <a href="#">Figure 8</a>				
		$V_{CC} = 1.2\text{ V}$	-	-10	-	ns
		$V_{CC} = 2.0\text{ V}$	5	-3	-	ns
		$V_{CC} = 2.7\text{ V}$	5	-2	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	5	-2	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	5	-1	-	ns
$f_{max}$	maximum clock frequency	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.0\text{ V}$	14	40	-	MHz
		$V_{CC} = 2.7\text{ V}$	19	58	-	MHz
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	24	70	-	MHz
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	36	100	-	MHz
		$V_{CC} = 3.3\text{ V}$ ; $C_L = 15\text{ pF}$	-	78	-	MHz
$C_{PD}$	power dissipation capacitance per gate	$V_{CC} = 3.3\text{ V}$	<a href="#">[2]</a> <a href="#">[3]</a>	40	-	pF
<b><math>T_{amb} = -40\text{ }^\circ\text{C to }+125\text{ }^\circ\text{C}</math></b>						
$t_{PHL}$ , $t_{PLH}$	propagation delay CP to Qn	see <a href="#">Figure 6</a>				
		$V_{CC} = 1.2\text{ V}$	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	-	-	49	ns
		$V_{CC} = 2.7\text{ V}$	-	-	36	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	-	29	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	24	ns
$t_{PHL}$	propagation delay $\overline{MR}$ to Qn	see <a href="#">Figure 7</a>				
		$V_{CC} = 1.2\text{ V}$	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	-	-	49	ns
		$V_{CC} = 2.7\text{ V}$	-	-	36	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	-	29	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	24	ns

**Table 8: Dynamic characteristics ...continued**

$GND = 0\text{ V}$ ;  $t_r = t_f \leq 2.5\text{ ns}$ ;  $C_L = 50\text{ pF}$ ;  $R_L = 1\text{ k}\Omega$ ; for test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_W$	pulse width CP	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.0\text{ V}$	41	-	-	ns
		$V_{CC} = 2.7\text{ V}$	30	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	24	-	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	16	-	-	ns
$t_W$	pulse width $\overline{MR}$	see <a href="#">Figure 7</a>				
		$V_{CC} = 2.0\text{ V}$	41	-	-	ns
		$V_{CC} = 2.7\text{ V}$	30	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	24	-	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	16	-	-	ns
$t_{rem}$	removal time $\overline{MR}$ to CP	see <a href="#">Figure 7</a>				
		$V_{CC} = 1.2\text{ V}$	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	24	-	-	ns
		$V_{CC} = 2.7\text{ V}$	18	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	14	-	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	10	-	-	ns
$t_{su}$	set-up time Dn to CP	see <a href="#">Figure 8</a>				
		$V_{CC} = 1.2\text{ V}$	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	26	-	-	ns
		$V_{CC} = 2.7\text{ V}$	19	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	15	-	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	10	-	-	ns
$t_h$	hold time Dn to CP	see <a href="#">Figure 8</a>				
		$V_{CC} = 1.2\text{ V}$	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	5	-	-	ns
		$V_{CC} = 2.7\text{ V}$	5	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	5	-	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	5	-	-	ns
$f_{max}$	maximum clock frequency	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.0\text{ V}$	12	-	-	MHz
		$V_{CC} = 2.7\text{ V}$	16	-	-	MHz
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	20	-	-	MHz
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	30	-	-	MHz

[1] Typical values are measured at nominal  $V_{CC}$  and  $T_{amb} = 25\text{ }^\circ\text{C}$ .

[2]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

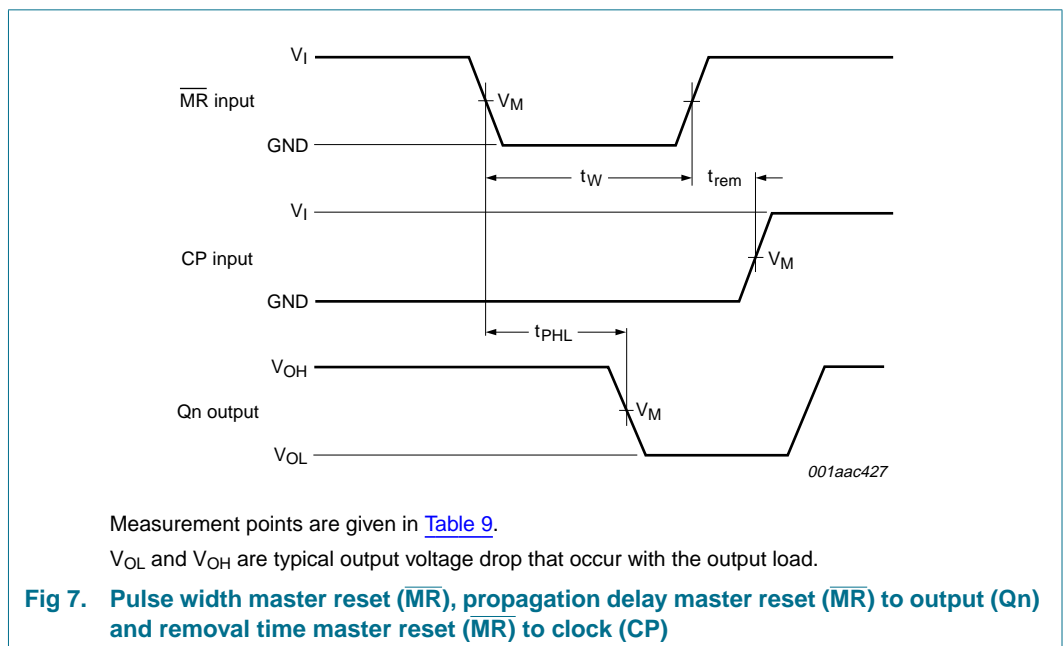
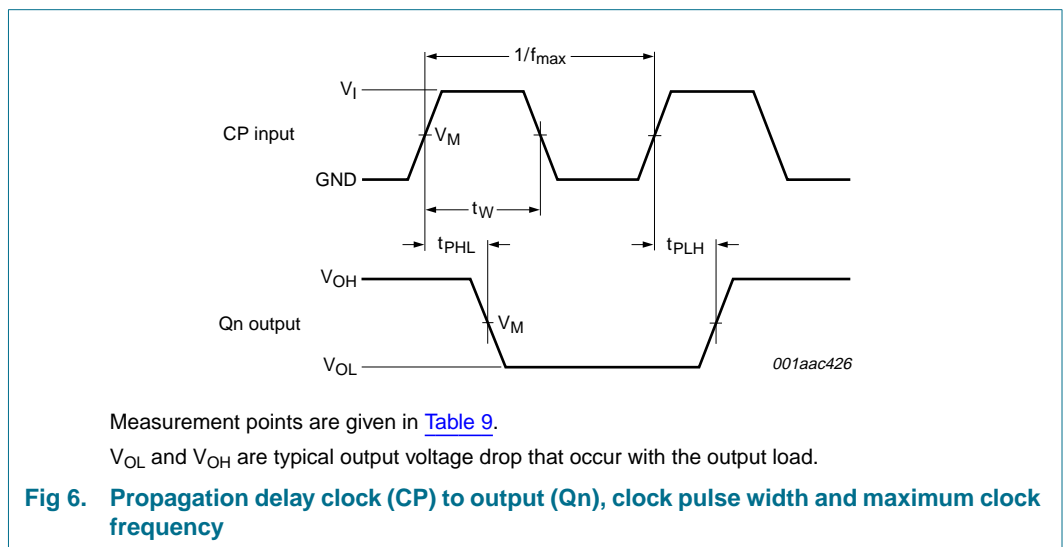
$V_{CC}$  = supply voltage in V;

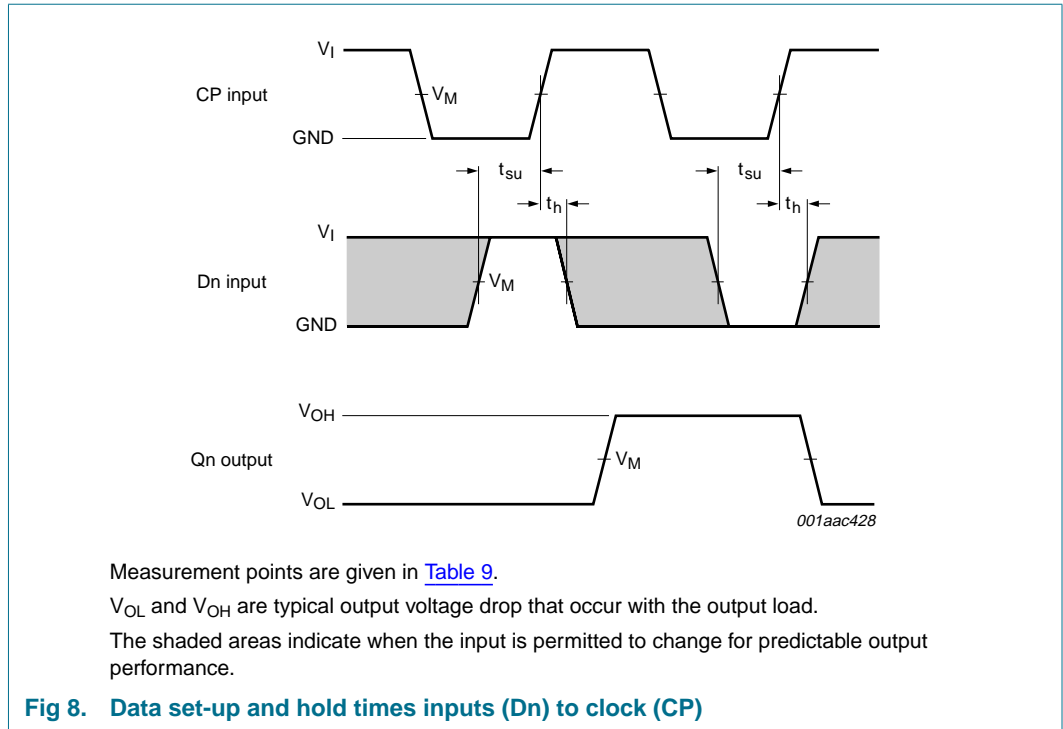
$N$  = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

[3] The condition is  $V_I = GND$  to  $V_{CC}$ .

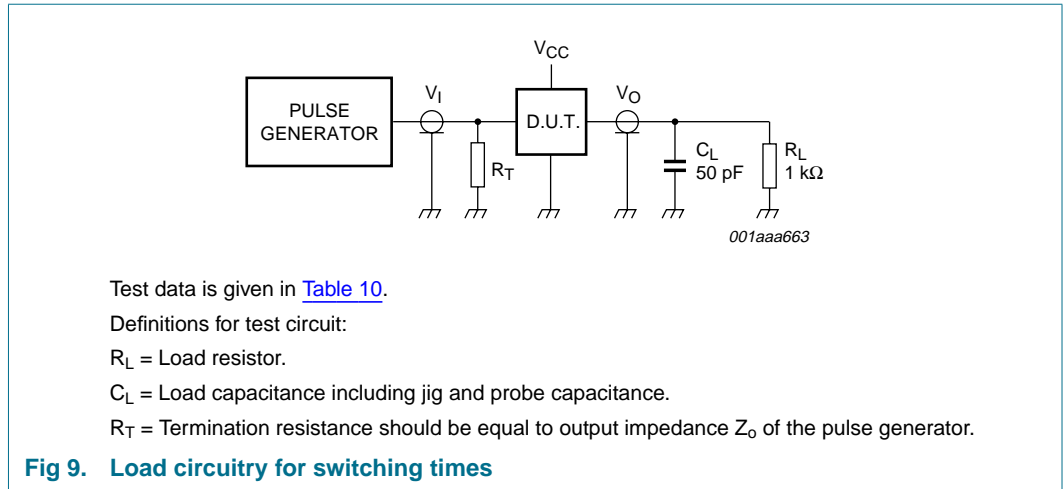
## 12. Waveforms





**Table 9: Measurement points**

Supply voltage	Input	Output
$V_{CC}$	$V_M$	$V_M$
1.2 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.0 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$



**Table 10: Test data**

Supply voltage	Input		Load		Test
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	
1.2 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	1 kΩ	$t_{PHL}, t_{PLH}$
2.0 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	1 kΩ	$t_{PHL}, t_{PLH}$
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	1 kΩ	$t_{PHL}, t_{PLH}$
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF, 15 pF	1 kΩ	$t_{PHL}, t_{PLH}$
4.5 V to 5.5 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	1 kΩ	$t_{PHL}, t_{PLH}$

13. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

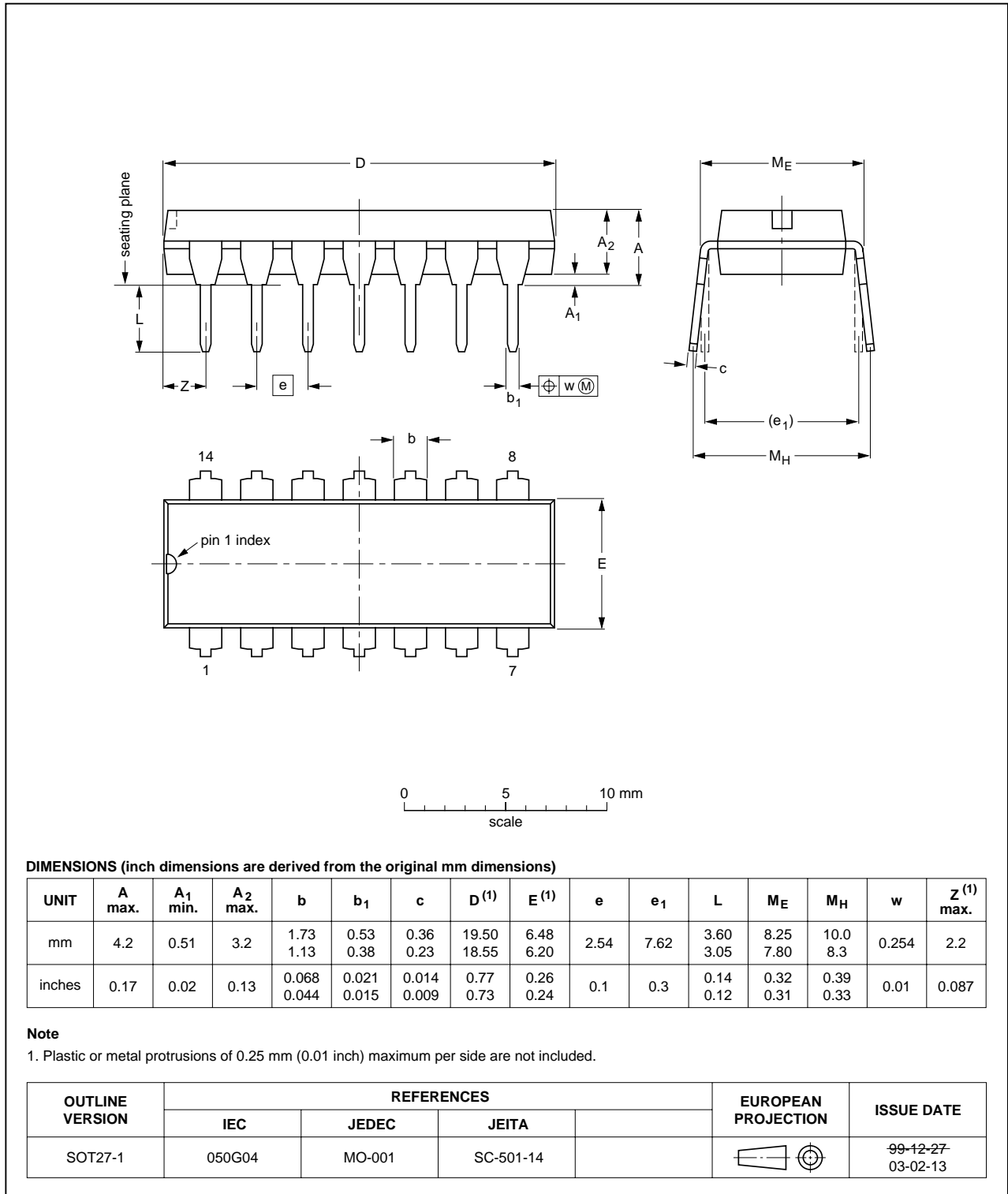


Fig 10. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

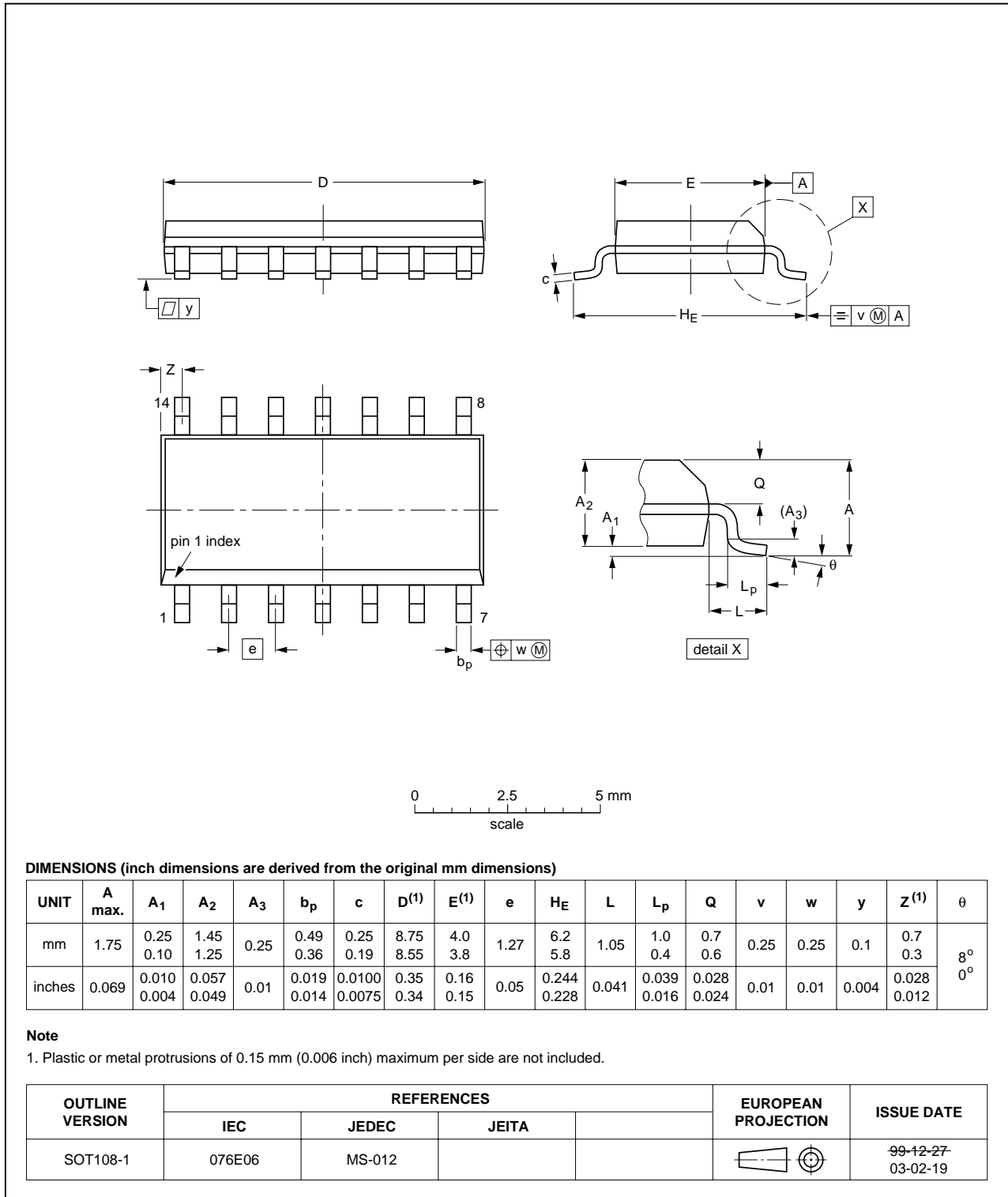


Fig 11. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

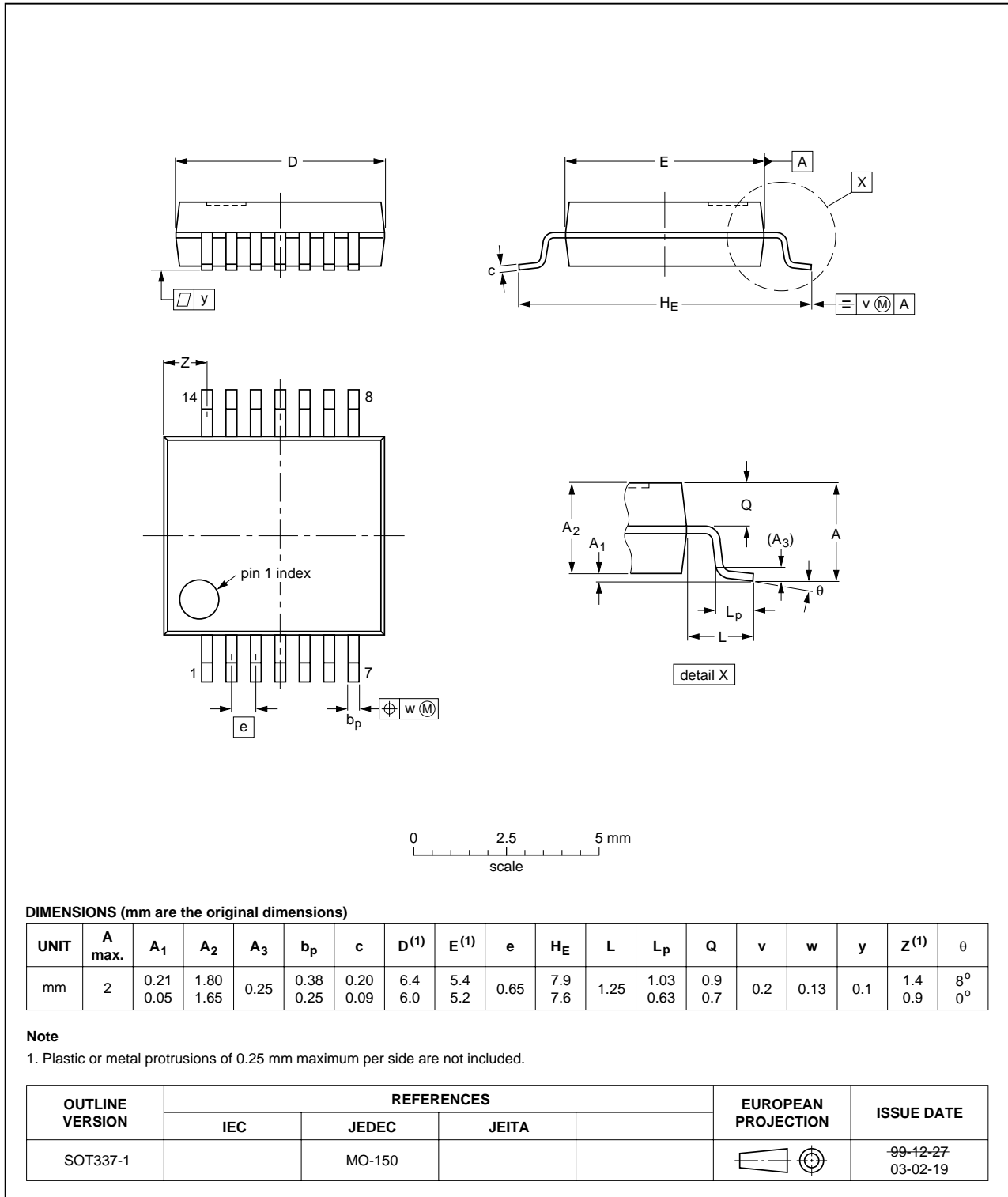


Fig 12. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

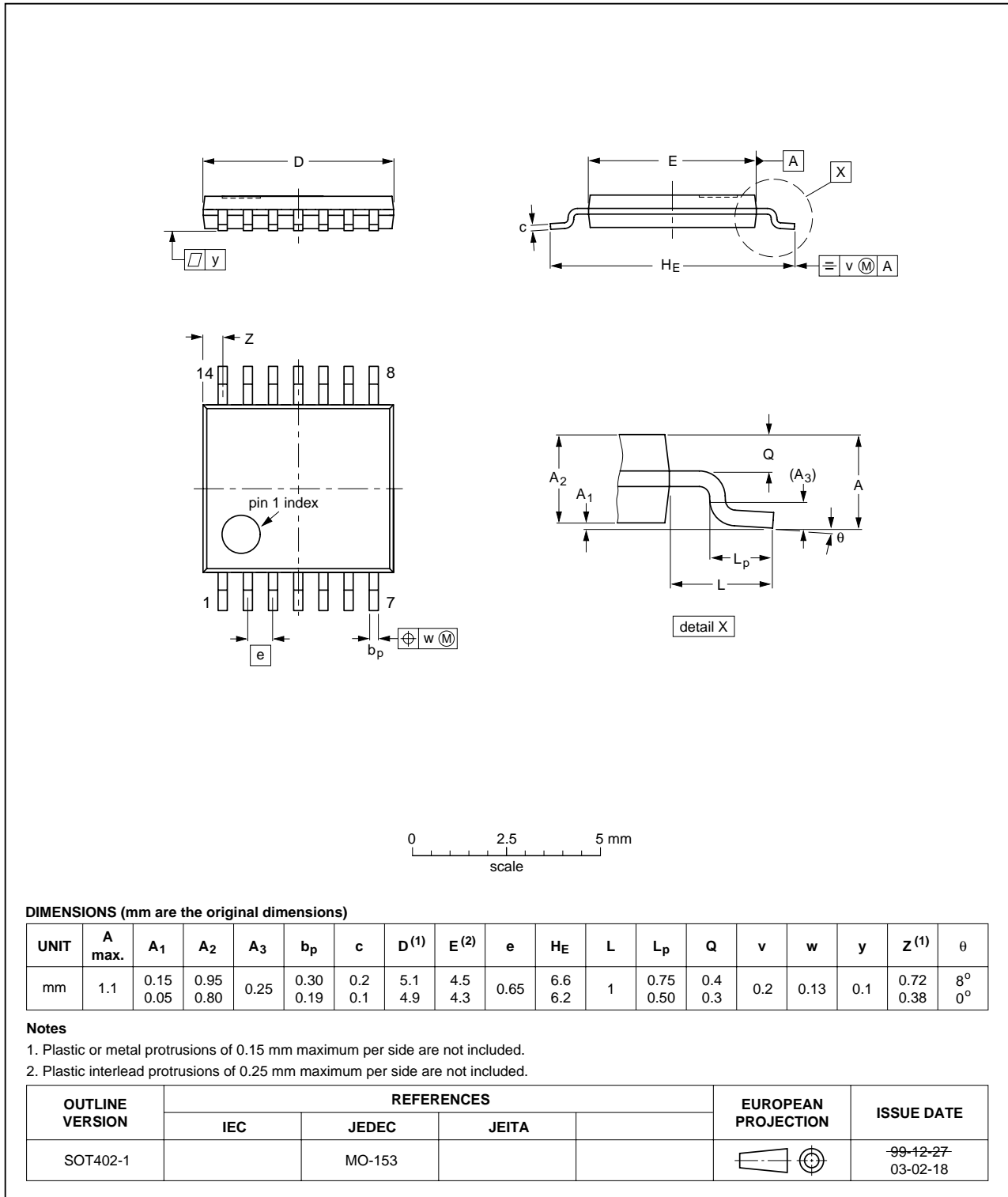


Fig 13. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

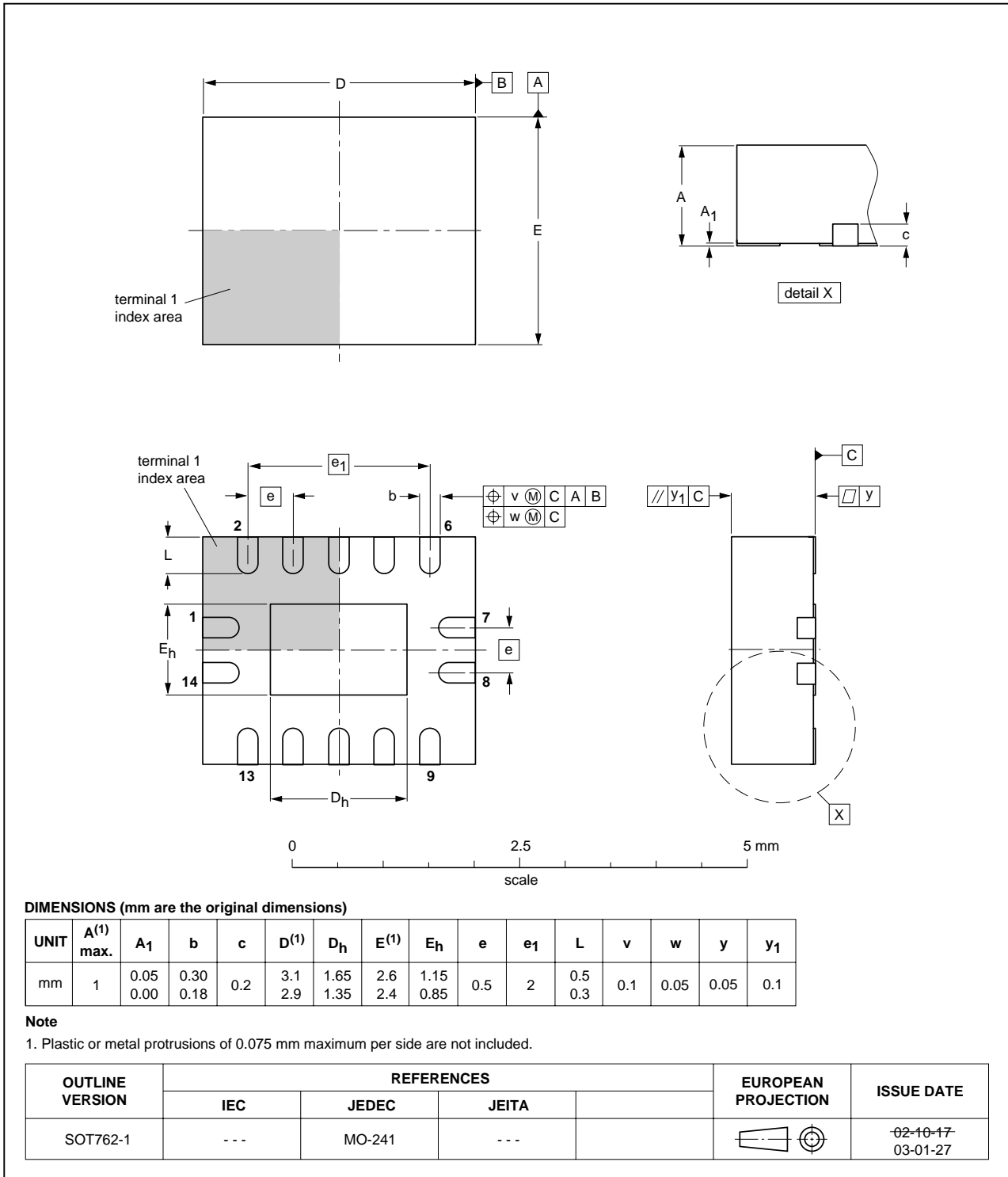


Fig 14. Package outline SOT762-1 (DHVQFN14)

## 14. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74LV164_3	20050204	Product data sheet	-	9397 750 14501	74LV164_2
Modifications:					
					<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the current presentation and information standard of Philips Semiconductors</li><li>• Added: type number 74LV164BQ (DHVQFN14 package).</li></ul>
74LV164_2	19980507	Product specification	-	9397 750 04431	74LV164_1
74LV164_1	19970328	Product specification	-	-	-

## 15. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup> <sup>[3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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