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74LCX74

Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop with 5V Tolerant Inputs

Features

- 5V tolerant inputs
- 2.3V–3.6V V_{CC} specifications provided
- 7.0ns t_{PD} max. ($V_{CC} = 3.3V$), $10\mu A$ I_{CC} max.
- Power down high impedance inputs and outputs
- $\pm 24mA$ output drive ($V_{CC} = 3.0V$)
- Implements proprietary noise/EMI reduction circuitry
- Latch-up performance exceeds JEDEC 78 conditions
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V
- Leadless Pb-Free DQFN package

General Description

The LCX74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, \bar{Q}) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:

- LOW input to \bar{S}_D (Set) sets Q to HIGH level
- LOW input to \bar{C}_D (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on \bar{C}_D and \bar{S}_D makes both Q and \bar{Q} HIGH


Ordering Information

| Order Number | Package Number | Package Description |
|---------------------------|----------------|---|
| 74LCX74M | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| 74LCX74SJ | M14D | 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74LCX74BQX ⁽¹⁾ | MLP14A | 14-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0mm |
| 74LCX74MTC | MTC14 | 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |

Note:

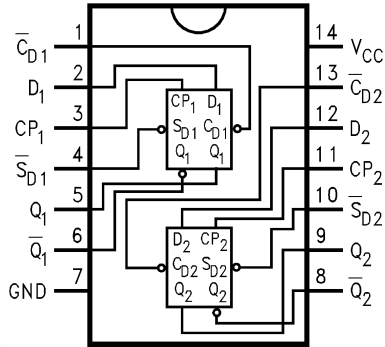
1. DQFN package available in Tape and Reel only.

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

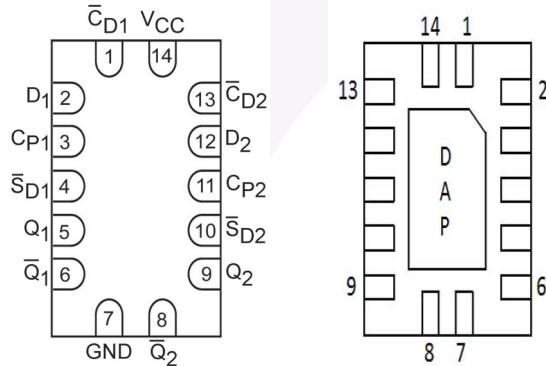
 All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagrams

Pin Assignments for SOIC, SOP, and TSSOP



Pad Assignment for DQFN



(Top View)

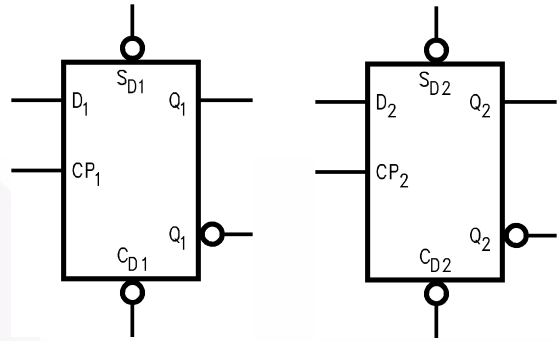
(Bottom View)

Pin Description

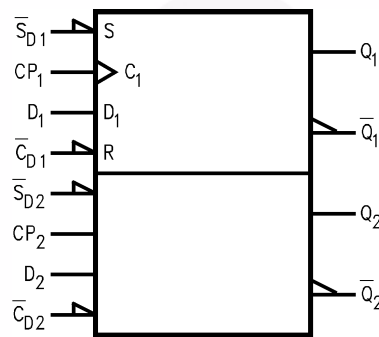
| Pin Names | Description |
|---|---------------------|
| D ₁ , D ₂ | Data Inputs |
| CP ₁ , CP ₂ | Clock Pulse Inputs |
| C _{D1} , C _{D2} | Direct Clear Inputs |
| S _{D1} , S _{D2} | Direct Set Inputs |
| Q ₁ , Q ₁ [̄] , Q ₂ , Q ₂ [̄] | Outputs |
| DAP | No Connect |

Note: DAP (Die Attach Pad)

Logic Symbols



IEEE/IEC



Truth Table

(Each Half)

| Inputs | | | | Outputs | |
|----------------|----------------|----|---|----------------|-----------------------------|
| S _D | C _D | CP | D | Q | Q [̄] |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H | H |
| H | H | ↗ | H | H | L |
| H | H | ↘ | L | L | H |
| H | H | L | X | Q ₀ | Q ₀ [̄] |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

↗ = LOW-to-HIGH Clock Transition

Q₀(Q₀[̄]) = Previous Q(Q[̄]) before LOW-to-HIGH Transition of Clock

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Rating |
|-----------|---|--------------------------|
| V_{CC} | Supply Voltage | -0.5V to +7.0V |
| V_I | DC Input Voltage | -0.5V to +7.0V |
| V_O | DC Output Voltage, Output in HIGH or LOW State ⁽²⁾ | -0.5V to $V_{CC} + 0.5V$ |
| I_{IK} | DC Input Diode Current, $V_I < GND$ | -50mA |
| I_{OK} | DC Output Diode Current $V_O < GND$ | -50mA |
| | $V_O > V_{CC}$ | +50mA |
| I_O | DC Output Source/Sink Current | $\pm 50mA$ |
| I_{CC} | DC Supply Current per Supply Pin | $\pm 100mA$ |
| I_{GND} | DC Ground Current per Ground Pin | $\pm 100mA$ |
| T_{STG} | Storage Temperature | -65°C to +150°C |

Note:

2. I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions⁽³⁾

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Min. | Max. | Units |
|-----------------------|---|------|----------|-------|
| V_{CC} | Supply Voltage Operating | 2.0 | 3.6 | V |
| | Data Retention | 1.5 | 3.6 | |
| V_I | Input Voltage | 0 | 5.5 | V |
| V_O | Output Voltage, HIGH or LOW State | 0 | V_{CC} | V |
| I_{OH} / I_{OL} | Output Current $V_{CC} = 3.0V-3.6V$ | | ± 24 | mA |
| | $V_{CC} = 2.7V-3.0V$ | | ± 12 | |
| | $V_{CC} = 2.3V-2.7V$ | | ± 8 | |
| T_A | Free-Air Operating Temperature | -40 | 85 | °C |
| $\Delta t / \Delta V$ | Input Edge Rate, $V_{IN} = 0.8V-2.0V$, $V_{CC} = 3.0V$ | 0 | 10 | ns/V |

Note:

3. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = -40°C to +85°C | | Units |
|------------------|---------------------------------------|---------------------|--|---------------------------------|------|-------|
| | | | | Min. | Max. | |
| V _{IH} | HIGH Level Input Voltage | 2.3–2.7 | | 1.7 | | V |
| | | 2.7–3.6 | | 2.0 | | |
| V _{IL} | LOW Level Input Voltage | 2.3–2.7 | | | 0.7 | V |
| | | 2.7–3.6 | | | 0.8 | |
| V _{OH} | HIGH Level Output Voltage | 2.3–3.6 | I _{OH} = -100μA | V _{CC} - 0.2 | | V |
| | | 2.3 | I _{OH} = -8mA | 1.8 | | |
| | | 2.7 | I _{OH} = -12mA | 2.2 | | |
| | | 3.0 | I _{OH} = -18mA | 2.4 | | |
| | | | I _{OH} = -24mA | 2.2 | | |
| V _{OL} | LOW Level Output Voltage | 2.3–3.6 | I _{OL} = 100μA | | 0.2 | V |
| | | 2.3 | I _{OL} = 8mA | | 0.6 | |
| | | 2.7 | I _{OL} = 12mA | | 0.4 | |
| | | 3.0 | I _{OL} = 16mA | | 0.4 | |
| | | | I _{OL} = 24mA | | 0.55 | |
| I _I | Input Leakage Current | 2.3–3.6 | 0 ≤ V _I ≤ 5.5V | | ±5.0 | μA |
| I _{OFF} | Power-Off Leakage Current | 0 | V _I or V _O = 5.5V | | 10 | μA |
| I _{CC} | Quiescent Supply Current | 2.3–3.6 | V _I = V _{CC} or GND | | 10 | μA |
| | | | 3.6V ≤ V _I ≤ 5.5V | | ±10 | |
| ΔI _{CC} | Increase in I _{CC} per Input | 2.3–3.6 | V _{IH} = V _{CC} - 0.6V | | 500 | μA |

AC Electrical Characteristics

| Symbol | Parameter | T _A = -40°C to +85°C, R _L = 500Ω | | | | | | Units |
|---------------------------------------|--|---|------|--|------|---|------|-------|
| | | V _{CC} = 3.3V ± 0.3V, C _L = 50pF | | V _{CC} = 2.7V, C _L = 50pF | | V _{CC} = 2.5V ± 0.2V, C _L = 30pF | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| f _{MAX} | Maximum Clock Frequency | 150 | | 150 | | 150 | | MHz |
| t _{PHL} , t _{PLH} | Propagation Delay, CP _n to Q _n or \overline{Q}_n | 1.5 | 7.0 | 1.5 | 8.0 | 1.5 | 8.4 | ns |
| t _{PHL} , t _{PLH} | Propagation Delay, \overline{C}_Dn or \overline{S}_Dn to Q _n or \overline{Q}_n | 1.5 | 7.0 | 1.5 | 8.0 | 1.5 | 8.4 | ns |
| t _S | Setup Time | 2.5 | | 2.5 | | 4.0 | | ns |
| t _H | Hold Time | 1.5 | | 1.5 | | 2.0 | | ns |
| t _W | Pulse Width CP | 3.3 | | 3.3 | | 4.0 | | ns |
| t _W | Pulse Width and \overline{C}_D , \overline{S}_D | 3.3 | | 3.6 | | 4.0 | | ns |
| t _{REC} | Recovery Time | 2.5 | | 3.0 | | 4.5 | | ns |
| t _{OSHL} , t _{OSLH} | Output to Output Skew ⁽⁴⁾ | | 1.0 | | | | | ns |

Note:

4. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = 25°C | |
|------------------|---|---------------------|---|-----------------------|------|
| | | | | Typical | Unit |
| V _{OLP} | Quiet Output Dynamic Peak V _{OL} | 3.3 | C _L = 50pF, V _{IH} = 3.3V, V _{IL} = 0V | 0.8 | V |
| | | 2.5 | C _L = 30pF, V _{IH} = 2.5V, V _{IL} = 0V | 0.6 | |
| V _{OLV} | Quiet Output Dynamic Valley V _{OL} | 3.3 | C _L = 50pF, V _{IH} = 3.3V, V _{IL} = 0V | -0.8 | V |
| | | 2.5 | C _L = 30pF, V _{IH} = 2.5V, V _{IL} = 0V | -0.6 | |

Capacitance

| Symbol | Parameter | Conditions | Typical | Units |
|------------------|-------------------------------|--|---------|-------|
| C _{IN} | Input Capacitance | V _{CC} = Open, V _I = 0V or V _{CC} | 7 | pF |
| C _{OUT} | Output Capacitance | V _{CC} = 3.3V, V _I = 0V or V _{CC} | 8 | pF |
| C _{PD} | Power Dissipation Capacitance | V _{CC} = 3.3V, V _I = 0V or V _{CC} , f = 10MHz | 25 | pF |

AC Loading and Waveforms (Generic for LCX Family)

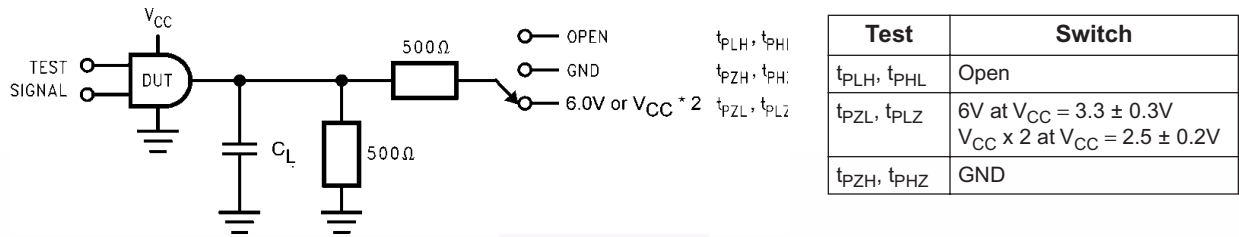
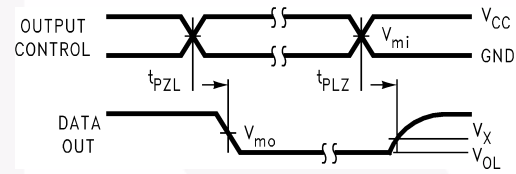
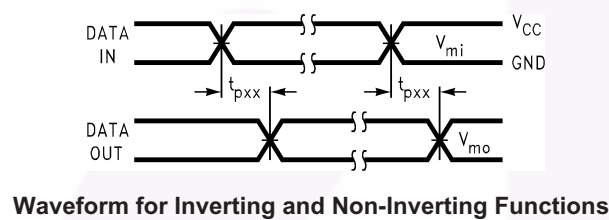
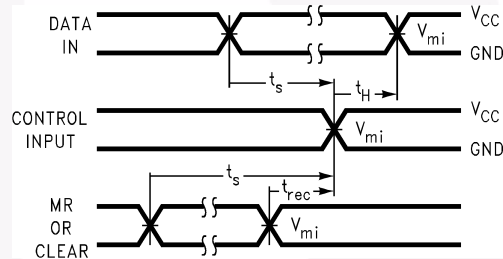
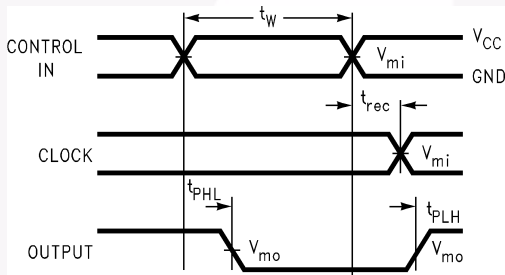


Figure 1. AC Test Circuit (C_L includes probe and jig capacitance)



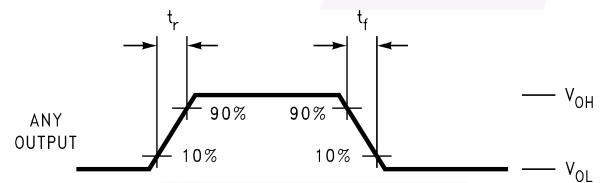
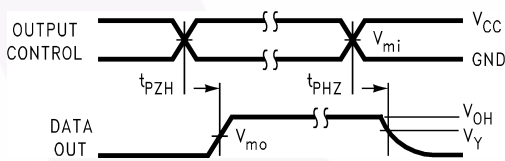
Waveform for Inverting and Non-Inverting Functions

3-STATE Output Low Enable and Disable Times for Logic



Propagation Delay, Pulse Width and t_{rec} Waveforms

Setup Time, Hold Time and Recovery Time for Logic



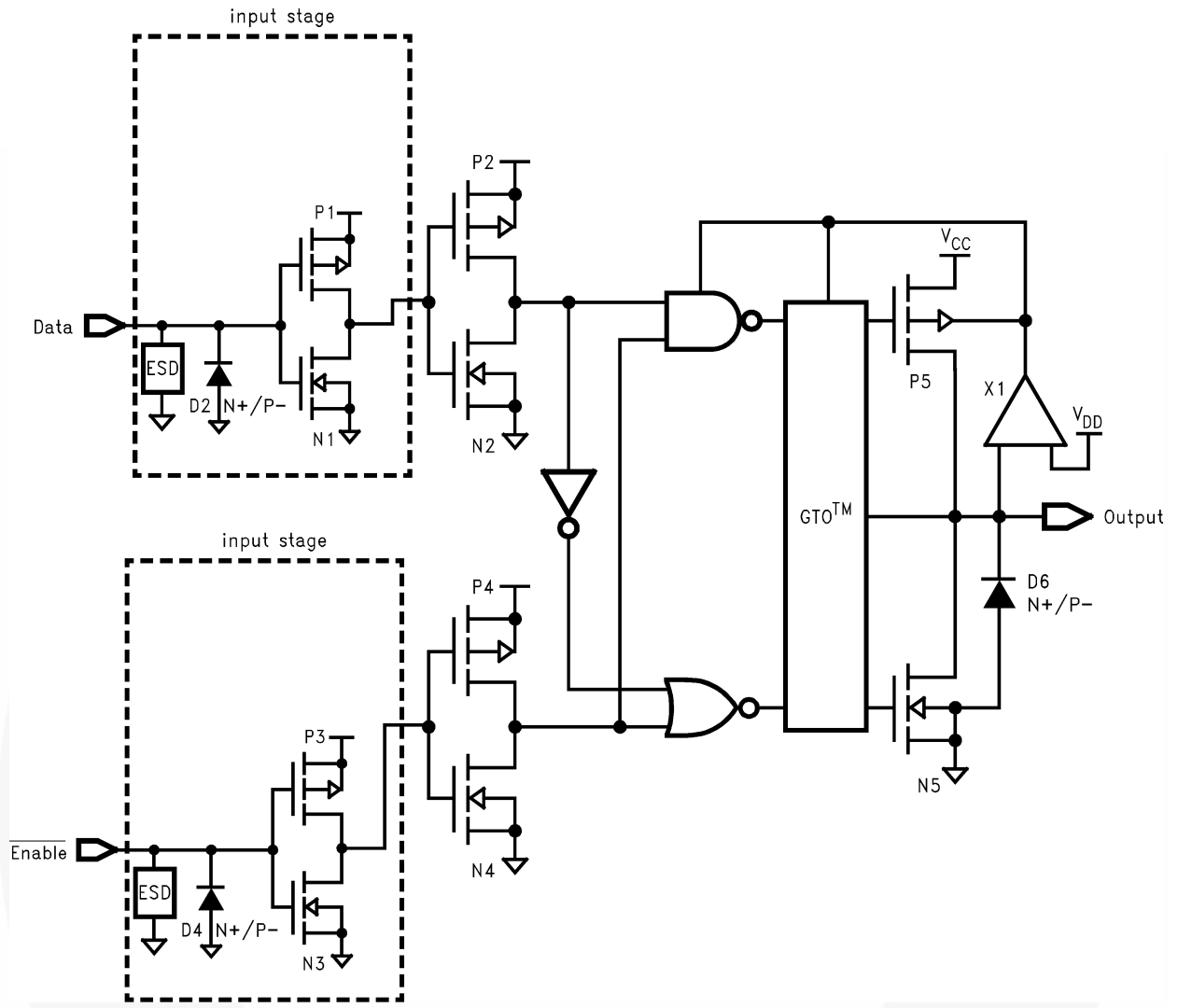
3-STATE Output High Enable and Disable Times for Logic

t_{rise} and t_{fall}

| Symbol | V_{CC} | | |
|----------|-----------------|-----------------|------------------|
| | $3.3V \pm 0.3V$ | 2.7V | $2.5V \pm 0.2V$ |
| V_{mi} | 1.5V | 1.5V | $V_{CC}/2$ |
| V_{mo} | 1.5V | 1.5V | $V_{CC}/2$ |
| V_x | $V_{OL} + 0.3V$ | $V_{OL} + 0.3V$ | $V_{OL} + 0.15V$ |
| V_y | $V_{OH} - 0.3V$ | $V_{OH} - 0.3V$ | $V_{OH} - 0.15V$ |

Figure 2. Waveforms (Input Characteristics; $f = 1MHz, t_r = t_f = 3ns$)

Schematic Diagram (Generic for LCX Family)

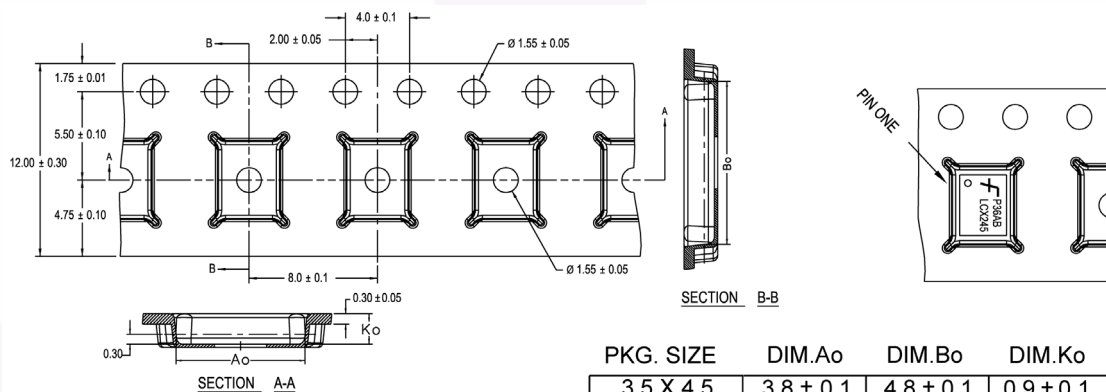


Tape and Reel Specification

Tape Format for DQFN

| Package Designator | Tape Section | Number of Cavities | Cavity Status | Cover Tape Status |
|--------------------|--------------------|--------------------|---------------|-------------------|
| BQX | Leader (Start End) | 125 (Typ.) | Empty | Sealed |
| | Carrier | 3000 | Filled | Sealed |
| | Trailer (Hub End) | 75 (Typ.) | Empty | Sealed |

Tape Dimensions inches (millimeters)



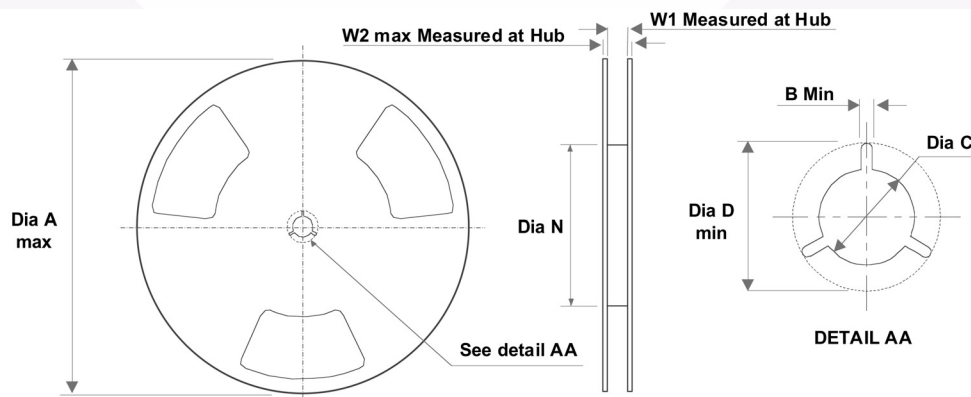
| PKG. SIZE | DIM.Ao | DIM.Bo | DIM.Ko |
|-----------|-----------|-----------|-----------|
| 3.5 X 4.5 | 3.8 ± 0.1 | 4.8 ± 0.1 | 0.9 ± 0.1 |
| 3.0 X 3.0 | 3.3 ± 0.1 | 3.3 ± 0.1 | 0.9 ± 0.1 |
| 2.5 X 4.5 | 2.8 ± 0.1 | 4.8 ± 0.1 | 0.9 ± 0.1 |
| 2.5 X 3.5 | 2.8 ± 0.1 | 3.8 ± 0.1 | 0.9 ± 0.1 |
| 2.5 X 3.0 | 2.8 ± 0.1 | 3.3 ± 0.1 | 0.9 ± 0.1 |
| 2.5 X 2.5 | 2.8 ± 0.1 | 2.8 ± 0.1 | 0.9 ± 0.1 |

DIMENSIONS ARE IN MILLIMETERS

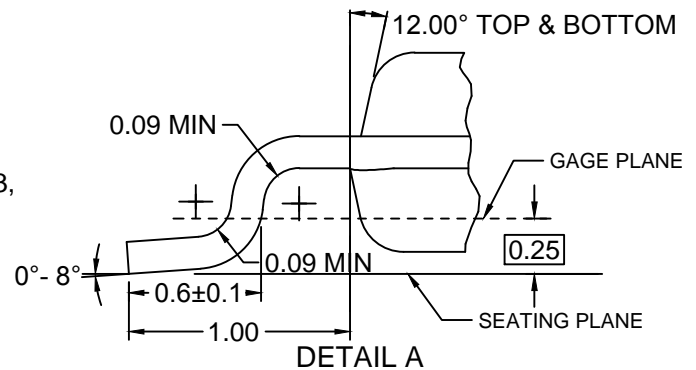
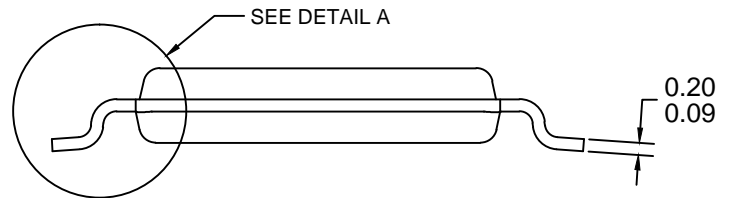
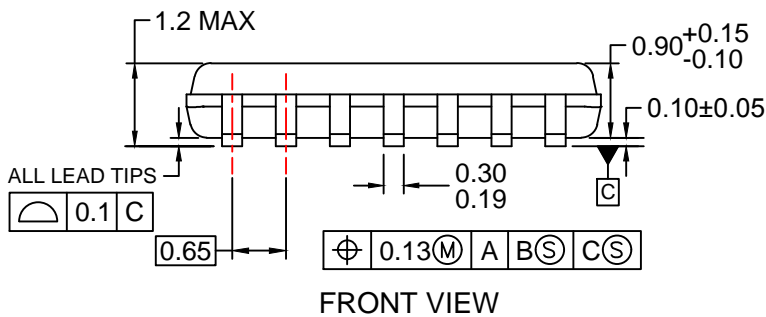
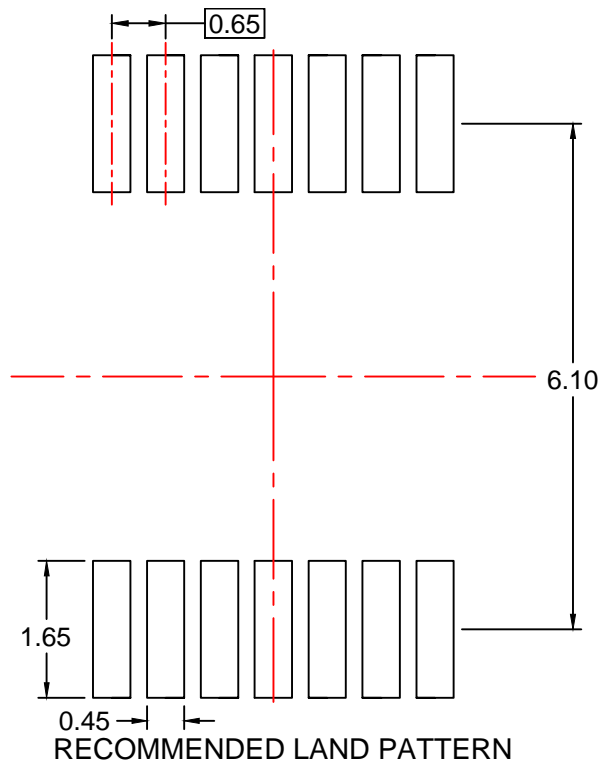
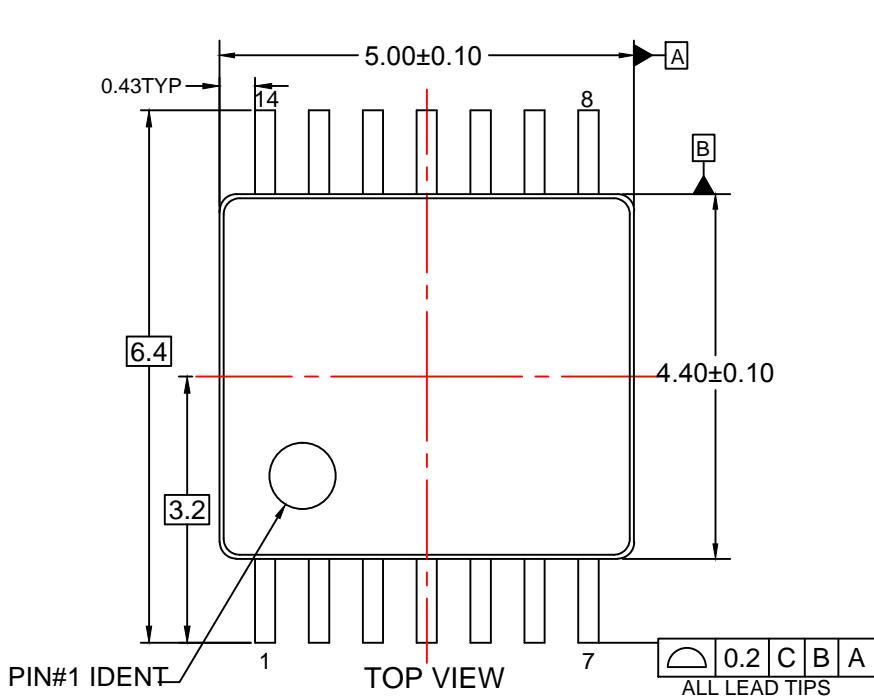
NOTES: unless otherwise specified

1. Cumulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is $\pm 0.002[0.05]$ for these dimensions on all 12mm tapes.
5. A_o and B_o measured on a plane 0.120[0.30] above the bottom of the pocket.
6. K_o measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Dimension in inches rounded.

Reel Dimensions inches (millimeters)



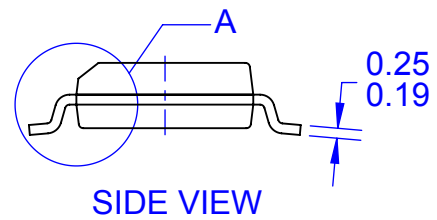
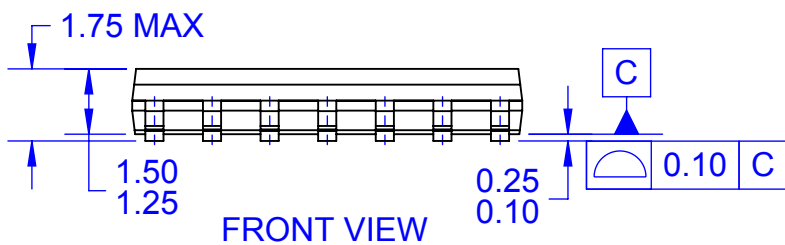
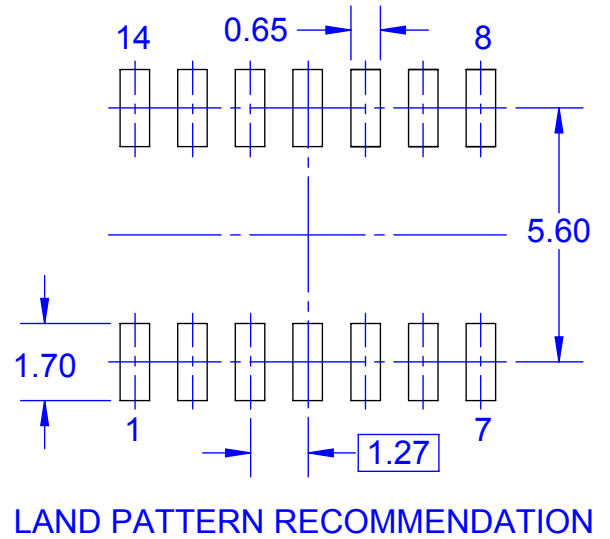
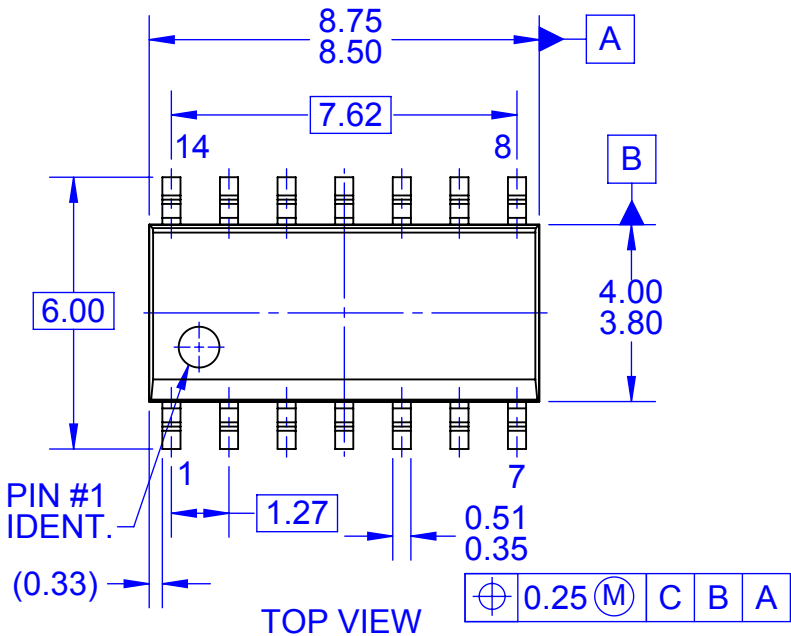
| Tape Size | A | B | C | D | N | W1 | W2 |
|-----------|--------------|--------------|---------------|---------------|---------------|--------------|--------------|
| 12mm | 13.0 (330.0) | 0.059 (1.50) | 0.512 (13.00) | 0.795 (20.20) | 2.165 (55.00) | 0.488 (12.4) | 0.724 (18.4) |



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 2009.
- E. LANDPATTERN STANDARD: SOP65P640X110-14M.
- F. DRAWING FILE NAME: MKT-MTC14rev7.





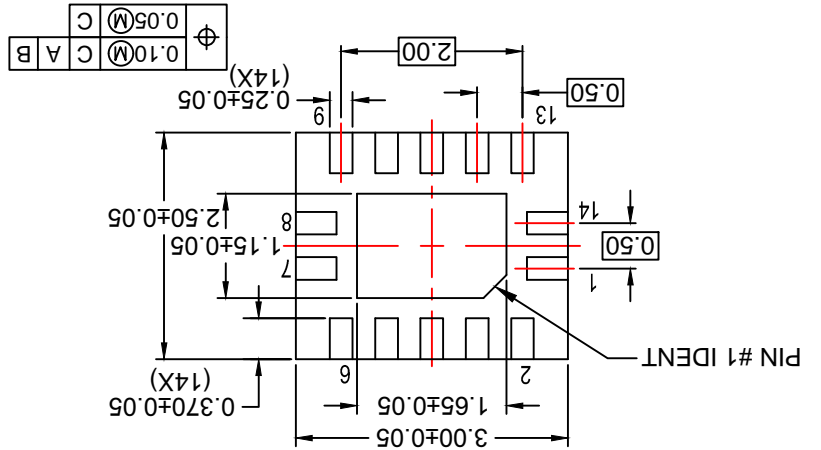
NOTES:

- A. CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C
- B. ALL DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
- D. LAND PATTERN STANDARD: SOIC127P600X145-14M
- E. CONFORMS TO ASME Y14.5M, 2009
- D. DRAWING FILENAME: MKT-M14Arev14

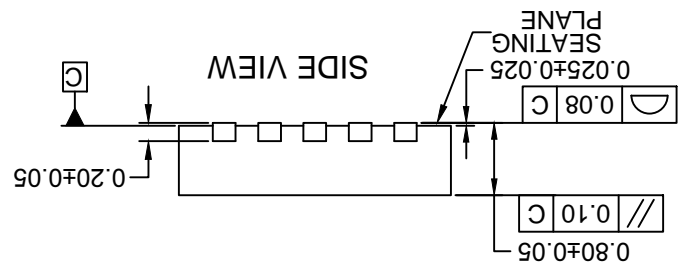




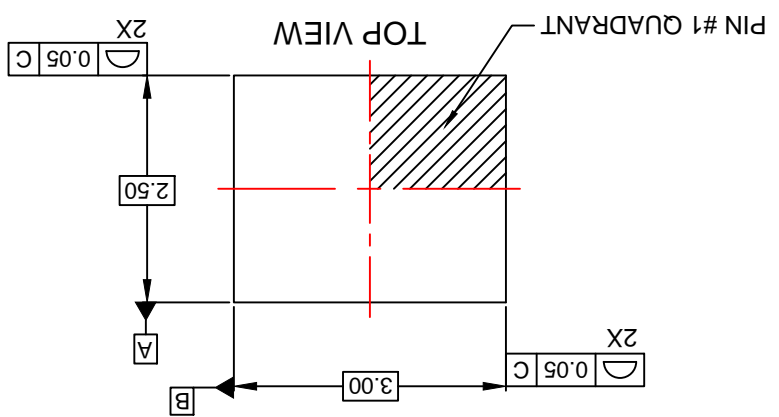
BOTTOM VIEW



SIDE VIEW

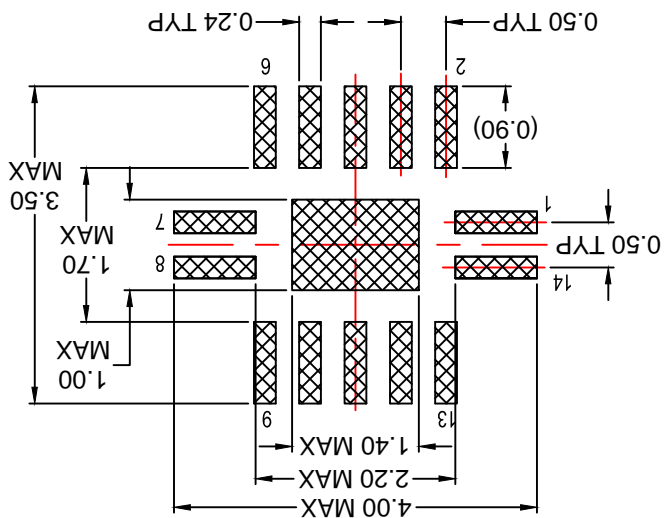


TOP VIEW



- NOTES:**
 A. CONFORMS TO JEDEC REGISTRATION MO-241, VARIATION AA
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
 D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
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RECOMMENDED LAND PATTERN



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