THE DATASHEET OF

SPEAR320-2

SPEAr320

Embedded MPU with ARM926 core, optimized for factory automation and consumer applications

Features

- ARM926EJ-S 333 MHz core
- High-performance 8-channel DMA
- Dynamic power-saving features
- Configurable peripheral functions on 102 shared I/Os.
- Memory:
  - 32 KB ROM and 8 KB internal SRAM
  - LPDDR-333/DDR2-666 external memory interface
  - SDIO/MMC card interface
  - Serial Flash memory interface (SMI)
  - Flexible static memory controller (FSMC) up to 16-bit data bus width, supporting NAND Flash
  - External memory interface (EMI) up to 16-bit data bus width, supporting NOR Flash and FPGAs
- Security
  - Cryptographic accelerator
- Connectivity
  - 2 x USB 2.0 Host
  - 1 x USB 2.0 Device
  - 2 x Fast Ethernet ports (for external MII/SMII PHY)
  - 2 x CAN interface
  - 3 x SSP Synchronous serial port (SPI, Microwire or TI protocol)
  - 2 x I^2C
  - 1 x fast IrDA interface
  - 3 x UART interface
  - 1 x standard parallel device port
- Peripherals supported
  - TFT/STN LCD controller (resolution up to 1024 x 768 and up to 24 bpp)
  - Touchscreen support

LFBGA289 (15 x 15 x 1.7 mm)

- Miscellaneous functions
  - Integrated real time clock, watchdog, and system controller
  - 8-channel 10-bit ADC, 1 Msps
  - 4 x PWM timers
  - JPEG CODEC accelerator
  - 6x 16-bit general purpose timers with programmable prescaler, 4 capture inputs
  - Up to 102 GPIOs with interrupt capability

Applications

The SPEAr320 embedded MPU is configurable for a range of industrial and consumer applications such as:

- Programmable logic controllers
- Factory automation
- Printers

Table 1. Device summary

Order code	Temp range, °C	Package	Packing
SPEAR320-2	-40 to 85	LFBGA289 (15x15 mm, pitch 0.8 mm)	Tray

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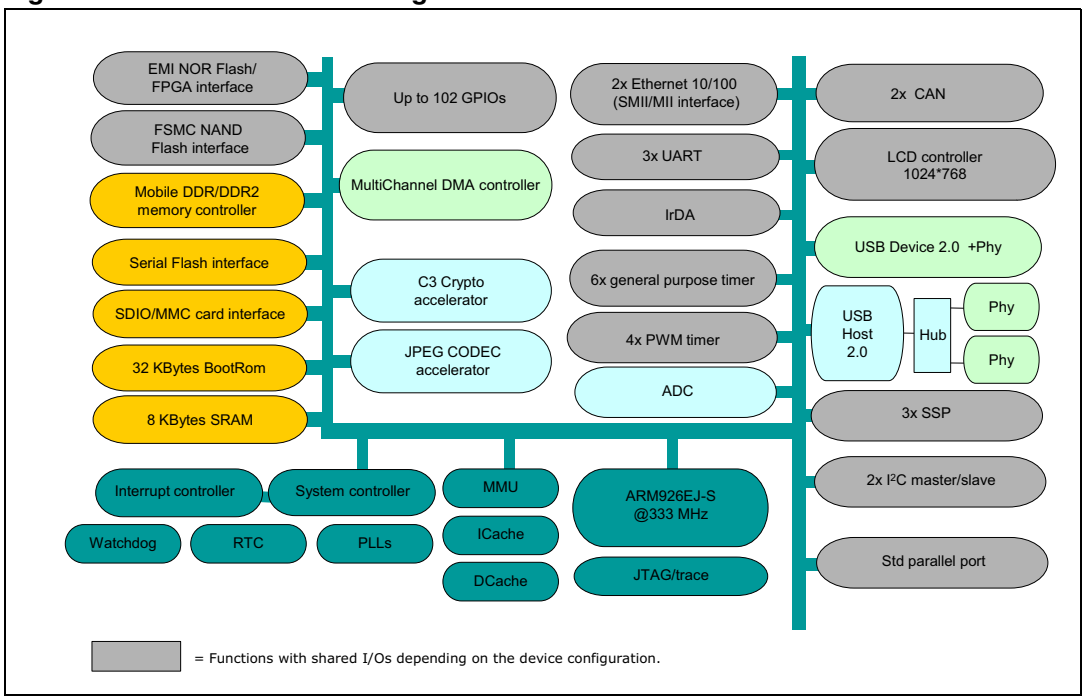
1 Description

The SPEAr320 is a member of the SPEAr family of embedded MPUs, optimized for industrial automation and consumer applications. It is based on the powerful ARM926EJ-S processor (up to 333 MHz), widely used in applications where high computation performance is required.

In addition, SPEAr320 has an MMU that allows virtual memory management - making the system compliant with Linux operating system. It also offers 16 KB of data cache, 16 KB of instruction cache, JTAG and ETM (Embedded Trace Macrocell™) for debug operations.

A full set of peripherals allows the system to be used in many applications, some typical applications being factory automation, printer and consumer applications.

Figure 1. Functional block diagram



2 Main features

- ARM926EJ-S 32-bit RISC CPU, up to 333 MHz
  - 16 Kbytes of instruction cache, 16 Kbytes of data cache
  - 3 instruction sets: 32-bit for high performance, 16-bit (Thumb) for efficient code density, byte Java mode (Jazelle™) for direct execution of Java code.
  - Tightly Coupled Memory
- 32-KByte on-chip BootROM
- 8-KByte on-chip SRAM
- External DRAM memory interface:
  - 8/16-bit (mobile DDR@166 MHz)
  - 8/16-bit (DDR2@333 MHz)
- Serial memory interface
- SDIO interface supporting SPI, SD1, SFD4 and SD8 modes
- 8/16-bits NAND Flash controller (FSMC)
- External memory interface (EMI) for connecting NOR Flash or FPGAs
- Boot capability from NAND Flash, serial/parallel NOR Flash
- Boot and field upgrade capability from USB
- High performance 8-channel DMA controller
- 3x Ethernet controllers (up to 2 operating concurrently)
- Two USB2.0 Host (high-full-low speed) with integrated PHY transceiver
- One USB2.0 Device (high-full-low speed) with integrated PHY transceiver
- 2x CAN 2.0 interfaces
- Up to 102 GPIOs with interrupt capability
- Up to 4 PWM outputs
- 3x SSP master/slave (supporting Motorola, Texas instruments, National semiconductor protocols) up to 41.5 Mbps
- Standard parallel port (SPP device implementation)
- 2 x I^2C master/slave interface (slow-fast-high speed, up to 1.2 Mb/s)
- 3x UART:
  - UART0 (up to 3 Mbps) with hardware flow control and modem interface
  - UART1 (up to 7 Mbps) with hardware flow control (in some operating modes)
  - UART2 (up to 7 Mbps) with software flow control
- ADC 10-bit, 1 Msps 8 inputs
- JPEG CODEC accelerator 1 clock/pixel
- Color LCD interface (up to 1024X768, 24-bits CLCD controller, TFT and STN panels)
- Touchscreen support
- Crypto accelerator (DES/3DES/AES/SHA1)

- Advanced power saving features
  - Normal, Slow, Doze and Sleep modes CPU clock with software-programmable frequency
  - Enhanced dynamic power-domain management
  - Clock gating functionality
  - Low frequency operating mode
  - Automatic power saving controlled from application activity demands
- Vectored interrupt controller
- System and peripheral controller
  - 3 pairs of 16-bit general purpose timers with programmable prescaler
  - RTC with separate power supply allowing battery connection
  - Watchdog timer
  - Miscellaneous registers array for embedded MPU configuration
- Programmable PLL for CPU and system clocks
- JTAG IEEE 1149.1 boundary scan
- ETM functionality multiplexed on primary pins
- Supply voltages
  - 1.2 V core, 1.8 V/2.5 V DDR, 2.5 V PLLs, 1.5 V RTC and 3.3 V I/Os
- Operating temperature: - 40 to 85 °C
- LFBGA289 (15 x 15 mm, pitch 0.8 mm)

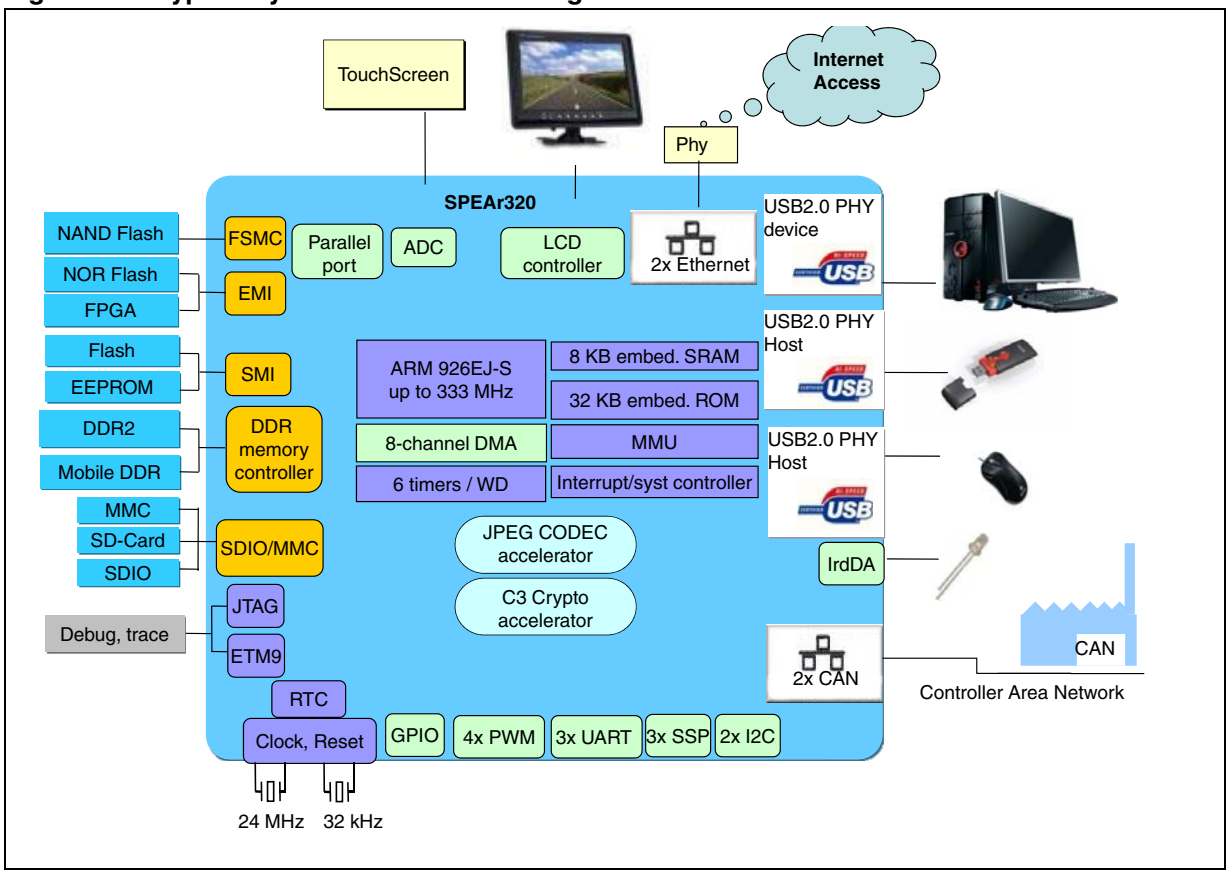
3 Architecture overview

The SPEAr320 internal architecture is based on several shared subsystem logic blocks interconnected through a multilayer interconnection matrix.

The switch matrix structure allows different subsystem dataflow to be executed in parallel improving the core platform efficiency.

High performance master agents are directly interconnected with the memory controller reducing the memory access latency. The overall memory bandwidth assigned to each master port can be programmed and optimized through an internal efficient weighted round-robin arbitration mechanism.

Figure 2. Typical system architecture using SPEAr320



3.1 CPU ARM 926EJ-S

The core of the SPEAr320 is an ARM926EJ-S reduced instruction set computer (RISC) processor.

It supports the 32-bit ARM and 16-bit Thumb instruction sets, enabling the user to trade off between high performance and high code density and includes features for efficient execution of Java byte codes.

The ARM CPU and is clocked at a frequency up to 333 MHz. It has a 16-Kbyte instruction cache, a 16-Kbyte data cache, and features a memory management unit (MMU) which makes it fully compliant with Linux and VxWorks operating systems.

It also includes an embedded trace module (ETM Medium+) for real-time CPU activity tracing and debugging. It supports 4-bit and 8-bit normal trace mode and 4-bit demultiplexed trace mode, with normal or half-rate clock.

3.2 Embedded memory units

- 32 Kbytes of BootROM
- 8 Kbytes of SRAM

3.2.1 BootROM

BootROM is small firmware program that is executed just after the SPEAr320 exits from reset.

It supports the following boot modes:

- Boot from NOR serial Flash
- Boot from NAND Flash
- Boot from NOR parallel Flash
- Boot / Upgrade from USB

The first three modes support different ways of booting the application software, they require a second-level boot software (Xloader) to be located in Flash.

USB boot mode can be used for software maintenance or upgrade, if booting from any of the Flash memories is not possible.

The BootROM selects the boot mode from the boot pin settings (see *Section 4.3.4: Boot pins*). A setting is available to allow the BootROM to be bypassed.

3.3 Mobile DDR/DDR2 memory controller

SPEAr320 integrates a high performance multi-channel memory controller able to support low power Mobile DDR and DDR2 double data rate memory devices. The multi-port architecture ensures memory is shared efficiently among different high-bandwidth client modules.

It has 6 internal ports. One of them is reserved for register access during the controller initialization while the other five are used to access the external memory.

It also includes the physical layer (PHY) and DLLs for fine tuning the timing parameters to maximize the data valid windows at different frequencies.

3.4 Serial memory interface

SPEAr320 provides a serial memory interface (SMI), acting as an AHB slave interface (32-, 16- or 8-bit) to SPI-compatible off-chip memories.

These serial memories can be used either as data storage or for code execution.

Main features:

- Supports SPI-compatible Flash and EEPROM devices
- Acts always as a SPI master and up to 2 SPI slave memory devices are supported (with separate chip select signals), with up to 16 MB address space each
- SMI clock signal (SMICLK) is generated by SMI (and input to all slaves) using a clock provided by the AHB bus
- SMICLK can be up to 50 MHz in fast read mode (or 20 MHz in normal mode). It can be controlled by a programmable 7-bit prescaler allowing up to 127 different clock frequencies.

3.5 External memory interface (EMI)

The EMI Controller provides a simple external memory interface that can be used for example to connect to NOR Flash memory or FPGA devices.

Main features:

- EMI bus master
- 16 and 8-bit transfers
- Can access 4 different peripherals using CS#, one at a time.
- Supports single asynchronous transfers.
- Supports peripherals which use Byte Lane procedure

3.6 SDIO controller/MMC card interface

The SDIO host controller conforms to the SD host Controller Standard Specification Version 2.0. It handles SDIO/SD Protocol at transmission level, packing data, adding cyclic redundancy check (CRC), start/end bit and checking for transaction format correctness. The host controller provides programmed I/O and DMA data transfer method.

Main features:

- Meets the following specifications:
  - SD Host Controller Standard Specification Version 2.0
  - SDIO card specification version 2.0
  - SD Memory Card Specification Draft version 2.0
  - SD Memory Card Security Specification version 1.01
  - MMC Specification version 3.31 and 4.2
- Supports both DMA and Non-DMA mode of operation
- Supports MMC Plus and MMC Mobile
- Card Detection (Insertion / Removal)
- Card password protection
- Host clock rate variable between 0 and 48 MHz
- Supports 1 bit, 4 bit and 8 bit SD modes and SPI mode
- Supports Multi Media Card Interrupt mode
- Allows card to interrupt host in 1 bit, 4 bit, 8 bit SD modes and SPI mode.
- Up to 100 Mbits per second data rate using 4 parallel data lines (SD4 bit mode)

- Up to 416 Mbits per second data rate using 8 bit parallel data lines (SD8 bit mode)
- Cyclic Redundancy Check CRC7 for command and CRC16 for data integrity
- Designed to work with I/O cards, Read-only cards and Read/Write cards
- Error Correction Code (ECC) support for MMC4.2 cards
- Supports Read wait Control, Suspend/Resume operation
- Supports FIFO Overrun and Underrun condition by stopping SD clock

3.7 Flexible static memory controller (FSMC)

SPEAr320 provides a Flexible Static Memory Controller (FSMC) which interfaces to external parallel NAND Flash memories.

Main features:

- 8/16-bit wide data path
- FSMC performs only one access at a time and only one external device is accessed
- Supports little-endian and big-endian memory architectures
- AHB burst transfer handling to reduce access time to external devices
- Supplies an independent configuration for each memory bank
- Programmable timings to support a wide range of devices
  - Programmable wait states (up to 31)
  - Programmable bus turnaround cycles (up to 15)
  - Programmable output enable and write enable delays (up to 15)
- Independent chip select control for each memory bank
- Shares the address bus and the data bus with all the external peripherals
- Only chips selects are unique for each peripheral
- External asynchronous wait control
- Boot memory bank configurable at reset using external control pins

3.8 Multichannel DMA controller

Within its basic subsystem, SPEAr320 provides a DMA controller (DMAC) able to service up to 8 independent DMA channels for serial data transfers between single source and destination (i.e., memory-to-memory, memory-to-peripheral, peripheral to- memory, and peripheral-to-peripheral).

Each DMA channel can support a unidirectional transfer, with internal four-word FIFO per channel.

3.9 Ethernet controllers

SPEAr320 features three multiplexed Ethernet MACs, supporting up to two ports concurrently.

The three controllers are named:

- MII0
- SMII0
- SMII1/MII1

Table 2. Ethernet port multiplexing

Configuration mode (see *Section 4.3.2: Configuration modes*)	Available interfaces	Interface name
Mode 1 or Mode 4	2 x SMII	SMII0 + SMII1
Mode 1 or Mode 4 with MII0 alternate I/O functions enabled	1 x SMII + 1 x MII	SMII0+ MII0
Mode 2 with MII0 alternate I/O functions enabled	2 x MII	MII1 + MII0
Mode 3	1 x SMII	SMII0
Mode 3 with MII0 alternate I/O functions enabled	1 x MII	MII0

3.9.1 MII0 Ethernet controller

Main features:

- Supports the default Media Independent Interface (MII) defined in the IEEE 802.3 specifications.
- Supports 10/100 Mbps data transfer rates
- Local FIFO available (4 Kbyte RX, 2 Kbyte TX)
- Supports both half-duplex and full-duplex operation. In half-duplex operation, CSMA/CD protocol is provided
- Programmable frame length to support both standard and jumbo Ethernet frames with size up to 16 Kbytes
- 32/64/128-bit data transfer interface on system-side.
- A variety of flexible address filtering modes are supported
- A set of control and status registers (CSRs) to control GMAC core operation
- Native DMA with single-channel transmit and receive engines, providing 32/64/128-bit data transfers
- DMA implements dual-buffer (ring) or linked-list (chained) descriptor chaining
- An AHB slave acting as programming interface to access all CSRs, for both DMA and GMAC core subsystems
- An AHB master for data transfer to system memory
- 32-bit AHB master bus width, supporting 32, 64, and 128-bit wide data transactions
- It supports both big-endian and little-endian.

3.9.2 SMII0/SMII1/MII1 Ethernet controllers

The two Ethernet controllers called SMII0 and SMII1/MII1 each have dedicated TX/RX signals while synchronization and clock signals are common for PHY connection.

Each of the two ports provides the following features:

- Compatible with IEEE Standard 802.3
- 10 and 100 Mbit/s operation
- Full and half duplex operation
- Statistics counter registers for RMON/MIB
- Interrupt generation to signal receive and transmit completion
- Automatic pad and CRC generation on transmitted frames
- Automatic discard of frames received with errors
- Address checking logic supports up to four specific 48-bit addresses
- Supports promiscuous mode where all valid received frames are copied to memory

- Hash matching of unicast and multicast destination addresses
- External address matching of received frames
- Physical layer management through MDIO interface
- Supports serial network interface operation
- Half duplex flow control by forcing collisions on incoming frames
- Full duplex flow control with recognition of incoming pause frames and hardware generation of transmitted pause frames
- Support for 802.1Q VLAN tagging with recognition of incoming VLAN and priority tagged frames
- Multiple buffers per receive and transmit frame
- Wake on LAN support
- Jumbo frames of up to 10240 bytes supported
- Configurable Endianess for the DMA Interface (AHB Master)

3.10 CAN controller

SPEAr320 has two CAN controllers for interfacing CAN 2.0 networks.

Main features:

- Supports CAN protocol version 2.0 part A and B
- Bit rates up to 1 MBit/s
- 16 message objects(136 X 16 message RAM)
- Each message object has its own identifier mask
- Maskable interrupt
- Programmable loop-back mode for self-test operation
- Disabled automatic retransmission mode for time triggered CAN applications

3.11 USB2 Host controller

SPEAr320 has two fully independent USB 2.0 Hosts. Each consists of 5 major blocks:

- EHCI capable of managing high-speed transfers (HS mode, 480 Mbps)
- OHCI that manages the full and the low speed transfers (12 and 1.5 Mbps)
- Local 2-Kbyte FIFO
- Local DMA
- Integrated USB2 transceiver (PHY)

Both Hosts can manage an external power switch, providing a control line to enable or disable the power, and an input line to sense any over-current condition detected by the external switch.

One Host controller at time can perform high speed transfer.

3.12 USB2 Device controller

Main features:

- Supports the 480 Mbps high-speed mode (HS) for USB 2.0, as well as the 12 Mbps full-speed (FS) and the low-speed (LS modes) for USB 1.1
- Supports 16 physical endpoints, configurable as different logical endpoints
- Integrated USB transceiver (PHY)
- Local 4 Kbyte FIFO shared among all the endpoints
- DMA mode and slave-only mode are supported
- In DMA mode, the UDC supports descriptor-based memory structures in application memory
- In both modes, an AHB slave is provided by UDC-AHB, acting as programming interface to access to memory-mapped control and status registers (CSRs)
- An AHB master for data transfer to system memory is provided, supporting 8, 16, and 32-bit wide data transactions on the AHB bus
- A USB plug (UPD) detects the connection of a cable.

3.13 CLCD controller

SPEAr320 has a color liquid crystal display controller (CLCDC) that provides all the necessary control signals to interface directly to a variety of color and monochrome LCD panels.

Main features:

- Resolution programmable up to 1024 x 768
- 16-bpp true-color non-palletized, for color STN and TFT
- 24-bpp true-color non-palletized, for color TFT
- Supports single and dual panel mono super twisted nematic (STN) displays with 4 or 8-bit interfaces
- Supports single and dual-panel color and monochrome STN displays
- Supports thin film transistor (TFT) color displays
- 15 gray-level mono, 3375 color STN, and 32 K color TFT support
- 1, 2, or 4 bits per pixel (bpp) palletized displays for mono STN
- 1, 2, 4 or 8-bpp palletized color displays for color STN and TFT
- Programmable timing for different display panels
- 256 entry, 16-bit palette RAM, arranged as a 128 x 32-bit RAM physically frame, line and pixel clock signals
- AC bias signal for STN and data enable signal for TFT panels patented gray scale algorithm
- Supports little and big-endian

3.14 GPIOs

A maximum of 102 GPIOs (PL_GPIOs) are available when part of the embedded IPs are not needed (see *Section 4.3: Shared I/O pins (PL_GPIOs)*).

Within its basic subsystem, SPEAr320 provides a base General Purpose Input/Output (GPIO) block (basGPIO). The base GPIO block provides 6 programmable inputs or outputs. Each input/output can be controlled in two distinct modes:

- Software mode, through an APB interface.
- Hardware mode, through a hardware control interface.

Main features of the base GPIO block are:

- Six individually programmable input/output pins (default to input at reset)
- An APB slave acting as control interface in "software mode"
- Programmable interrupt generation capability on any number of pins.
- Hardware control capability of GPIO lines for different system configurations.
- Bit masking in both read and write operation through address lines.

Other GPIO blocks are present in the reconfigurable array subsystem.

3.15 Parallel port

Main features:

- Slave mode device interface for standard parallel port host
- Supports unidirectional 8-bit data transfer from host to slave
- Supports 9th bit for parity/data/command etc.
- Maskable interrupts for data, device reset, auto line feed
- APB input clock frequency required is 83 MHz for acknowledgement timings

3.16 Synchronous serial ports (SSP)

SPEAr320 provides three synchronous serial ports (SSP) that offer a master or slave interface to enable synchronous serial communication with slave or master peripherals

Main features:

- Master or slave operation.
- Programmable clock bit rate and prescale.
- Separate transmit and receive first-in, first-out memory buffers, 16-bits wide, 8 locations deep.
- Programmable choice of interface operation:
  - SPI (Motorola)
  - Microwire (National Semiconductor)
  - TI synchronous serial.
- Programmable data frame size from 4 to 16-bits.
- Independent masking of transmit FIFO, receive FIFO, and receive overrun interrupts.
- Internal loopback test mode available.
- DMA interface

3.17 I2C

The SPEAr320 has 2 I2C interfaces:

Main features:

- Compliance to the I^2C bus specification (Philips)
- Supports three modes:
  - Standard (100 kbps)
  - Fast (400 kbps)
  - High-speed
- Clock synchronization
- Master and slave mode configuration possible
- Multi-master mode (bus arbitration)
- 7-bit or 10-bit addressing
- 7-bit or 10-bit combined format transfers

- Slave bulk transfer mode
- Ignores CBUS addresses (predessor to I2C that used to share the I2C bus)
- Transmit and receive buffers
- Interrupt or polled-mode operation
- Handles bit and byte waiting at all bus speeds
- Digital filter for the received SDA and SCL lines
- Handles component parameters for configurable software driver support
- Supports APB data bus widths of 8, 16 and 32 bits.

3.18 UARTs

The SPEAr320 has 3 UARTs with different capabilities.

3.18.1 UART0

Main features:

- Separate 16 x 8 (16 locations deep x 8-bit wide) transmit and 16 x 12 receive FIFOs to reduce CPU interrupts
- Speed up to 3 Mbps
- Hardware and/or software flow control
- Modem interface signals

3.18.2 UART1

Main features:

- Separate 16 x 8 (16 location deep x 8-bit wide) transmit and 16x12 receive FIFOs to reduce CPU interrupts
- Speed up to 7 Mbps
- Hardware flow control (in Small Printers and Automation Expansion modes only) and/or software flow control

3.18.3 UART2

Main features:

- Separate 16x8 (16 location deep x 8-bit wide) transmit and 16x12 receive FIFOs to reduce CPU interrupts
- Speed up to 7 Mbps
- Software flow control

3.19 JPEG CODEC

SPEAr320 provides a JPEG CODEC with header processing (JPGC), able to decode (or encode) image data contained in the SPEAr320 RAM, from the JPEG (or MCU) format to the MCU (or JPEG) format.

Main features:

- Compliance with the baseline JPEG standard (ISO/IEC 10918-1)
- Single-clock per pixel encoding/decoding
- Support for up to four channels of component color
- 8-bit/channel pixel depths
- Programmable quantization tables (up to four)
- Programmable Huffman tables (two AC and two DC)
- Programmable minimum coded unit (MCU)
- Configurable JPEG header processing
- Support for restart marker insertion
- Use of two DMA channels and of two 8 x 32-bits FIFO's (local to the JPEG) for efficient transferring and buffering of encoded/decoded data from/to the CODEC core.

3.20 Cryptographic co-processor (C3)

SPEAr320 has an embedded Channel Control Coprocessor (C3). C3 is a high-performance instruction driven DMA based co-processor. It executes instruction flows generated by the host processor. After it has been set-up by the host it runs in a completely autonomous way (DMA data in, data processing, DMA data out), until the completion of all the requested operations.

C3 has been used to accelerate the processing of cryptographic, security and network security applications. It can be used for other types of data intensive applications as well.

Main features:

- Supported cryptographic algorithms:
  - Advanced encryption standard (AES) cipher in ECB, CBC, CTR modes.
  - Data encryption standard (DES) cipher in ECB and CBC modes.
  - SHA-1, HMAC-SHA-1, MD5, HMAC-MD5 digests.
- Instruction driven DMA based programmable engine.
- AHB master port for data access from/to system memory.
- AHB slave port for co-processor register accesses and initial engine-setup.
- The co-processor is fully autonomous (DMA input reading, cryptographic operation execution, DMA output writing) after being set up by the host processor.
- The co-processor executes programs written by the host in memory, it can execute an unlimited list of programs.
- The co-processor supports hardware chaining of cryptographic blocks for optimized execution of data-flow requiring multiple algorithms processing over the same set of data (for example encryption + hashing on the fly).

3.21 8-channel ADC

Main features:

- Successive approximation conversion method
- 10-bit resolution @1 Msps
- Hardware supporting up to 13.5 bits resolution at 8 ksps by oversampling and accumulation
- Eight analog input (AIN) channels, ranging from 0 to 2.5 V
- INL ± 1 LSB, DNL ± 1 LSB
- Programmable conversion speed, (min. conversion time is 1 µs)
- Programmable averaging of results from 1 (No averaging) up to 128
- Programmable auto scan for all the eight channels.

3.22 System controller

The System Controller provides an interface for controlling the operation of the overall system.

Main features:

- Power saving system mode control
- Crystal oscillator and PLL control
- Configuration of system response to interrupts
- Reset status capture and soft reset generation
- Watchdog and timer module clock enable

3.22.1 Power saving system mode control

Using three mode control bits, the system controller switch the SPEAr320 to any one of four different modes: DOZE, SLEEP, SLOW and NORMAL.

- **SLEEP mode**: In this mode the system clocks, HCLK and CLK, are disabled and the System Controller clock SCLK is driven by a low speed oscillator (nominally 32768 Hz). When either a FIQ or an IRQ interrupt is generated (through the VIC) the system enters DOZE mode. Additionally, the operating mode setting in the system control register automatically changes from SLEEP to DOZE.
- **DOZE mode**: In this mode the system clocks, HCLK and CLK, and the System Controller clock SCLK are driven by a low speed oscillator. The System Controller moves into SLEEP mode from DOZE mode only when none of the mode control bits are set and the processor is in Wait-for-interrupt state. If SLOW mode or NORMAL mode is required the system moves into the XTAL control transition state to initialize the crystal oscillator.
- **SLOW mode**: During this mode, both the system clocks and the System Controller clock are driven by the crystal oscillator. If NORMAL mode is selected, the system goes into the "PLL control" transition state. If neither the SLOW nor the NORMAL mode control bits are set, the system goes into the "Switch from XTAL" transition state.
- **NORMAL mode**: In NORMAL mode, both the system clocks and the System Controller clock are driven by the PLL output. If the NORMAL mode control bit is not set, then the system goes into the "Switch from PLL" transition state.

3.22.2 Clock and reset system

The clock system is a fully programmable block that generates all the clocks necessary to the chip.

The default operating clock frequencies are:

- Clock @ 333 MHz for the CPU.
- Clock @ 166 MHz for AHB bus and AHB peripherals.
- Clock @ 83 MHz for, APB bus and APB peripherals.
- Clock @ 333 MHz for DDR memory interface.

The default values give the maximum allowed clock frequencies. The clock frequencies are fully programmable through dedicated registers.

The clock system consists of 2 main parts: a multi clock generator block and two internal PLLs.

The multi clock generator block, takes a reference signal (which is usually delivered by the PLL), generates all clocks for the IPs of SPEAr320 according to dedicated programmable registers.

Each PLL uses an oscillator input of 24 MHz to generate a clock signal at a frequency corresponding at the highest of the group. This is the reference signal used by the multi clock generator block to obtain all the other requested clocks for the group. Its main feature is electromagnetic interference reduction capability.

The user can set up the PLL in order to modulate the VCO with a triangular wave. The resulting signal has a spectrum (and power) spread over a small programmable range of frequencies centered on F0 (the VCO frequency), obtaining minimum electromagnetic emissions. This method replaces all the other traditional methods of EMI reduction, such as filtering, ferrite beads, chokes, adding power layers and ground planes to PCBs, metal shielding and so on. This gives the customer appreciable cost savings.

In sleep mode the SPEAr320 runs with the PLL disabled so the available frequency is 24 MHz or a sub-multiple (/2, /4, /8).

3.23 Vectored interrupt controller (VIC)

The VIC allows the OS interrupt handler to quickly dispatch interrupt service routines in response to peripheral interrupts. There are 32 interrupt lines and the VIC uses a separate bit position for each interrupt source. Software controls each request line to generate software interrupts.

3.24 General purpose timers

SPEAr320 provides 6 general purpose timers (GPTs) acting as APB slaves.

Each GPT consists of 2 channels, each one made up of a programmable 16-bit counter and a dedicated 8-bit timer clock prescaler. The programmable 8-bit prescaler performs a clock division by 1 up to 256, and different input frequencies can be chosen through configuration registers (a frequency range from 3.96 Hz to 48 MHz can be synthesized).

Two different modes of operation are available :

- Auto-reload mode, an interrupt source is activated, the counter is automatically cleared and then it restarts incrementing.
- Single-shot mode, an interrupt source is activated, the counter is stopped and the GPT is disabled.

3.25 PWM timers

SPEAr320 provides 4 PWM timers.

Main features:

- Prescaler to define the input clock frequency to each timer
- Programmable duty cycle from 0% to 100%
- Programmable pulse length
- APB slave interface for register programming

3.26 Watchdog timer

The ARM watchdog module consists of a 32-bit down counter with a programmable timeout interval that has the capability to generate an interrupt and a reset signal on timing out. The watchdog module is intended to be used to apply a reset to a system in the event of a software failure.

3.27 RTC oscillator

The RTC provides a 1-second resolution clock. This keeps time when the system is inactive and can be used to wake the system up when a programmed alarm time is reached. It has a clock trimming feature to compensate for the accuracy of the 32.768 kHz crystal and a secured time update.

Main features:

- Time-of-day clock in 24 hour mode
- Calendar
- Alarm capability
- Isolation mode, allowing RTC to work even if power is not supplied to the rest of the device.

4 Pin description

The following tables describe the pinout of the SPEAr320 listed by functional block.

List of abbreviations:

PU = Pull Up

PD = Pull Down

4.1 Required external components

1. DDR_COMP_1V8: place an external 121 kΩ resistor between ball P4 and ball R4
2. USB_TX_RTUNE: connect an external 43.2 Ω pull-down resistor to ball K5
3. DIGITAL_REXT: place an external 121 kΩ resistor between ball G4 and ball F4
4. DITH_VDD_2V5: Add a ferrite bead to ball M4

4.2 Dedicated pins

Table 3. Master clock, RTC, Reset and 3.3 V comparator pin descriptions

Group	Signal name	Ball	Direction	Function	Pin type
Master Clock	MCLK_XI	P1	In	24 MHz (typical) crystal in	Oscillator 2.5 V capable
	MCLK_XO	P2	Out	24 MHz (typical) crystal out	
RTC	RTC_XI	E2	In	32 kHz crystal in	Oscillator 1V5 capable
	RTC_XO	E1	Out	32 kHz crystal out	
Reset	MRESET	M17	In	Main Reset	TTL Schmitt trigger input buffer, 3.3 V tolerant
3.3 V Comp.	DIGITAL_REXT	G4	Out	Configuration	Analog, 3.3 V capable
	DIGITAL_GNDBG COMP	F4	Power	Power	Power

Table 4. Power supply pin description

Group	Signal name	Ball	Value
DIGITAL GROUND	GND	G6 G7 G8 G9 G10 G11 H6 H7 H8 H9 H10 H11 J6 J7 J8 J9 J10 J11 K6 K7 K8 K9 K10 K11 L6 L7 L8 L9 L10 M8 M9 M10	0 V
	USB_HOST1_HOST0_DEVICE_DVSS	L5	

Table 4. Power supply pin description (continued)

Group	Signal name	Ball	Value
ANALOG GROUND	RTC_GND	F2	0 V
	DITH_PLL_VSS_ANA	G1	
	USB_HOST1_VSSA	J2	
	USB_HOST0_VSSA	L1	
	USB_COMMON_VSSAC	L3	
	USB_DEVICE_VSSA	N2	
	DITH_VSS2V5	N4	
	MCLK_GND	P3	
	MCLK_GNDSUB	R3	
	ADC_AGND	N12	
I/O	DIGITAL_VDDE3V3	F5 F6 F7 F10 F11 F12 G5 J12 K12 L12 M12	3.3 V
CORE	VDD	F8 F9 G12 H5 H12 J5 L11 M6 M7 M11	1.2 V
USB HOST0 PHY	USB_HOST0_VDD2V5	L2	2.5 V
	USB_HOST0_VDD3V3	K4	3.3 V
USB HOST1 PHY	USB_HOST1_VDD2V5	K3	2.5 V
	USB_HOST1_VDD3V3	J1	3.3 V
USB DEVICE PHY	USB_DEVICE_VDD2V5	N1	2.5 V
	USB_DEVICE_VDD3V3	N3	3.3 V
	USB_HOST1_HOST0_DEVICE_DVDD1V2	M3	1.2 V
OSCI (master clock)	MCLK_VDD	R1	1.2 V
	MCLK_VDD2V5	R2	2.5 V
PLL1	DITH_PLL_VDD_ANA	G2	2.5 V
PLL2	DITH_VDD_2V5	M4	2.5 V
DDR I/O	DDR_VDDE1V8	M5 N5 N6 N7 N8 N9 N10 N11	1.8 V
ADC	ADC_AVDD	N13	2.5 V
OSCI RTC	RTC_VDD1V5	F1	1.5 V

Note: All the VDD 2V5 power supplies are analog VDD.

Table 5. Debug pin description

Signal name	Ball	Direction	Function	Pin type
TEST_0	K16	In	Test configuration ports. For functional mode, they have to be set to zero.	TTL input buffer, 3.3 V tolerant, PD
TEST_1	K15			
TEST_2	K14			
TEST_3	K13			
TEST_4	J15			
BOOT_SEL	J14		Reserved, to be fixed at high level	
nTRST	L16	In	Test reset input	TTL Schmitt trigger input buffer, 3.3 V tolerant, PU
TDO	L15	Out	Test data output	TTL output buffer, 3.3 V capable 4 mA
TCK	L17	In	Test clock	TTL Schmitt trigger input buffer, 3.3 V tolerant, PU
TDI	L14	In	Test data input	
TMS	L13	In	Test mode select	

Table 6. SMI pin description

Signal name	Ball	Direction	Function	Pin type
SMI_DATAIN	M13	In	Serial Flash input data	TTL Input Buffer 3.3 V tolerant, PU
SMI_DATAOUT	M14	Out	Serial Flash output data	TTL output buffer 3.3 V capable 4 mA
SMI_CLK	N17	I/O	Serial Flash clock	
SMI_CS_0	M15	Out	Serial Flash chip select	
SMI_CS_1	M16			

Table 7. USB pin description

Group	Signal name	Ball	Direction	Function	Pin type
USB Device	USB_DEVICE_DP	M1	I/O	USB Device D+	Bidirectional analog buffer 5 V tolerant
	USB_DEVICE_DM	M2		USB Device D-	
	USB_DEVICE_VBUS	G3	In	USB Device VBUS	TTL input buffer 3.3 V tolerant, PD

Table 7. USB pin description (continued)

Group	Signal name	Ball	Direction	Function	Pin type
USB Host	USB_HOST1_DP	H1	I/O	USB HOST1 D+	Bidirectional analog buffer 5 V tolerant
	USB_HOST1_DM	H2		USB HOST1 D-	
	USB_HOST1_VBUS	H3	Out	USBHOST1 VBUS	TTL output buffer 3.3 V capable, 4 mA
	USB_HOST1_OVERCUR	J4	In	USB Host1 Over-Current	TTL input buffer 3.3 V tolerant, PD
	USB_HOST0_DP	K1	I/O	USB HOST0 D+	Bidirectional analog buffer 5 V tolerant
	USB_HOST0_DM	K2		USB HOST0 D-	
	USB_HOST0_VBUS	J3	Out	USB HOST0 VBUS	TTL output buffer 3.3 V capable, 4 mA
	USB_HOST0_OVERCUR	H4	In	USB Host0 Over-current	TTL Input Buffer 3.3 V tolerant, PD
USB	USB_TXRTUNE	K5	Out	Reference resistor	Analog
	USB_ANALOG_TEST	L4	Out	Analog Test Output	Analog

Table 8. ADC pin description

Signal name	Ball	Direction	Function	Pin type
AIN_0	N16	In	ADC analog input channel	Analog buffer 2.5 V tolerant
AIN_1	N15			
AIN_2	P17			
AIN_3	P16			
AIN_4	P15			
AIN_5	R17			
AIN_6	R16			
AIN_7	R15			
ADC_VREFN	N14		ADC negative voltage reference	
ADC_VREFP	P14		ADC positive voltage reference	

Table 9. DDR pin description

Signal name	Ball	Direction	Function	Pin type
DDR_MEM_ADD_0	T2	Out	Address Line	SSTL_2/SSTL_18
DDR_MEM_ADD_1	T1			
DDR_MEM_ADD_2	U1			
DDR_MEM_ADD_3	U2			
DDR_MEM_ADD_4	U3			
DDR_MEM_ADD_5	U4			
DDR_MEM_ADD_6	U5			
DDR_MEM_ADD_7	T5			
DDR_MEM_ADD_8	R5			
DDR_MEM_ADD_9	P5			
DDR_MEM_ADD_10	P6			
DDR_MEM_ADD_11	R6			
DDR_MEM_ADD_12	T6			
DDR_MEM_ADD_13	U6			
DDR_MEM_ADD_14	R7			
DDR_MEM_BA_0	P7	Out	Bank select	
DDR_MEM_BA_1	P8			
DDR_MEM_BA_2	R8			
DDR_MEM_RAS	U8	Out	Row Add. Strobe	
DDR_MEM_CAS	T8	Out	Col. Add. Strobe	
DDR_MEM_WE	T7	Out	Write enable	
DDR_MEM_CLKEN	U7	Out	Clock enable	
DDR_MEM_CLKP	T9	Out	Differential clock	Differential SSTL_2/ SSTL_18
DDR_MEM_CLKN	U9			
DDR_MEM_CS_0	P9	Out	Chip Select	SSTL_2/ SSTL_18
DDR_MEM_CS_1	R9			
DDR_MEM_ODT_0	T3	I/O	On-Die Termination Enable lines	
DDR_MEM_ODT_1	T4			

Table 9. DDR pin description (continued)

Signal name	Ball	Direction	Function	Pin type
DDR_MEM_DQ_0	P11	I/O	Data Lines (Lower byte)	SSTL_2/ SSTL_18
DDR_MEM_DQ_1	R11			
DDR_MEM_DQ_2	T11			
DDR_MEM_DQ_3	U11			
DDR_MEM_DQ_4	T12			
DDR_MEM_DQ_5	R12			
DDR_MEM_DQ_6	P12			
DDR_MEM_DQ_7	P13			
DDR_MEM__DQS_0	U10	Out	Lower Data Strobe	Differential SSTL_2/ SSTL_18
nDDR_MEM_DQS_0	T10			
DDR_MEM_DM_0	U12	Out	Lower Data Mask	SSTL_2/ SSTL_18
DDR_MEM_GATE_OPEN_0	R10	I/O	Lower Gate Open	
DDR_MEM_DQ_8	T17	I/O	Data Lines (Upper byte)	
DDR_MEM_DQ_9	T16			
DDR_MEM_DQ_10	U17			
DDR_MEM_DQ_11	U16			
DDR_MEM_DQ_12	U14			
DDR_MEM_DQ_13	U13			
DDR_MEM_DQ_14	T13			
DDR_MEM_DQ_15	R13			
DDR_MEM_DQS_1	U15	I/O	Upper Data Strobe	Differential SSTL_2/ SSTL_18
nDDR_MEM_DQS_1	T15			
DDR_MEM_DM_1	T14	I/O	Upper Data Mask	SSTL_2/ SSTL_18
DDR_MEM_GATE_OPEN_1	R14		Upper Gate Open	
DDR_MEM_VREF	P10	In	Reference Voltage	Analog
DDR_MEM_COMP2V5_GNDBGCOMP	R4	Power	Return for Ext. Resistors	Power
DDR_MEM_COMP2V5_REXT	P4	Power	Ext. Resistor	Analog
DDR2_EN	J13	In	Configuration	TTL Input Buffer 3.3 V Tolerant, PU

4.3 Shared I/O pins (PL_GPIOs)

The 98 PL_GPIO and 4 PL_CLK pins have the following characteristics:

- Output buffer: TTL 3.3 V capable up to 10 mA
- Input buffer: TTL, 3.3 V tolerant, selectable internal pull up/pull down (PU/PD)

The PL_GPIOs can be configured in different modes. This allows SPEAr320 to be tailored for use in various applications like:

- Metering concentrators
- Large power supply controllers
- Small printers

4.3.1 PL_GPIO pin description

Table 10. PL_GPIO pin description

Group	Signal name	Ball	Direction	Function	Pin type
PL_GPIOs	PL_GPIO_97... PL_GPIO_0	(see the *Table 11*)	I/O	General purpose I/O or multiplexed pins (see *Table 11*)	(see the introduction of the *Section 4.3* here above)
	PL_CLK1... PL_CLK4			programmable logic external clocks	

4.3.2 Configuration modes

This section describes the main operating modes created by using a selection of the embedded IPs.

The following modes can be selected by programming some control registers present in the reconfigurable array subsystem.

- Mode 1: SMII automation networking mode
- Mode 2: MII automation networking mode
- Mode 3: Expanded automation mode
- Mode 4: Printer mode

Table 11: PL_GPIO multiplexing scheme shows all the I/O functions available in each mode.

Mode 1 is the default mode for SPEAr320.

SMII automation networking mode

The “SMII Automation networking” operating mode mainly provides:

- NAND Flash interface (8 bits, 4 chip selects)
- 2 CAN2.0 interfaces
- 2 SMII interfaces
- 3 UARTs
  - 1 with hardware flow control (up to 3 Mbps)
  - 2 with software flow control (baud rate up to 7 Mbps)
- LCD interface (up to 1024x768, 24-bits LCD controller, TFT and STN panels)
- Touchscreen facilities
- 3 independent SSP Synchronous Serial Port (SPI, Microwire or TI protocol) ports
- GPIOs with interrupt capability
- SDIO interface supporting SPI, SD1, SD4 and SD8 mode

MII automation networking mode

The “MII Automation networking” operating mode mainly provides:

- NAND Flash interface (8 bits, 4 chip selects)
- 2 CAN2.0 interfaces
- 2 MII interfaces
- 3 UARTs
  - 1 with hardware flow control (up to 3 Mbps)
  - 2 with software flow control (baud rate up to 7 Mbps)
- 3 independent SSP Synchronous Serial Port (SPI, Microwire or TI protocol) ports
- GPIOs with interrupt capability
- SDIO interface supporting SPI, SD1, SD4 and SD8 mode

Expanded automation mode

The “Expanded automation” operating mode mainly provides:

- External Memory Interface (16 data bits, 24 address bits and 4 chip selects)
- NAND Flash interface (8-16 bits and 4 chip selects shared with EMI)
- 2 CAN2.0 interfaces
- SMII or MII interface
- 3 UARTs
  - 1 with hardware flow control (up to 3 Mbps)
  - 1 with hardware flow control (baud rate up to 7 Mbps)
  - 1 with software flow control (baud rate up to 7 Mbps)
- SSP port
- 2 independent I2C interfaces
- Up to 4 PWM outputs
- GPIOs with interrupt capabilities

Printer mode

The “printer” operating mode mainly provides:

- NAND Flash interface (8 bits, 4 chip selects)
- Up to 4 PWM outputs
- 2 SMII interfaces
- 3 UARTs
  - 1 with hardware flow control (up to 3 Mbps)
  - 1 with hardware flow control (baud rate up to 7 Mbps)
  - 1 with software flow control (baud rate up to 7 Mbps)
- SDIO interface supporting SPI, SD1, SD4 and SD8 mode
- Standard Parallel Port (SPP device implementation)
- 2 independent SSP Synchronous Serial Ports (SPI, Microwire or TI protocol)
- GPIOs with interrupt capabilities
-

4.3.3 Alternate functions

Other peripheral functions are listed in the Alternate Functions column of *Table 11: PL_GPIO multiplexing scheme* and can be individually enabled/disabled configuring the bits of a dedicated control register.

4.3.4 Boot pins

The status of the boot pins is read at startup by the BootROM.

4.3.5 GPIOs

The PL_GPIO pins can be used as software controlled general purpose I/Os (GPIOs) if they are not used by the I/O functions of the SPEAr320 IPs.

To configure any PL_GPIO pin as GPIO, set the corresponding bit in the GPIO_Select(0 ..3) registers that are 102 bits write registers that select GPIO versus some IPs.

4.3.6 Multiplexing scheme

To provide the best I/O multiplexing flexibility and the higher number of GPIOs for ARM controlled input-output function, the following hierarchical multiplexing scheme has been implemented.

Figure 3. Hierarchical multiplexing scheme

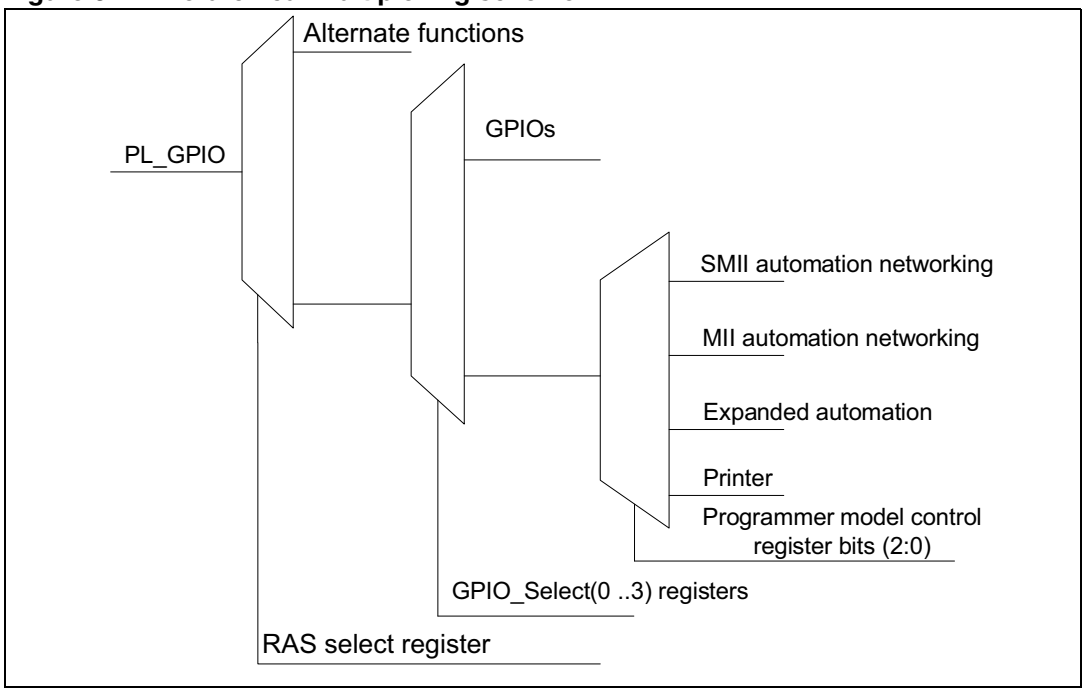


Table 11. PL_GPIO multiplexing scheme

PL_GPIO_# / ball number	Configuration mode (enabled by Programmer model control register bits (2:0))				Alternate function (enabled by RAS select register)	Boot pins	Function in GPIO alternative mode
	1	2	3	4			
PL_GPIO_97/H16	CLD0	MII1_TXCLK	EMI_A0	0			GPIO_97
PL_GPIO_96/H15	CLD1	MII1_TXD0	EMI_A1	0			GPIO_96
PL_GPIO_95/H14	CLD2	MII1_TXD1	EMI_A2	0			GPIO_95
PL_GPIO_94/H13	CLD3	MII1_TXD2	EMI_A3	0			GPIO_94
PL_GPIO_93/G17	CLD4	MII1_TXD3	EMI_A4	0			GPIO_93
PL_GPIO_92/G16	CLD5	MII1_TXEN	EMI_A5	0			GPIO_92
PL_GPIO_91/G15	CLD6	MII1_TXER	EMI_A6	0			GPIO_91
PL_GPIO_90/G14	CLD7	MII1_RXCLK	EMI_A7	0			GPIO_90
PL_GPIO_89/F17	CLD8	MII1_RXDV	EMI_A8	0			GPIO_89
PL_GPIO_88/F16	CLD9	MII1_RXER	EMI_A9	0			GPIO_88
PL_GPIO_87/G13	CLD10	MII1_RXD0	EMI_A10	0			GPIO_87

Table 11. PL_GPIO multiplexing scheme (continued)

PL_GPIO_# / ball number	Configuration mode (enabled by Programmer model control register bits (2:0))				Alternate function (enabled by RAS select register)	Boot pins	Function in GPIO alternative mode
	1	2	3	4			
PL_GPIO_86/E17	CLD11	MII1_RXD1	EMI_A11	0			GPIO_86
PL_GPIO_85/F15	CLD12	MII1_RXD2	EMI_A12	SPP_DATA0			GPIO_85
PL_GPIO_84/D17	CLD13	MII1_RXD3	EMI_A13	SPP_DATA1			GPIO_84
PL_GPIO_83/E16	CLD14	MII1_COL	EMI_A14	SPP_DATA2			GPIO_83
PL_GPIO_82/E15	CLD15	MII1_CRS	EMI_A15	SPP_DATA3			GPIO_82
PL_GPIO_81/C17	CLD16	MII1_MDIO	EMI_A16	SPP_DATA4			GPIO_81
PL_GPIO_80/D16	CLD17	MII1_MDC	EMI_A17	SPP_DATA5			GPIO_80
PL_GPIO_79/F14	CLD18	0	EMI_A18	SPP_DATA6			GPIO_79
PL_GPIO_78/D15	CLD19	0	EMI_A19	SPP_DATA7			GPIO_78
PL_GPIO_77/B17	CLD20	0	EMI_A20	SPP_STRBn			GPIO_77
PL_GPIO_76/F13	CLD21	0	EMI_A21	SPP_ACKn			GPIO_76
PL_GPIO_75/E14	CLD22	0	EMI_A22	SPP_BUSY			GPIO_75
PL_GPIO_74/C16	CLD23	0	EMI_A23	SPP_PERROR			GPIO_74
PL_GPIO_73/A17	CLAC	0	EMI_D8/ FSMC_D8	SPP_SELECT			GPIO_73
PL_GPIO_72/B16	CLFP	0	EMI_D9/ FSMC_D9	SPP_AUTOFDn			GPIO_72
PL_GPIO_71/D14	CLLP	0	EMI_D10/ FSMC_D10	SPP_FAULTn			GPIO_71
PL_GPIO_70/C15	CLLE	0	EMI_D11/ FSMC_D11	SPP_INITn			GPIO_70
PL_GPIO_69/A16	CLPOWER	0	EMI_WAIT	SPP_SELINn			GPIO_69
PL_GPIO_68/B15	FSMC_D0	FSMC_D0	EMI_D0/ FSMC_D0	FSMC_D0			GPIO_68
PL_GPIO_67/C14	FSMC_D1	FSMC_D1	EMI_D1/ FSMC_D0	FSMC_D1			GPIO_67
PL_GPIO_66/E13	FSMC_D2	FSMC_D2	EMI_D2/ FSMC_D2	FSMC_D2			GPIO_66
PL_GPIO_65/B14	FSMC_D3	FSMC_D3	EMI_D3/ FSMC_D3	FSMC_D3			GPIO_65
PL_GPIO_64/D13	FSMC_D4	FSMC_D4	EMI_D4/ FSMC_D4	FSMC_D4			GPIO_64
PL_GPIO_63/C13	FSMC_D5	FSMC_D5	EMI_D5/ FSMC_D5	FSMC_D5			GPIO_63
PL_GPIO_62/A15	FSMC_D6	FSMC_D6	EMI_D6/ FSMC_D6	FSMC_D6		H7	GPIO_62
PL_GPIO_61/E12	FSMC_D7	FSMC_D7	EMI_D7/ FSMC_D7	FSMC_D7		H6	GPIO_61
PL_GPIO_60/A14	FSMC_ADDR_LE	FSMC_ADDR_LE	FSMC_ADDR_LE	FSMC_ADDR_LE		H5	GPIO_60
PL_GPIO_59/B13	FSMC_WE	FSMC_WE	EMI_WE/ FSMC_WE	FSMC_WE		H4	GPIO_59
PL_GPIO_58/D12	FSMC_RE	FSMC_RE	EMI_OE/ FSMC_RE	FSMC_RE		H3	GPIO_58

Table 11. PL_GPIO multiplexing scheme (continued)

PL_GPIO_# / ball number	Configuration mode (enabled by Programmer model control register bits (2:0))				Alternate function (enabled by RAS select register)	Boot pins	Function in GPIO alternative mode
	1	2	3	4			
PL_GPIO_57/E11	FSMC_CMD_LE	FSMC_CMD_LE	FSMC_CMD_LE	FSMC_CMD_LE		H2	GPIO_57
PL_GPIO_56/C12	FSMC_RDY /BSY	FSMC_RDY/ BSY	FSMC_RDY/BSY	FSMC_RDY/ BSY		H1	GPIO_56
PL_GPIO_55/A13	FSMC_CS0	FSMC_CS0	EMI_CE0/ FSMC_CS0	FSMC_CS0		H0	GPIO_55
PL_GPIO_54/E10	FSMC_CS1	FSMC_CS1	EMI_CE1/ FSMC_CS1	FSMC_CS1		B3	GPIO_54
PL_GPIO_53/D11	FSMC_CS2	FSMC_CS2	EMI_CE2/ FSMC_CS2	FSMC_CS2		B2	GPIO_53
PL_GPIO_52/B12	FSMC_CS3	FSMC_CS3	EMI_CE_3/ FSMC_CS3	FSMC_CS3		B1	GPIO_52
PL_GPIO_51/D10	SD_CD	SD_CD	EMI_BYTEN0	SD_CD		B0	GPIO_51
PL_GPIO_50/A12	SD_DAT7	SD_DAT7	EMI_BYTEN1	SD_DAT7	TMR_CPTR4		GPIO_50
PL_GPIO_49/C11	SD_DAT6	SD_DAT6	EMI_D12/ FSMC_D12	SD_DAT6	TMR_CPTR3		GPIO_49
PL_GPIO_48/B11	SD_DAT5	SD_DAT5	EMI_D13/ FSMC_D13	SD_DAT5	TMR_CPTR2		GPIO_48
PL_GPIO_47/C10	SD_DAT4	SD_DAT4	EMI_D14/ FSMC_D14	SD_DAT4	TMR_CPTR1		GPIO_47
PL_GPIO_46/A11	SD_DAT3	SD_DAT3	EMI_D15/ FSMC_D15	SD_DAT3	TMR_CLK4		GPIO_46
PL_GPIO_45/B10	SD_DAT2	SD_DAT2	UART1_DCD	SD_DAT2	TMR_CLK3		GPIO_45
PL_GPIO_44/A10	SD_DAT1	SD_DAT1	UART1_DSR	SD_DAT1	TMR_CLK2		GPIO_44
PL_GPIO_43/E9	SD_DAT0	SD_DAT0	UART1_RTS	SD_DAT0	TMR_CLK1		GPIO_43
PL_GPIO_42/D9	Reserved	Reserved	0	0	UART0_DTR		GPIO_42
PL_GPIO_41/C9	Reserved	Reserved	0	0	UART0_RI		GPIO_41
PL_GPIO_40/B9	Reserved	Reserved	0	0	UART0_DSR		GPIO_40
PL_GPIO_39/A9	Reserved	Reserved	0	0	UART0_DCD		GPIO_39
PL_GPIO_38/A8	PWM0	PWM0	0	0	UART0_CTS		GPIO_38
PL_GPIO_37/B8	PWM1	PWM1	0	0	UART0_RTS		GPIO_37
PL_GPIO_36/C8	TOUCH SCREEN X	0	UART1_CTS	UART1_CTS	SSP0_CS4		GPIO_36
PL_GPIO_35/D8	Reserved	0	UART1_DTR	UART1_DTR	SSP0_CS3		GPIO_35
PL_GPIO_34/E8	SD_LED / PWM2	SD_LED / PWM2	UART1_RI	UART1_RI	SSP0_CS2		GPIO_34

Table 11. PL_GPIO multiplexing scheme (continued)

PL_GPIO_# / ball number	Configuration mode (enabled by Programmer model control register bits (2:0))				Alternate function (enabled by RAS select register)	Boot pins	Function in GPIO alternative mode
	1	2	3	4			
PL_GPIO_33/E7	CAN0_TX	CAN0_TX	CAN0_TX	UART1_DCD	basGPIO5		GPIO_33
PL_GPIO_32/D7	CAN0_RX	CAN0_RX	CAN0_RX	UART1_DSR	basGPIO4		GPIO_32
PL_GPIO_31/C7	CAN1_TX	CAN1_TX	CAN1_TX	UART1_RTS	basGPIO3		GPIO_31
PL_GPIO_30/B7	CAN1_RX	CAN1_RX	CAN1_RX		basGPIO2		GPIO_30
PL_GPIO_29/A7	UART1_TX	UART1_TX	UART1_TX	UART1_TX	basGPIO1		GPIO_29
PL_GPIO_28/A6	UART1_RX	UART1_RX	UART1_RX	UART1_RX	basGPIO0		GPIO_28
PL_GPIO_27/B6	SMII0_TX	0	SMII0_TX	SMII0_TX	MII0_TXCLK		GPIO_27
PL_GPIO_26/A5	SMII0_RX	0	SMII0_RX	SMII0_RX	MII0_TXD0		GPIO_26
PL_GPIO_25/C6	SMII1_TX	0	0	SMII1_TX	MII0_TXD1		GPIO_25
PL_GPIO_24/B5	SMII1_RX	0	0	SMII1_RX	MII0_TXD2		GPIO_24
PL_GPIO_23/A4	SMII_SYNC	0	SMII_SYNC	SMII_SYNC	MII0_TXD3		GPIO_23
PL_GPIO_22/D6	SMII_CLKOUT	0	SMII_CLKOUT	SMII_CLKOUT	MII0_TXEN		GPIO_22
PL_GPIO_21/C5	SMII_CLKIN	0	SMII_CLKIN	SMII_CLKIN	MII0_TXER		GPIO_21
PL_GPIO_20/B4	SSP1_MOSI	0	0	SSP1_MOSI	MII0_RXCLK		GPIO_20
PL_GPIO_19/A3	SSP1_CLK	0	0	SSP1_CLK	MII0_RXDV		GPIO_19
PL_GPIO_18/D5	SSP1_SS0	0	0	SSP1_SS0	MII0_RXER		GPIO_18
PL_GPIO_17/C4	SSP1_MISO	0	0	SSP1_MISO	MII0_RXD0		GPIO_17
PL_GPIO_16/E6	SSP2_MOSI	0	0	0	MII0_RXD1		GPIO_16
PL_GPIO_15/B3	SSP2_CLK	0	PWM0	PWM0	MII0_RXD2		GPIO_15
PL_GPIO_14/A2	SSP2_SS0	0	PWM1	PWM1	MII0_RXD3		GPIO_14
PL_GPIO_13/A1	SSP2_MISO	0	PWM2	PWM2	MII0_COL		GPIO_13
PL_GPIO_12/D4	PWM3	0	PWM3	PWM3	MII0_CRS		GPIO_12
PL_GPIO_11/E5	SMII_MDIO	0	SMII_MDIO	SMII_MDIO	MII0_MDC		GPIO_11
PL_GPIO_10/C3	SMII_MDC	0	SMII_MDC	SMII_MDC	MII0_MDIO		GPIO_10
PL_GPIO_9/B2	0	0	0	0	SSP0_MOSI		GPIO_9
PL_GPIO_8/C2	0	0	0	0	SSP0_CLK		GPIO_8
PL_GPIO_7/D3	0	0	0	0	SSP0_SS0		GPIO_7
PL_GPIO_6/B1	0	0	0	0	SSP0_MISO		GPIO_6
PL_GPIO_5/D2	0	0	0	0	I2C0_SDA		GPIO_5
PL_GPIO_4/C1	0	0	0	0	I2C0_SCL		GPIO_4
PL_GPIO_3/D1	0	0	0	0	UART0_RX		GPIO_3
PL_GPIO_2/E4	0	0	0	0	UART0_TX		GPIO_2

Table 11. PL_GPIO multiplexing scheme (continued)

PL_GPIO_# / ball number	Configuration mode (enabled by Programmer model control register bits (2:0))				Alternate function (enabled by RAS select register)	Boot pins	Function in GPIO alternative mode
	1	2	3	4			
PL_GPIO_1/E3	UART2_TX	UART2_TX	UART2_TX	UART2_TX	IrDA_RX		GPIO_1
PL_GPIO_0/F3	UART2_RX	UART2_RX	UART2_RX	UART2_RX	IrDA_TX		GPIO_0
PL_CLK1/K17	CLCP	0	I2C1_SDA	SD_LED	PL_CLK1		GPIO_98
PL_CLK2/J17	SD_CLK	SD_CLK	I2C1_SCL	SD_CLK	PL_CLK2		GPIO_99
PL_CLK3/J16	SD_WP	SD_WP	0	SD_WP	PL_CLK3		GPIO_100
PL_CLK4/H17	SD_CMD	SD_CMD	0	SD_CMD	PL_CLK4		GPIO_101

Note: 1 Table 11 cells filled with '0' or '1' are unused and unless otherwise configured as Alternate function or GPIO, the corresponding pin is held at low or high level respectively by the internal logic.

2 Pins shared by EMI and FSMC: Depending on the AHB address to be accessed the pins are used for EMI or FSMC transfers.

Table 12. Table shading

Shading	Pin group
FSMC	FSMC pins: NAND Flash
EMI	EMI pins
CLCD	Color LCD controller pins
Touchscreen	Touchscreen pins
UART	UART pins
CAN	CAN pins
Ethernet MAC	MII/SMII Ethernet Mac pins
SDIO/MMC	SD card controller pins
PWM timers	Pulse-width modulator timer module pins
GPT	Timer pins
IrDa	IrDa pins
SSP	SSP pins
I2C	I2C pins
Standard Parallel port	Standard parallel port pins

4.4 PL_GPIO pin sharing for debug modes

In some cases the PL_GPIO pins may be used in different ways for debugging purposes. There are three different cases (see also *Table 13*):

1. Case 1 - All the PL_GPIO get values from Boundary scan registers during Ex-test instruction of JTAG . Typically this configuration is used to verify correctness of the soldering process during the production flow .
2. Case 2 - All the PL_GPIO maintain their original meaning but the JTAG Interface is connected to the processor. This configuration is useful during the development phase but offers only "static" debug.
3. Case 3 - Some PL_GPIO, as shown in *Table 13: Ball sharing during debug*, are used to connect the ETM9 lines to an external box. This configuration is typically used only during the development phase. It offers a very powerful debug capability. When the processor reaches a breakpoint it is possible, by analyzing the trace buffer, to understand the reason why the processor has reached the break.

Table 13. Ball sharing during debug

Signals	Case 1 - no debug	Case 2 - static debug	Case 3 - full debug
Test[0]	0	1	0
Test[1]	0	0	1
Test[2]	0	0/1	0/1
Test[3]	0	0/1	0/1
Test[4]	1	0/1	0/1
nTRST	nTRST_bscan	nTRST_ARM	nTRST_ARM
TCK	TCK_bscan	TCK_ARM	TCK_ARM
TMS	TSM_bscan	TMS_ARM	TSM_ARM
TDI	TDI_bscan	TDI_ARM	TDI_ARM
TDO	TDO_bscan	TDO_ARM	TDO_ARM
PL_GPIO[97]	BSR Value	Original meaning	ARM_TRACE_CLK
PL_GPIO[96]	BSR Value	Original meaning	ARM_TRACE_PKTA[0]
PL_GPIO[95]	BSR Value	Original meaning	ARM_TRACE_PKTA[1]
PL_GPIO[94]	BSR Value	Original meaning	ARM_TRACE_PKTA[2]
PL_GPIO[93]	BSR Value	Original meaning	ARM_TRACE_PKTA[3]
PL_GPIO[92]	BSR Value	Original meaning	ARM_TRACE_PKTB[0]
PL_GPIO[91]	BSR Value	Original meaning	ARM_TRACE_PKTB[1]
PL_GPIO[90]	BSR Value	Original meaning	ARM_TRACE_PKTB[2]
PL_GPIO[89]	BSR Value	Original meaning	ARM_TRACE_PKTB[3]
PL_GPIO[88]	BSR Value	Original meaning	ARM_TRACE_SYNCA
PL_GPIO[87]	BSR Value	Original meaning	ARM_TRACE_SYNCB
PL_GPIO[86]	BSR Value	Original meaning	ARM_PIPESTATA[0]
PL_GPIO[85]	BSR Value	Original meaning	ARM_PIPESTATA[1]

Table 13. Ball sharing during debug (continued)

Signals	Case 1 - no debug	Case 2 - static debug	Case 3 - full debug
PL_GPIO[84]	BSR Value	Original meaning	ARM_PIPESTATA[2]
PL_GPIO[83]	BSR Value	Original meaning	ARM_PIPESTATB[0]
PL_GPIO[82]	BSR Value	Original meaning	ARM_PIPESTATB[1]
PL_GPIO[81]	BSR Value	Original meaning	ARM_PIPESTATB[2]
PL_GPIO[80]	BSR Value	Original meaning	ARM_TRACE_PKTA[4]
PL_GPIO[79]	BSR Value	Original meaning	ARM_TRACE_PKTA[5]
PL_GPIO[78]	BSR Value	Original meaning	ARM_TRACE_PKTA[6]
PL_GPIO[77]	BSR Value	Original meaning	ARM_TRACE_PKTA[7]
PL_GPIO[76]	BSR Value	Original meaning	ARM_TRACE_PKTB[4]
PL_GPIO[75]	BSR Value	Original meaning	ARM_TRACE_PKTB[5]
PL_GPIO[74]	BSR Value	Original meaning	ARM_TRACE_PKTB[6]
PL_GPIO[73]	BSR Value	Original meaning	ARM_TRACE_PKTB[7]
PL_GPIO[72:0]			

5 Memory map

Table 14. SPEAr320 main memory map

Start address	End address	Peripheral	Description
0x0000.0000	0x3FFF.FFFF	External DRAM	Low power DDR or DDR2
0x4000.0000	0xBFFF.FFFF	-	Reconfigurable array subsystem (See *Table 15*)
0xC000.0000	0xCFFF.FFFF	-	Reserved
0xD000.0000	0xD007.FFFF	UART0	
0xD008.0000	0xD00F.FFFF	ADC	
0xD010.0000	0xD017.FFFF	SSP0	
0xD018.0000	0xD01F.FFFF	I2C0	
0xD020.0000	0xD07F.FFFF	-	Reserved
0xD080.0000	0xD0FF.FFFF	JPEG CODEC	
0xD100.0000	0xD17F.FFFF	IrDA	
0xD180.0000	0xD1FF.FFFF	-	Reserved
0xD280.0000	0xD7FF.FFFF	SRAM	Static RAM shared memory (8 Kbytes)
0xD800.0000	0xE07F.FFFF	-	Reserved
0xE080.0000	0xE0FF.FFFF	Ethernet controller	MAC
0xE100.0000	0xE10F.FFFF	USB 2.0 device	FIFO
0xE110.0000	0xE11F.FFFF	USB 2.0 device	Configuration registers
0xE120.0000	0xE12F.FFFF	USB 2.0 device	Plug detect
0xE130.0000	0xE17F.FFFF	-	Reserved
0xE180.0000	0xE18F.FFFF	USB2.0 EHCI 0-1	
0xE190.0000	0xE19F.FFFF	USB2.0 OHCI 0	
0xE1A0.0000	0xE20F.FFFF	-	Reserved
0xE210.0000	0xE21F.FFFF	USB2.0 OHCI 1	
0xE220.0000	0xE27F.FFFF	-	Reserved
0xE280.0000	0xE28F.FFFF	ML USB ARB	Configuration register
0xE290.0000	0xE7FF.FFFF	-	Reserved
0xE800.0000	0xEFFF.FFFF	-	Reserved
0xF000.0000	0xF00F.FFFF	Timer0	
0xF010.0000	0xF10F.FFFF	-	Reserved
0xF110.0000	0xF11F.FFFF	ITC Primary	
0xF120.0000	0xF7FF.FFFF	-	Reserved
0xF800.0000	0xFBFF.FFFF	Serial Flash memory	

Table 14. SPEAr320 main memory map (continued)

Start address	End address	Peripheral	Description
0xFC00.0000	0xFC1F.FFFF	Serial Flash controller	
0xFC20.0000	0xFC3F.FFFF	-	Reserved
0xFC40.0000	0xFC5F.FFFF	DMA controller	
0xFC60.0000	0xFC7F.FFFF	DRAM controller	
0xFC80.0000	0xFC87.FFFF	Timer 1	
0xFC88.0000	0xFC8F.FFFF	Watchdog timer	
0xFC90.0000	0xFC97.FFFF	Real time clock	
0xFC98.0000	0xFC9F.FFFF	basGPIO	
0xFCA0.0000	0xFCA7.FFFF	System controller	
0xFCA8.0000	0xFCAF.FFFF	Miscellaneous registers	
0xFCB0.0000	0xFCB7.FFFF	Timer 2	
0xFCB8.0000	0xFCFF.FFFF	-	Reserved
0xFD00.0000	0xFEFF.FFFF	-	Reserved
0xFF00.0000	0xFFFF.FFFF	BootROM	

Table 15. Reconfigurable array subsystem memory map

Start address	End address	Peripheral	Description
0x4000_0000	0x47FF_FFFF	EMI	
0x4800_0000	0x4BFF_FFFF	-	Reserved
0x4C00_0000	0x5FFF_FFFF	FSMC	
0x6000_0000	0x6FFF_FFFF	-	Reserved
0x7000_0000	0x7FFF_FFFF	SDIO	
0x8000_0000	0x8000_3FFF	Boot memory	
0x8000_4000	0x8FFF_FFFF	-	Reserved
0x9000_0000	0x9FFF_FFFF	CLCD	
0xA000_0000	0xA0FF_FFFF	Parallel port	
0xA100_0000	0xA1FF_FFFF	CAN0	
0xA200_0000	0xA2FF_FFFF	CAN1	
0xA300_0000	0xA3FF_FFFF	UART1	
0xA400_0000	0xA4FF_FFFF	UART2	
0xA500_0000	0xA5FF_FFFF	SSP1	
0xA600_0000	0xA6FF_FFFF	SSP2	
0xA700_0000	0xA7FF_FFFF	I2C1	
0xA800_0000	0xA8FF_FFFF	Quad PWM timer	
0xA900_0000	0xA9CF_FFFF	GPIO	

Table 15. Reconfigurable array subsystem memory map (continued)

Start address	End address	Peripheral	Description
0xA9D0_0000	0xA9FF_FFFF	-	Reserved
0xAA00_0000	0xAAFF_FFFF	SMII0	
0xAB00_0000	0xABFF_FFFF	SMII1/MII	
0xAC00_0000	0xB2FF_FFFF	-	Reserved
0xB300_0000	0xBFFF_FFFF	AHB interface	

6 Electrical characteristics

6.1 Absolute maximum ratings

This product contains devices to protect the inputs against damage due to high/low static voltages. However it is advisable to take normal precaution to avoid application of any voltage higher/lower than the specified maximum/minimum rated voltages.

The absolute maximum rating is the maximum stress that can be applied to a device without causing permanent damage. However, extended exposure to minimum/maximum ratings may affect long-term device reliability.

Table 16. Absolute maximum ratings

Symbol	Parameter	Minimum value	Maximum value	Unit
V_{DD} 1.2	Supply voltage for the core	- 0.3	1.44	V
V_{DD} 3.3	Supply voltage for the I/Os	- 0.3	3.9	V
V_{DD} 2.5	Supply voltage for the analog blocks	- 0.3	3	V
V_{DD} 1.8	Supply voltage for the DRAM interface	- 0.3	2.16	V
V_{DD} RTC	RTC supply voltage	-0.3	2.16	V
T_{STG}	Storage temperature	-55	150	°C
T_J	Junction temperature	-40	125	°C

6.2 Maximum power consumption

Note: These values take into consideration the worst cases of process variation and voltage range and must be used to design the power supply section of the board.

Table 17. Maximum power consumption

Symbol	Description	Max	Unit
$I_{DD(1.2Vsupply)}$	Current consumption of V_{DD} 1.2 supply voltage for the core	400	mA
$I_{DD(1.8Vsupply)}$	Current consumption of V_{DD} 1.8 supply voltage for the DRAM interface (1)	150	mA
$I_{DD(RTC)}$	Current consumption of RTC supply voltage	8	µA
$I_{DD(2.5Vsupply)}$	Current consumption of 2.5V supply voltage for the analog blocks	30	mA
$I_{DD(3.3Vsupply)}$	Current consumption of 3.3V supply voltage for the I/Os (2)	12	mA
P_D	Maximum power consumption(3)	930	mW

1. Peak current with Linux memory test (50% write and 50% read) plus DMA reading memory.
2. With 30 logic channels connected to the device and simultaneously switching at 10 MHz.

3. Based on bench measurements for worst case silicon under worst case operating conditions. Devices tested with operating system running, CPU and DDR2 running at 333 MHz, DDR2 driven by PLL2, SDRAM and all on-chip peripherals and internal modules enabled.

   1.2 V current and power are primarily dependent on the applications running and the use of internal chip functions (DMA, USB, Ethernet, and so on).

   3.3 V current and power are primarily dependent on the capacitive loading, frequency, and utilization of the external buses.

6.3 DC electrical characteristics

The recommended operating conditions are listed in the following table:

Table 18. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD} 1.2	Supply voltage for the core	1.14	1.2	1.3	V
V_{DD} 3.3	Supply voltage for the I/Os	3	3.3	3.6	V
V_{DD} 2.5	PLL supply voltage(1)	2.25	2.5	2.75	V
V_{DD} 2.5	Oscillator supply voltage	2.25	2.5	2.75	V
V_{DD} 1.8	Supply voltage for DRAM interface	1.70	1.8	1.9	V
V_{DD} RTC	RTC supply voltage	1.3	1.5	1.8	V
T_O	Operating temperature	-40		85	°C

1. For power supply filtering it is required to add an external ferrite inductor.

6.4 Overshoot and undershoot

This product can support the following values of overshoot and undershoot.

Table 19. Overshoot and undershoot specifications

Parameter	3V3 I/Os	2V5 I/Os	1V8 I/Os
Amplitude	500 mV	500 mV	500 mV
Ratio of overshoot (or undershoot) duration with respect to pulse width	1/3	1/3	1/3

If the amplitude of the overshoot/undershoot increases (decreases), the ratio of overshoot/undershoot width to the pulse width decreases (increases). The formula relating the two is:

Amplitude of OS/US = 0.75*(1- ratio of OS (or US) duration with respect to pulse width)

Note: The value of overshoot/undershoot should not exceed the value of 0.5 V. However, the duration of the overshoot/undershoot can be increased by decreasing its amplitude.

6.5 3.3V I/O characteristics

The 3.3 V I/Os are compliant with JEDEC standard JESD8b.

Table 20. Low voltage TTL DC input specification (3 V< V_{DD} <3.6 V)

Symbol	Parameter	Min	Max	Unit
V_{IL}	Low level input voltage		0.8	V
V_{IH}	High level input voltage	2		V
V_{hyst}	Schmitt trigger hysteresis	300	800	mV

Table 21. Low voltage TTL DC output specification (3 V< V_{DD} <3.6 V)

Symbol	Parameter	Test condition	Min	Max	Unit
V_{OL}	Low level output voltage	I_{OL}= X mA (1)		0.3	V
V_{OH}	High level output voltage	I_{OH}= -X mA (1)	V_{DD} - 0.3		V

1. Maximum current load (IOL) = 10 mA for PL_GPIO and PL_CLK pins. For the IOL max value of dedicated pins, refer to *Chapter 4: Pin description*.

Table 22. Pull-up and pull-down characteristics

Symbol	Parameter	Test condition	Min	Max	Unit
R_{PU}	Equivalent pull-up resistance	V_I = 0 V	29	67	kΩ
R_{PD}	Equivalent pull-down resistance	V_I = V_{DDE}3V3	29	103	kΩ

6.6 LPDDR and DDR2 pin characteristics

Table 23. DC characteristics

Symbol	Parameter	Test condition	Min	Max	Unit
V_{IL}	Low level input voltage	SSTL18	-0.3	V_{REF}-0.125	V
V_{IH}	High level input voltage	SSTL18	V_{REF}+0.125	V_{DDE}1V8+0.3	V
V_{hyst}	Input voltage hysteresis		200		mV

Table 24. Driver characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R_O	Output impedance		45		Ω

Table 25. On die termination

Symbol	Parameter	Min	Typ	Max	Unit
RT1	Termination value of resistance for on die termination		75		Ω
RT2	Termination value of resistance for on die termination		150		Ω

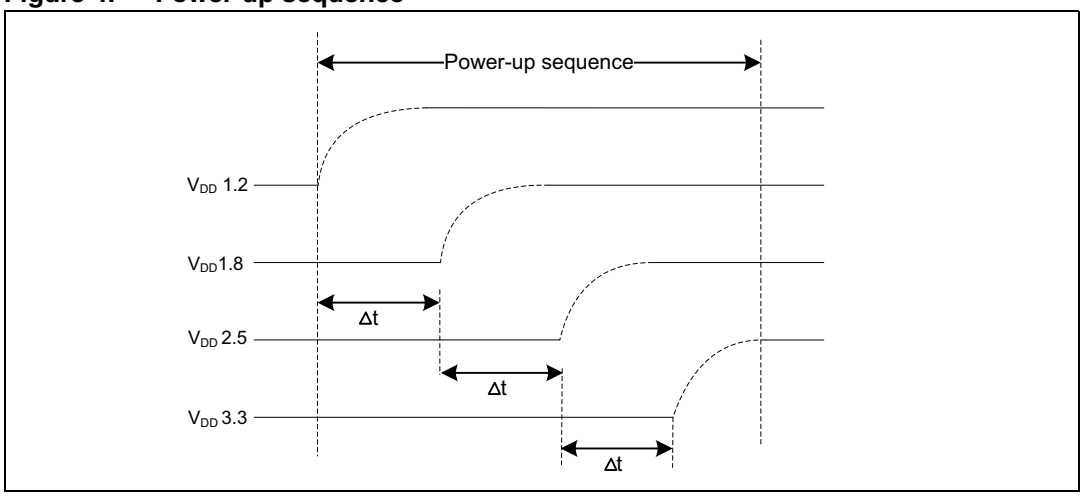
Table 26. Reference voltage

Symbol	Parameter	Min	Typ	Max	Unit
V_{REFIN}	Voltage applied to core/pad	0.49 * V_{DDE}	0.500 * V_{DDE}	0.51 * V_{DDE}	V

6.7 Power up sequence

It is recommended to power up the power supplies in the order shown in *Figure 4*. V_{DD} 1.2 is brought up first, followed by V_{DD} 1.8, then V_{DD} 2.5 and finally V_{DD} 3.3. The minimum time (Δt) between each power up is >0 µs.

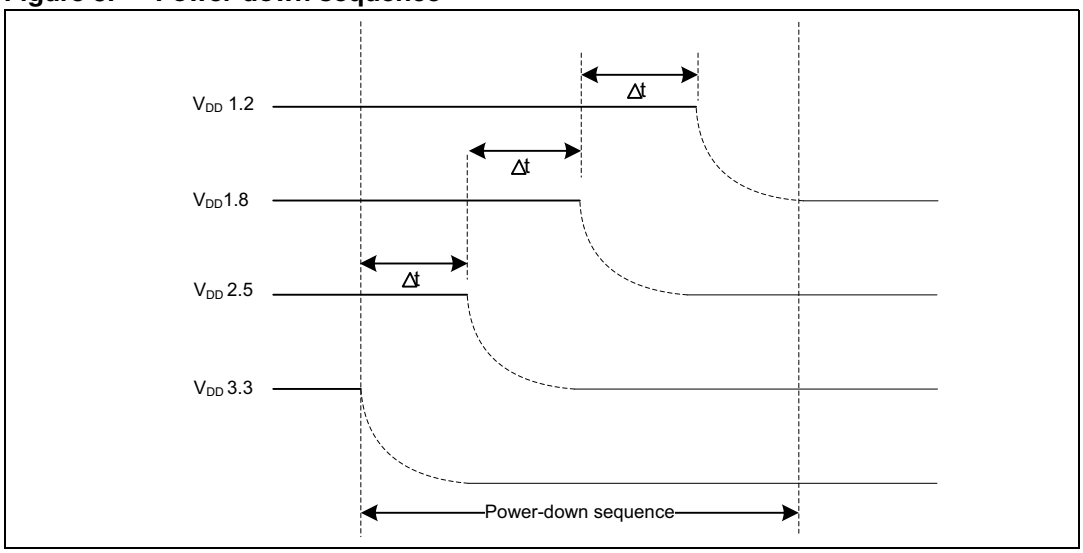
Figure 4. Power-up sequence



6.8 Removing power supplies for power saving

It is recommended to remove the the power supplies in the order shown in *Figure 5*. So V_{DD} 3.3 supply is to be removed first, then the V_{DD} 2.5 supply, followed by the V_{DD} 1.8 supply and last the V_{DD} 1.2. The minimum time (Δt) between each power down is >0 µs.

Figure 5. Power-down sequence



6.9 Power on reset (MRESET)

The MRESET must remain active for at least 10 ms after all the power supplies are in the correct range and should become active in no more than 10 µs when one of the power supplies goes out of the correct range.

7 Timing requirements

*Note: Signal transition levels used for timing measurements are 0.2*VDD and 0.8*VDD.*

7.1 External interrupt timing characteristics

Table 27. PL_GPIO external interrupt input timing

Symbol	Description	Min	Unit
tINT	Minimum width for rising edge interrupt pulse	24	ns

7.2 Reset timing characteristics

Table 28. Cold (power-on) reset

Symbol	Description	Min	Unit
tRP	MRESET pin active low state duration	10	ms

Note: Warm reset is generated by writing any value to the System controller SYSSTAT register.

7.3 DDR2 timing characteristics

The characterization timing is done considering an output load of 10 pF on all the DDR pads.

The timing parameters listed are defined by JEDEC for DDR memories. DDR memories whose parameters are within the ranges defined in *Table 29*, *Table 30* and *Table 31* can be interfaced with SPEAr320.

Read cycle timing apply to DQS and DQ input to SPEAr. Write cycle timings refer to DQS and DQ output to SPEAr.

7.3.1 DDR2 read cycle timings

Figure 6. DDR2 read cycle waveforms

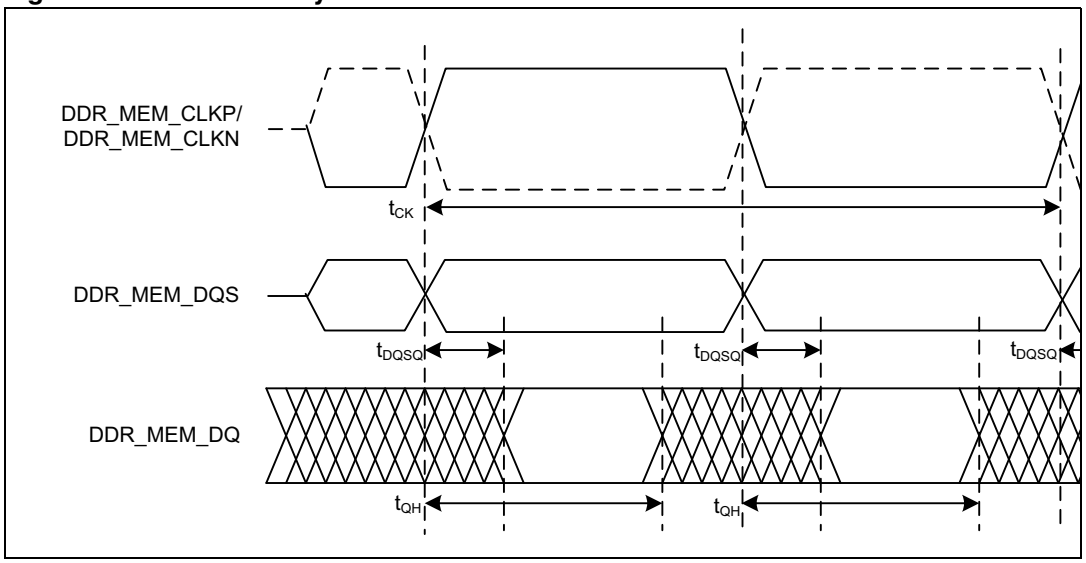


Table 29. DDR2 read cycle timings

Symbol	Description	Min	Max	Unit
t_{CK}	DDR_MEM_CLKP/CLKN cycle time	3		ns
t_{DQSQ}	DQS to DQ input setup time	0	$0.25t_{CK}+0.4$	ns
t_{QH}	DQS to DQ input hold time	$0.25t_{CK}+0.7$	$0.5t_{CK}$	ns

7.3.2 DDR2 write cycle timings

Figure 7. DDR2 write cycle waveforms

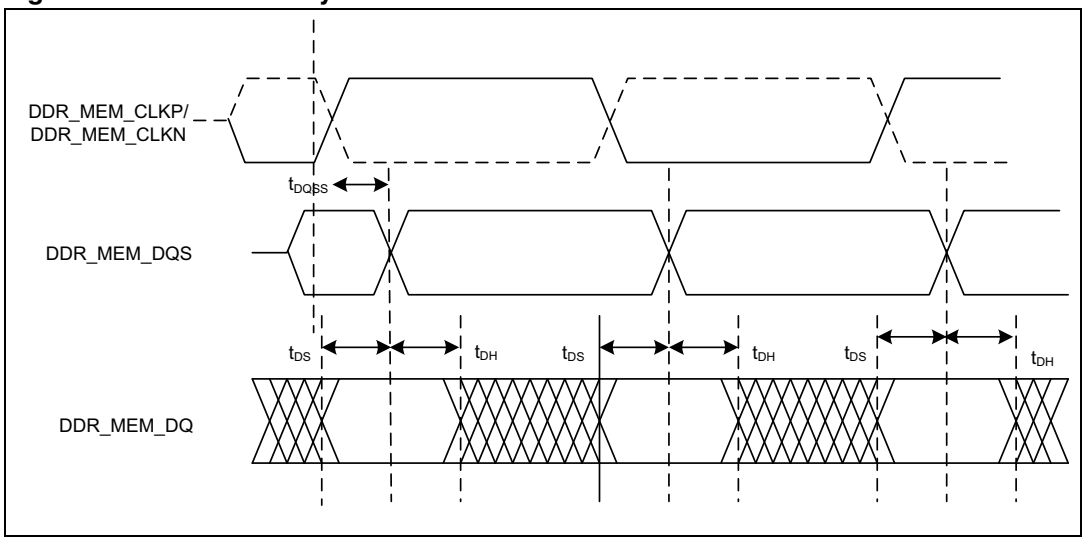


Table 30. DDR2 write cycle timings

Symbol	Description	Min	Max	Unit
t_{DQSS}	Positive DQS latching edge to associated CK edge	-0.5	0.5	ns
t_{DS}	DQ & DQM output setup time relative to DQS	0	$0.25t_{CK} – 0.76$	ns
t_{DH}	DQ & DQM output hold time relative to DQS	0	$0.25t_{CK} – 0.84$	ns

7.3.3 DDR2 command timings

Figure 8. DDR2 command waveforms

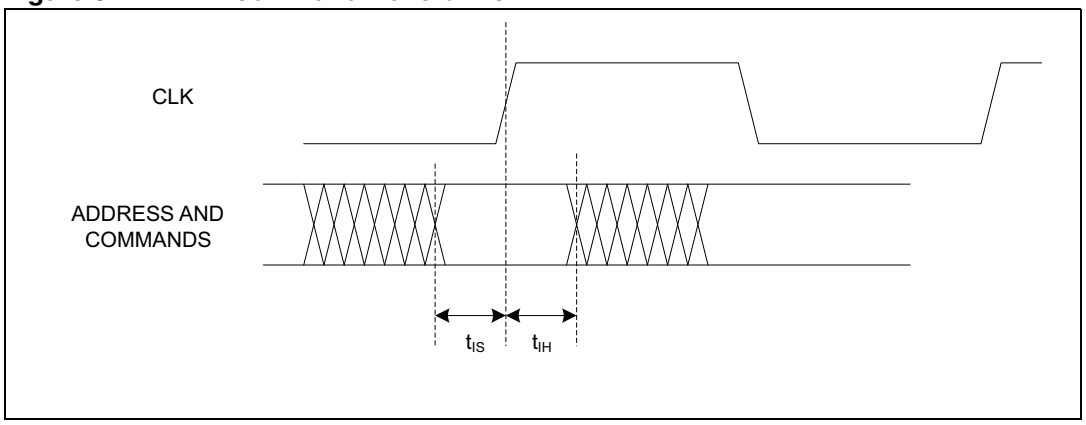


Table 31. DDR2 command timings

Symbol	Description	Min	Max	Unit
t_{IS}	Address and control output setup time	0	$0.5t_{CK} – 0.5$	ns
t_{IH}	Address and control output hold time	0	$0.5t_{CK} – 0.59$	ns

7.4 CLCD timing characteristics

The characterization timing is done considering an output load of 10 pF on all the outputs.

The CLCD has a wide variety of configurations and setting and the parameters change accordingly. *Figure 9* and *Table 32* specify the clock to output delay.

Figure 9. CLCD waveform

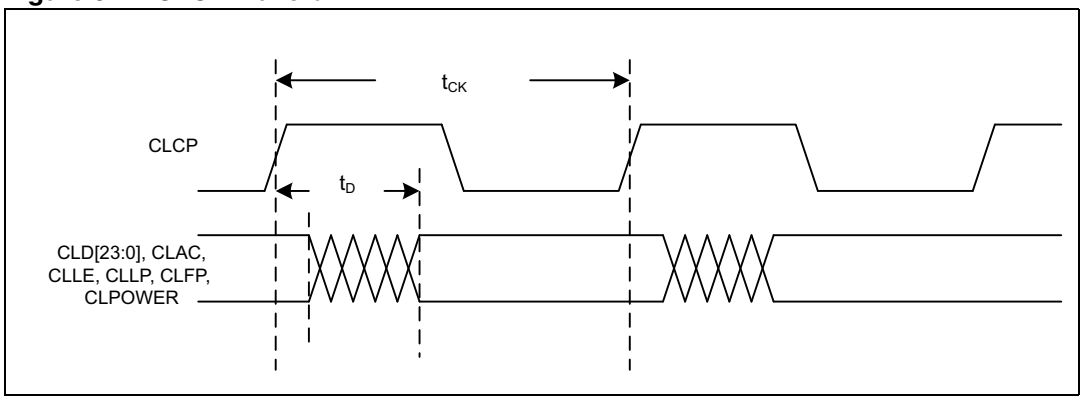


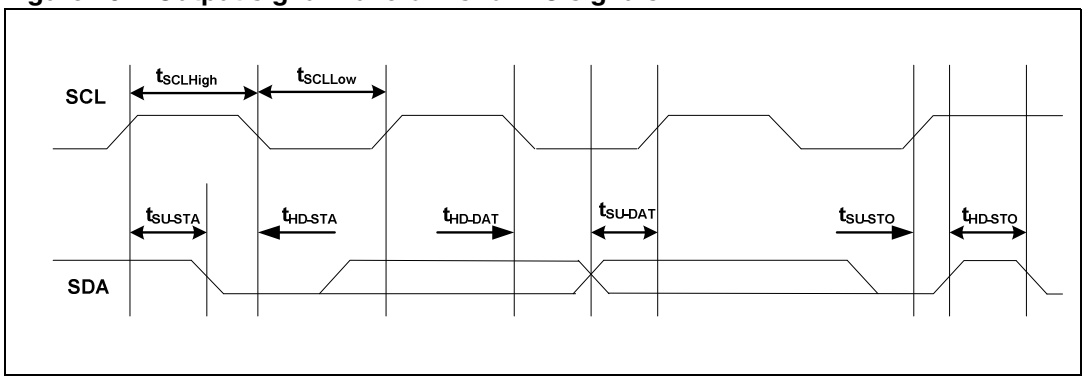
Table 32. CLCD timings

Symbol	Description	Min	Max	Unit
t_{CK}	CLCP clock period	20.83	41.66	ns
t_D	CLCP to CLCD output data delay	0.97	3.74	ns

7.5 I²C timing characteristics

The characterization timing is done using primetime considering an output load of 10 pF on SCL and SDA.

Figure 10. Output signal waveforms for I²C signals



The timings of the high and low level of SCL ($t_{SCLHigh}$ and t_{SCLLow}) are programmable.

Table 33. Timing characteristics for I²C in high-speed mode

Parameter	Min	Unit
t_{SU-STA}	157.6	ns
t_{HD-STA}	325.9	
t_{SU-DAT}	314.0	
t_{HD-DAT}	0.8	
t_{SU-STO}	637.7	
t_{HD-STO}	4742.2	

Table 34. Timing characteristics for I²C in fast speed mode

Parameter	Min	Unit
t_{SU-STA}	637.6	ns
t_{HD-STA}	602.2	
t_{SU-DAT}	1286.1	
t_{HD-DAT}	0.8	
t_{SU-STO}	637.7	
t_{HD-STO}	4742.2	

Table 35. Timing characteristics for I²C in standard speed mode

Parameter	Min	Unit
t_{SU-STA}	4723.6	ns
t_{HD-STA}	3991.9	
t_{SU-DAT}	4676.1	
t_{HD-DAT}	0.8	
t_{SU-STO}	4027.7	
t_{HD-STO}	4742.2	

Note: The timings shown in Figure 10 depend on the programmed value of $t_{SCLHigh}$ and t_{SCLLow}, so the values present in the three tables here above have been calculated using the minimum programmable values of :

- *IC_HS_SCL_HCNT=19 and IC_HS_SCL_LCNT=53 registers (for High-Speed mode);*
- *IC_FS_SCL_HCNT=99 and IC_FS_SCL_LCNT=215 registers (for Fast-Speed mode);*
- *IC_SS_SCL_HCNT=664 and IC_SS_SCL_LCNT=780 registers (for Standard-Speed mode).*

These minimum values depend on the AHB clock frequency, which is 166 MHz.

7.6 FSMC timing characteristics

The characterization timing is done using primetime considering an output load of 3 pF on the data, 15 pF on FSMC_CSx, FSMC_RE and FSMC_WE and 10 pF on FSMC_ADDR_LE and FSMC_CMD_LE.

7.6.1 NAND Flash configuration

Figure 11. Output command signal waveforms for NAND Flash

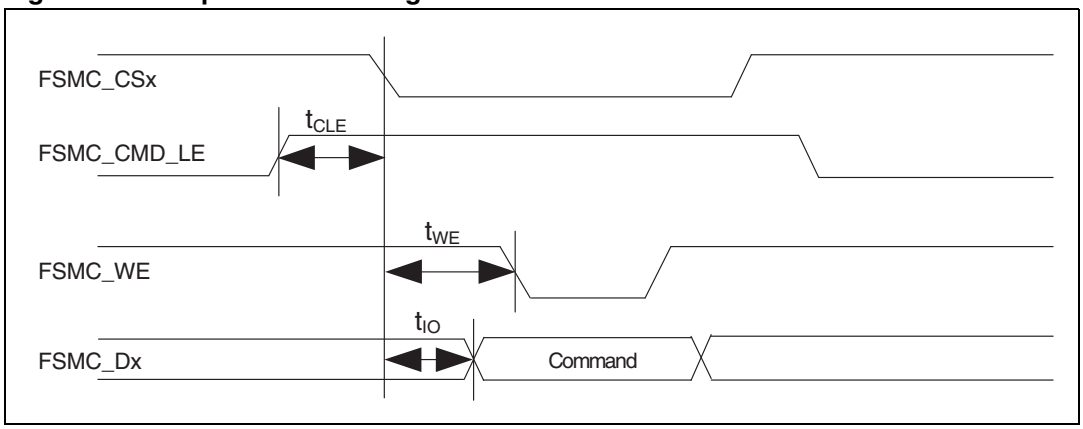


Figure 12. Output address signal waveforms for NAND Flash

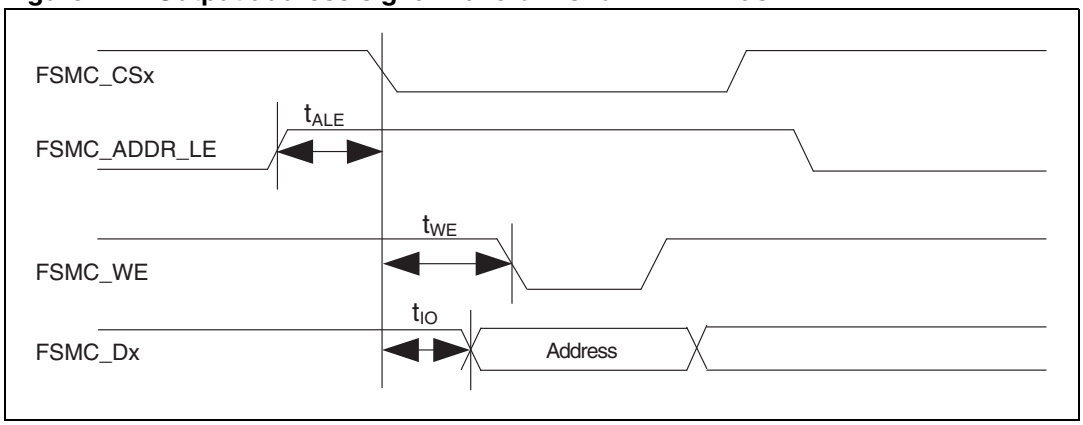


Figure 13. In/out data address signal waveforms for NAND Flash

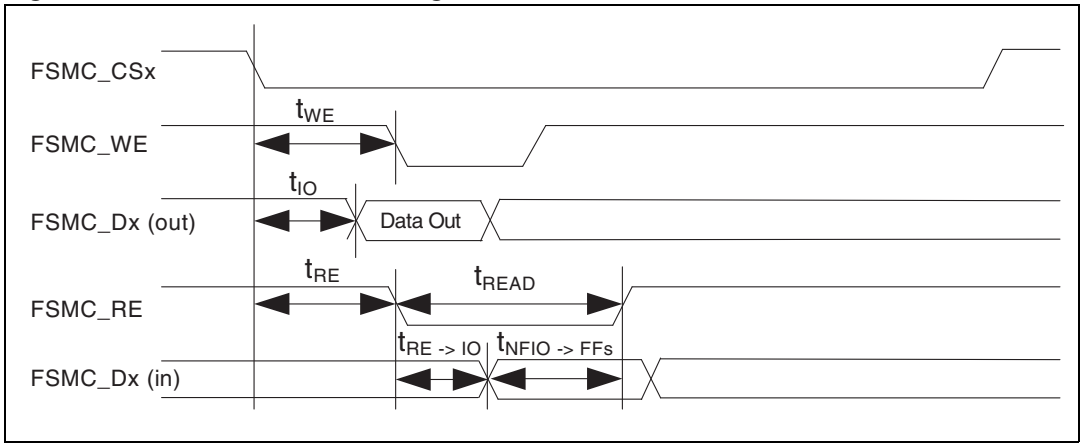


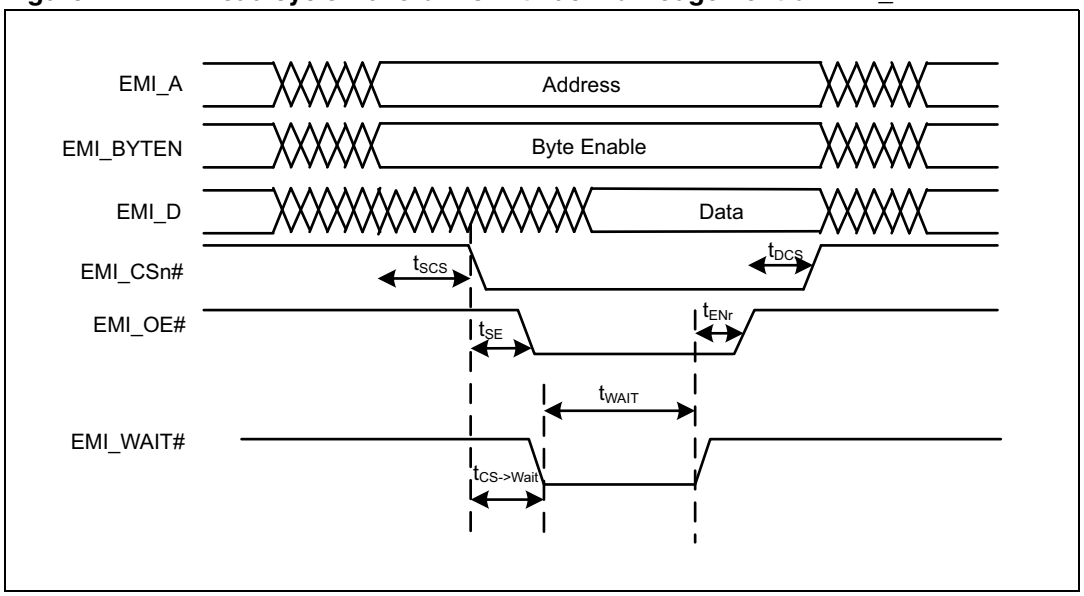
Table 36. Timing characteristics for NAND Flash

Parameter	Min	Max
t_{CLE}	-3.9	2.8
t_{ALE}	-4.2	2.6
t_{WE} (programmable by the Tset bits in the FSMC registers)	(((Tset+1) * t_{HCLK}) - 3 ns)	(((Tset+1) * t_{HCLK}) + 3 ns)
t_{RE} (programmable by the Tset bits in the FSMC registers)	(((Tset+1) * t_{HCLK}) - 3 ns)	(((Tset+1) * t_{HCLK}) + 3 ns)
t_{IO} (programmable by the Thiz bits in the FSMC registers)	(((Thiz +1) * t_{HCLK}) - 3 ns)	(((Thiz +1) * t_{HCLK})+ 3 ns)
t_{READ} (programmable by the Twait bits in the FSMC registers)	((Twait+1)* t_{HCLK}	

Note: Values in Table 36 are referred to the common internal source clock which has a period of t_{HCLK} = 6 ns.

7.7 EMI timing characteristics

Figure 14. EMI read cycle waveforms with acknowledgement on EMI_WAIT#



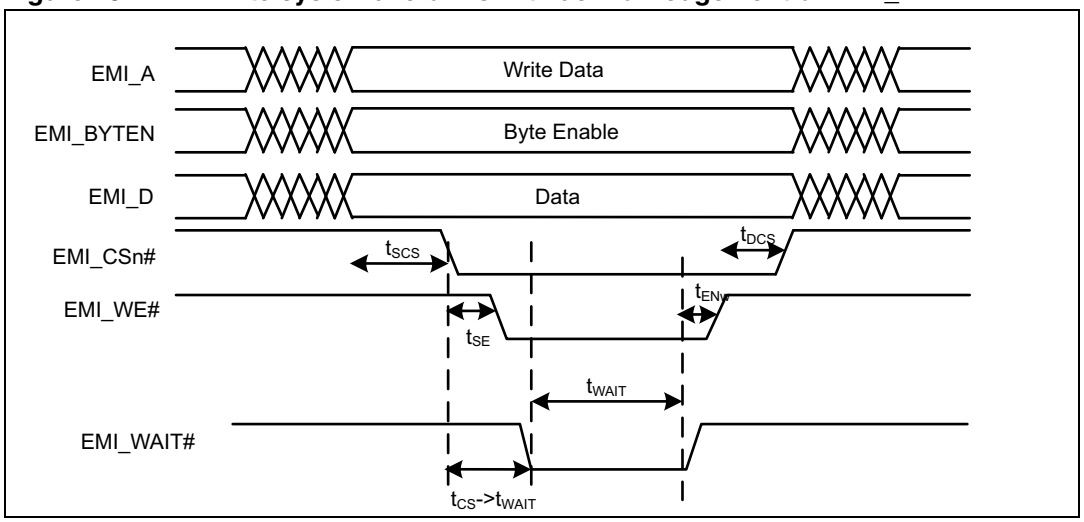
Note: The values of t_{SE}, t_{ENr}, t_{DCS}, t_{SCS} are programmable via the EMI registers.

Table 37. EMI timings for read cycle with acknowledgement on WAIT#

Symbol	Min
$t_{CS->Wait}$	t_{HCLK}
t_{WAIT}	$4*t_{HCLK}$

Note: Values in the above table are referred to the common internal source clock which has a period of t_{HCLK} = 6 ns.

Figure 15. EMI write cycle waveforms with acknowledgement on EMI_WAIT#



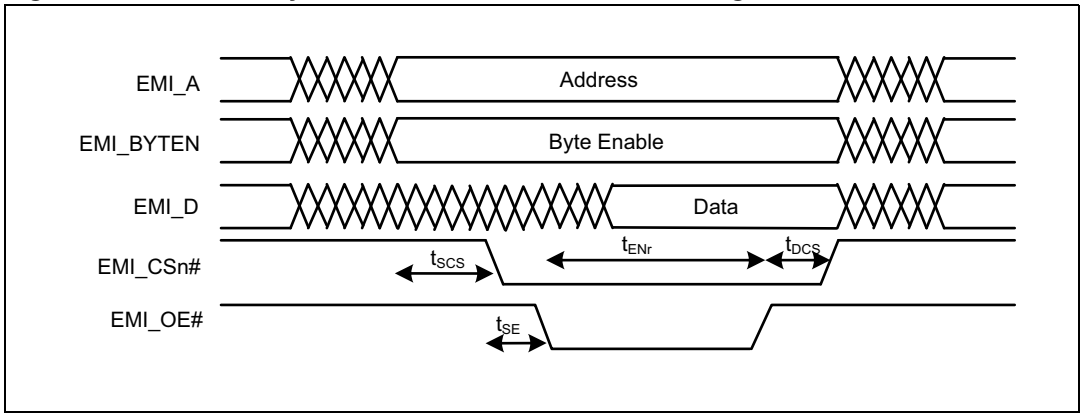
Note: The values of t_{SE}, t_{ENw}, t_{DCS}, t_{SCS} are programmable via the EMI registers.

Table 38. EMI timings for write cycle with acknowledgement on WAIT#

Symbol	Min
$t_{CS->Wait}$	t_{HCLK}
t_{WAIT}	$4*t_{HCLK}$

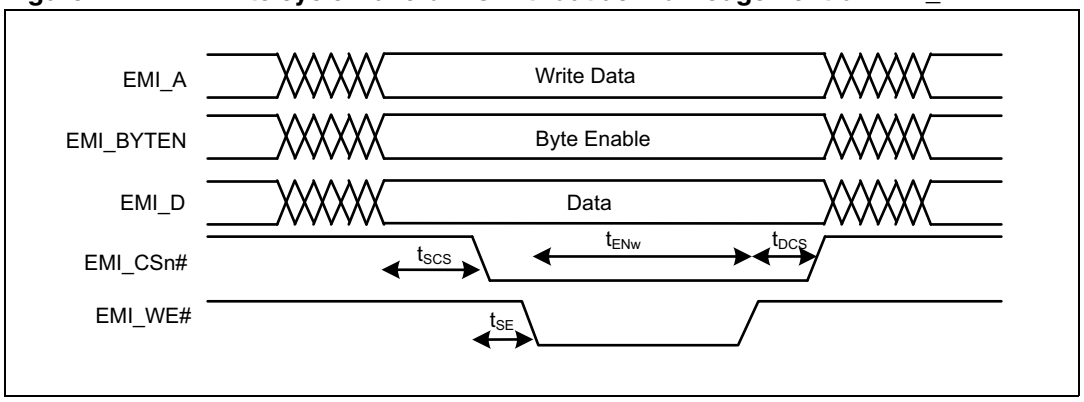
Note: Values in the above table are referred to the common internal source clock which has a period of t_{HCLK} = 6 ns.

Figure 16. EMI read cycle waveforms without acknowledgement on EMI_WAIT#



Note: The values of t_{SE}, t_{ENr}, t_{DCS}, t_{SCS} are programmable via the EMI registers.

Figure 17. EMI write cycle waveforms without acknowledgement on EMI_WAIT#



Note: The values of t_{SE}, t_{ENw}, t_{DCS}, t_{SCS} are programmable via the EMI registers.

7.8 SDIO timing characteristics

Figure 18. SDIO timing diagram

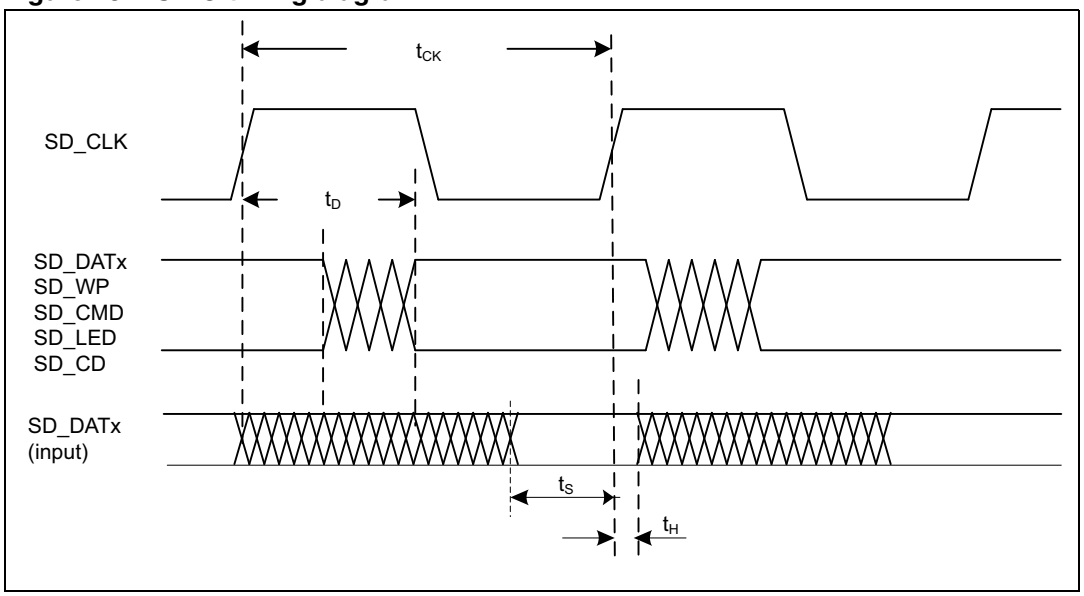


Table 39. SDIO timings

Symbol	Description	Min	Max	Unit
t_{CK}	SD_CLK clock period	20.8	41.6	ns
t_D	SD_CLK to SD output delay	6.14	7.79	
t_S	Setup time requirement for SD inputs	9.65		
t_H	Hold time requirement for SD inputs	-1.9		

7.9 MII Ethernet MAC 10/100 Mbps timing characteristics

The characterization timing is given for an output load of 5 pF on the MII TX clock and 10 pF on the other pads.

7.9.1 MII transmit timing specifications

Figure 19. MII TX waveforms

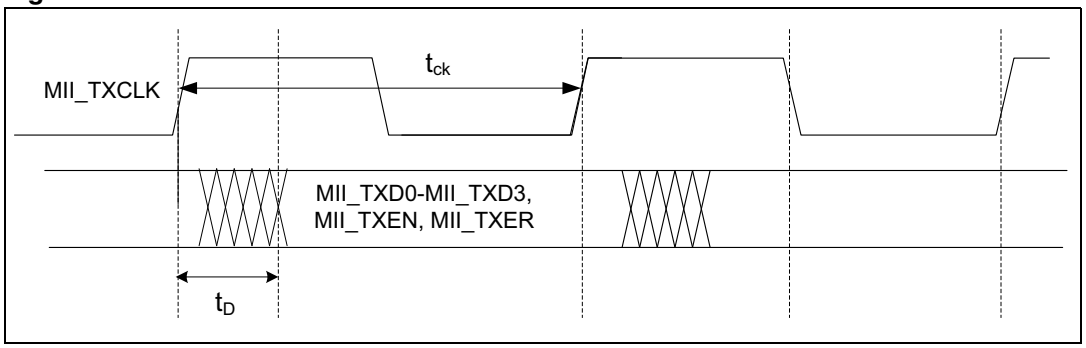


Table 40. MII TX timings

Symbol	Description	Min	Max	Unit
t_{CK}	MII_TXCLK clock period	40	40	ns
t_D	MII_TXCLK to MII output data delay	-1	8.9	

Note: To calculate the t_{SETUP} value for the PHY you have to consider the next t_{CLK} rising edge, so you have to apply the following formula: $t_{SETUP} = t_{CLK} - t_{max}$

7.9.2 MII receive timing specifications

Figure 20. MII RX waveforms

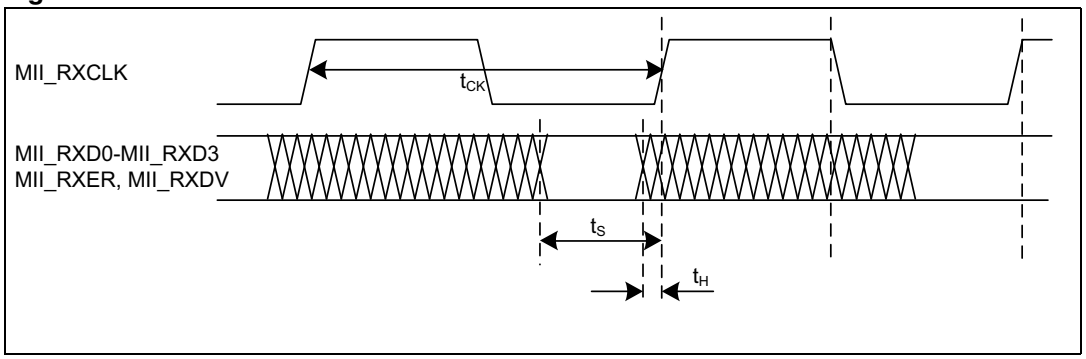


Table 41. MII RX timings

Symbol	Description	Min	Max	Unit
t_{CK}	MII_TXCLK clock period	40	40	ns
t_S	Setup time requirement for MII receive data	1.6		
t_H	Hold time requirement for MII receive data	0.7		

7.9.3 MDIO timing specifications

Figure 21. MDC waveforms

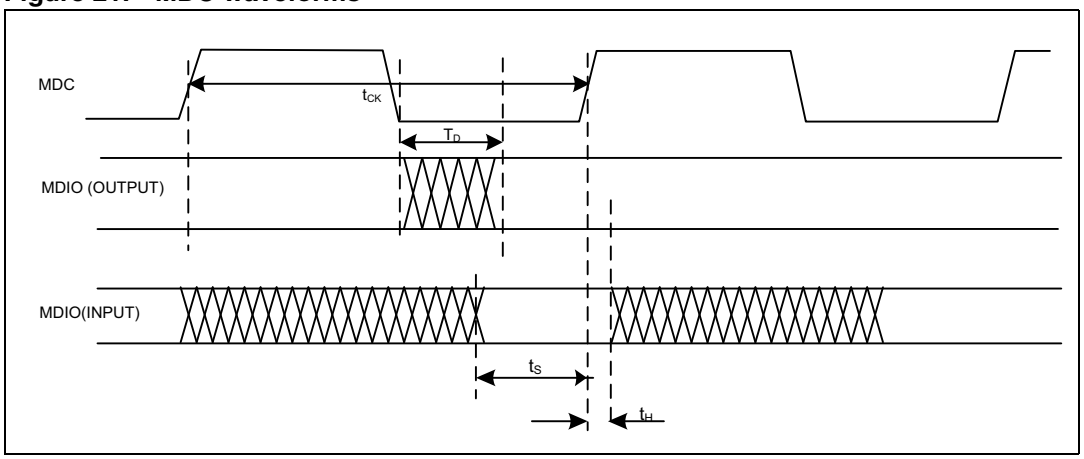


Table 42. MDC timings

Symbol	Description	Min	Max	Unit
t_{CK}	MDC clock	614.4	614.4	ns
t_D	Falling edge of MDC to MDIO output delay	204	0.64	
t_S	Setup time requirement for MDIO input	9.6		
t_H	Hold time requirement for MDIO input	-6.6		

Note: When MDIO is used as output the data are launched on the falling edge of the clock as shown in Figure 21.

7.10 SMII Ethernet MAC timing characteristics

Figure 22. SMII input/output timing waveform

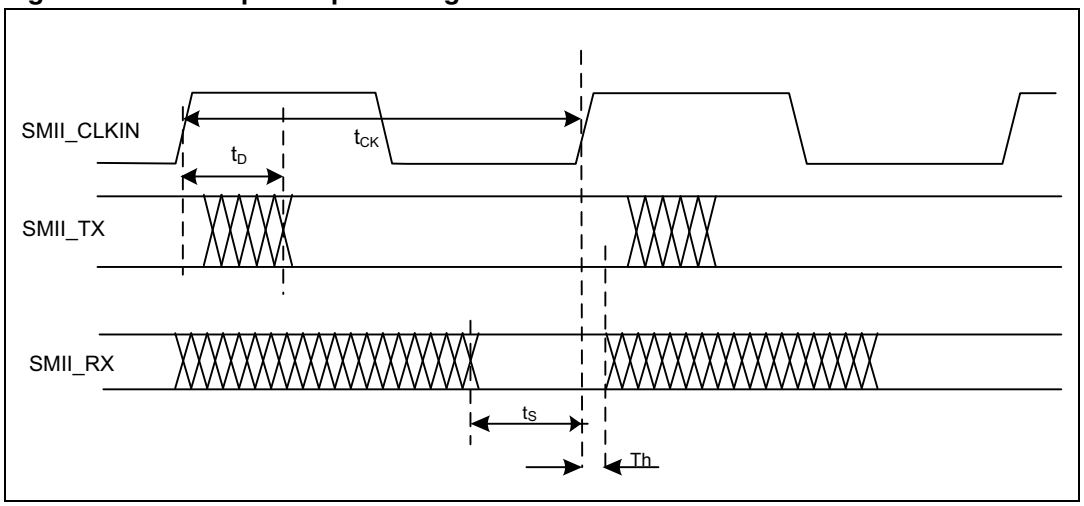


Table 43. SMII timings

Symbol	Description	Min	Max	Unit
t_{CK}	SMII clock	8	8	ns
t_S	Setup time requirement for SMII_RX	-0.90		
t_H	Hold time requirement for receive SMII_RX	2.904		
t_D	SMII_CLKIN to SMII_TX output delay	4.12	14.17	

Caution: Data in *Table 43* subject to SMII functional issue described in the SPEAr320 errata sheet.

7.11 SMI - Serial memory interface timing characteristics

Figure 23. SMI I/O waveforms

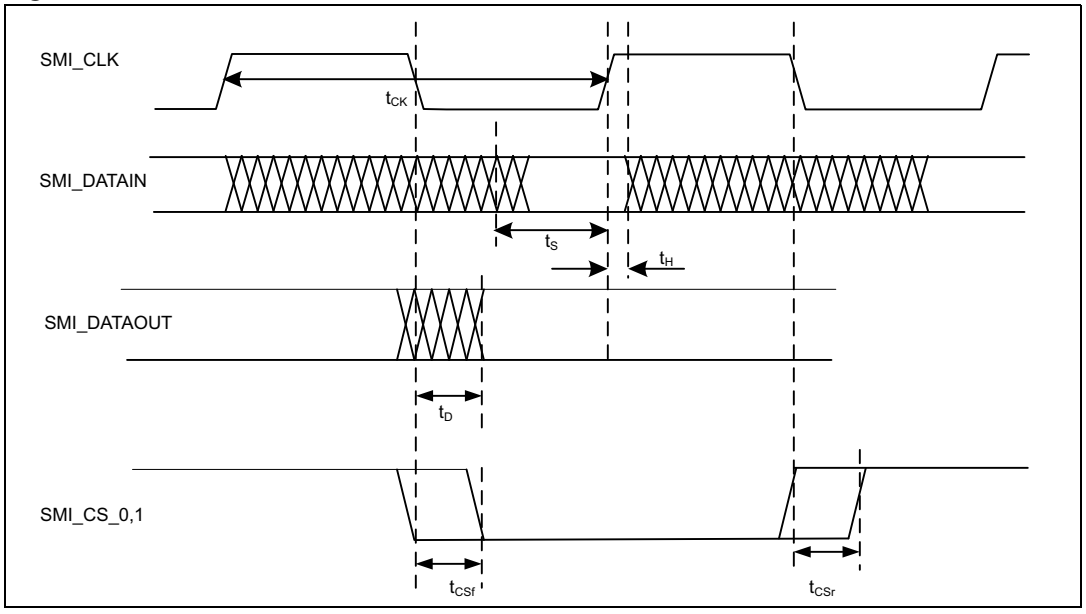


Table 44. SMI timings

Symbol	Description	Min	Max	Unit
t_{CK}	SMI clock period	20	50	ns
t_D	SMI_CLK to SMI_DATAOUT output delay	-2.96	3.05	
t_S	Setup requirement for SMI_DATAIN	9.69		
t_H	Hold requirement for SMI_DATAIN	-2.53		
t_{CSf}	Min and max delay of falling edge of SMI_CS_0 , 1 w.r.t SMI_CLK	-3.0	2.9	
t_{CSr}	Min and max delay of rising edge of SMI_CS_0 , 1 w.r.t SMI_CLK	-2.8	2.8	

7.12 SSP timing characteristics

This module provides a programmable length shift register which allows serial communication with other SSP devices through a 3 or 4 wire interface (SSP_CLK, SSP_MISO, SSP_MOSI and SSP_CSn). The SSP supports the following features:

- Master/Slave mode operations
- Chip-selects for interfacing to multiple slave SPI devices.
- 3 or 4 wire interface (SSP_SCK, SSP_MISO, SSP_MOSI and SSP_CSn)
- Single interrupt
- Separate DMA events for SPI Receive and Transmit
- 16-bit shift register
- Receive buffer register
- Programmable character length (2 to 16 bits)
- Programmable SSP clock frequency range
- 8-bit clock pre-scaler
- Programmable clock phase (delay or no delay)
- Programmable clock polarity

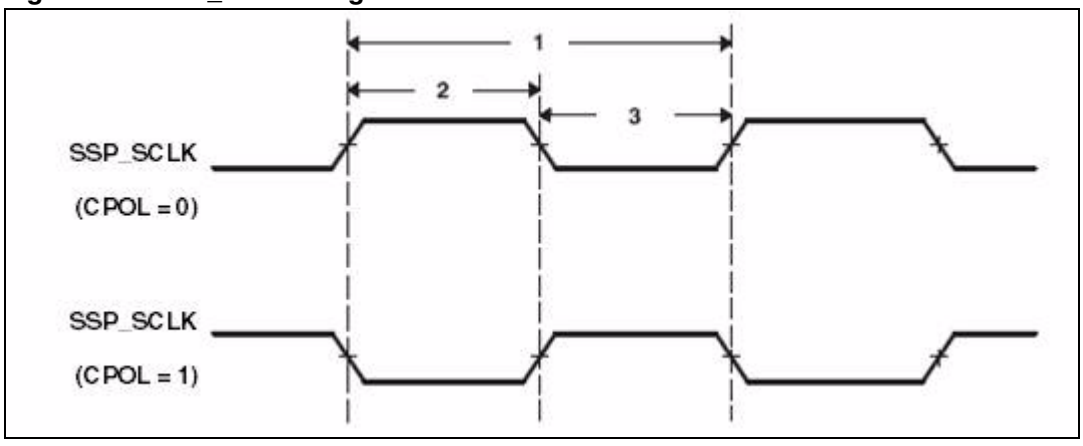
Note: The following tables and figures show the characterization of the SSP using the SPI protocol.

Table 45. Timing requirements for SSP (all modes)

No.	parameters		Min	Max	Unit
1	$T_{c(CLK)}$	Cycle time, SSP_CLK	24	–	ns
2	$T_{w(CLKH)}$	Pulse duration, SSP_CLK high	0.49*To	0.51*To	ns
3	$T_{w(CLKL)}$	Pulse duration, SSP_CLK low	0.49*To	0.51*To	ns

T = Tc(CLK) = SSP_CLK period is equal to the SSP module master clock divided by a configurable divider.

Figure 24. SSP_CLK timings



7.12.1 SPI master mode timings (clock phase = 0)

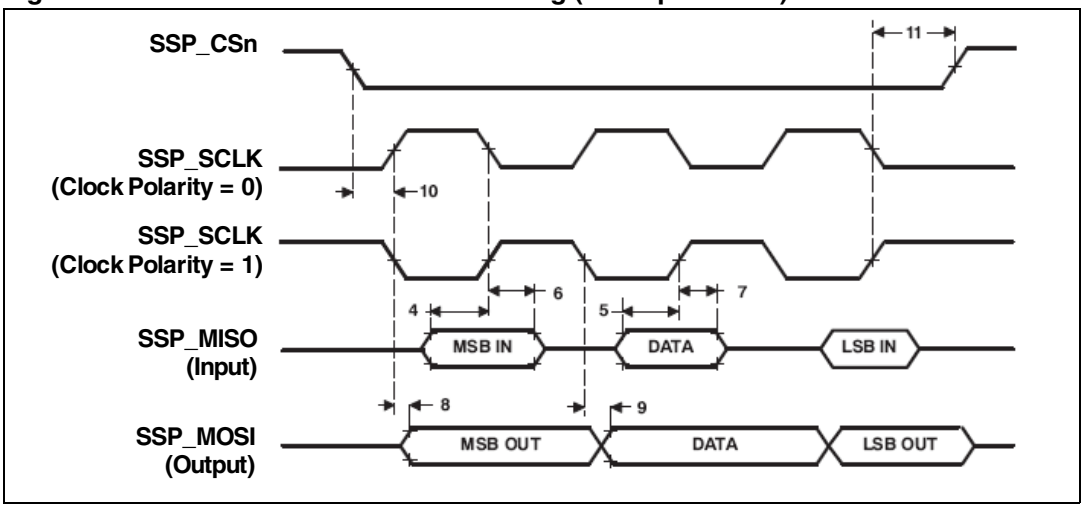
Table 46. Timing requirements for SPI master mode (clock phase = 0)

No.	Parameters			Min	Max	Unit
4	$t_{su(DIV-CLKL)}$	Setup time, MISO (input) valid before SSP_CLK (output) falling edge	Clock polarity = 0	-0.4	-0.3	ns
5	$t_{su(DIV-CLKH)}$	Setup time, MISO (input) valid before SSP_CLK (output) rising edge	Clock polarity = 1	-0.4	-0.3	ns
6	$t_{h(CLKL-DIV)}$	Hold time, MISO (input) valid after SSP_CLK (output) falling edge	Clock polarity = 0	0.9	1.7	ns
7	$t_{h(CLKH-DIV)}$	Hold time, MISO (input) valid after SSP_CLK (output) rising edge	Clock polarity = 1	0.9	1.7	ns

Table 47. Switching characteristics over recommended operating conditions for SPI master mode (clock phase =0)

No.	Parameters			Min	Max	Unit
8	$t_{d(CLKH-DOV)}$	Delay time, SSP_CLK (output) rising edge to MOSI (output) transition	Clock Polarity = 0	-3.1	2.2	ns
9	$t_{d(CLKL-DOV)}$	Delay time, SSP_CLK (output) falling edge to MOSI (output) transition	Clock Polarity = 1	-3.1	2.2	ns
10	$t_{d(ENL-CLKH/L)}$	Delay time, SSP_CSn (output) falling edge to first SSP_CLK (output) rising or falling edge		T		ns
11	$td_{(CLKH/L-ENH)}$	Delay time, SSP_CLK (output) rising or falling edge to SSP_CSn (output) rising edge		T/2		ns

Figure 25. SPI master mode external timing (clock phase = 0)



7.12.2 SPI master mode timings (clock phase = 1)

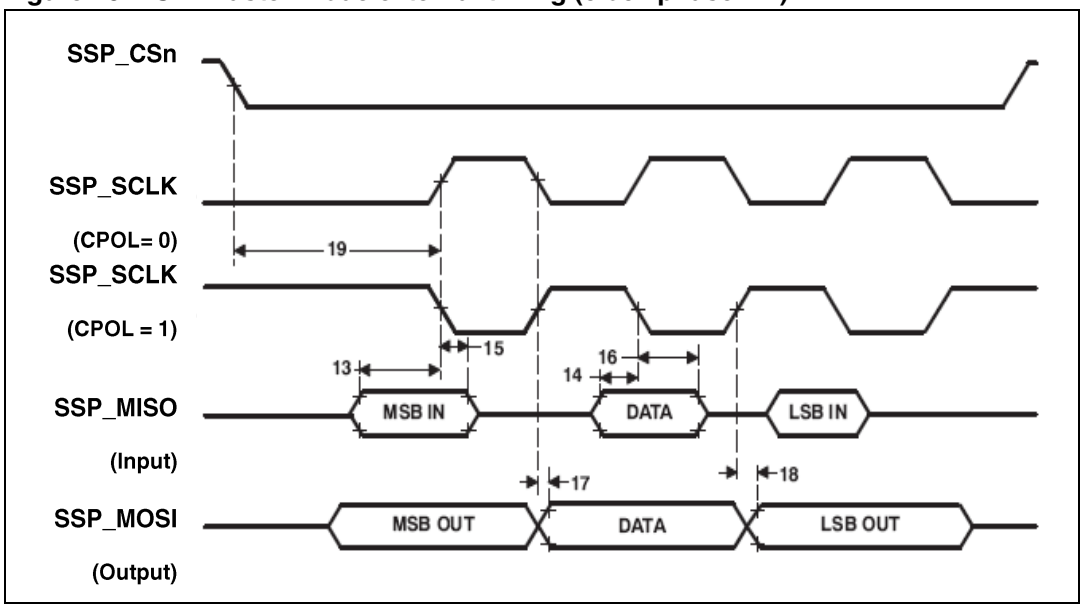
Table 48. Timing requirements for SPI master mode (clock phase = 1)

No.	Parameters			Min	Max.	Unit
13	$t_{su(DIV-CLKL)}$	Setup time, MISO (input) valid before SSP_CLK (output) rising edge	Clock Polarity = 0	-0.4	-0.3	ns
14	$t_{su(DIV-CLKH)}$	Setup time, MISO (input) valid before SSP_CLK (output) falling edge	Clock Polarity = 1	-0.4	-0.3	ns
15	$t_{h(CLKL-DIV)}$	Hold time, MISO (input)valid after SSP_CLK (output) rising edge	Clock Polarity = 0	0.9	1.7	ns
16	$t_{h(CLKH-DIV)}$	Hold time, MISO (input) valid after SSP_CLK (output) falling edge	Clock Polarity = 1	0.9	1.7	ns

Table 49. Switching characteristics over recommended operating conditions for SPI master mode (clock phase = 1)

No.	Parameters			Min	Max	Unit
17	$t_{d(CLKH-DOV)}$	Delay time, SSP_CLK (output) falling edge to MOSI (output) transition	Clock Polarity = 0	-3.1	2.2	ns
18	$t_{d(CLKL-DOV)}$	Delay time, SSP_CLK (output) rising edge to MOSI (output) transition	Clock Polarity = 1	-3.1	2.2	ns
19	$t_{d(ENL-CLKH/L)}$	Delay time, SSP_CSn (output) falling edge to first SSP_CLK (output) rising or falling edge		T/2		ns
20	$t_{d(CLKH/L-ENH)}$	Delay time, SSP_CLK (output) rising or falling edge to SSP_CSn (output) rising edge		T		ns

Figure 26. SPI master mode external timing (clock phase = 1)



7.13 UART timing characteristics

Figure 27. UART transmit and receive timings

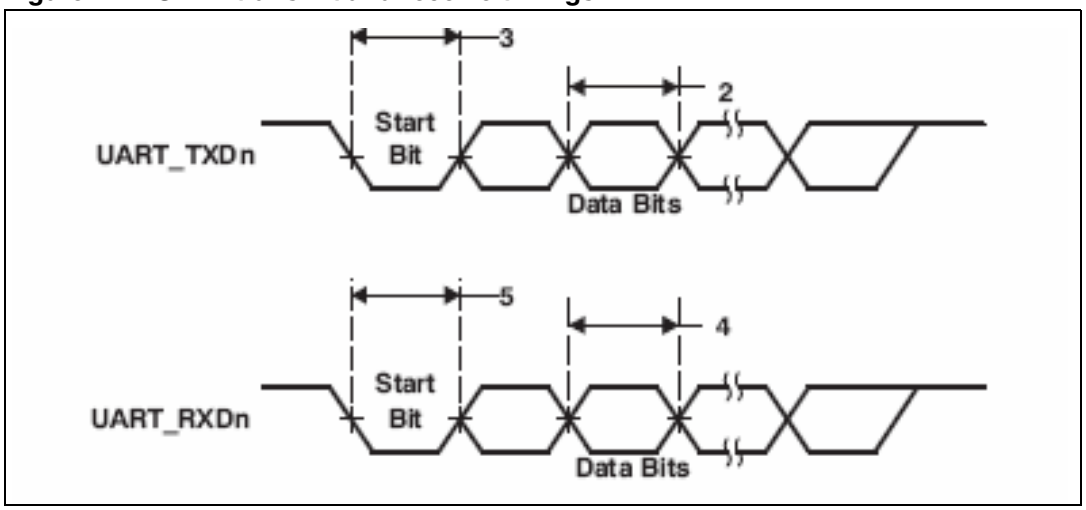


Table 50. UART transmit timing characteristics

S.No.	Parameters	Min	Max	Unit
1	UART0 Maximum Baud Rate		3	Mbps
	UART1/UART2 Maximum Baud Rate		7	
2	UART Pulse Duration Transmit Data (TxD)	$0.99B_{(1)}$	$B_{(1)}$	ns
3	UART Transmit Start Bit	$0.99B_{(1)}$	$B_{(1)}$	ns

Table 51. UART receive timing characteristics

S.No.	Parameters	Min	Max	Units
4	UART Pulse Duration Receive Data (RxD)	$0.97B_{(1)}$	$1.06B_{(1)}$	ns
5	UART Receive Start Bit	$0.97B_{(1)}$	$1.06B_{(1)}$	ns

where (1) B = UART baud rate

7.14 ADC characteristics

Table 52. 10-bit ADC characteristics

Symbol	Parameters	Min	Typ	Max	Unit
f_{ADC_CLK}	ADC_CLK frequency	3		14	MHz
AV_{DD}	ADC supply voltage			2.5	V
V_{REFP}	Positive reference voltage			2.5	V
V_{REFN}	Negative reference voltage	0			V
V_{IREF}	Internal reference voltage	1.95	2	2.05	V
$t_{STARTUP}$	Startup time		50		µs
V_{AIN}	Input range (absolute)	AGND - 0.3		AVDD - 0.3	V
	Conversion range	V_{REFN}		V_{REFP}	
C_{AIN}	Input capacitance	5	6.4	8	pF
R_{AIN}	Input mux resistance (total equivalent sampling resistance)	1.5	2	2.5	KΩ
t_{CONV}	Conversion time (f_{ADC_CLK}=14 MHz)			1	µs
	Conversion time	13			ADC_CLK cycles
INL	Integral linearity error			±1	LSB
DNL	Differential linearity error			±1	LSB

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 53. LFBGA289 (15 x 15 x 1.7 mm) mechanical data

Dim.	mm			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.700			0.0669
A1	0.270			0.0106		
A2		0.985			0.0387	
A3		0.200			0.0078	
A4			0.800			0.0315
b	0.450	0.500	0.550	0.0177	0.0197	0.0217
D	14.850	15.000	15.150	0.5846	0.5906	0.5965
D1		12.800			0.5039	
E	14.850	15.000	15.150	0.5846	0.5906	0.5965
E1		12.800			0.5039	
e		0.800			0.0315	
F		1.100			0.0433	
ddd			0.200			0.0078
eee			0.150			0.0059
fff			0.080			0.0031

Figure 28. LFBGA289 package dimensions

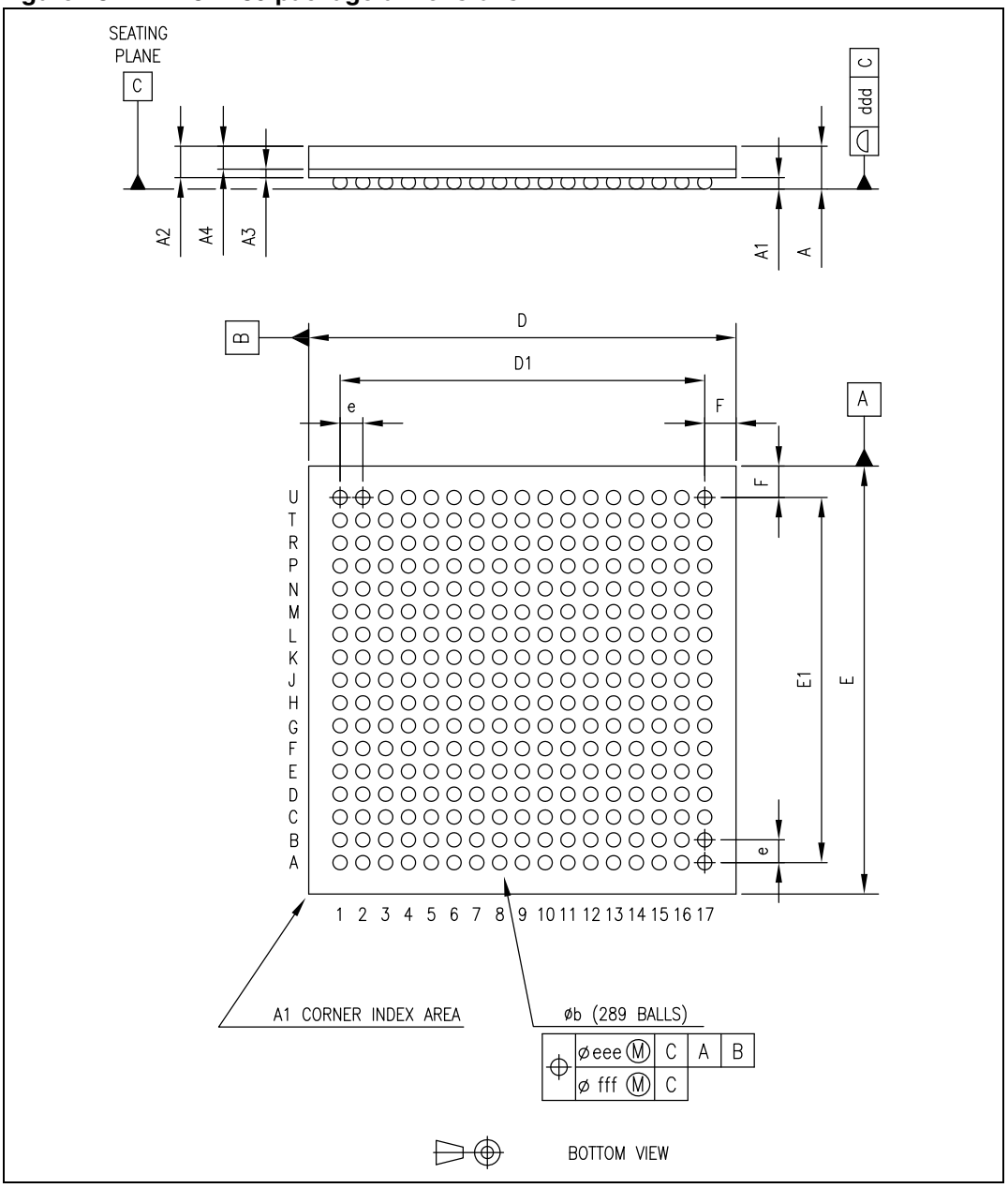


Table 54. Thermal resistance characteristics

package	Θ_{JC} (°C/W)	Θ_{JB} (°C/W)	Θ_{JA}(°C/W)(1)
LFBGA289	18.5	24.5	33

1. Measured on JESD51 2s2p test board.

9 Revision history

Table 55. Document revision history

Date	Revision	Changes
12-Nov-2009	1	Initial release.
2-Feb-2010	2	Removed I2S feature. Changed “SPI” to “SSP” where applicable. Updated *Figure 1: Functional block diagram* and *Figure 2: Typical system architecture using SPEAr320*. Corrected *Figure 3: Typical SMII system*. Updated the *Features* on the first page. Updated *Section 3.14: GPIOs*. Added *Table 10: PL_GPIO pin description*. Reviewed and updated the *Section 4.3: Shared I/O pins (PL_GPIOs)*. Added *Section 4.4: PL_GPIO pin sharing for debug modes*. Updated *Section 6.1: Absolute maximum ratings*. Deleted the first footnote at the end of the *Table 17: Maximum power consumption* and modified the text in footnote *3. on page 46* Updated *Table 18: Recommended operating conditions*. Added V_{DD} RTC line in the *Table 16: Absolute maximum ratings* and *Table 17: Maximum power consumption*. Updated *Table 24: Driver characteristics*. Deleted “GMII” form *Section 7.9: MII Ethernet MAC 10/100 Mbps timing characteristics* and also “1000 Mbps”. Added *Section 3.6: SDIO controller/MMC card interface*. Updated *Section 7.12: SSP timing characteristics*. Updated *Section 6.7: Power up sequence* and added *Section 6.8: Removing power supplies for power saving*. Separated *Electrical characteristics* and *Timing requirements* into two chapters. Changed the title of *Section 6.5: 3.3V I/O characteristics*. Added *Table 54: Thermal resistance characteristics*. Changed all the UART numbering (from 1..3 to 0..2). UART baud rate changed in *Section 2: Main features* and *Section 4.3.2: Configuration modes* from > 6 Mbps into up to 6 Mbps.

Table 55. Document revision history (continued)

Date	Revision	Changes
02-Feb-2010	2 (continued)	Changed the baud rate for the UARTs with Hardware flow control from “up to 460.8 Kbaud” into “up to 3 Mbps”. *Table 15: Reconfigurable array subsystem memory map*: changed a typo error “UART23” into “UART2”. *Section 3.10: CAN controller*: changed “32 message objects (132 x 32 message RAM)” to “16 message objects (136 x 16 message RAM)”. Corrected a typo error in the *Figure 13: In/out data address signal waveforms for NAND Flash* and *Figure 16: In/out data signal waveforms for 16-bit NAND Flash configuration*. Updated *Table 4: Power supply pin description* and added a note at the end of the table. Corrected the voltage capable of RTC in the *Table 3: Master clock, RTC, Reset and 3.3 V comparator pin descriptions*. Updated figures of *Section 7.6: FSMC timing characteristics*. Updated *Figure 19: MII TX waveforms*, *Figure 26: Block diagram of MII TX pins*, *Figure 20: MII RX waveforms* Corrected the speed of UART1 and UART2 in *Section 3.18.2: UART1* from “5 Mbps” into “6 Mbps”. Updated *Table 3: Master clock, RTC, Reset and 3.3 V comparator pin descriptions*, *Table 7: USB pin description* and *Table 9: DDR pin description* Minor text corrections.
18-Nov-2010	3	Corrected pin assignment of UART0_RTS and CTS in *Table 11: PL_GPIO multiplexing scheme* Added *Section 7.14: ADC characteristics* Changed max. speed of UART2 and UART3 in feature descriptions from 6 Mbps to 7 Mbps and updated *Table 50: UART transmit timing characteristics on page 66*.
02-Dec-2010	4	Corrected SRAM size from 56 K to 8 Kbytes in *Chapter 2: Main features* Updated feature descriptions for the 3 UARTs in *Section 3.18: UARTs*

Table 55. Document revision history (continued)

Date	Revision	Changes
05-Jul-2011	5	Removed PU from description of MRESET in *Table 3: Master clock, RTC, Reset and 3.3 V comparator pin descriptions* Updated figures and tables in: – *Section 6.7: Power up sequence* – *Section 7.3: DDR2 timing characteristics* – *Section 7.4: CLCD timing characteristics* – *Section 7.5: I^2C timing characteristics* – *Section 7.6: FSMC timing characteristics* – *Section 7.9: MII Ethernet MAC 10/100 Mbps timing characteristics* – *Section 7.10: SMII Ethernet MAC timing characteristics* – *Section 7.11: SMI - Serial memory interface timing characteristics* Added *Section 7.7: EMI timing characteristics*. Added *Section 7.8: SDIO timing characteristics*. Updated *Table 52: 10-bit ADC characteristics*. Updated *Table 54: Thermal resistance characteristics*. Added the T_{ck} max value for CLCP clock period in *Table 32: CLCD timings*. Updated *Figure 19: MII TX waveforms*. Replaced “43.2 kΩ” by “43.2 Ω” in *Section 4.1: Required external components* (*USB_TX_RTUNE* bullet). *Table 45: Timing requirements for SSP (all modes)*: replaced column “*Value*” by columns “*Min*” and “*Max*”. Replaced “*clock phase = 1*” by “*clock phase = 0*” at the figure caption of *Figure 25*. *Section 4.1: Required external components*: added new bullet “*DITH_VDD_2V5: Add a ferrite bead to ball M4*”. Added a footnote for V_{DD} 2.5 at *Table 18: Recommended operating conditions*. Updated the footnote at *Table 21: Low voltage TTL DC output specification (3 V< V_{DD} <3.6 V)*. Added a note at the beginning of *Chapter 7: Timing requirements* Added *Section 7.1: External interrupt timing characteristics* and *Section 7.2: Reset timing characteristics*. Replaced “*Embedded/custom selector*” by “*RAS select register*” in *Figure 3: Hierarchical multiplexing scheme* and *Table 11: PL_GPIO multiplexing scheme*. Replaced “*Embedded IPs*” by “*Alternate functions*” in *Figure 3: Hierarchical multiplexing scheme*. Replaced the FSMC pins naming in *Section 7.6: FSMC timing characteristics*, as follows: – NFIO by FSMC_Dx (where x=0 to 15) – NF_CE by FSMC_CSx (where x= 0 to 3) – NF_ALE by FSMC_ADDR_LE – NF_WE by FSMC_WE – NF_RE by FSMC_RE – NF_CLE by FSMC_CMD_LE

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