



THE DATASHEET OF SN75ALS181NSR

DIFFERENTIAL DRIVER AND RECEIVER PAIR

Check for Samples: [SN75ALS181](#)

FEATURES

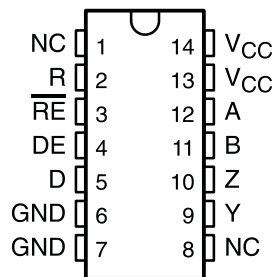
- Meets TIA/EIA-422-B, TIA/EIA-485-A, and CCITT Recommendations V.11 and X.27
- Low Supply-Current Requirements...
30 mA Max
- Driver Output Capacity...±60 mA
- Thermal Shutdown Protection
- Driver Common-Mode Output Voltage Range of –7 V to 12 V
- Receiver Input Impedance...12 kΩ Min
- Receiver Input Sensitivity...±200 mV
- Receiver Input Hysteresis...60 mV Typ
- Receiver Common-Mode Input Voltage Range of ±12 V
- Operates From Single 5-V Supply
- Glitch-Free Power-Up and Power-Down Protection

DESCRIPTION

The SN75ALS181 is a differential driver and receiver pair designed for bidirectional data communication on multipoint bus transmission lines. The design provides for balanced transmission lines and meets TIA/EIA-422-B and TIA/EIA-485-A, and CCITT recommendations V.10, V.11, X.26, and X.27.

The SN75ALS181 combines a 3-state differential line driver and a differential-input line receiver that operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be connected together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected to separate pins for greater flexibility and are designed to offer minimum loading to the bus when the driver is disabled or $V_{CC} = 0$. These ports feature wide positive and negative common-mode voltage changes, making the device suitable for party-line applications.

**N OR NS PACKAGE
(TOP VIEW)**



N.C. – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FUNCTION TABLES

Each Driver

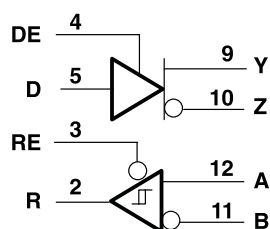
INPUTS D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

Each Receiver⁽¹⁾

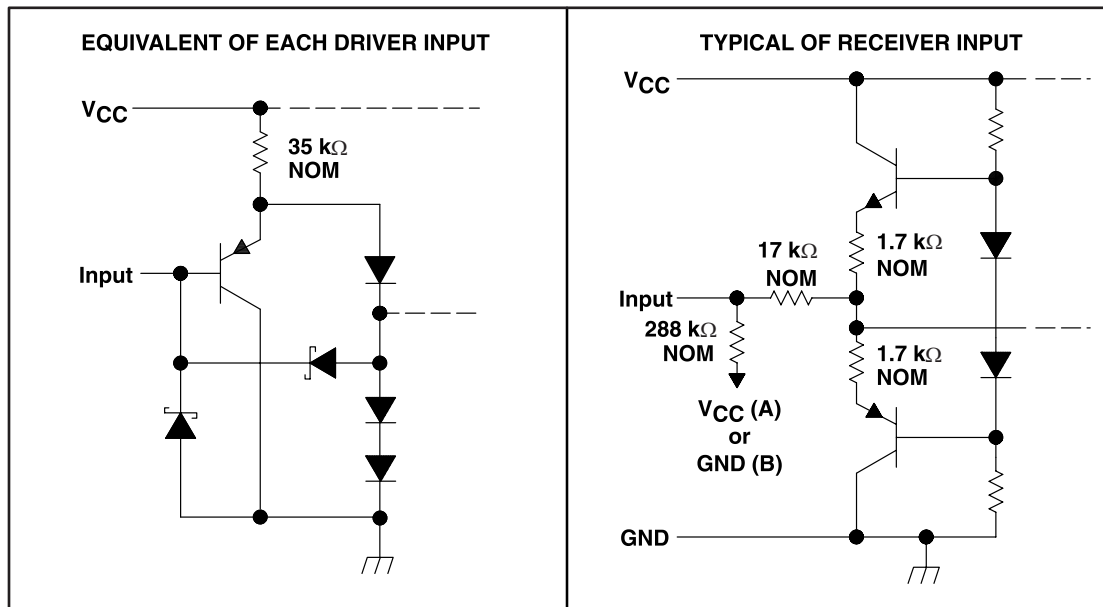
DIFFERENTIAL A–B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2 \text{ V}$	L	H
$-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$	L	?
$V_{ID} \leq -0.2 \text{ V}$	L	L
X	H	Z

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant,
Z = high impedance (off)

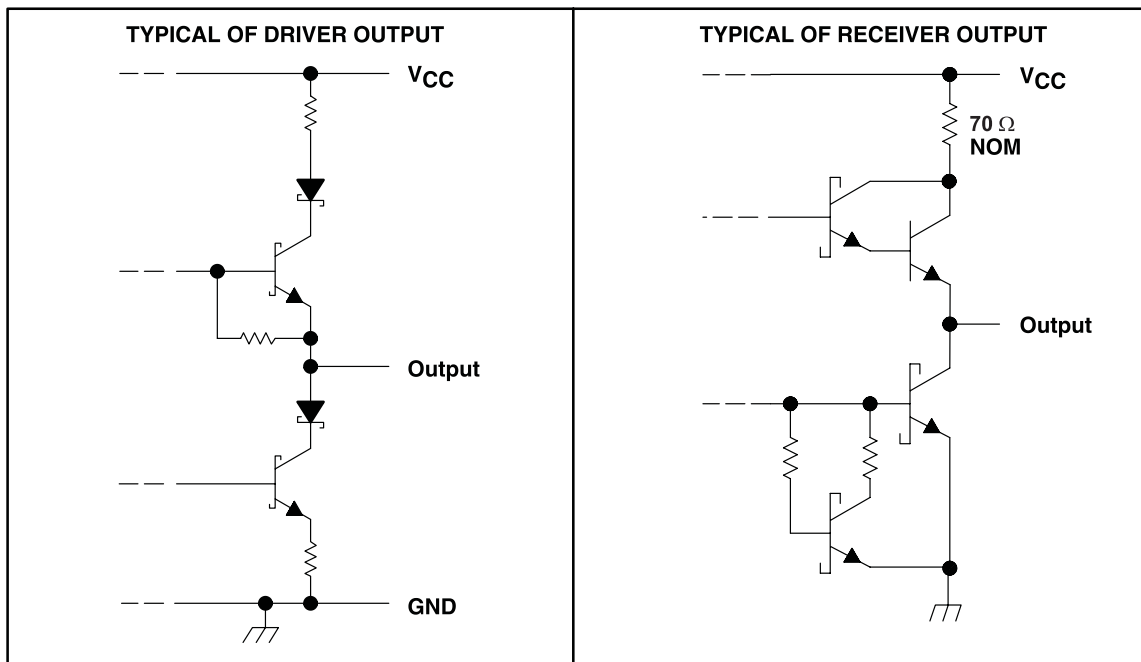
LOGIC DIAGRAM (POSITIVE LOGIC)



SCHEMATICS OF INPUTS



SCHEMATICS OF OUTPUTS



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range ⁽²⁾			7	V
	Input voltage range	D, DE, and $\overline{RE}$ inputs		7	V
	Output voltage range	Driver	–9	14	V
	Input voltage range	Receiver	–14	14	V
	Receiver differential input voltage range ⁽³⁾		–14	14	V
θ_{JA}	Package thermal impedance ⁽⁴⁾⁽⁵⁾	N package		80	°C/W
		NS package		76	
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260	°C
T _{stg}	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential input voltage, are with respect to network ground terminal.
- (3) Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.
- (4) Maximum power dissipation is a function of T_J(max), θ_{JA} , and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $PD = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (5) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		4.75	5	5.25	V
V _{OC}	Common-mode output voltage ⁽¹⁾	Driver	–7		12	V
V _{IC}	Common-mode input voltage ⁽¹⁾	Receiver	–12		12	V
V _{IH}	High-level input voltage	D, DE, and $\overline{RE}$	2			V
V _{IL}	Low-level input voltage	D, DE, and $\overline{RE}$			0.8	V
V _{ID}	Differential input voltage				±12	V
I _{OH}	High-level output current	Driver			–60	mA
		Receiver			–400	μA
I _{OL}	Low-level output current	Driver			60	mA
		Receiver			8	
T _A	Operating free-air temperature		0		70	°C

- (1) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this table for common-mode output voltage level only.

Driver Section

ELECTRICAL CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IK} Input clamp voltage	$I_I = -18 \text{ mA}$			-1.5	V
V_O Output voltage	$I_O = 0$	0		6	V
$ V_{OD1} $ Differential output voltage	$I_O = 0$	1.5		6	V
$ V_{OD2} $ Differential output voltage	$V_{CC} = 5 \text{ V}$, $R_L = 100 \Omega$	See Figure 1		$1/2 V_{OD1}$	V
	$R_L = 54 \Omega$			2	
				1.5 2.3 5	
$ V_{OD3} $ Differential output voltage	$V_{test} = -7 \text{ V to } 12 \text{ V}$, See Figure 2	1.5		5	V
$\Delta V_{OD} $ Change in magnitude of differential output voltage	$R_L = 54 \Omega$ or 100Ω , See Figure 1			± 0.2	V
V_{OC} Common mode output voltage	$R_L = 54 \Omega$ or 100Ω , See Figure 1			3	V
				-1	
$\Delta V_{OC} $ Change in magnitude of common-mode output voltage ⁽²⁾	$R_L = 54 \Omega$ or 100Ω , See Figure 1			± 0.2	V
I_{OZ} High-impedance-state output current	$V_O = -7 \text{ V to } 12 \text{ V}$ ⁽³⁾			± 100	μA
I_{IH} High-level input current	$V_{IH} = 2.4 \text{ V}$			20	μA
I_{IL} Low-level input current	$V_{IL} = 0.4 \text{ V}$			-100	μA
I_{OS} Short circuit output current	$V_O = -7 \text{ V}$			-250	mA
	$V_O = V_{CC}$			250	
	$V_O = 12 \text{ V}$			250	
	$V_O = 0 \text{ V}$			-150	
I_{CC} Supply current (total package)	No load	Outputs enabled	21	30	mA
		Outputs disabled	14	21	

(1) All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

(2) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level.

(3) This applies for both power on and power off. Refer to TIA/EIA-485-A for exact conditions

SWITCHING CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{dD} Differential output delay time, t_{dDH} or t_{dDL}	$R_L = 54 \Omega$, $C_L = 50 \text{ pF}$, See Figure 3	9	13	20	ns
$t_{sk(p)}$ Pulse skew ($ t_{dDH} - t_{dDL} $)	$R_L = 54 \Omega$, $C_L = 50 \text{ pF}$, See Figure 3		1	8	ns
t_t Differential output transition time	$R_L = 54 \Omega$, $C_L = 50 \text{ pF}$, See Figure 3	3	10	16	ns
t_{PZH} Output enable time to high level	$R_L = 110 \Omega$, See Figure 4		36	53	ns
t_{PZL} Output enable time to low level	$R_L = 110 \Omega$, See Figure 5		39	56	ns
t_{PHZ} Output disable time from high level	$R_L = 110 \Omega$, See Figure 4		20	31	ns
t_{PLZ} Output disable time from low level	$R_L = 110 \Omega$, See Figure 5		9	20	ns

(1) All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

Receiver Section

ELECTRICAL CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{T+}	Positive-going threshold voltage, differential input	$V_O = 2.7\text{ V}$, $I_O = -0.4\text{ mA}$				0.2	V
V_{T-}	Negative-going threshold voltage, differential input	$V_O = 0.5\text{ V}$, $I_O = 8\text{ mA}$		-0.2			V
V_{hys}	Input hysteresis ($V_{T+} - V_{T-}$)				60		mV
V_{IK}	Input clamp voltage, $\overline{RE}$	$I_I = -18\text{ mA}$				-1.5	V
V_{OH}	High-level output voltage	$V_{ID} = 200\text{ mV}$, $I_{OH} = -400\text{ }\mu\text{A}$, See Figure 6		2.7			V
V_{OL}	Low-level output voltage	$V_{ID} = 200\text{ mV}$, $I_{OL} = 8\text{ mA}$, See Figure 6				0.45	V
I_{OZ}	High-impedance-state output current	$V_O = 0.4\text{ V to } 2.4\text{ V}$				± 20	μA
I_I	Line input current	Other input at 0 V ⁽²⁾ , $V_I = 12\text{ V}$ $V_I = -7\text{ V}$				1	mA
						-0.8	
I_{IH}	High-level input current, $\overline{RE}$	$V_{IH} = 2.7\text{ V}$				20	μA
I_{IL}	Low-level input current, $\overline{RE}$	$V_{IL} = -7\text{ V}$				-100	μA
R_I	Input resistance			12			k Ω
I_{OS}	Short circuit output current	$V_{ID} = 200\text{ mV}$, $V_O = 0\text{ V}$		-15		-85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled		21	30	mA
			Outputs disabled		14	21	

(1) All typical values are at $V_{CC} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

(2) This applies for both power on and power off. Refer to TIA/EIA-485-A for exact conditions

SWITCHING CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PHL}	Differential output delay time, t_{dDH} or t_{dDL}	$V_{ID} = -1.5\text{ V to } 1.5\text{ V}$		10	16	25	ns
t_{PLH}	Propagation delay time, low- to high-level output	$V_{ID} = -1.5\text{ V to } 1.5\text{ V}$		10	16	25	ns
$t_{sk(p)}$	Pulse skew ($ t_{dDH} - t_{dDL} $)	$V_{ID} = -1.5\text{ V to } 1.5\text{ V}$			1	8	ns
t_{PZH}	Output enable time to high level				7	15	ns
t_{PZL}	Output enable time to low level				9	19	ns
t_{PHZ}	Output disable time from high level				18	27	ns
t_{PLZ}	Output disable time from low level				10	15	ns

(1) All typical values are at $V_{CC} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION

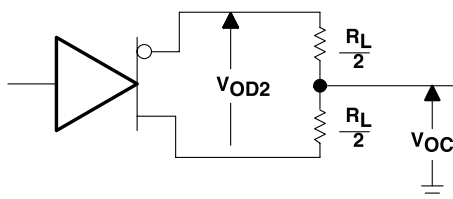


Figure 1. Driver Test Circuit, V_{OD} and V_{OC}

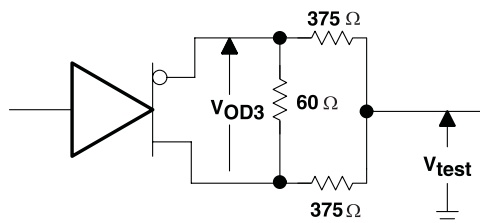


Figure 2. Driver Circuit, V_{OD3}

- The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$
- C_L includes probe and jig capacitance.

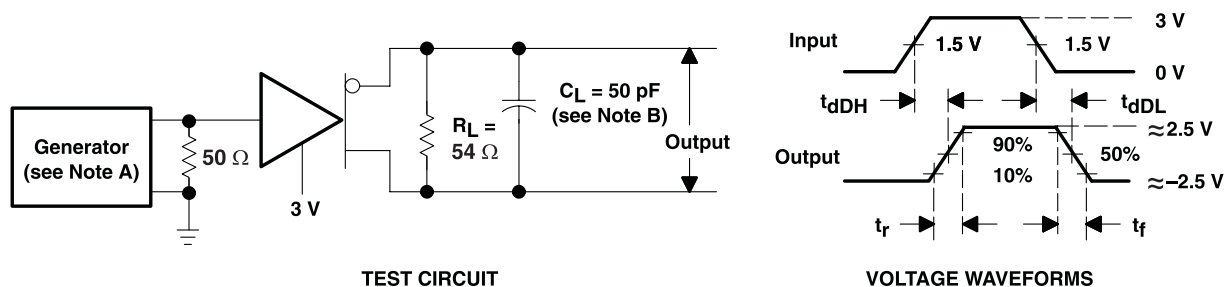


Figure 3. Driver Differential-Output Delay and Transition Times

- The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$
- C_L includes probe and jig capacitance.

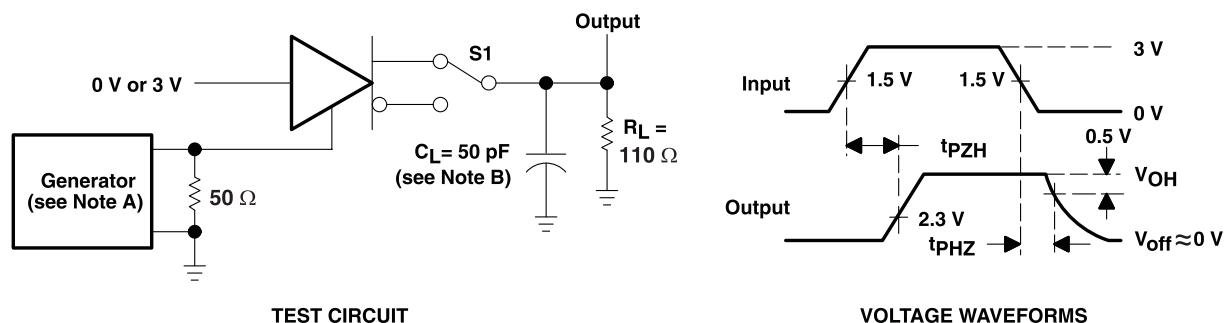
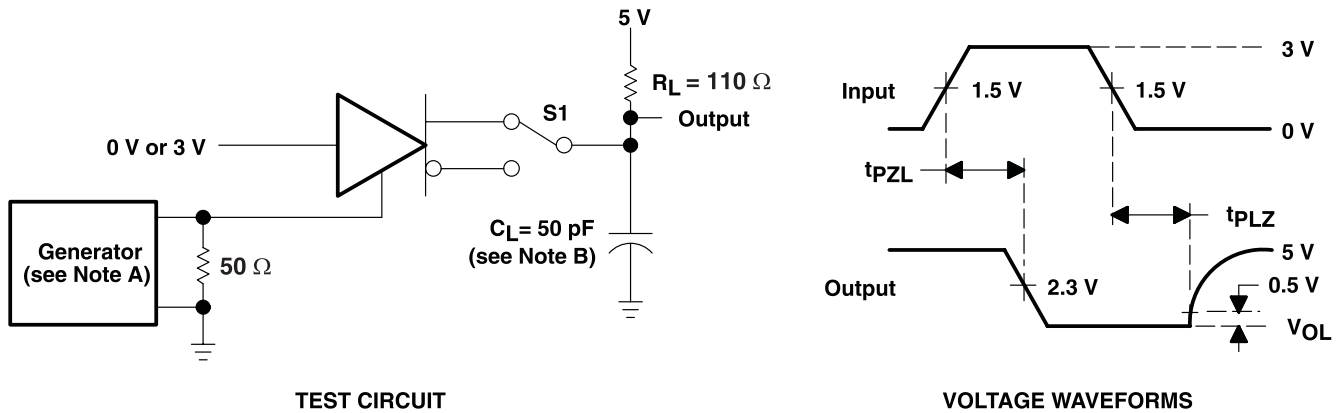
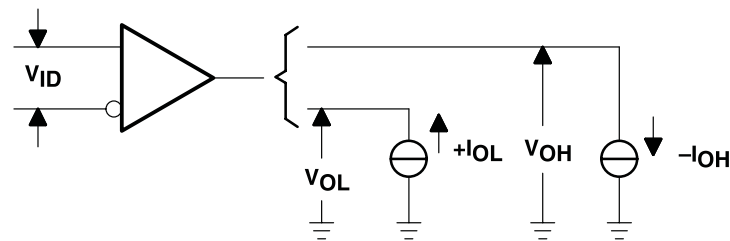
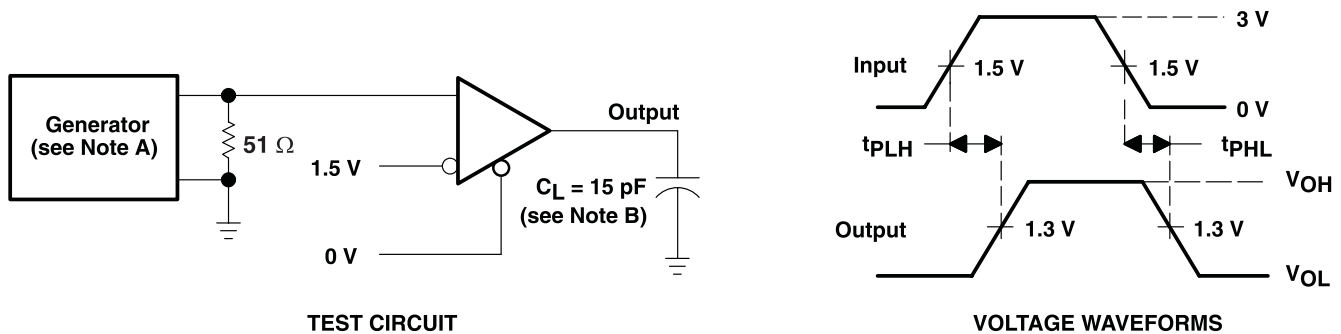


Figure 4. Driver Enable and Disable Times

- The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$
- C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION (continued)**Figure 5. Driver Enable and Disable Times****Figure 6. Receiver, V_{OH} and V_{OL}**

- A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$
- B. C_L includes probe and jig capacitance.

**Figure 7. Receiver Propagation-Delay Times**

- A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$
- B. C_L includes probe and jig capacitance.

TEST CIRCUIT

Figure 8. Receiver Output Enable and Disable Times

REVISION HISTORY

Changes from Revision C (May 2010) to Revision D	Page
• Removed Ordering Information table.	2
• Fixed graphical error in schematic.	3
• Fixed typographical error in MAX value for $\Delta V_{OD} $	5
• Fixed typographical error in UNITS for $\Delta V_{OC} $	5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75ALS181N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75ALS181N	Samples
SN75ALS181NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS181	Samples
SN75ALS181NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS181	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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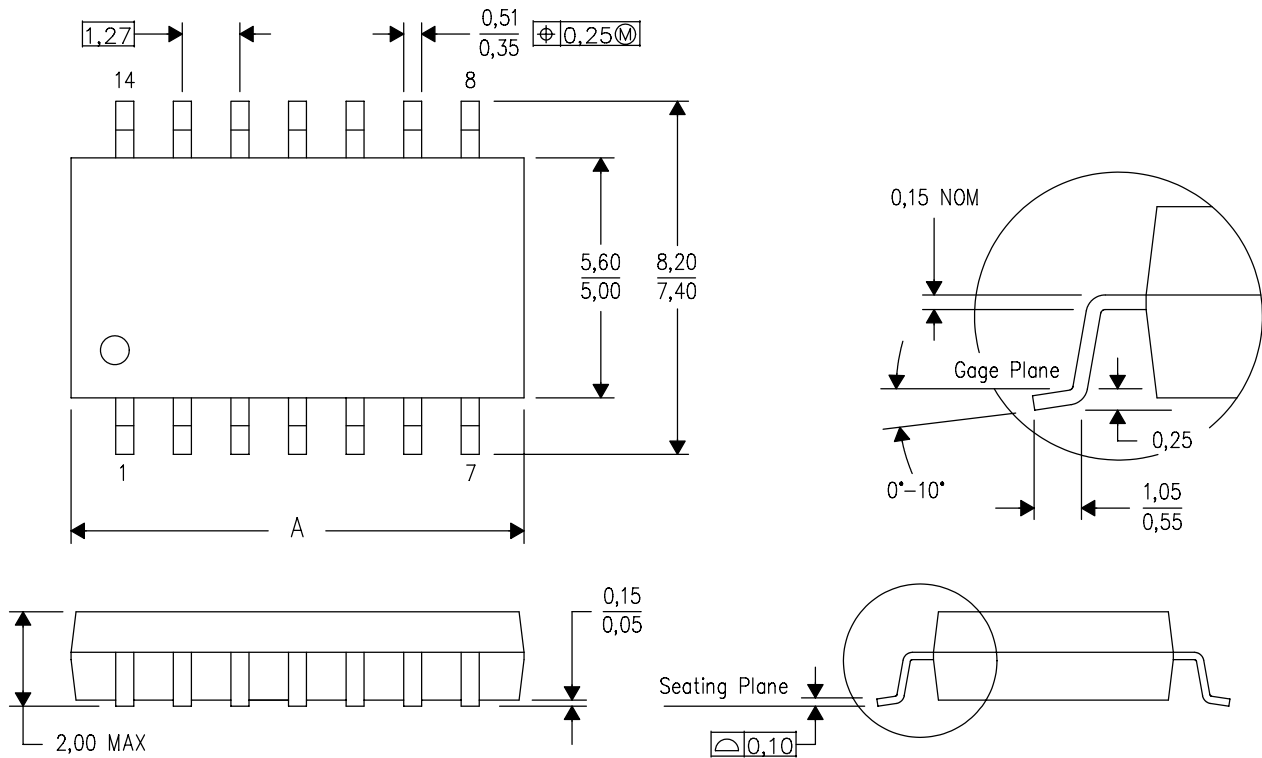
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MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

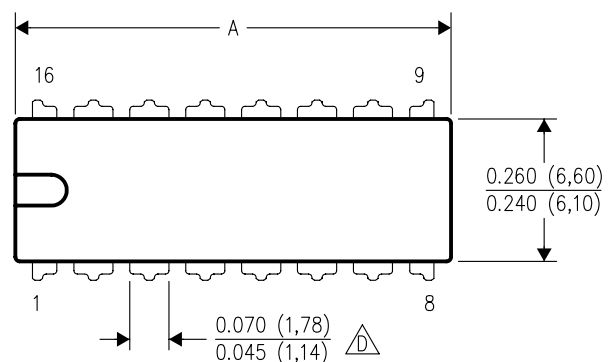
4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

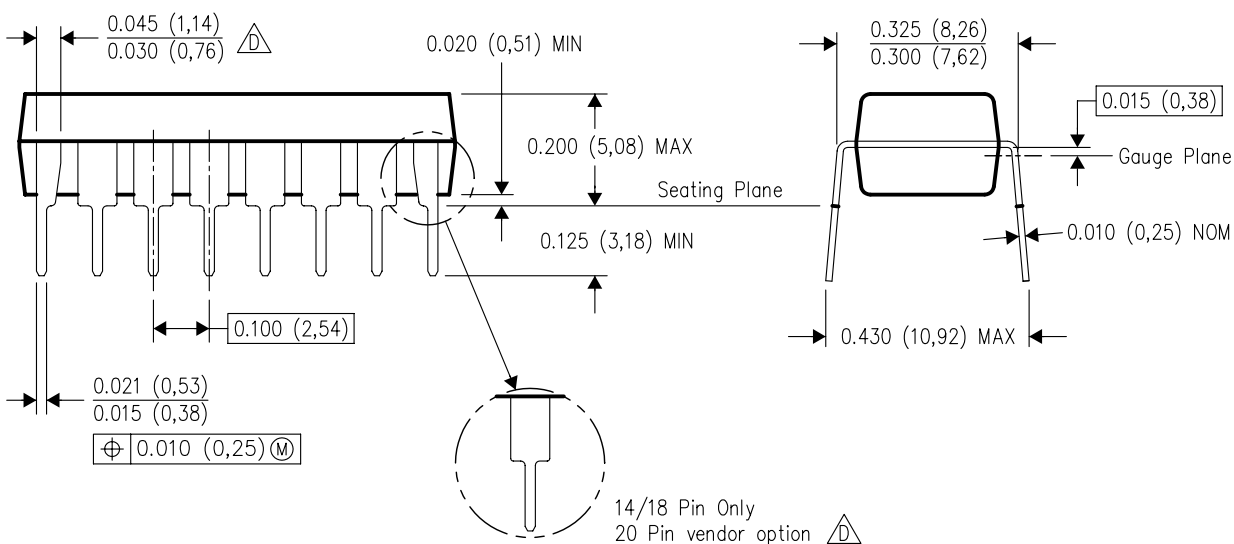
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management