



**THE DATASHEET OF
SN75ALS162DW**



SN75ALS162

OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

SLLS020C – JUNE 1986 – REVISED MAY 1995

- Meets IEEE Standard 488-1978 (GPIB)
- 8-Channel Bidirectional Transceiver
- Designed to Implement Control Bus Interface
- Designed for Multicontrollers
- High-Speed Advanced Low-Power Schottky Circuitry
- Low-Power Dissipation . . . 46 mW Max per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance PNP Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device Is Powered Down ($V_{CC} = 0$)
- Power-Up/Power-Down Protection (Glitch Free)

description

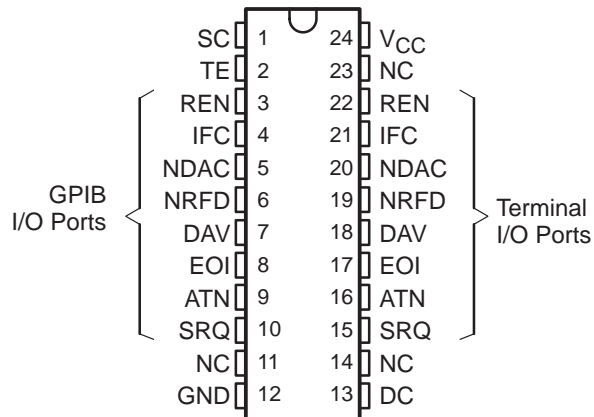
The SN75ALS162 eight-channel general-purpose interface bus (GPIB) transceiver is a monolithic, high-speed, advanced low-power Schottky process device designed to provide the bus-management and data-transfer signals between operating units of a multiple-controller instrumentation system. When combined with the SN75ALS160 octal bus transceiver, the SN75ALS162 provides the complete 16-wire interface for the IEEE 488 bus.

The SN75ALS162 features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. The direction of data through these driver-receiver pairs is determined by the DC, TE, and SC enable signals. The SC input allows the REN and IFC transceivers to be controlled independently.

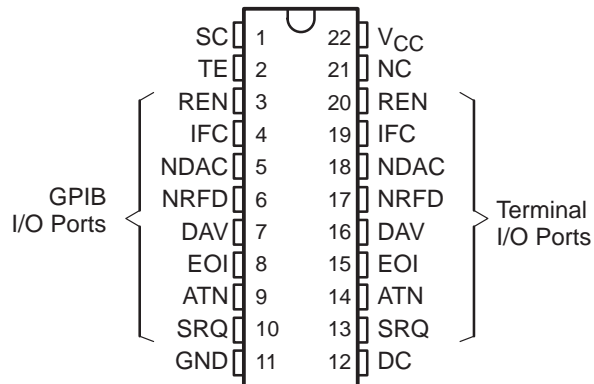
The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when $V_{CC} = 0$. The drivers are designed to handle loads up to 48 mA of sink current. Each receiver features pnp transistor inputs for high input impedance and hysteresis of 400 mV minimum for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

The SN75ALS162 is characterized for operation from 0°C to 70°C.

DW PACKAGE
(TOP VIEW)



N PACKAGE
(TOP VIEW)



NC—No internal connection



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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SN75ALS162 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

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RECEIVE/TRANSMIT FUNCTION TABLE

| CONTROLS | | | | BUS-MANAGEMENT CHANNELS | | | | DATA-TRANSFER CHANNELS | | | | |
|----------|----|----|------|----------------------------|-----|---------------------------|-----|------------------------|-----|------|----------------------------|---|
| SC | DC | TE | ATN† | ATN† (controlled by DC) | SRQ | REN (controlled by SC) | IFC | EOI | DAV | NDAC | NRFD (controlled by TE) | |
| | H | H | H | R | T | | | T | T | R | R | |
| | H | H | L | | | | | R | | | | |
| | L | L | H | T | R | | | R | R | T | T | T |
| | L | L | L | | | | | T | | | | |
| | H | L | X | R | T | | | R | R | T | T | |
| | L | H | X | T | R | | | T | T | R | R | |
| H | | | | | | T | T | | | | | |
| L | | | | | | R | R | | | | | |

H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side.

Data transfer is noninverting in both directions.

† ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

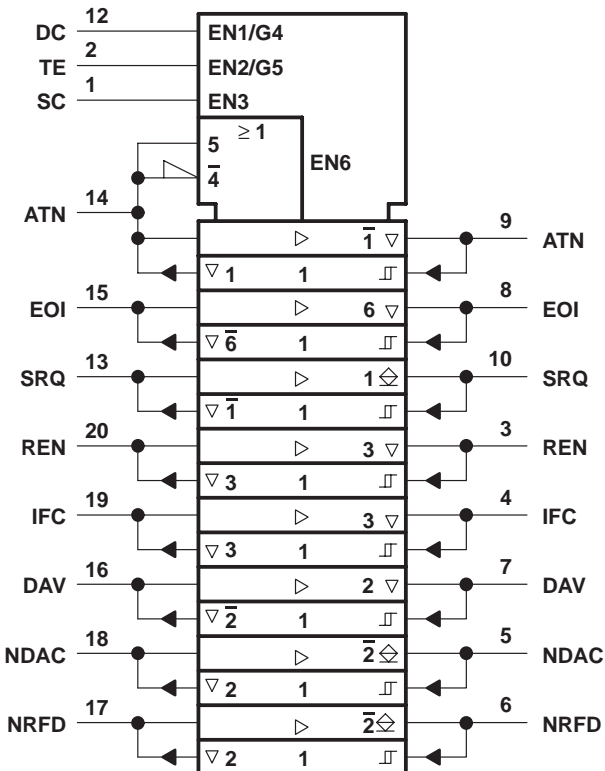
CHANNEL IDENTIFICATION TABLE

| NAME | IDENTITY | CLASS |
|------|--------------------|----------------|
| DC | Direction Control | Control |
| TE | Talk Enable | |
| SC | System Control | |
| ATN | Attention | Bus Management |
| SRQ | Service Request | |
| REN | Remote Enable | |
| IFC | Interface Clear | |
| EOI | End or Identify | |
| DAV | Data Valid | Data Transfer |
| NDAC | No Data Accepted | |
| NRFD | Not Ready for Data | |

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logic symbol†



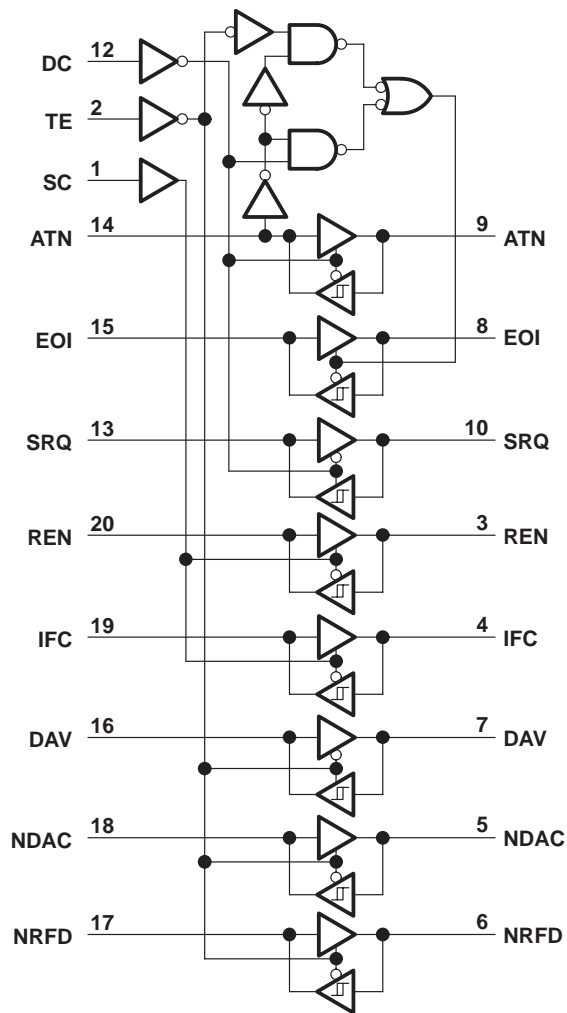
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

▽ Designates 3-state outputs

◇ Designates passive-pullup outputs

Pin numbers shown are for the N package.

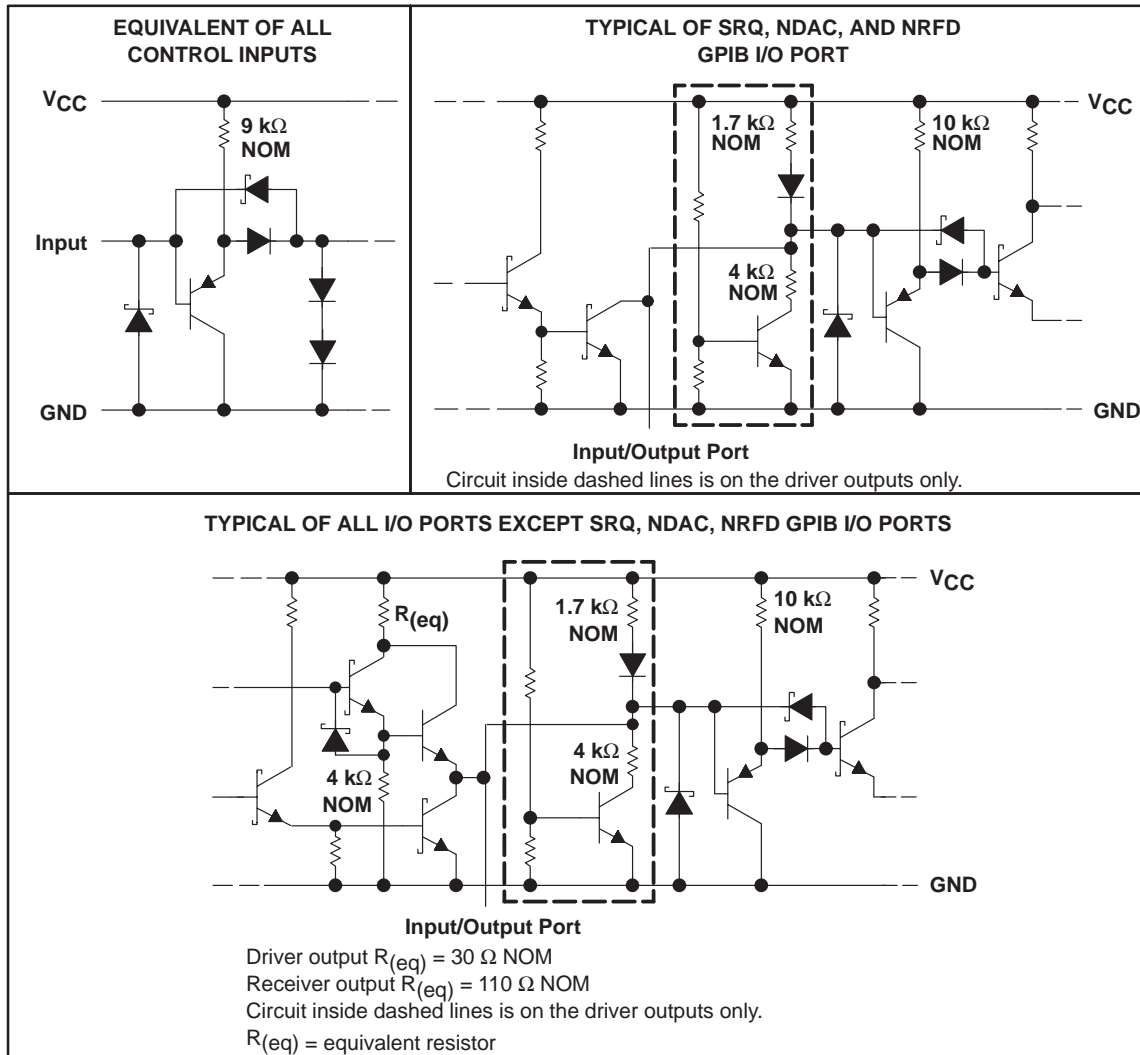
logic diagram (positive logic)



SN75ALS162 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|------------------------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage, V_I | 5.5 V |
| Low-level driver output current, I_{OL} | 100 mA |
| Continuous total dissipation | See Dissipation Rating Table |
| Operating free-air temperature range, T_A | 0°C to 70°C |
| Storage temperature range, T_{stg} | -65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds | 260°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal.

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OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

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DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR | $T_A = 70^\circ\text{C}$ POWER RATING |
|---------|---|-----------------|--|
| DW | 1350 mW | 10.8 mW/°C | 864 mW |
| N | 1700 mW | 13.6 mW/°C | 1088 mW |

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---------------------------------------|--------------------------------|------|-----|-------|---------------|
| Supply voltage, V_{CC} | | 4.75 | 5 | 5.25 | V |
| High-level input voltage, V_{IH} | | 2 | | | V |
| Low level input voltage, V_{IL} | | | | 0.8 | V |
| High-level output current, I_{OH} | Bus ports with 3-state outputs | | | – 5.2 | mA |
| | Terminal ports | | | – 800 | μA |
| Low-level output current, I_{OL} | Bus ports | | | 48 | mA |
| | Terminal ports | | | 16 | mA |
| Operating free-air temperature, T_A | | 0 | | 70 | °C |

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT | |
|-----------------------|---|--|---|--|-------|-------|---------------|--|
| V_{IK} | Input clamp voltage | $I_I = -18 \text{ mA}$ | | – 0.8 | – 1.5 | | V | |
| V_{hys} | Hysteresis voltage ($V_{IT+} - V_{IT-}$) | Bus | | 0.4 | 0.65 | | V | |
| V_{OH}^\ddagger | High-level output voltage | Terminal | $I_{OH} = -800 \mu\text{A}$ | 2.7 | 3.5 | | V | |
| | | Bus | $I_{OH} = -5.2 \text{ mA}$ | 2.5 | 3.3 | | V | |
| V_{OL} | Low-level output voltage | Terminal | $I_{OL} = 16 \text{ mA}$ | | 0.3 | 0.5 | V | |
| | | Bus | $I_{OL} = 48 \text{ mA}$ | | 0.35 | 0.5 | V | |
| I_I | Input current at maximum input voltage | Terminal | $V_I = 5.5 \text{ V}$ | | 0.2 | 100 | μA | |
| I_{IH} | High-level input current | Terminal and control inputs | $V_I = 2.7 \text{ V}$ | | 0.1 | 20 | μA | |
| I_{IL} | Low-level input current | | $V_I = 0.5 \text{ V}$ | | – 10 | – 100 | μA | |
| $V_{I/O}(\text{bus})$ | Voltage at bus port | Driver disabled | $I_I(\text{bus}) = 0$ | 2.5 | 3.0 | 3.7 | V | |
| | | | $I_I(\text{bus}) = -12 \text{ mA}$ | | | – 1.5 | | |
| $I_{I/O}(\text{bus})$ | Current into bus port | Power on | Driver disabled | $V_I(\text{bus}) = -1.5 \text{ V to } 0.4 \text{ V}$ | – 1.3 | | mA | |
| | | | | $V_I(\text{bus}) = 0.4 \text{ V to } 2.5 \text{ V}$ | 0 | – 3.2 | | |
| | | | | $V_I(\text{bus}) = 2.5 \text{ V to } 3.7 \text{ V}$ | | + 2.5 | – 3.2 | |
| | | | | $V_I(\text{bus}) = 3.7 \text{ V to } 5 \text{ V}$ | 0 | 2.5 | | |
| | | | | $V_I(\text{bus}) = 5 \text{ V to } 5.5 \text{ V}$ | 0.7 | 2.5 | | |
| | Power off | $V_{CC} = 0,$ | $V_I(\text{bus}) = 0 \text{ to } 2.5 \text{ V}$ | | | – 40 | μA | |
| I_{OS} | Short-circuit output current | Terminal | | – 15 | – 35 | – 75 | mA | |
| | | Bus | | – 25 | – 50 | – 125 | mA | |
| I_{CC} | Supply current | No load, TE, DC, and SC low | | 55 | 75 | | mA | |
| $C_{I/O}(\text{bus})$ | Bus-port capacitance | $V_{CC} = 0 \text{ to } 5 \text{ V}, V_{I/O} = 0 \text{ to } 2 \text{ V}, f = 1 \text{ MHz}$ | | 30 | | | pF | |

† All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

‡ V_{OH} applies to 3-state outputs only.



SN75ALS162

OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

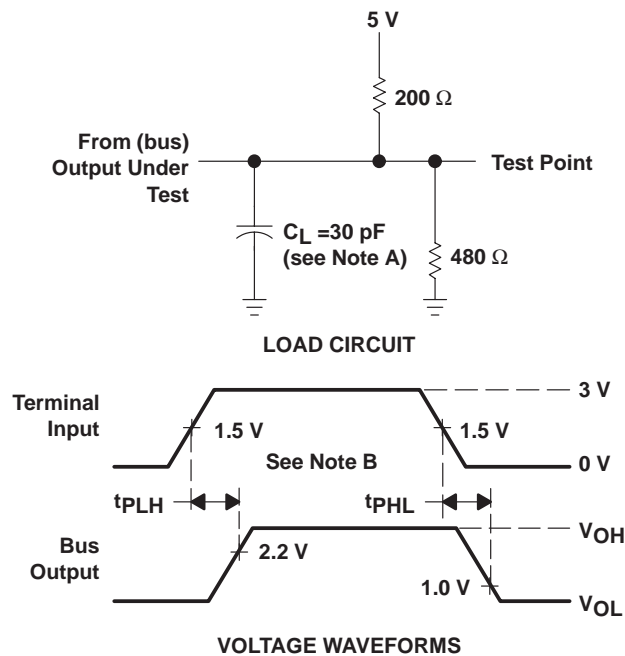
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switching characteristics over recommended range of operating free-air temperature, $V_{CC} = 5\text{ V}$

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|-----------|---|---------------|-----------------------------------|--|-----|------|-----|------|
| t_{PLH} | Propagation delay time, low- to high-level output | Terminal | Bus | $C_L = 30\text{ pF}$, See Figure 1 | 10 | 20 | ns | |
| t_{PHL} | Propagation delay time, high- to low-level output | | | | 12 | 20 | | |
| t_{PLH} | Propagation delay time, low- to high-level output | Bus | Terminal | $C_L = 30\text{ pF}$, See Figure 2 | 5 | 10 | ns | |
| t_{PHL} | Propagation delay time, high- to low-level output | | | | 7 | 14 | | |
| t_{PZH} | Output enable time to high level | TE, DC, or SC | Bus (ATN, EOI, REN, IFC, and DAV) | $C_L = 15\text{ pF}$, See Figure 3 | | | 30 | ns |
| t_{PHZ} | Output disable time from high level | | | | | | 20 | |
| t_{PZL} | Output enable time to low level | | | | | | 45 | |
| t_{PLZ} | Output disable time from low level | | | | | | 20 | |
| t_{PZH} | Output enable time to high level | TE, DC, or SC | Terminal | $C_L = 15\text{ pF}$, See Figure 4 | | | 30 | ns |
| t_{PHZ} | Output disable time from high level | | | | | | 25 | |
| t_{PZL} | Output enable time to low level | | | | | | 30 | |
| t_{PLZ} | Output disable time from low level | | | | | | 25 | |

† All typical values are at $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION

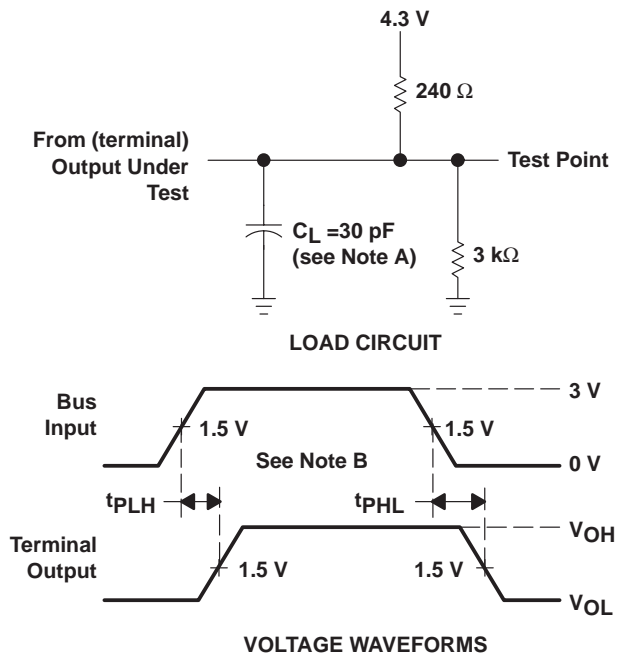


NOTES: A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1\text{ MHz}$, 50% duty cycle, $t_r \leq 6\text{ ns}$, $t_f \leq 6\text{ ns}$, $Z_O = 50\ \Omega$.

Figure 1. Terminal-to-Bus Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



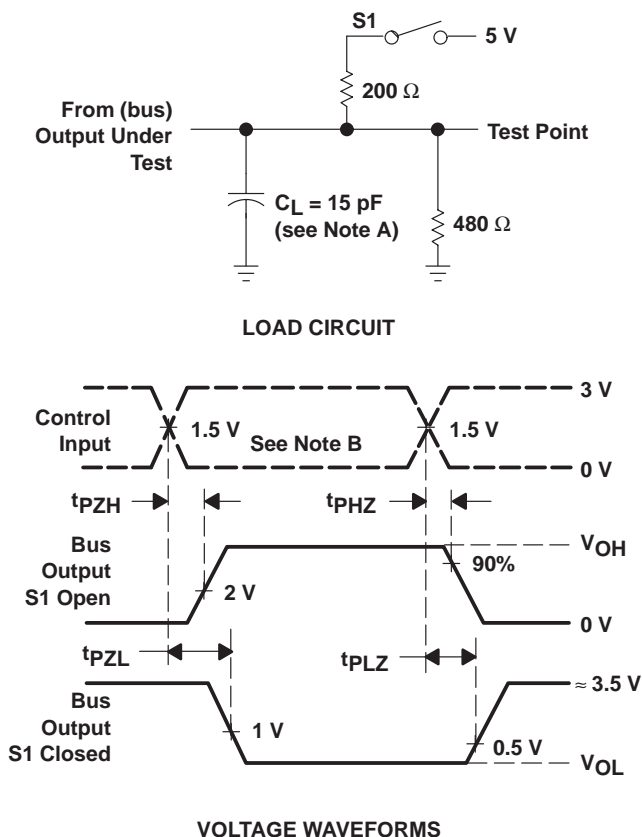
- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_O = 50 \Omega$.

Figure 2. Bus-to-Terminal Load Circuit and Voltage Waveforms

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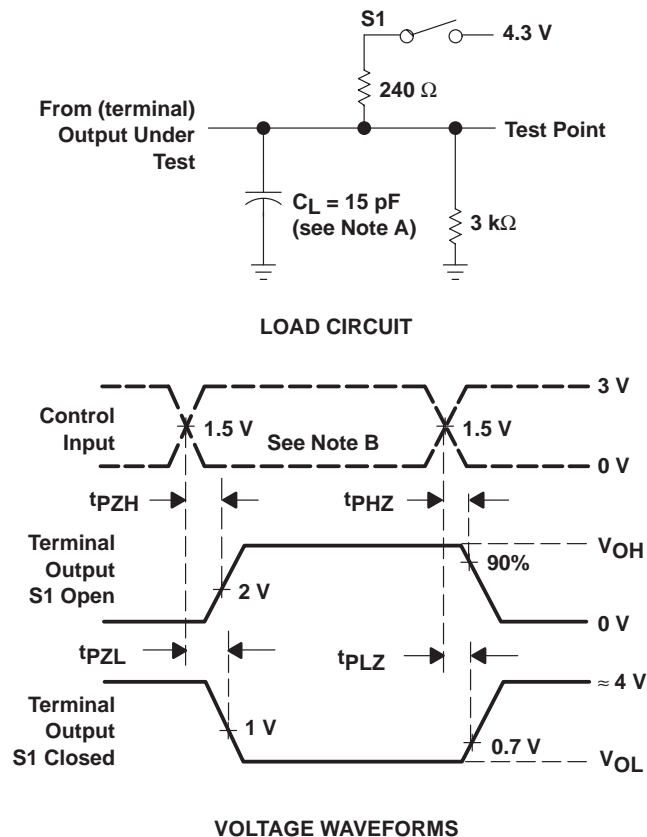
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

Figure 3. Bus Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

Figure 4. Terminal Load Circuit and Voltage Waveforms

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TYPICAL CHARACTERISTICS

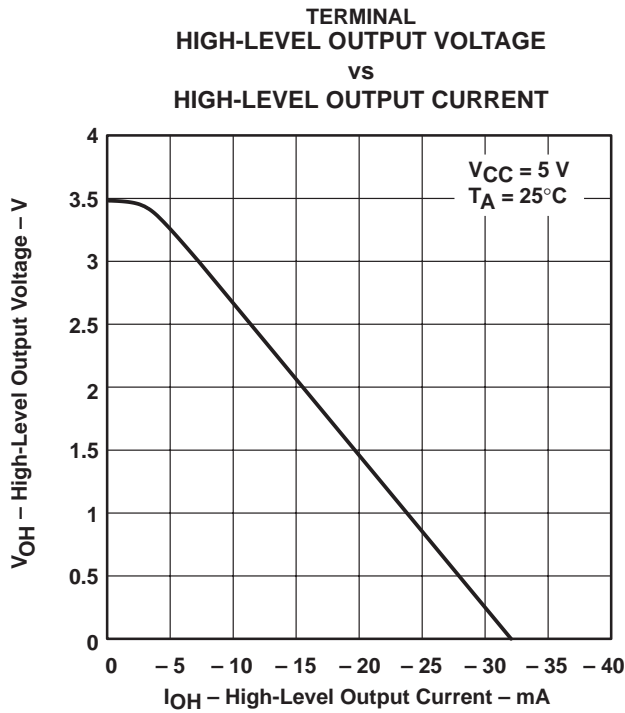


Figure 5

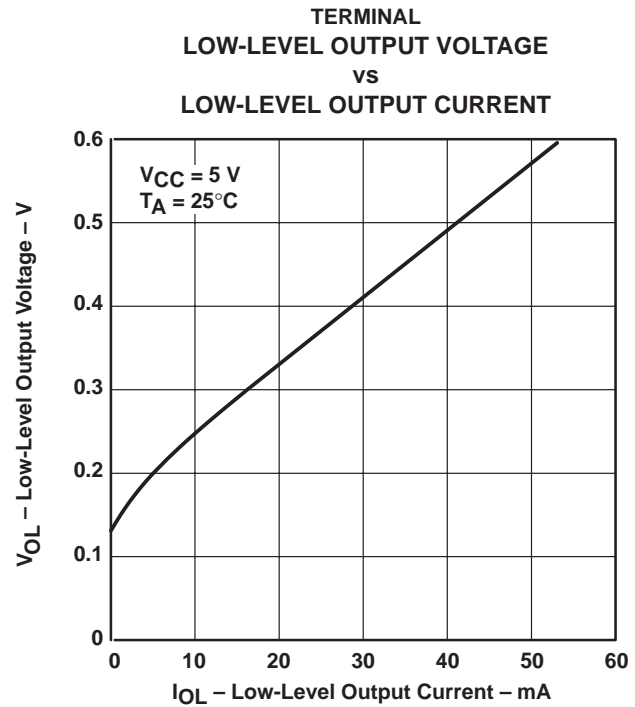


Figure 6

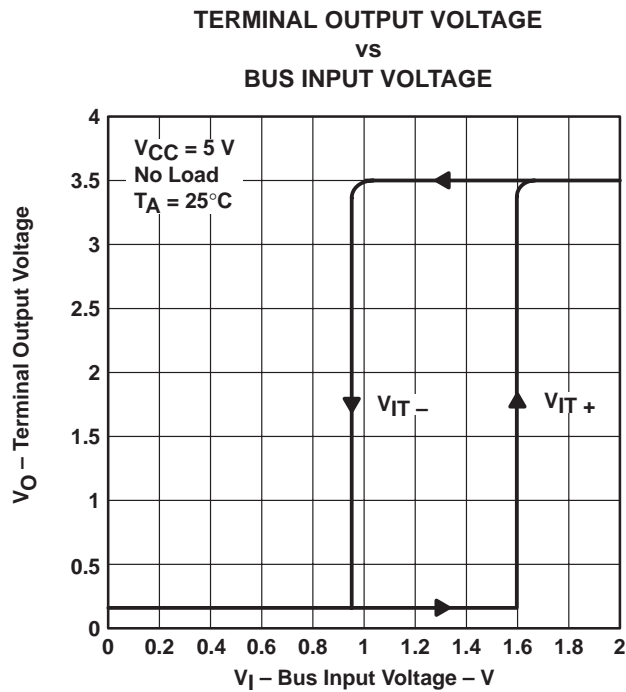


Figure 7



TYPICAL CHARACTERISTICS

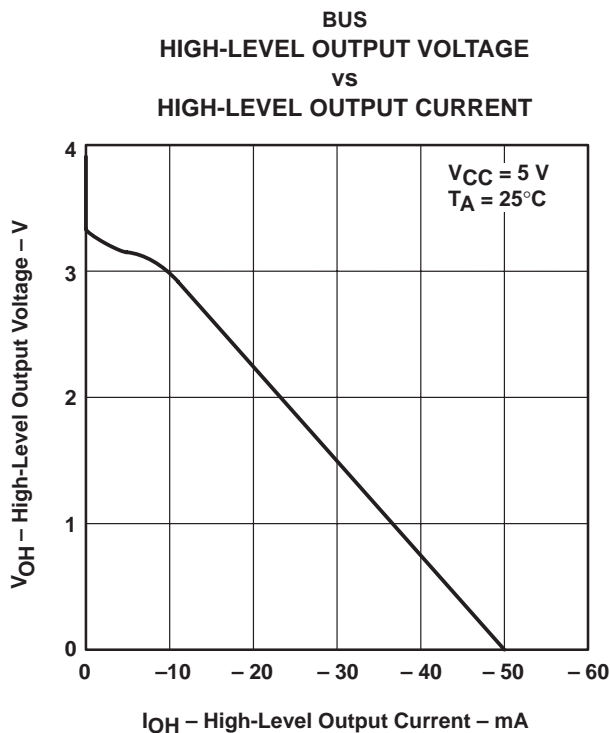


Figure 8

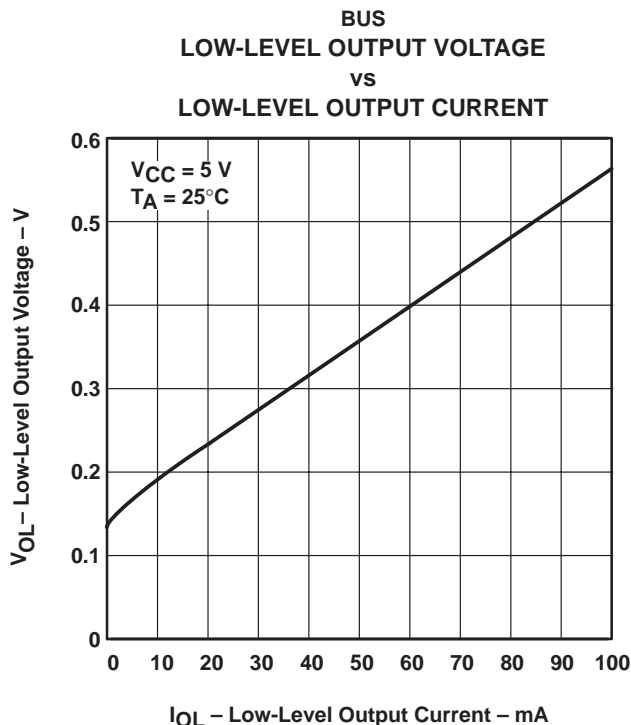


Figure 9

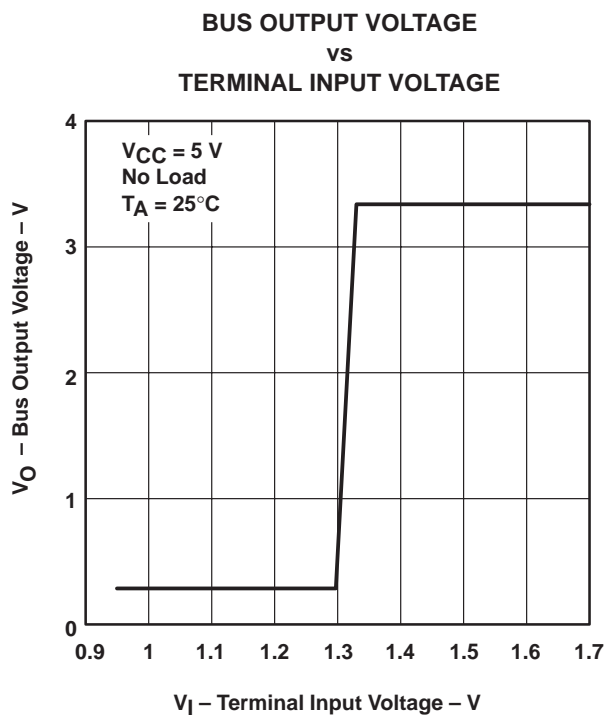


Figure 10

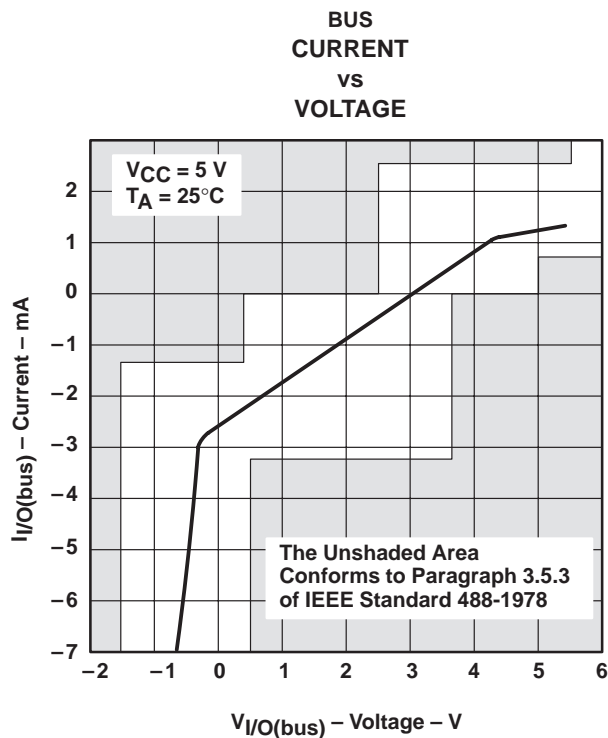


Figure 11

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN75ALS162DW | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75ALS162 | Samples |
| SN75ALS162DWE4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75ALS162 | Samples |
| SN75ALS162DWR | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75ALS162 | Samples |
| SN75ALS162DWRG4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75ALS162 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN75ALS162DWR | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN75ALS162DWR | SOIC | DW | 24 | 2000 | 350.0 | 350.0 | 43.0 |

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