



**THE DATASHEET OF  
74HC85PW,118**



# 74HC85; 74HCT85

## 4-bit magnitude comparator

Rev. 3 — 20 April 2018

Product data sheet

## 1 General description

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The 74HC85; 74HCT85 is a 4-bit magnitude comparator that can be expanded to almost any length. They perform comparison of two 4-bit binary, BCD or other monotonic codes and present the three possible magnitude results at the outputs ( $Q_{A>B}$ ,  $Q_{A=B}$  and  $Q_{A<B}$ ). The 4-bit inputs are weighted (A0 to A3 and B0 to B3), where A3 and B3 are the most significant bits. For proper compare operation the expander inputs ( $I_{A>B}$ ,  $I_{A=B}$  and  $I_{A<B}$ ) to the least significant position must be connected as follows:  $I_{A<B} = I_{A>B} = \text{LOW}$  and  $I_{A=B} = \text{HIGH}$ . For words greater than 4-bits, units can be cascaded by connecting outputs  $Q_{A>B}$ ,  $Q_{A=B}$  and  $Q_{A<B}$  to the corresponding inputs of the significant comparator. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

## 2 Features and benefits

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- Wide supply voltage range from 2.0 to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Input levels:
  - For 74HC85: CMOS level
  - For 74HCT85: TTL level
- Complies with JEDEC standard: no. 7A
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
  - HBM JESD22-A114-A exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

## 3 Applications

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- Process controllers
- Servo-motor control

## 4 Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC85D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT85D				
74HC85DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT85DB				
74HC85PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

## 5 Functional diagram

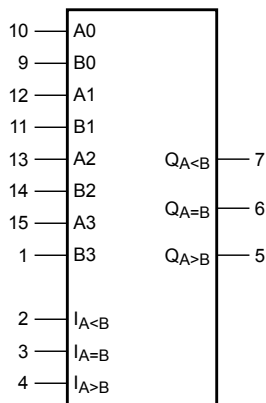


Figure 1. Logic symbol

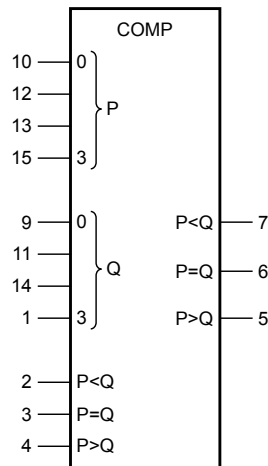


Figure 2. IEC logic symbol

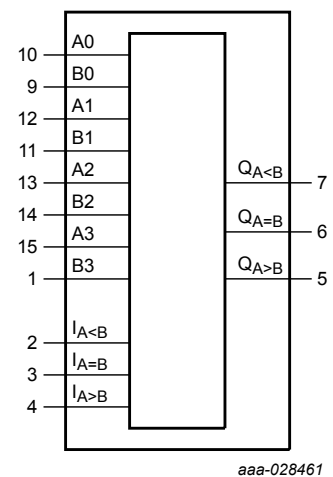
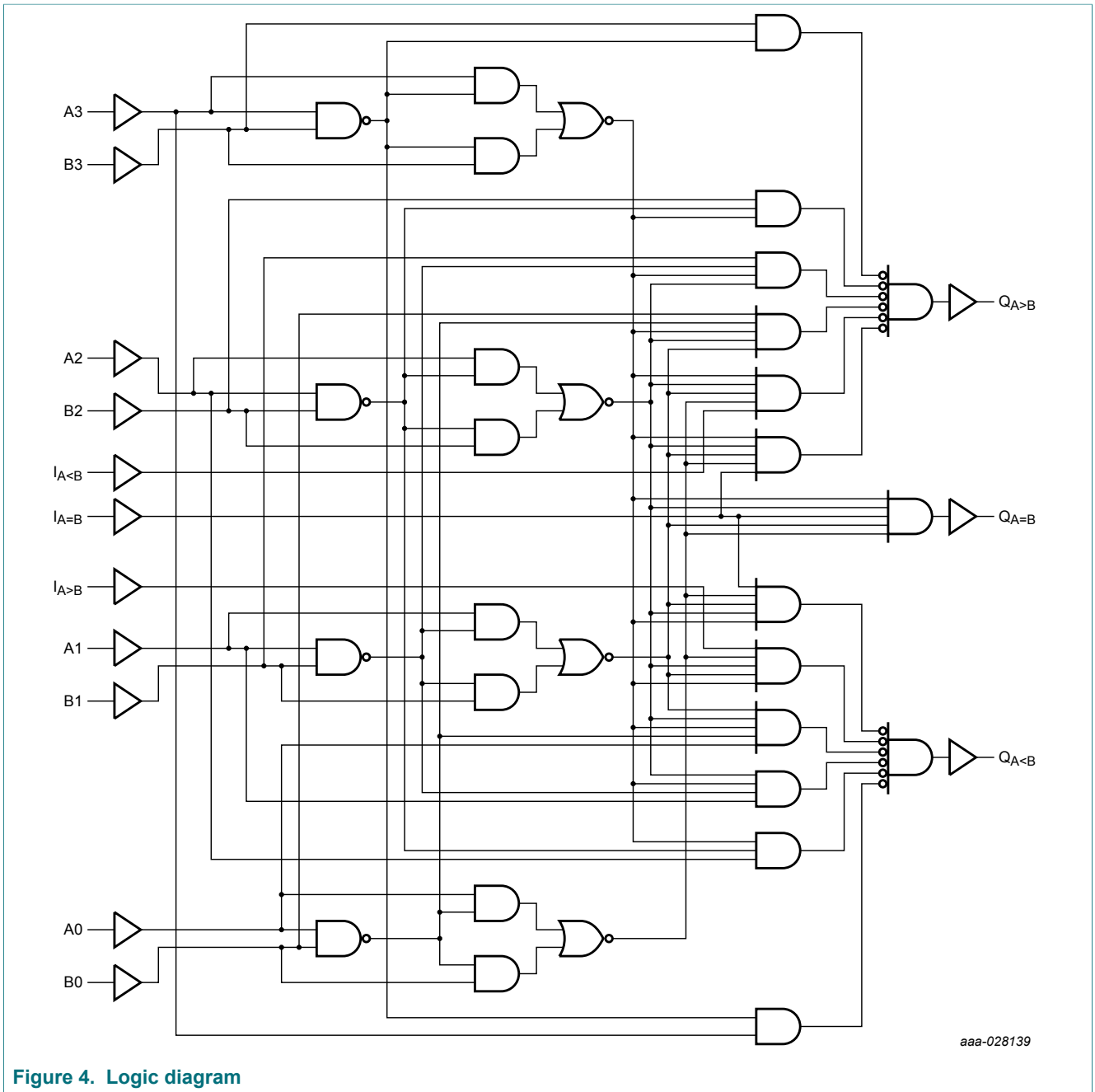
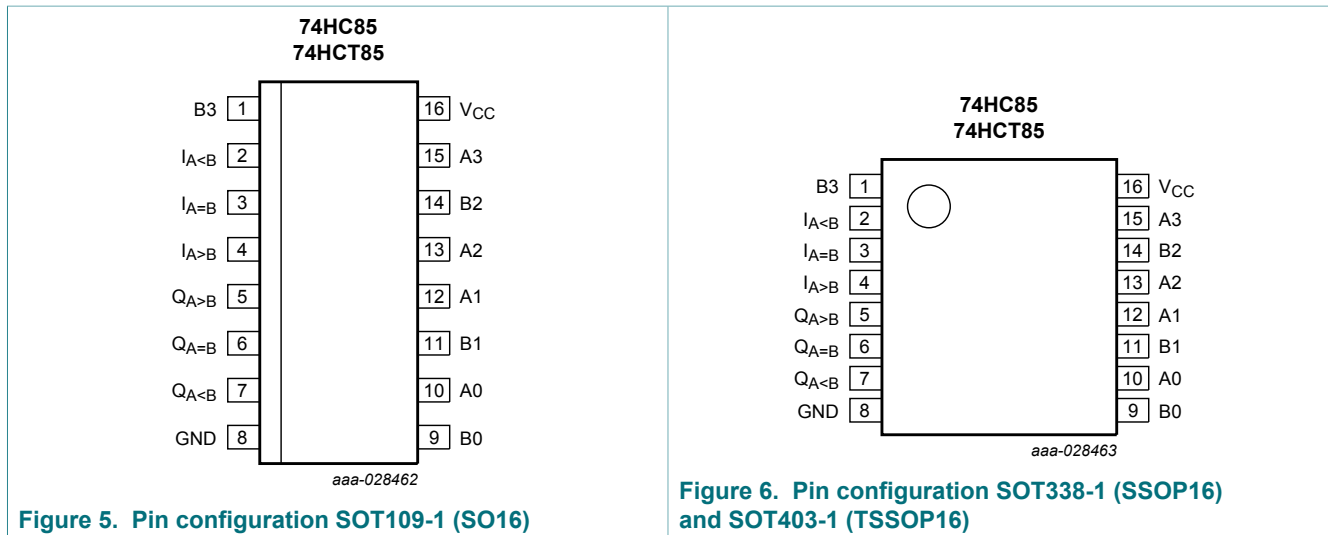


Figure 3. Functional diagram



## 6 Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$I_{A<B}$	2	A<B expansion input
$I_{A=B}$	3	A=B expansion input
$I_{A>B}$	4	A>B expansion input
$Q_{A>B}$	5	A>B output
$Q_{A=B}$	6	A=B output
$Q_{A<B}$	7	A<B output
A0 to A3	10, 12, 13, 15	word A inputs
B0 to B3	9, 11, 14, 1	word B inputs
GND	8	ground (0 V)
V <sub>CC</sub>	16	supply voltage

## 7 Functional description

**Table 3. Function table**

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Comparing inputs				Cascading inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	I <sub>A&gt;B</sub>	I <sub>A&lt;B</sub>	I <sub>A=B</sub>	Q <sub>A&gt;B</sub>	Q <sub>A&lt;B</sub>	Q <sub>A=B</sub>
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

## 8 Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V <sup>[1]</sup>	-	±20	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V <sup>[1]</sup>	-	±20	mA
I <sub>O</sub>	output current	-0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V	-	±25	mA
I <sub>CC</sub>	supply current		-	50	mA
I <sub>GND</sub>	ground current		-50	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C <sup>[2]</sup>	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO16 Packages: P<sub>tot</sub> derates linearly with 8 mW/K above 70 °C.

For (T)SSOP16 Packages: P<sub>tot</sub> derates linearly with 5.5 mW/K above 60 °C.

## 9 Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC85			74HCT85			Unit
			Min	Typ	Max	Min	Typ	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	-	+125	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.0 V	-	-	625	-	-	-	ns/V
		V <sub>CC</sub> = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V <sub>CC</sub> = 6.0 V	-	-	83	-	-	-	ns/V

## 10 Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC85</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I <sub>O</sub> = -5.2 mA; V <sub>CC</sub> = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$I_I$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu$ A
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	8.0	-	80	-	160	$\mu$ A
$C_I$	input capacitance		-	3.5	-	-	-	-	-	pF
<b>74HCT85</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5$ V								
		$I_O = -20$ $\mu$ A	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4.0$ mA	3.98	4.32	-	3.84	-	3.7	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5$ V								
		$I_O = 20$ $\mu$ A	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0$ mA	-	0.15	0.26	-	0.33	-	0.4	V
$I_I$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu$ A
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	8.0	-	80	-	160	$\mu$ A
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = V_{CC} - 2.1$ V; other inputs at $V_{CC}$ or GND; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A								
		$I_{A<B}$ and $I_{A>B}$ inputs	-	100	360	-	450	-	490	$\mu$ A
		$A_n$ , $B_n$ and $I_{A=B}$ inputs	-	150	540	-	675	-	735	$\mu$ A
$C_I$	input capacitance		-	3.5	-	-	-	-	-	pF

## 11 Dynamic characteristics

**Table 7. Dynamic characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);

$C_L = 50$  pF unless otherwise specified; for test circuit, see [Figure 8](#)

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit	
			Min	Typ	Max	Min	Max	Min	Max		
<b>74HC85</b>											
$t_{pd}$	propagation delay	An, Bn to $Q_{A>B}$ ; An, Bn to $Q_{A<B}$ ; see <a href="#">Figure 7</a>	[1]								
		$V_{CC} = 2.0$ V	-	63	195	-	245	-	295	ns	
		$V_{CC} = 4.5$ V	-	23	39	-	49	-	59	ns	
		$V_{CC} = 6.0$ V	-	18	33	-	42	-	50	ns	
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	20	-	-	-	-	-	ns	
		An, Bn to $Q_{A=B}$ ; see <a href="#">Figure 7</a>									
		$V_{CC} = 2.0$ V	-	58	175	-	220	-	265	ns	
		$V_{CC} = 4.5$ V	-	21	35	-	44	-	53	ns	
		$V_{CC} = 6.0$ V	-	17	30	-	37	-	45	ns	
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	18	-	-	-	-	-	ns	
		$I_{A=B}$ or $I_{A>B}$ to $Q_{A<B}$ ; $I_{A<B}$ or $I_{A=B}$ to $Q_{A>B}$ ; see <a href="#">Figure 7</a>									
		$V_{CC} = 2.0$ V	-	50	140	-	175	-	210	ns	
		$V_{CC} = 4.5$ V	-	18	28	-	35	-	42	ns	
		$V_{CC} = 6.0$ V	-	14	24	-	30	-	36	ns	
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	15	-	-	-	-	-	ns	
		$I_{A=B}$ to $Q_{A=B}$ ; see <a href="#">Figure 7</a>									
$V_{CC} = 2.0$ V	-	39	120	-	150	-	180	ns			
$V_{CC} = 4.5$ V	-	14	24	-	30	-	36	ns			
$V_{CC} = 6.0$ V	-	11	20	-	26	-	31	ns			
$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	11	-	-	-	-	-	ns			
$t_t$	transition time	see <a href="#">Figure 7</a>	[2]								
		$V_{CC} = 2.0$ V	-	19	75	-	95	-	110	ns	
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns	
		$V_{CC} = 6.0$ V	-	6	13	-	16	-	19	ns	
$C_{PD}$	power dissipation capacitance	per package; $V_I = \text{GND}$ to $V_{CC}$	[3]	-	18	-	-	-	-	pF	

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HCT85</b>										
$t_{pd}$	propagation delay	An, Bn to $Q_{A>B}$ ; [1] An, Bn to $Q_{A<B}$ ; see <a href="#">Figure 7</a>								
		$V_{CC} = 4.5\text{ V}$	-	26	44	-	55	-	66	ns
		$V_{CC} = 5.0\text{ V}; C_L = 15\text{ pF}$	-	22	-	-	-	-	-	ns
		An, Bn to $Q_{A=B}$ ; see <a href="#">Figure 7</a>								
		$V_{CC} = 4.5\text{ V}$	-	24	40	-	50	-	60	ns
		$V_{CC} = 5.0\text{ V}; C_L = 15\text{ pF}$	-	20	-	-	-	-	-	ns
		$I_{A=B}$ or $I_{A>B}$ to $Q_{A<B}$ ; $I_{A<B}$ or $I_{A=B}$ to $Q_{A>B}$ ; see <a href="#">Figure 7</a>								
		$V_{CC} = 4.5\text{ V}$	-	18	31	-	39	-	47	ns
		$V_{CC} = 5.0\text{ V}; C_L = 15\text{ pF}$	-	15	-	-	-	-	-	ns
		$I_{A=B}$ to $Q_{A=B}$ ; see <a href="#">Figure 7</a>								
$V_{CC} = 4.5\text{ V}$	-	18	31	-	39	-	47	ns		
$V_{CC} = 5.0\text{ V}; C_L = 15\text{ pF}$	-	15	-	-	-	-	-	ns		
$t_t$	transition time	$V_{CC} = 4.5\text{ V}$ ; see <a href="#">Figure 7</a> [2]	-	7	15	-	19	-	22	ns
$C_{PD}$	power dissipation capacitance	per package; $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$ [3]	-	20	-	-	-	-	-	pF

[1]  $t_{pd}$  is the same as  $t_{PHL}$  and  $t_{PLH}$ .

[2]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

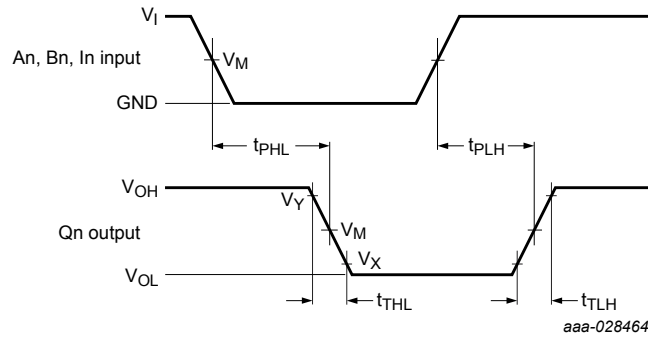
$f_o$  = output frequency in MHz;

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V.

11.1 Waveforms and test circuit



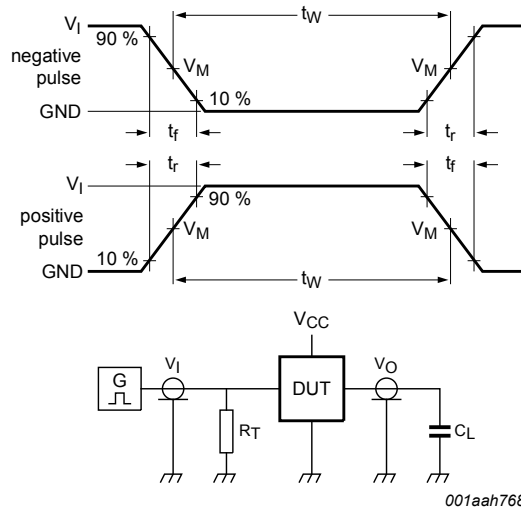
Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

Figure 7. Word A inputs (An), word B inputs (Bn) and expansion inputs (In) to the outputs (Qn) propagation delays and the output transition times

Table 8. Measurement points

Type	Input		Output		
	$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
74HC85	$V_{CC}$	$0.5V_{CC}$	$0.5V_{CC}$	$0.1 V_{CC}$	$0.9 V_{CC}$
74HCT85	3 V	1.3 V	1.3 V	$0.1 V_{CC}$	$0.9 V_{CC}$



Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = load capacitance including jig and probe capacitance.

Figure 8. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	$V_I$	$t_r, t_f$	$C_L$	
74HC85	$V_{CC}$	6.0 ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$
74HCT85	3.0 V	6.0 ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$

## 12 Application information

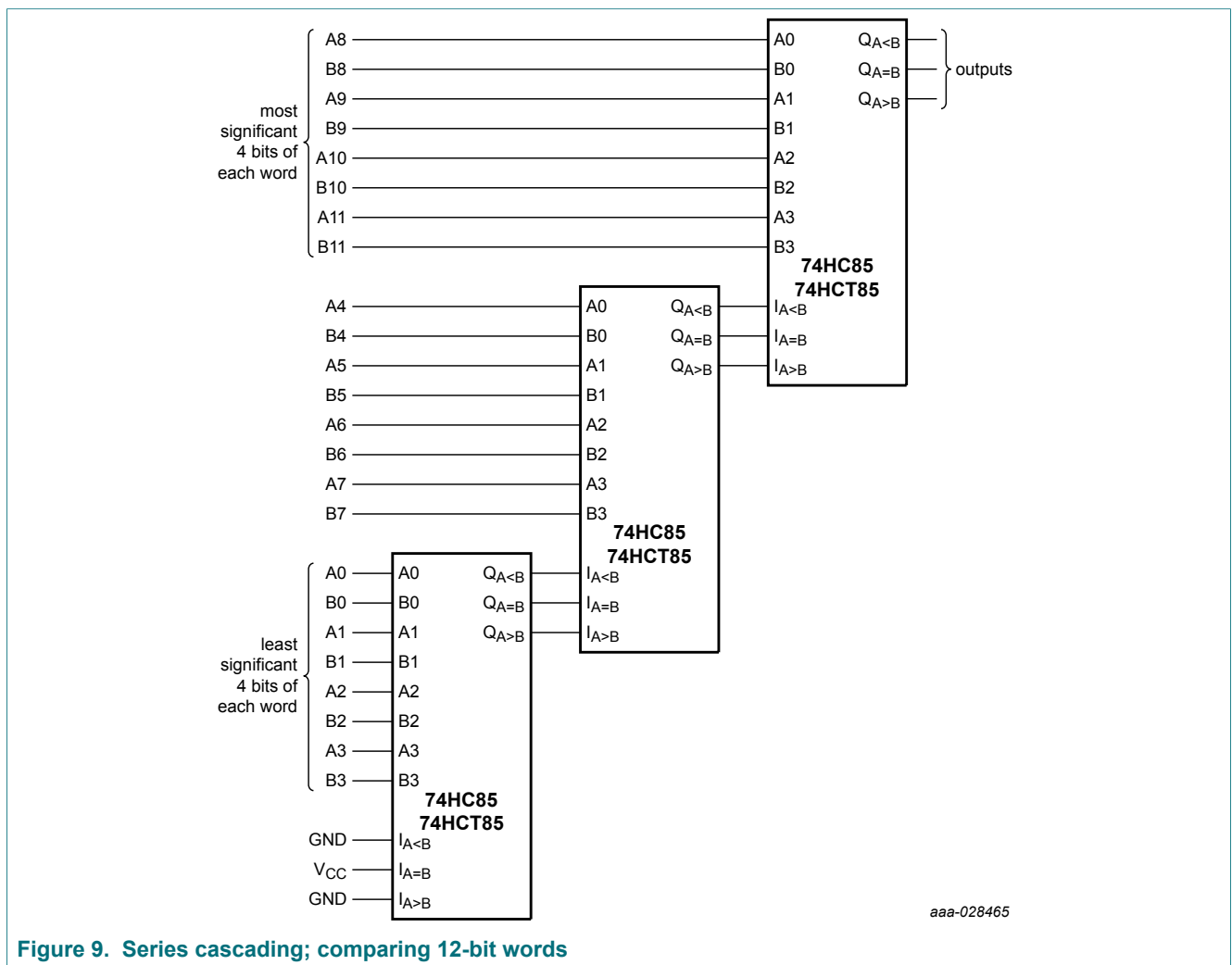


Figure 9. Series cascading; comparing 12-bit words

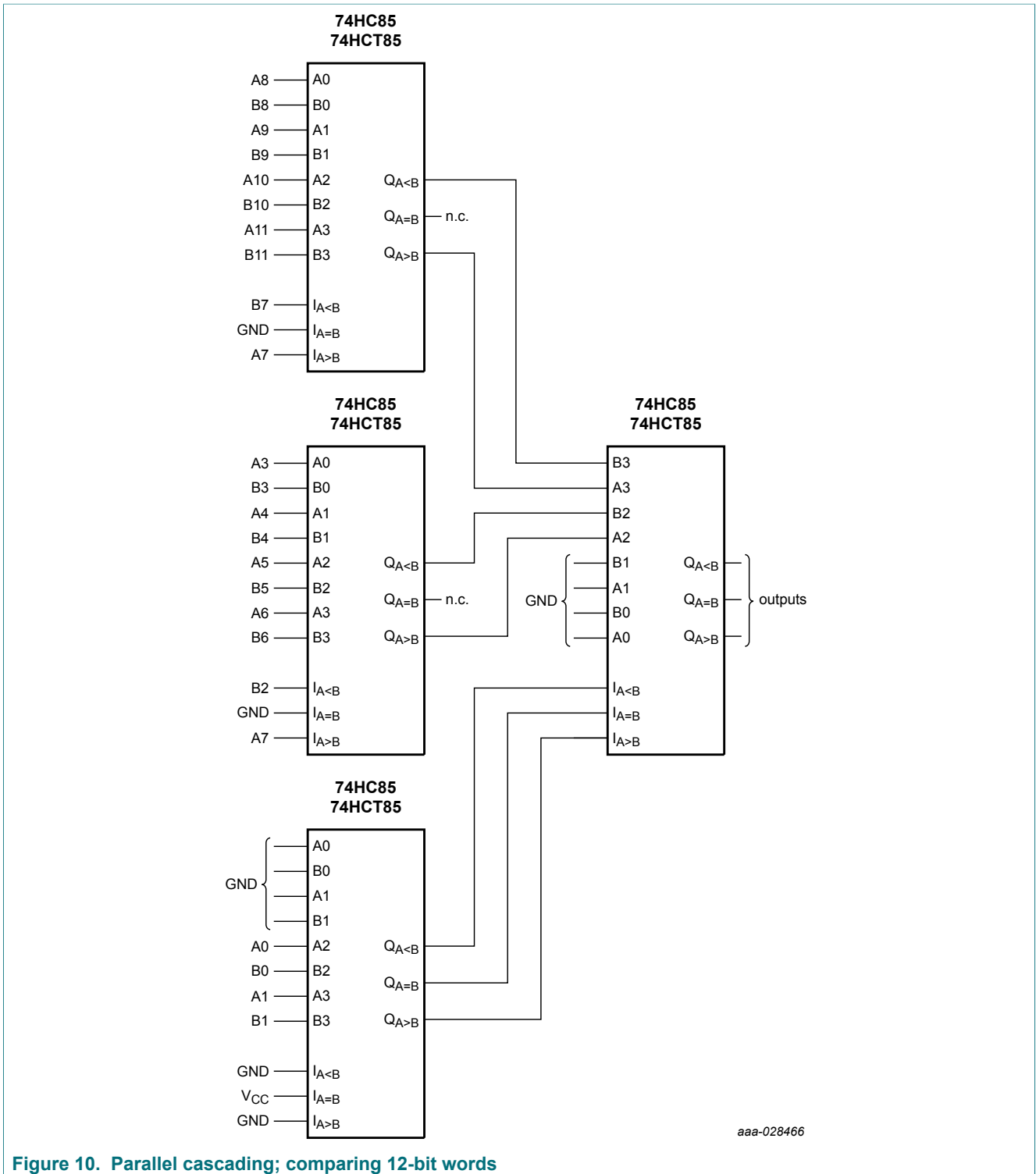


Figure 10. Parallel cascading; comparing 12-bit words

13 Package outline

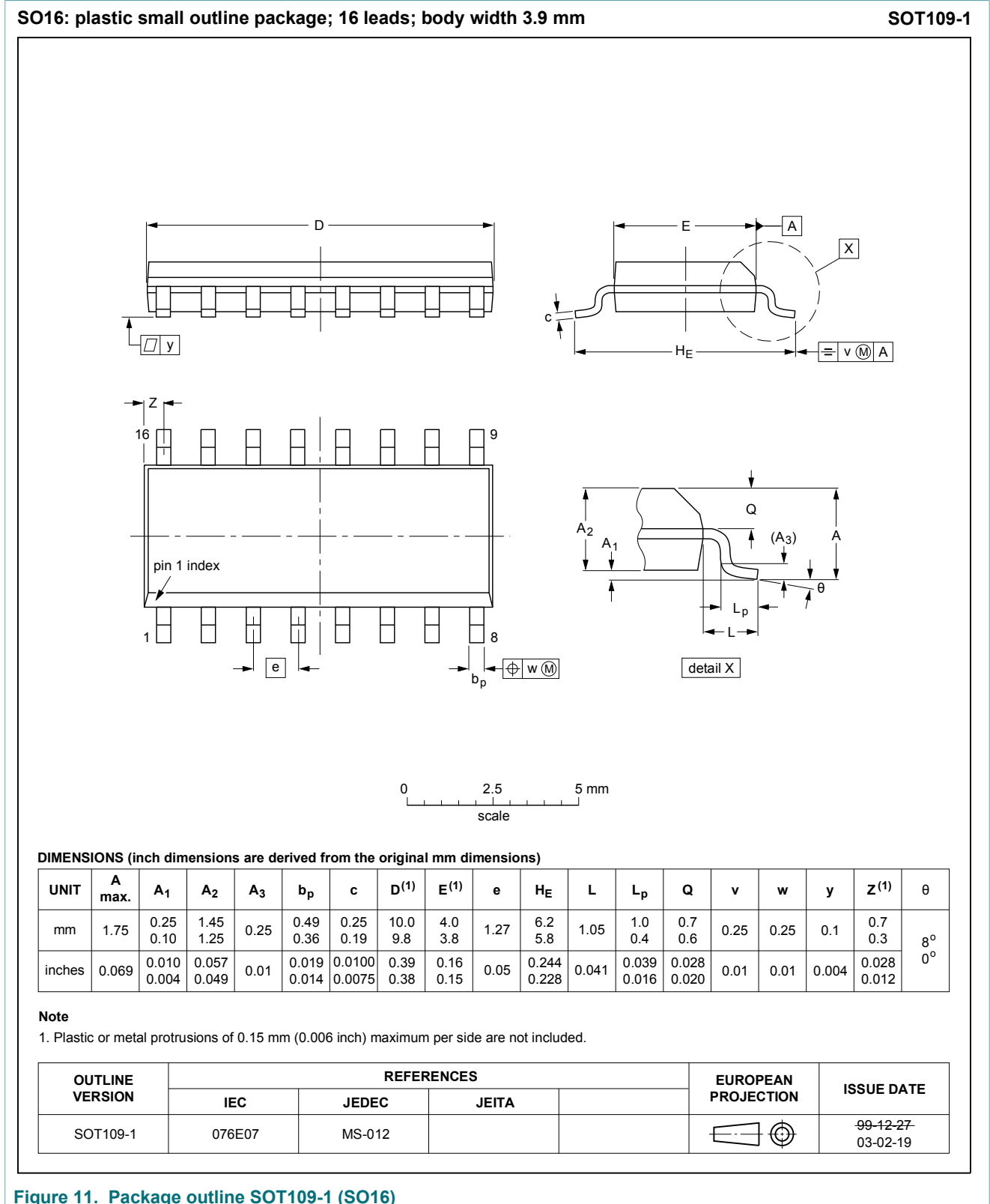
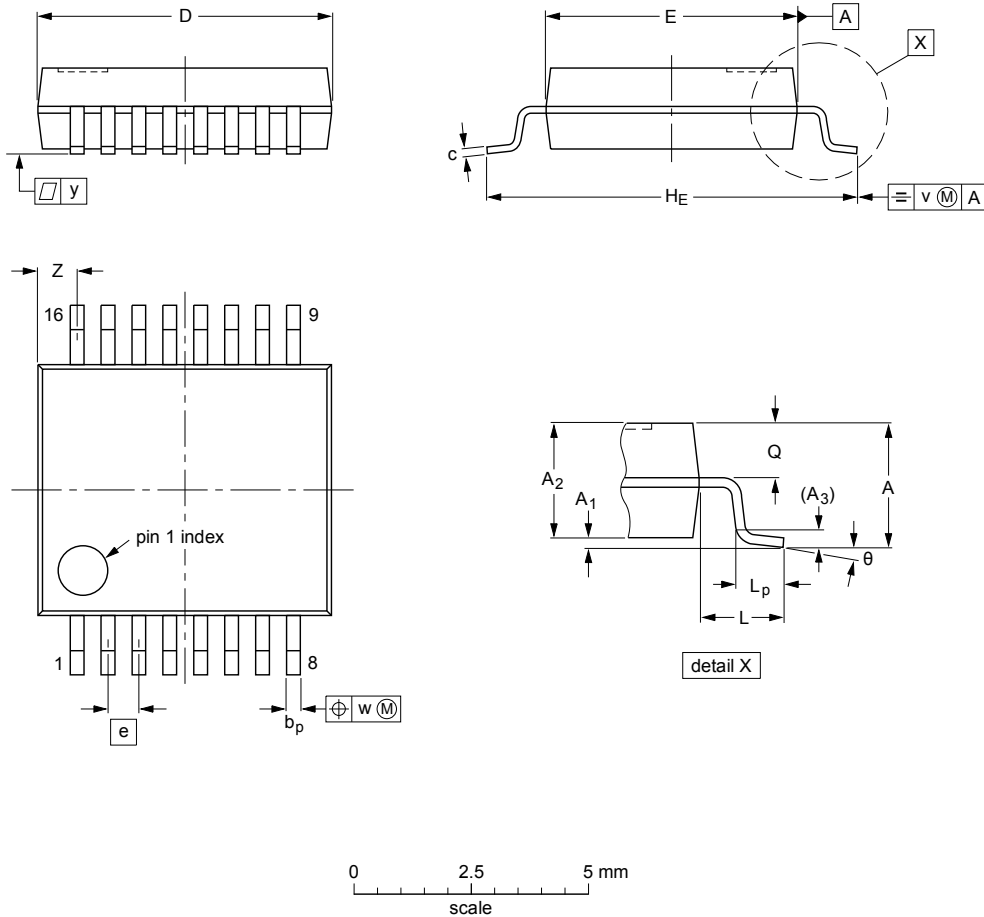


Figure 11. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

**Note**

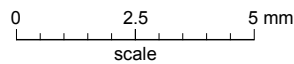
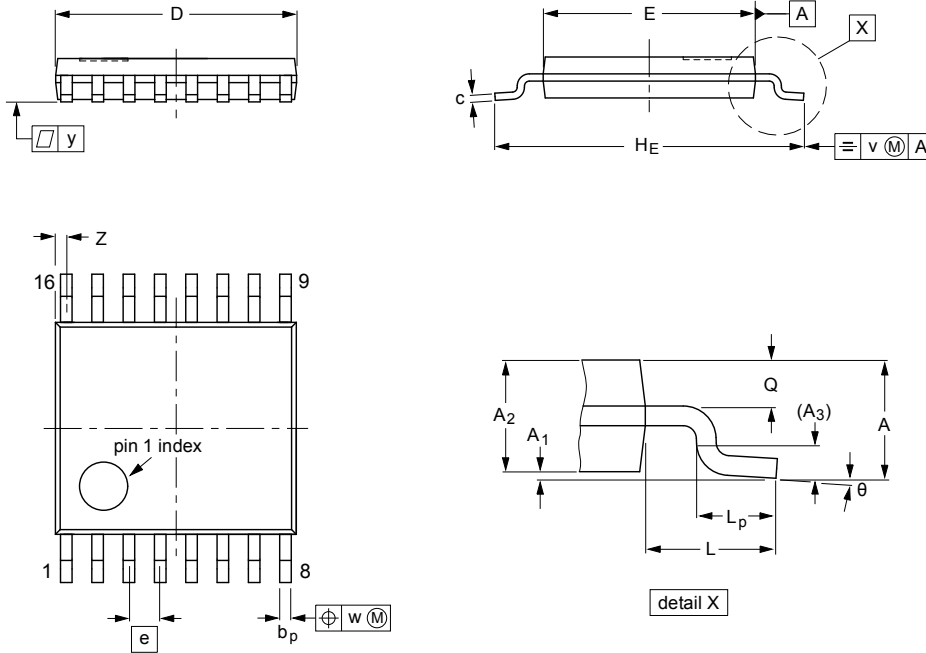
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				99-12-27 03-02-19

Figure 12. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				-99-12-27 03-02-18

Figure 13. Package outline SOT403-1 (TSSOP16)

## 14 Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 15 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT85 v.3	20180420	Product data sheet	-	74HC_HCT85 v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74HC_HCT85 v.2	19901201	Product specification	-	74HC_HCT85 v.1
74HC_HCT85 v.1	19901201	Product specification	-	-

## 16 Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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**Contents**

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<b>1</b>	<b>General description .....</b>	<b>1</b>
<b>2</b>	<b>Features and benefits .....</b>	<b>1</b>
<b>3</b>	<b>Applications .....</b>	<b>1</b>
<b>4</b>	<b>Ordering information .....</b>	<b>2</b>
<b>5</b>	<b>Functional diagram .....</b>	<b>2</b>
<b>6</b>	<b>Pinning information .....</b>	<b>4</b>
6.1	Pinning .....	4
6.2	Pin description .....	4
<b>7</b>	<b>Functional description .....</b>	<b>5</b>
<b>8</b>	<b>Limiting values .....</b>	<b>5</b>
<b>9</b>	<b>Recommended operating conditions .....</b>	<b>6</b>
<b>10</b>	<b>Static characteristics .....</b>	<b>6</b>
<b>11</b>	<b>Dynamic characteristics .....</b>	<b>8</b>
11.1	Waveforms and test circuit .....	10
<b>12</b>	<b>Application information .....</b>	<b>11</b>
<b>13</b>	<b>Package outline .....</b>	<b>13</b>
<b>14</b>	<b>Abbreviations .....</b>	<b>16</b>
<b>15</b>	<b>Revision history .....</b>	<b>16</b>
<b>16</b>	<b>Legal information .....</b>	<b>17</b>

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