



**THE DATASHEET OF  
SN75172N**



# SN75172 Quadruple Differential Line Driver

## 1 Features

- Meets or exceeds the requirements of ANSI standards EIA/TIA-422-B and RS-485 and ITU recommendation V.11
- Designed for multipoint transmission on long bus lines in noisy environments
- 3-state outputs
- Common-mode output voltage range of: -7V to 12V
- Active-high and active-low enables
- Thermal shutdown protection
- Positive- and negative-current limiting
- Operates from single 5V supply
- Logically interchangeable with AM26LS31

## 2 Applications

- Chemical and gas sensors
- **Field transmitters:** temperature sensors and pressure sensors
- **Motor drives:** brushless DC and brushed DC
- **Temperature sensors** and controllers using modbus

## 3 Description

The SN75172 is a monolithic quadruple differential line driver with 3-state outputs. Designed to meet the

requirements of ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendation V.11. The device is optimized for balanced multipoint bus transmission at rates of up to 4 megabaud. Each driver features wide positive and negative common-mode output voltage ranges, making it suitable for party-line applications in noisy environments.

The SN75172 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C. This device offers optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

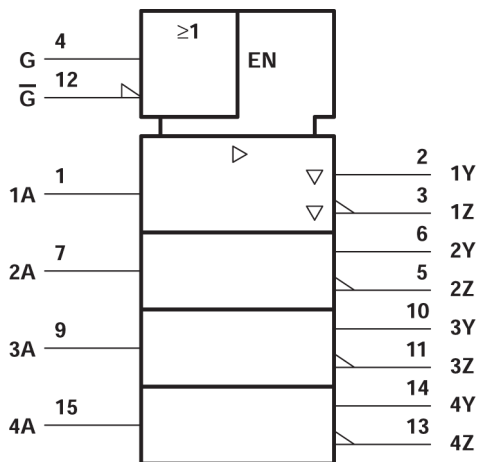
The SN75172 is characterized for operation from 0°C to 70°C.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
SN75172	N (PDIP, 16)	19.3mm × 9.4mm
	DW (SOIC, 20)	12.8mm × 10.3mm

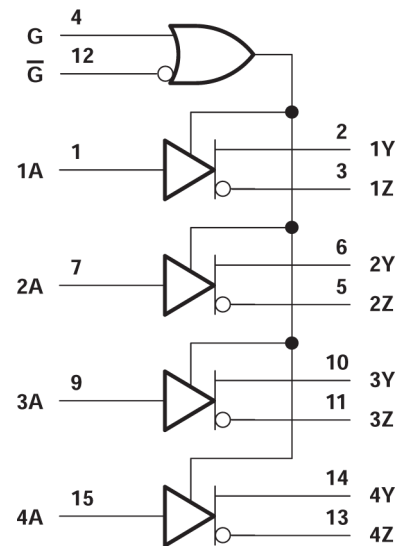
(1) For more information, see [Section 11](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



A. Pin numbers shown are for the N package.

**Logic Symbol<sup>1</sup>**



**Logic Diagram (Positive Logic)**

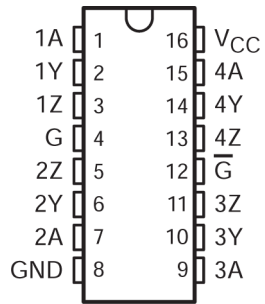
<sup>1</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



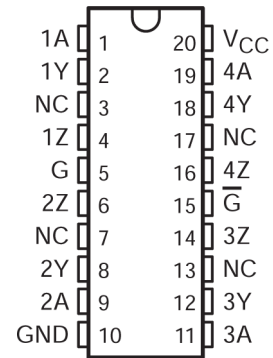
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## 4 Pin Configuration and Functions



**Figure 4-1. N Package (Top View)**



NC – No internal connection

**Figure 4-2. DW Package (Top View)**

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage, see <sup>(2)</sup>	-0.3	7	V
$V_{BUS}$	Voltage range at any bus terminal	-10	15	V
$V_I$	Input voltage	-0.3	5.5	V
$P_D$	Continuous total dissipation	See Dissipation Rating Table		
$T_A$	Operating free-air temperature range	0	70	°C
$T_{stg}$	Storage temperature range	-65	150	°C
$T_{LEAD}$	Lead temperature 1,6 mm (1/16 inch) from case for 10		260	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the network ground terminal.

### 5.2 Dissipation Ratings

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
DW	1125mW	9mW/°C	720mW
N	1150mW	9.2mW/°C	736mW

### 5.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$	4.75	5	5.25	V
High-level input voltage, $V_{IH}$	2			V
Low-level input voltage, $V_{IL}$			0.8	V
Common-mode output voltage, $V_{OC}$	-7		12	V
High-level output current, $I_{OH}$			-60	mA
Low-level output current, $I_{OL}$			60	mA
Operating free-air temperature, $T_A$	0		70	°C

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		N (PDIP)	DW	UNIT
		16 PINS	20 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	60.6	66.8	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	48.1	34.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	40.6	39.7	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	27.5	8.9	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	40.3	39	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IK</sub>	Input clamp voltage	I <sub>I</sub> = ±18mA					±1.5	V
V <sub>O</sub>	Output voltage	I <sub>O</sub> = 0			0		6	V
V <sub>OH</sub>	High-level output voltage	V <sub>IH</sub> = 2V,	V <sub>IL</sub> = 0.8V,	I <sub>OH</sub> = ±33mA		3.7		V
V <sub>OL</sub>	Low-level output voltage	V <sub>IH</sub> = 2V,	V <sub>IL</sub> = 0.8V,	I <sub>OH</sub> = 33mA		1.1		V
V <sub>OD1</sub>	Differential output voltage	I <sub>O</sub> = 0			1.5		6	V
V <sub>OD2</sub>	Differential output voltage	R <sub>L</sub> = 100Ω,	See Figure 6-1		1/2 V <sub>OD1</sub> or 2 <sup>(2)</sup>			V
		R <sub>L</sub> = 54Ω,	See Figure 6-1		1.5	1.5	5	V
V <sub>OD3</sub>	Differential output voltage	See <sup>(5)</sup>			1.5		5	V
Δ V <sub>OD</sub>	Change in magnitude of differential output voltage <sup>(3)</sup>						±0.2	V
V <sub>OC</sub>	Common-mode output voltage <sup>(4)</sup>	R <sub>L</sub> = 54Ω or 100Ω		See Figure 6-1	-1		3	V
Δ V <sub>OC</sub>	Change in magnitude of common-mode output voltage <sup>(3)</sup>						±0.2	V
I <sub>O</sub>	Output current with power off	V <sub>CC</sub> = 0	V <sub>O</sub> = ±7V to 12V				±100	μA
I <sub>OZ</sub>	High-impedance-state output current	V <sub>O</sub> = ±7V to 12V					±100	μA
I <sub>IH</sub>	High-level input current	V <sub>I</sub> = 1.7V					20	μA
I <sub>IL</sub>	Low-level input current	V <sub>I</sub> = 0.5V					±360	μA
I <sub>OS</sub>	Short-circuit output current	V <sub>O</sub> = ±7V					±180	mA
		V <sub>O</sub> = V <sub>CC</sub>					180	
		V <sub>O</sub> = 12V					500	
I <sub>CC</sub>	Supply current (all drivers)	No load	Outputs enabled			38	60	mA
			Outputs disabled			18	40	

(1) All typical values are at V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C.

(2) The minimum V<sub>OD2</sub> with a 100Ω load is either 1/2 V<sub>OD1</sub> or 2V, whichever is greater.

(3) Δ|V<sub>OD</sub>| and Δ|V<sub>OC</sub>| are the changes in magnitude of V<sub>OD</sub> and V<sub>OC</sub>, respectively, that occur when the input is changed from a high level to a low level.

(4) In ANSI Standard EIA/TIA-422-B, V<sub>OC</sub>, which is the average of the two output voltages with respect to ground, is called output offset voltage, V<sub>OS</sub>.

(5) See Figure 6-3 of EIA Standard RS-485.

**Table 5-1. Symbol Equivalents**

DATA SHEET PARAMETER	EIA/TIA-422-B	RS-485
$V_O$	$V_{oa}, V_{ob}$	$V_{oa}, V_{ob}$
$ V_{OD1} $	$V_o$	$V_o$
$ V_{OD2} $	$V_t (R_L = 100\Omega)$	$V_t (R_L = 54\Omega)$
$ V_{OD2} $		$V_t$ (Test Termination Measurement <sup>(5)</sup> )
$\Delta V_{OD} $	$  V_t  -  \bar{V}_t  $	$  V_t  -  \bar{V}_t  $
$V_{OC}$	$ V_{os} $	$ V_{os} $
$\Delta V_{OC} $	$ V_{os} - \bar{V}_{os} $	$ V_{os} - \bar{V}_{os} $
$I_{OS}$	$ I_{sa} ,  I_{sb} $	
$I_O$	$ I_{xa} ,  I_{xb} $	$I_{ia}, I_{ib}$

## 5.6 Switching Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	$R_L = 54\Omega$ ,	See <a href="#">Figure 6-2</a>		45	65	ns
$t_{t(OD)}$	Differential-output transition time				80	120	ns
$t_{PZH}$	Output enable time to high level	$R_L = 110\Omega$ ,	See <a href="#">Figure 6-3</a>		80	120	ns
$t_{PZL}$	Output enable time to low level	$R_L = 110\Omega$ ,	See <a href="#">Figure 6-4</a>		45	80	ns
$t_{PHZ}$	Output disable time from high level	$R_L = 110\Omega$ ,	See <a href="#">Figure 6-3</a>		78	115	ns
$t_{PLZ}$	Output disable time from low level	$R_L = 110\Omega$ ,	See <a href="#">Figure 6-4</a>		18	30	ns

### 5.7 Typical Characteristics

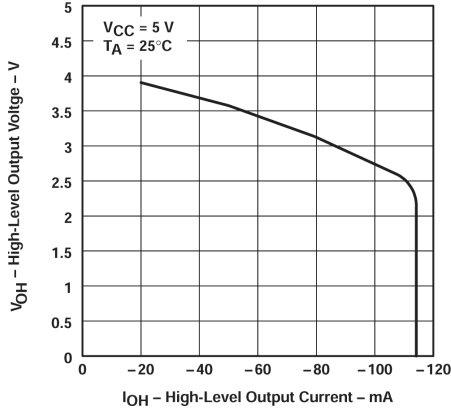


Figure 5-1. High-level Output Voltage vs High-level Output Current

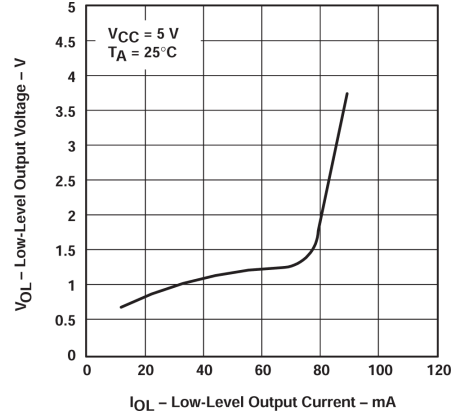


Figure 5-2. Low-level Output Voltage vs Low-level Output Current

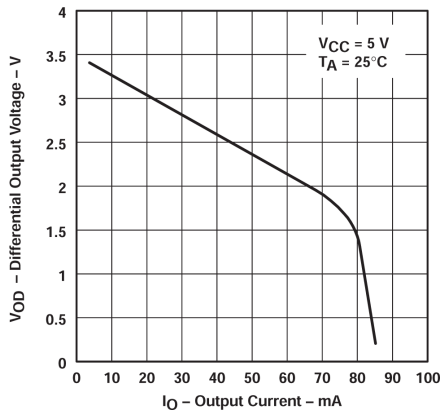


Figure 5-3. Differential Output Voltage vs Output Current

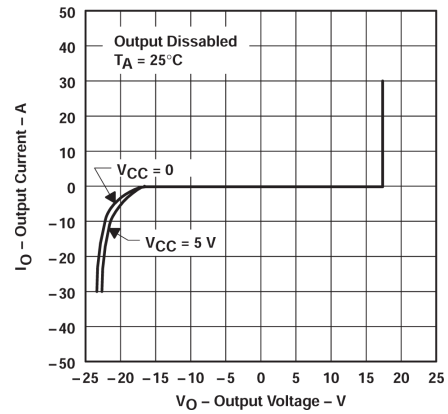


Figure 5-4. Output Current vs Output Voltage

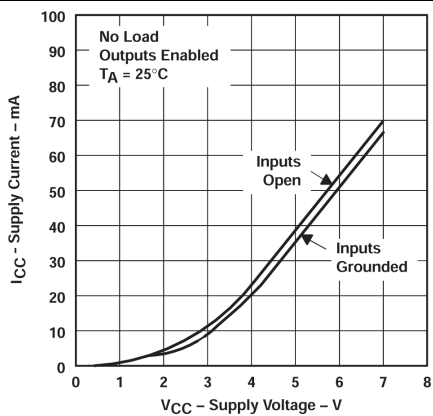


Figure 5-5. Supply Current vs Supply Voltage

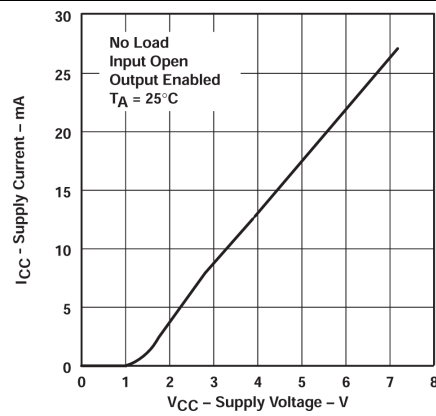


Figure 5-6. Supply Current vs Supply Voltage

## 6 Parameter Measurement Information

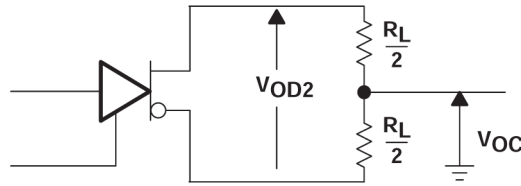
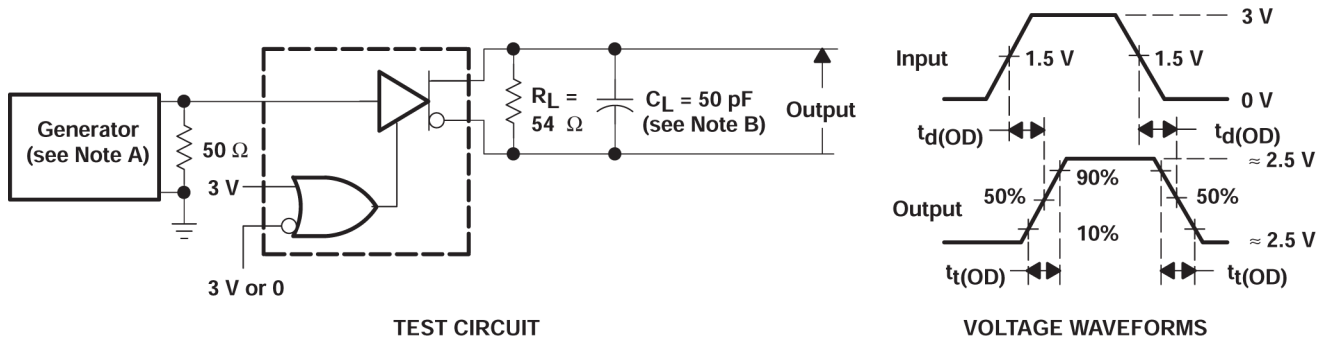
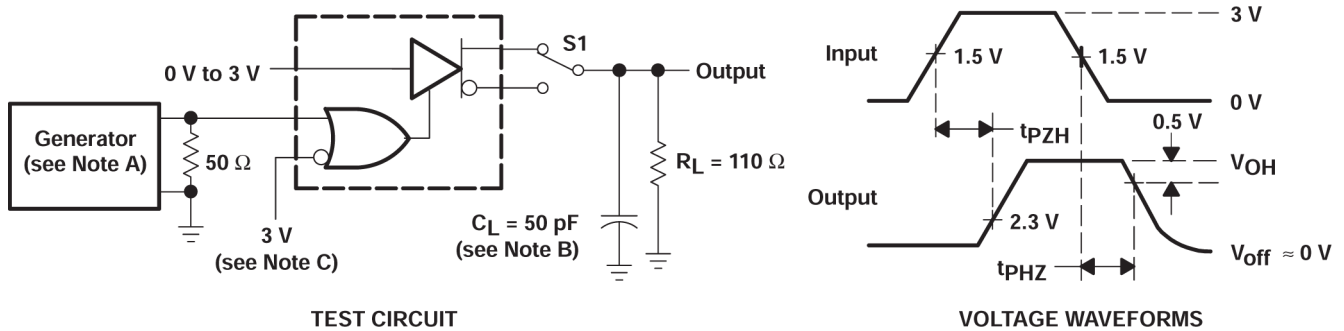


Figure 6-1. Differential and Common-Mode Output Voltages



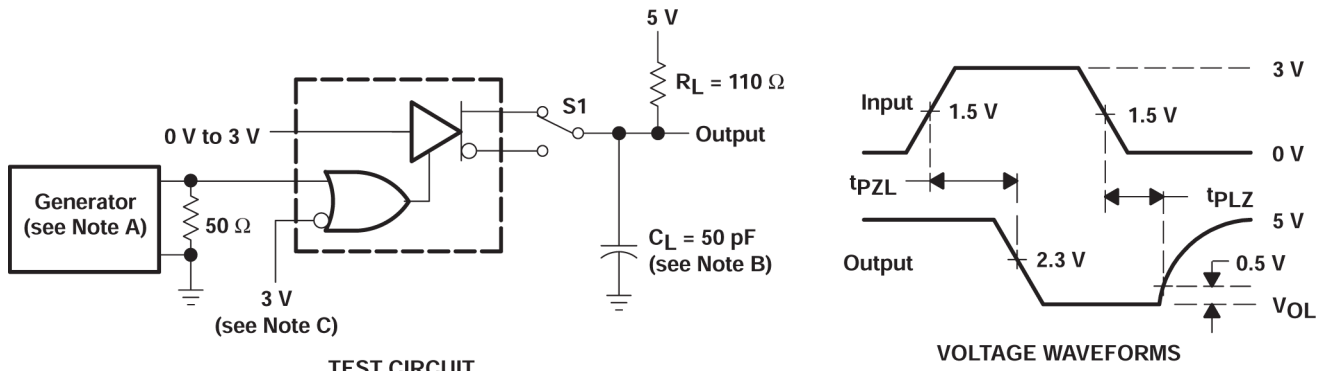
- A. The input pulse is supplied by a generator having the following characteristics:  $t_r \leq 10\text{ns}$ ,  $t_f \leq 10\text{ns}$ ,  $\text{PRR} \leq 1\text{MHz}$ , duty cycle = 50%,  $Z_O = 50\Omega$ .
- B.  $C_L$  includes probe and stray capacitance.

Figure 6-2. Differential-Output Test Circuit and Voltage Waveforms



- A. A. The input pulse is supplied by a generator having the following characteristics:  $\text{PRR} \leq 1\text{MHz}$ , duty cycle = 50%,  $t_r \leq 10\text{ns}$ ,  $t_f \leq 10\text{ns}$ ,  $Z_O = 50\Omega$ .
- B.  $C_L$  includes probe and stray capacitance.
- C. To test the active-low enable  $\overline{G}$ , ground G and apply an inverted waveform to  $\overline{G}$ .

Figure 6-3. Test Circuit and Voltage Waveforms



TEST CIRCUIT

VOLTAGE WAVEFORMS

- A. A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1MHz, duty cycle = 50%,  $t_r \leq$  5ns,  $t_f \leq$  5ns,  $Z_O = 50\Omega$ .
- B.  $C_L$  includes probe and stray capacitance.
- C. To test the active-low enable  $\overline{G}$ , ground G and apply an inverted waveform to  $\overline{G}$ .

**Figure 6-4. Test Circuit and Voltage Waveforms**

## 7 Detailed Description

### 7.1 Device Functional Modes

Function Table (Each Driver)

INPUT A <sup>(1)</sup>	ENABLES		OUTPUTS	
	G	$\bar{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

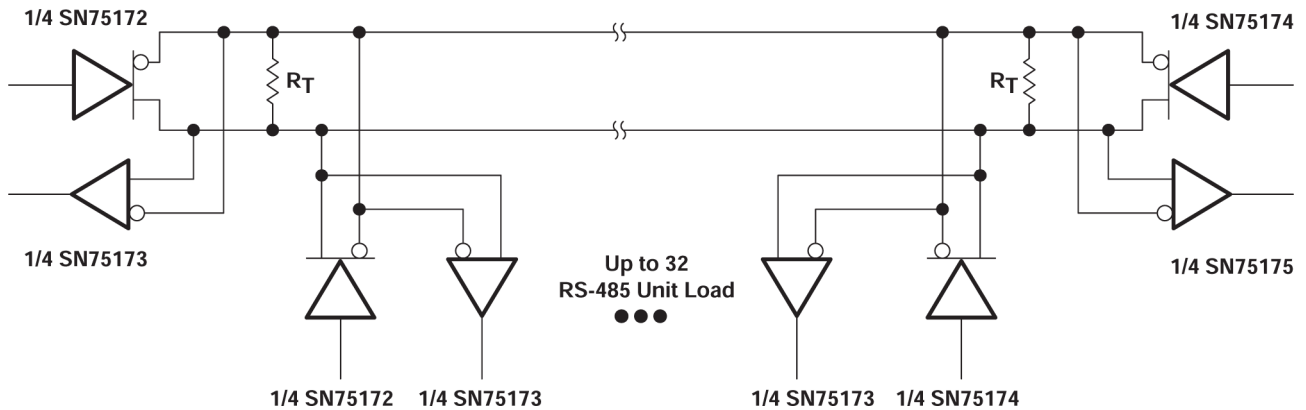
(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information



- A. The line length should be terminated at both ends in its characteristic impedance ( $R_T = Z_0$ ). Stub lengths off the main line should be kept as short as possible.

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision B (May 1995) to Revision C (April 2024)</b>	<b>Page</b>
• Changed the numbering format for tables, figures, and cross-references throughout the document.....	<b>1</b>
• Added the <i>Thermal Information</i> table.....	<b>5</b>
• Changed Note A in <a href="#">Figure 6-2</a> and <a href="#">Figure 6-3</a> .....	<b>8</b>

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75172DW	LIFEBUY	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75172	
SN75172DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75172	Samples
SN75172N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75172N	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75172DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75172DWR	SOIC	DW	20	2000	367.0	367.0	45.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75172DW	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN75172DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN75172N	N	PDIP	16	25	506	13.97	11230	4.32

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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